TRIQUINT SEMICONDUCTOR, INC.

TQS

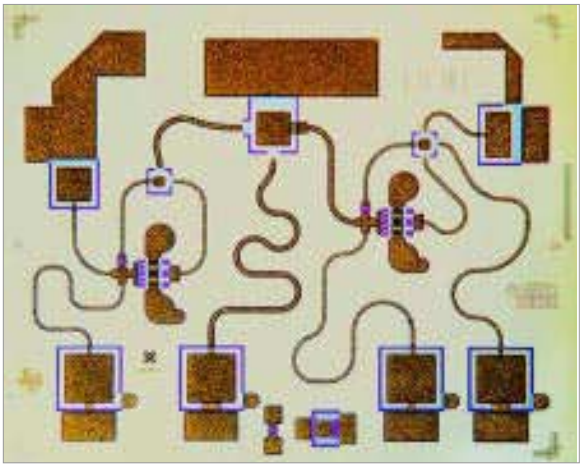
TGA8035-SCC

Gain Block Amplifier

8035

- **6 to 18-GHz Frequency Range**
- **13-dB Typical Gain**
- **2.2:1 Typical Input/Output SWR**
- **12.5-dBm Typical Output Power at 1-dB Gain Compression**
- **5-dB Typical Noise Figure**
- **2,4892 x 2,0574 x 0,1143 mm (0.098 x 0.081 x 0.0045 in.)**

PHOTO ENLARGEMENT



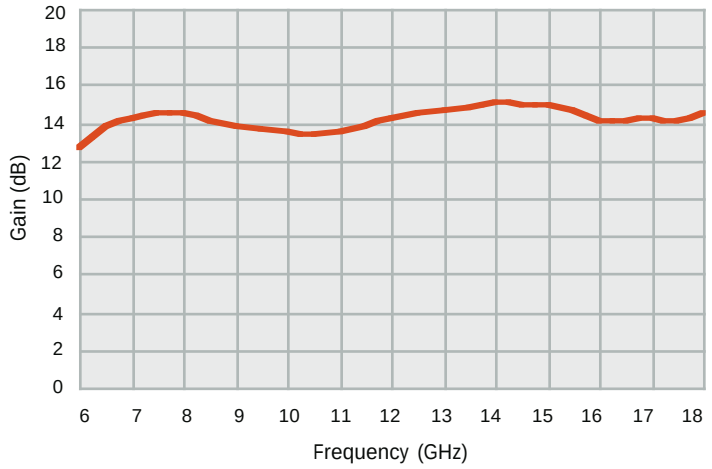
DESCRIPTION

The TriQuint TGA8035-SCC is a two-stage GaAs monolithic amplifier designed for use as a broadband general-purpose gain block. Two 300-µm gate-width FETs provide a 13-dB typical gain and a 5-dB noise figure from 6 to 18-GHz. Typical output power at 1-dB gain compression is 12.5-dBm. Shunt feedback is used around each active device to improve gain flatness and standing-wave ratio (SWR). Ground is provided to the circuitry through vias to the backside metallization.

The TGA8035-SCC amplifier is suitable for a variety of broadband electronic warfare (EW) applications. The combination of gain, power, and noise figure makes this device an exceptional post amplifier following a low-noise amplifier.

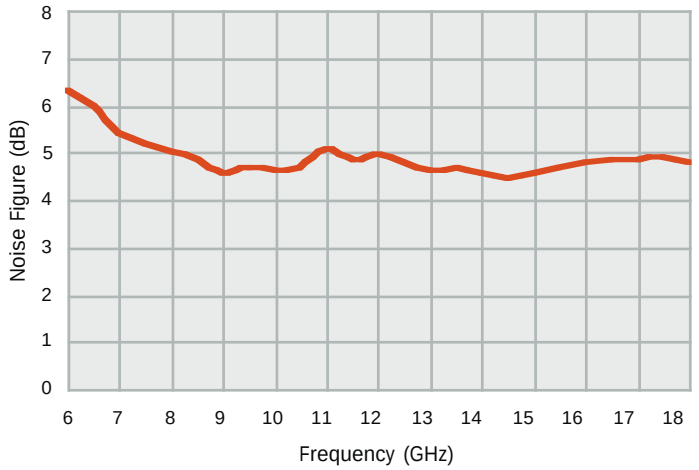
Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as thermocompression and thermosonic wire-bonding processes. The TGA8035-SCC is supplied in chip form and is readily assembled using automated equipment.

TYPICAL SMALL-SIGNAL POWER GAIN



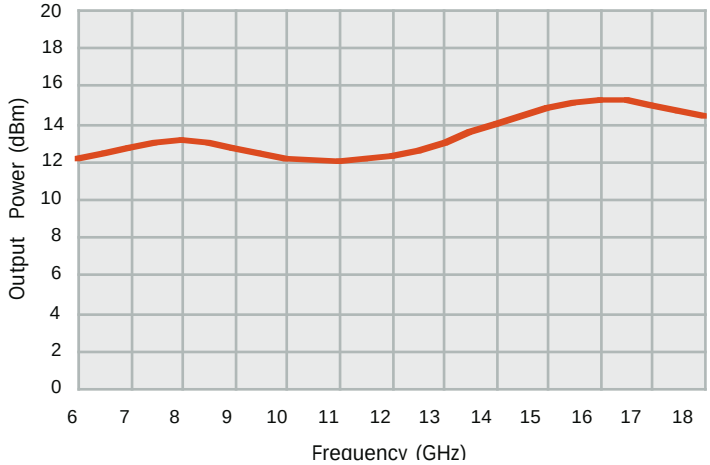
V_{D1}, V_{D2} = 5 V
I_{D1} = 50% I_{DSS1}
I_{D2} = 50% I_{DSS2}
T_A = 25°C

TYPICAL NOISE FIGURE



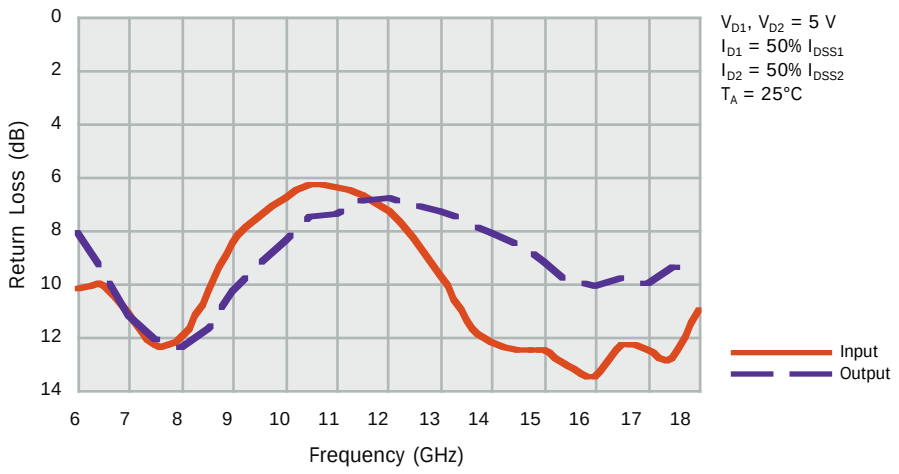
V_{D1}, V_{D2} = 5 V
I_{D1} = 50% I_{DSS1}
I_{D2} = 50% I_{DSS2}
T_A = 25°C

TYPICAL OUTPUT POWER
P_{1dB}



V_{D1}, V_{D2} = 5 V
I_{D1} = 50% I_{DSS1}
I_{D2} = 50% I_{DSS2}
T_A = 25°C

TYPICAL RETURN LOSS



ABSOLUTE MAXIMUM RATINGS

Drain supply voltage, V_{D1}, V_{D2}	8 V
Drain supply voltage range with respect to negative supply voltage, V_{D1} - V_{G1}, V_{D2} - V_{G2}	0 V to 8 V
Negative supply voltage range, V_{G1}, V_{G2}	0 V to - 5 V
Positive supply current, I_{D1}	I_{DSS1}
Positive supply current, I_{D2}	I_{DSS2}
Power dissipation at (or below) 25 C base-plate temperature, P_D*	1.4 W
Input continuous wave power, P_{IN}	20 dBm
Operating channel temperature, T_{CH} **	150 C
Mounting temperature (30 sec), T_M	320 C
Storage temperature range, T_{STG}	- 65 to 150 C

Ratings over operating channel temperature range, T_{CH} (unless otherwise noted)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "RF Characteristics" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

* For operation above 25 C base-plate temperature, derate linearly at the rate of 3 mW/ C.

* Operating channel temperature (T_{CH}) directly affects the device MTTF. For maximum life, it is recommended that channel temperature be maintained at the lowest possible level.

TYPICAL S-PARAMETERS

Frequency	S_{11}		S_{21}		S_{12}		S_{22}		GAIN
(GHz)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	(dB)
5.0	0.54	75	2.34	55	0.013	109	0.59	73	7.4
5.5	0.35	71	3.49	9	0.018	77	0.47	61	10.9
6.0	0.31	75	4.33	-34	0.021	46	0.39	49	12.7
6.5	0.31	62	4.89	-73	0.022	15	0.33	33	13.8
7.0	0.28	34	5.16	-108	0.022	-15	0.28	14	14.2
7.5	0.24	-7	5.28	-141	0.021	-44	0.25	-7	14.5
8.0	0.25	-53	5.27	-172	0.021	-75	0.24	-31	14.4
8.5	0.30	-91	5.05	161	0.020	-102	0.26	-52	14.1
9.0	0.37	-117	4.92	136	0.019	-124	0.30	-71	13.8
9.5	0.42	-138	4.82	112	0.021	-144	0.34	-88	13.7
10.0	0.46	-154	4.71	90	0.021	-164	0.38	-102	13.5
10.5	0.48	-168	4.68	69	0.020	177	0.42	-115	13.4
11.0	0.48	178	4.73	48	0.020	174	0.43	-125	13.5
11.5	0.46	166	4.91	27	0.021	161	0.45	-134	13.8
12.0	0.43	153	5.13	5	0.021	151	0.46	-144	14.2
12.5	0.38	140	5.28	-18	0.021	141	0.45	-154	14.5
13.0	0.33	129	5.42	-41	0.021	132	0.43	-164	14.7
13.5	0.27	123	5.52	-64	0.021	120	0.41	-173	14.8
14.0	0.25	118	5.68	-89	0.020	109	0.39	178	15.1
14.5	0.24	112	5.61	-113	0.017	97	0.38	167	15.0
15.0	0.24	100	5.59	-138	0.013	96	0.35	154	14.9
15.5	0.22	89	5.40	-163	0.014	94	0.32	143	14.6
16.0	0.21	81	5.10	174	0.015	80	0.31	136	14.1
16.5	0.24	67	5.05	153	0.012	47	0.33	123	14.1
17.0	0.24	46	5.12	129	0.007	44	0.32	114	14.2
17.5	0.23	27	5.06	103	0.010	28	0.34	108	14.1
18.0	0.28	-4	5.27	78	0.005	-38	0.35	93	14.4
18.5	0.35	-48	5.49	46	0.007	-17	0.33	83	14.8
19.0	0.41	-92	4.91	9	0.012	-85	0.29	73	13.8
19.5	0.53	-122	4.01	-23	0.012	-152	0.19	75	12.1
20.0	0.68	-149	3.37	-55	0.008	156	0.18	100	10.5

I_{D1} = 50% I_{DSS1}, I_{D2} = 50% I_{DSS2}, V_{D1}, V_{D2} = 5 V, T_A = 25°C

Reference planes for S-parameter data include bond wires as specified in the "Recommended Assembly Diagram."

RF CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	TYP	UNIT
G_P	Small–signal power gain	f = 6 to 18 GHz	13	dB
SWR(in)	Input standing–wave ratio	f = 6 to 18 GHz	2.2:1	—
SWR(out)	Output standing–wave ratio	f = 6 to 18 GHz	2.2:1	—
P_{1dB}	Output power at 1–dB gain compression	f = 6 to 18 GHz	12.5	dBm
NF	Noise figure	f = 6 to 18 GHz	5	dB

V_{D1}, V_{D2} = 5 V, V_{G1} = -1 V, V_{G2} = -1 V, T_A = 25°C

DC CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{DSS1}	Total zero–gate–voltage drain current at saturation for FET1 *	V_{DS} = 0.5 V to 3.5 V, V_{GS} = 0	36	108	mA
I_{DSS2}	Total zero–gate–voltage drain current at saturation for FET2 **	V_{DS} = 0.5 V to 3.5 V, V_{GS} = 0	36	108	mA

T_A = 25°C

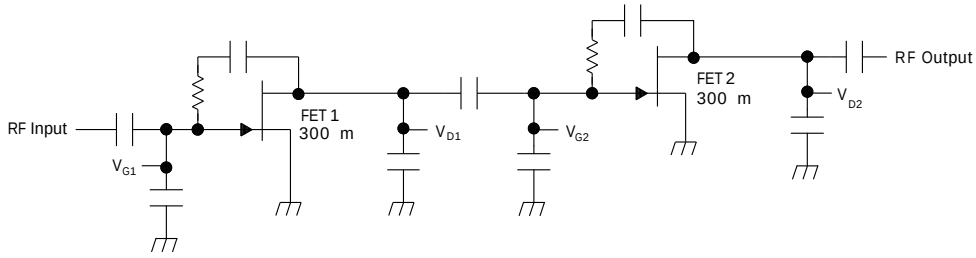
* V_{DS1} for I_{DSS1} is drain voltage between 0.5 V and 3.5 V at which drain current is highest at DC autoprobe.
** V_{DS2} for I_{DSS2} is drain voltage between 0.5 V and 3.5 V at which drain current is highest at DC autoprobe.

THERMAL INFORMATION

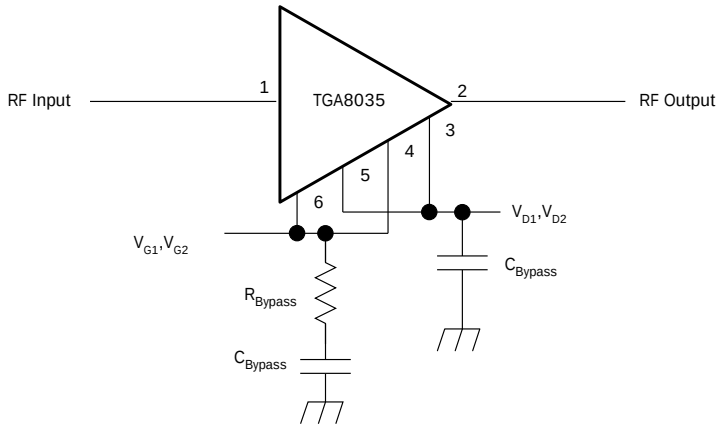
	PARAMETER	TEST CONDITIONS	TEST CONDITIONS	FET	MMIC*	UNIT
			25°C Base, 80°C Channel**	152.5	76.3	
R_{JC}	Thermal resistance, channel–to–backside	I_D=72 mA, V_D=5V	85°C Base, 151°C Channel**	184.7	92.4	°C/W
			100°C Base, 169°C Channel**	192.8	96.4	

* MMIC thermal resistance is the peak FET temperature rise divided by the total MMIC dissipated power (.72 W).
** Hottest Gate Channel (Center of either FET).

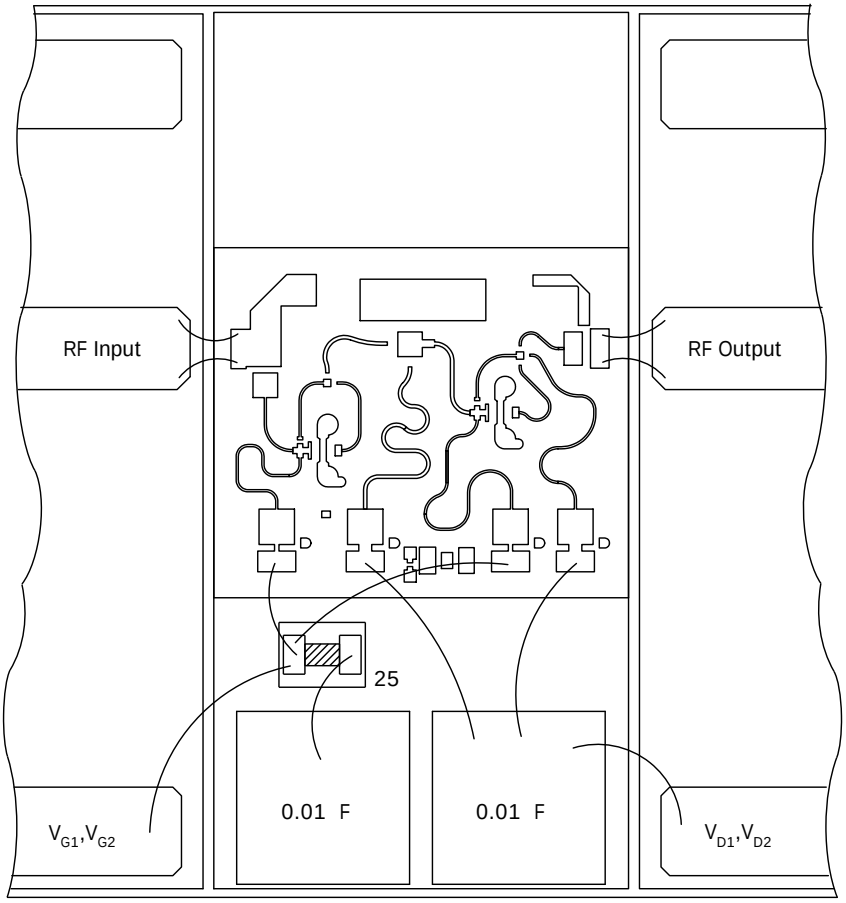
EQUIVALENT SCHEMATIC



TYPICAL BIAS NETWORK



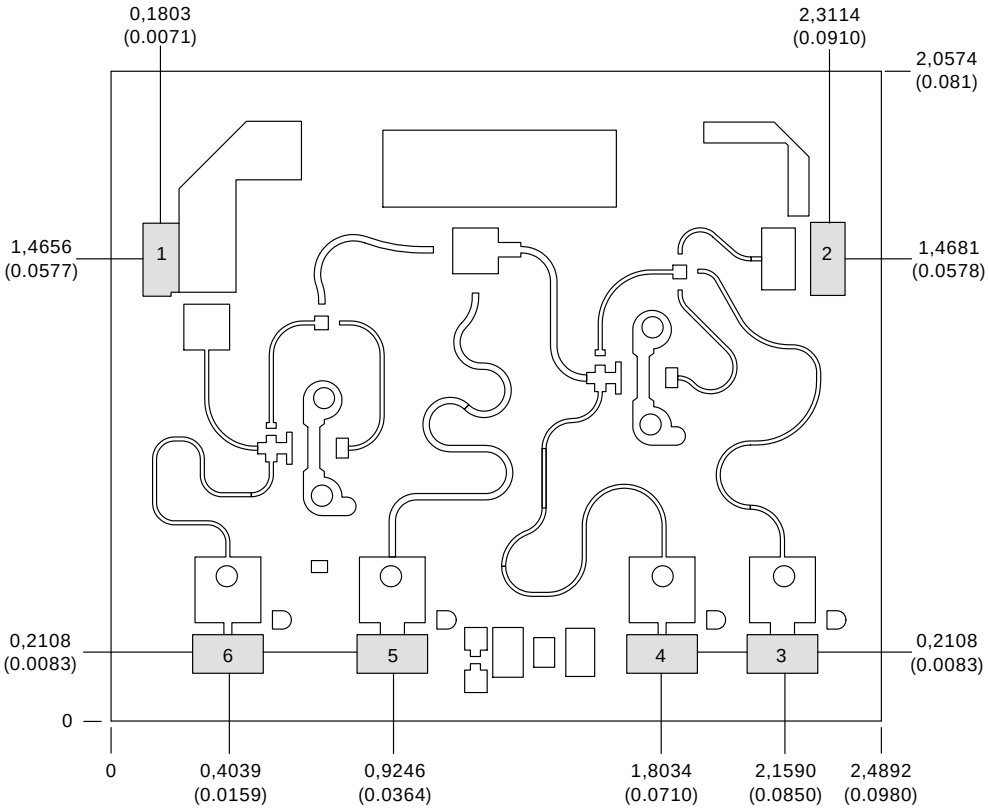
RECOMMENDED ASSEMBLY DIAGRAM



RF connections: bond using two 1-mil diameter, 20 to 25 - mil- length gold bond wires at both RF Input and RF Output for optimum RF performance.

Close placement of external components is essential to stability.

MECHANICAL DRAWING



Units: millimeters (inches)
Thickness: 0,1143 (0.045) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad.
Chip size tolerance: ± 0,0508 (0.002)

Bond pad #1 (RF Input):	0,0940 x 0,2362 (0.0037 x 0.0093)
Bond pad #2 (RF Output):	0,0991 x 0,2413 (0.0039 x 0.0095)
Bond pad #3 (V_{D2}):	0,2286 x 0,1143 (0.0090 x 0.0045)
Bond pad #4 (V_{G2}):	0,2286 x 0,1143 (0.0090 x 0.0045)
Bond pad #5 (V_{D1}):	0,2286 x 0,1143 (0.0090 x 0.0045)
Bond pad #6 (V_{G1}):	0,2286 x 0,1143 (0.0090 x 0.0045)