Artix-7 FPGAs Data Sheet: DC and Switching Characteristics

DS181 (v1.3) June 1, 2012 **Advance Product Specification**

Introduction

Artix™-7 FPGAs are available in -3, -2, -1, and -2L speed grades, with -3 having the highest performance. The -2L devices can operate at either of two V_{CCINT} voltages, 0.9V and 1.0V and are screened for lower maximum static power. When operated at V_{CCINT} = 1.0V, the speed specification of a -2L device is the same as the -2 speed grade. When operated at V_{CCINT} = 0.9V, the -2L static and dynamic power is reduced.

Artix-7 FPGA DC and AC characteristics are specified in commercial, extended, and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Artix-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

All specifications are subject to change without notice.

DC Characteristics

Table 1: **Absolute Maximum Ratings(1)**

Symbol	Description	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage relative to GND	–0.5	1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5	2.0	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.5	1.1	V
V_{CCO}	Output drivers supply voltage relative to GND for 3.3V HR I/O banks	–0.5	3.6	V
V_{REF}	Input reference voltage	–0.5	2.0	V
V_{IN}(2)	I/O input voltage relative to GND(3) (user and dedicated I/Os)	–0.5	V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state 3.3V or below output(3) (user and dedicated I/Os)	–0.5	V_{CCO} + 0.5	V
V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V
GTP Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	–0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTP transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies (4)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies (4)	–	+260	°C
T_j	Maximum junction temperature(4)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The 3.3V I/O absolute maximum limit applied to DC and AC signals.
3. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide*.
4. For soldering guidelines and thermal considerations, see UG475: *7 Series FPGA Packaging and Pinout Specification*.

Table 2: **Recommended Operating Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage relative to GND	0.95	1.00	1.05	V
	For -2L (0.9V) devices: internal supply voltage relative to GND	0.87	0.90	0.93	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	1.71	1.80	1.89	V
V_{CCBRAM}	Block RAM supply voltage	0.95	1.00	1.05	V
V_{CCO}(2)(3)	Supply voltage for 3.3V HR I/O banks relative to GND	1.14	–	3.465	V
V_{IN}	I/O input voltage relative to GND	GND – 0.20	–	V_{CCO} + 0.2	V
I_{IN}(4)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{CCBATT}(5)	Battery voltage relative to GND	1.0	–	1.89	V
GTP Transceiver					
$V_{MGTAVCC}$(6)(7)	Analog supply voltage for the GTP transmitter and receiver circuits relative to GND	0.97	1.0	1.03	V
$V_{MGTAVTT}$(6)(7)	Analog supply voltage for the GTP transmitter and receiver termination circuits relative to GND	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V

Table 2: **Recommended Operating Conditions[1] *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

1. All voltages are relative to ground.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
4. A total of 100 mA per bank should not be exceeded.
5. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
6. Each voltage listed requires the filter circuit described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.
7. Voltages are specified for the temperature range of T_j = 0°C to +85°C.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin		15		µA
I_L	Input or output leakage current per pin (sample-tested)		15		µA
C_{IN}[2]	Die input capacitance at the pad		8		pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V		330		µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V		250		µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V		220		µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V		150		µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V		120		µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V		330		µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V		180		µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}[3]	Battery supply current	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40) for commercial (C), and industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50) for commercial (C), and industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60) for commercial (C), and industrial (I), and extended (E) temperature devices	44	60	83	Ω

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[1]	Max	Units
n	Temperature diode ideality factor		1.0002		–
r	Temperature diode series resistance		2		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7A100T					mA
		XC7A200T					mA
		XC7A350T					mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7A100T					mA
		XC7A200T					mA
		XC7A350T					mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7A100T					mA
		XC7A200T					mA
		XC7A350T					mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7A100T					mA
		XC7A200T					mA
		XC7A350T					mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the XPower™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

Table 5 shows the minimum current, in addition to I_{CCQ}, that are required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Artix-7 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
	Typ(1)	Typ(1)	Typ(1)	Typ(1)	
XC7A100T					mA
XC7A200T					mA
XC7A350T					mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100°C$(1)	–	500	ms
		$T_J = 85°C$(1)	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of MGTAVCC		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of MGTAVTT		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **SelectIO DC Input and Output Levels(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	6.3	–6.3
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 3	Note 3
LVCMOS15	–0.300	30% V_{CCO}	70% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.300	0.800	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
PCI33_3	–0.500	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{REF} – 0.150	V_{REF} + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{REF} – 0.150	V_{REF} + 0.150	17.8	–17.8
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{REF} – 0.150	V_{REF} + 0.150	8.9	–8.9
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{TT} – 0.175	V_{TT} + 0.175	17.8	–17.8
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{TT} – 0.175	V_{TT} + 0.175	8.9	–8.9
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{TT} – 0.470	V_{TT} + 0.470	8	–8
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{TT} – 0.600	V_{TT} + 0.600	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see UG471: *7 Series FPGAs SelectIO Resources User Guide*.

Table 8: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. LVDS_25 is specified in Table 10.

Table 9: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]			V_{OL}[5]	V_{OH}[6]
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Max	V, Min
BLVDS_25		1.250		0.100				1.250					N/A	N/A
DIFF_HSTL_I		0.750		0.100				0.750					N/A	N/A
DIFF_HSTL_I_18		0.900		0.100				0.900					N/A	N/A
DIFF_HSTL_II		0.750		0.100				0.750					N/A	N/A
DIFF_HSTL_II_18		0.900		0.100				0.900					N/A	N/A
DIFF_HSUL_12		0.600		0.100				0.600					N/A	N/A
DIFF_MOBILE_DDR		0.900		0.100				0.900					N/A	N/A
DIFF_SSTL12		0.600		0.100				0.600						
DIFF_SSTL135		0.675		0.100				0.675					(V_{CCO}/2) – 0.160	(V_{CCO}/2) + 0.160
DIFF_SSTL15		0.750		0.100				0.750					(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175
DIFF_SSTL18_I		0.900		0.100				0.900					N/A	N/A
DIFF_SSTL18_II		0.900		0.100				0.900					N/A	N/A

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OL} is the single-ended low-output voltage.
6. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information on the LVDS_25 standard in the HR I/O banks.

Table 10: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

AC Switching Characteristics

All values represented in this data sheet are based on the advance speed specifications in ISE® software 14.1 v1.03 for the -3, -2, and -1 speed grades and v1.01 for the -2L speed grade.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Artix-7 FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 11 correlates the current status of each Artix-7 device on a per speed grade basis.

Table 11: **Artix-7 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7A100T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7A200T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7A350T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 12 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 12: **Artix-7 Device Production Software and Speed Specification Release**

Device	Speed Grade			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7A100T				
XC7A200T				
XC7A350T				

Notes:
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 8.

Table 13: **Networking Applications Interface Performances**

Description	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	710	710	625		Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950		Mb/s
SDR LVDS receiver (SFI-4.1)(1)	710	710	625		Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1250	1250	950		Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 14: **Maximum Physical Interface (PHY) Rate for Memory Interfaces(1)(2)**

Memory Standard	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
DDR3	1066	800	800	800	Mb/s
DDR3L	800	800	667	667	Mb/s
DDR2	800	800	667	667	Mb/s
LPDDR2	667	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).

IOB Pad Input/Output/3-State Switching Characteristics

Table 15 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 16 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 15: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.57	1.70	1.94	1.65	5.74	6.18	6.87	5.80	5.74	6.18	6.87	5.80	ns
LVTTL_S8	1.57	1.70	1.94	1.65	5.74	6.19	6.87	5.06	5.74	6.19	6.87	5.06	ns
LVTTL_S12	1.57	1.70	1.94	1.65	4.57	4.77	5.09	5.06	4.57	4.77	5.09	5.06	ns
LVTTL_S16	1.57	1.70	1.94	1.65	4.54	4.75	5.08	4.13	4.54	4.75	5.08	4.13	ns
LVTTL_S24	1.57	1.70	1.94	1.65	3.53	3.93	4.53	4.22	3.53	3.93	4.53	4.22	ns
LVTTL_F4	1.57	1.70	1.94	1.65	5.75	6.13	6.69	5.16	5.75	6.13	6.69	5.16	ns
LVTTL_F8	1.57	1.70	1.94	1.65	5.64	6.05	6.69	4.27	5.64	6.05	6.69	4.27	ns
LVTTL_F12	1.57	1.70	1.94	1.65	4.45	4.65	4.96	4.25	4.45	4.65	4.96	4.25	ns
LVTTL_F16	1.57	1.70	1.94	1.65	4.45	4.64	4.94	3.04	4.45	4.64	4.94	3.04	ns
LVTTL_F24	1.57	1.70	1.94	1.65	2.55	3.29	4.41	2.83	2.55	3.29	4.41	2.83	ns
LVDS_25	0.70	0.77	0.89	0.83	1.38	1.44	1.55	1.44	1.38	1.44	1.55	1.44	ns
MINI_LVDS_25	0.70	0.76	0.87	0.81	1.38	1.44	1.55	1.44	1.38	1.44	1.55	1.44	ns
BLVDS_25	0.70	0.77	0.91	0.84	1.91	2.07	2.32	2.02	1.91	2.07	2.32	2.02	ns
RSDS_25 (point to point)	0.70	0.77	0.89	0.83	1.38	1.44	1.55	1.44	1.38	1.44	1.55	1.44	ns
PPDS_25	0.73	0.79	0.91	0.85	1.35	1.44	1.58	1.50	1.35	1.44	1.58	1.50	ns
TMDS_33	0.84	0.92	1.07	0.91	1.45	1.51	1.62	1.50	1.45	1.51	1.62	1.50	ns
PCI33_3	1.54	1.68	1.92	1.64	2.94	3.22	3.66	2.92	2.94	3.22	3.66	2.92	ns
HSUL_12	0.65	0.69	0.77	0.75	2.31	2.60	3.04	2.35	2.31	2.60	3.04	2.35	ns
DIFF_HSUL_12	0.62	0.67	0.77	0.75	1.93	2.13	2.45	2.05	1.93	2.13	2.45	2.05	ns
HSTL_I_S	0.66	0.71	0.80	0.77	1.51	1.61	1.77	1.68	1.51	1.61	1.77	1.68	ns
HSTL_II_S	0.66	0.71	0.80	0.77	1.11	1.16	1.25	1.24	1.11	1.16	1.25	1.24	ns
HSTL_I_18_S	0.67	0.71	0.80	0.79	1.29	1.37	1.49	1.42	1.29	1.37	1.49	1.42	ns
HSTL_II_18_S	0.67	0.71	0.80	0.79	1.17	1.23	1.33	1.24	1.17	1.23	1.33	1.24	ns
DIFF_HSTL_I_S	0.70	0.75	0.84	0.81	1.40	1.48	1.61	1.52	1.40	1.48	1.61	1.52	ns
DIFF_HSTL_II_S	0.70	0.75	0.84	0.81	1.08	1.12	1.20	1.21	1.08	1.12	1.20	1.21	ns
DIFF_HSTL_I_18_S	0.72	0.77	0.87	0.83	1.23	1.29	1.40	1.35	1.23	1.29	1.40	1.35	ns

Table 15: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_18_S	0.72	0.77	0.87	0.83	1.07	1.11	1.20	1.21	1.07	1.11	1.20	1.21	ns
HSTL_I_F	0.66	0.71	0.80	0.77	1.07	1.13	1.24	1.22	1.07	1.13	1.24	1.22	ns
HSTL_II_F	0.66	0.71	0.80	0.77	0.97	1.02	1.11	1.13	0.97	1.02	1.11	1.13	ns
HSTL_I_18_F	0.67	0.71	0.80	0.79	1.05	1.10	1.21	1.20	1.05	1.10	1.21	1.20	ns
HSTL_II_18_F	0.67	0.71	0.80	0.79	0.97	1.02	1.12	1.11	0.97	1.02	1.12	1.11	ns
DIFF_HSTL_I_F	0.70	0.75	0.84	0.81	1.02	1.07	1.16	1.15	1.02	1.07	1.16	1.15	ns
DIFF_HSTL_II_F	0.70	0.75	0.84	0.81	0.94	0.99	1.08	1.09	0.94	0.99	1.08	1.09	ns
DIFF_HSTL_I_18_F	0.72	0.77	0.87	0.83	1.01	1.06	1.15	1.14	1.01	1.06	1.15	1.14	ns
DIFF_HSTL_II_18_F	0.72	0.77	0.87	0.83	0.93	0.98	1.07	1.07	0.93	0.98	1.07	1.07	ns
LVCMOS33_S4	1.78	1.90	2.12	1.66	5.65	6.03	6.60	5.79	5.65	6.03	6.60	5.79	ns
LVCMOS33_S8	1.78	1.90	2.12	1.66	4.79	5.21	5.86	5.06	4.79	5.21	5.86	5.06	ns
LVCMOS33_S12	1.78	1.90	2.12	1.66	3.86	4.23	4.80	4.12	3.86	4.23	4.80	4.12	ns
LVCMOS33_S16	1.78	1.90	2.12	1.66	3.30	3.66	4.21	3.65	3.30	3.66	4.21	3.65	ns
LVCMOS33_F4	1.78	1.90	2.12	1.66	5.04	5.32	5.76	5.15	5.04	5.32	5.76	5.15	ns
LVCMOS33_F8	1.78	1.90	2.12	1.66	4.29	4.55	4.97	4.25	4.29	4.55	4.97	4.25	ns
LVCMOS33_F12	1.78	1.90	2.12	1.66	2.72	3.39	4.42	3.04	2.72	3.39	4.42	3.04	ns
LVCMOS33_F16	1.78	1.90	2.12	1.66	2.59	2.82	3.19	2.88	2.59	2.82	3.19	2.88	ns
LVCMOS25_S4	1.49	1.58	1.76	1.39	4.95	5.41	6.11	4.82	4.95	5.41	6.11	4.82	ns
LVCMOS25_S8	1.49	1.58	1.76	1.39	3.88	4.29	4.92	4.07	3.88	4.29	4.92	4.07	ns
LVCMOS25_S12	1.49	1.58	1.76	1.39	3.07	3.59	4.40	3.14	3.07	3.59	4.40	3.14	ns
LVCMOS25_S16	1.49	1.58	1.76	1.39	3.52	3.93	4.55	3.64	3.52	3.93	4.55	3.64	ns
LVCMOS25_F4	1.49	1.58	1.76	1.39	4.69	5.02	5.54	4.33	4.69	5.02	5.54	4.33	ns
LVCMOS25_F8	1.49	1.58	1.76	1.39	2.73	3.25	4.05	2.95	2.73	3.25	4.05	2.95	ns
LVCMOS25_F12	1.49	1.58	1.76	1.39	2.72	3.24	4.04	2.69	2.72	3.24	4.04	2.69	ns
LVCMOS25_F16	1.49	1.58	1.76	1.39	2.17	2.48	2.97	2.20	2.17	2.48	2.97	2.20	ns
LVCMOS18_S4	0.78	0.82	0.92	0.78	3.72	3.90	4.19	3.45	3.72	3.90	4.19	3.45	ns
LVCMOS18_S8	0.78	0.82	0.92	0.78	2.91	3.23	3.74	2.94	2.91	3.23	3.74	2.94	ns
LVCMOS18_S12	0.78	0.82	0.92	0.78	2.91	3.23	3.74	2.94	2.91	3.23	3.74	2.94	ns
LVCMOS18_S16	0.78	0.82	0.92	0.78	2.01	2.22	2.56	2.05	2.01	2.22	2.56	2.05	ns
LVCMOS18_S24	0.78	0.82	0.92	0.78	1.87	2.03	2.28	1.94	1.87	2.03	2.28	1.94	ns
LVCMOS18_F4	0.78	0.82	0.92	0.78	3.58	3.71	3.93	3.33	3.58	3.71	3.93	3.33	ns
LVCMOS18_F8	0.78	0.82	0.92	0.78	2.11	2.42	2.89	2.15	2.11	2.42	2.89	2.15	ns
LVCMOS18_F12	0.78	0.82	0.92	0.78	2.11	2.42	2.89	2.15	2.11	2.42	2.89	2.15	ns
LVCMOS18_F16	0.78	0.82	0.92	0.78	1.59	1.73	1.96	1.69	1.59	1.73	1.96	1.69	ns
LVCMOS18_F24	0.78	0.82	0.92	0.78	1.34	1.44	1.60	1.47	1.34	1.44	1.60	1.47	ns
LVCMOS15_S4	0.80	0.86	0.97	0.81	4.14	4.36	4.71	3.82	4.14	4.36	4.71	3.82	ns
LVCMOS15_S8	0.80	0.86	0.97	0.81	2.50	2.81	3.29	2.67	2.50	2.81	3.29	2.67	ns

Table 15: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVCMOS15_S12	0.80	0.86	0.97	0.81	2.00	2.19	2.50	2.06	2.00	2.19	2.50	2.06	ns
LVCMOS15_S16	0.80	0.86	0.97	0.81	1.90	2.07	2.35	1.97	1.90	2.07	2.35	1.97	ns
LVCMOS15_F4	0.80	0.86	0.97	0.81	3.96	4.15	4.46	3.65	3.96	4.15	4.46	3.65	ns
LVCMOS15_F8	0.80	0.86	0.97	0.81	1.84	2.06	2.41	1.97	1.84	2.06	2.41	1.97	ns
LVCMOS15_F12	0.80	0.86	0.97	0.81	1.43	1.54	1.73	1.55	1.43	1.54	1.73	1.55	ns
LVCMOS15_F16	0.80	0.86	0.97	0.81	1.39	1.50	1.67	1.52	1.39	1.50	1.67	1.52	ns
LVCMOS12_S4	0.90	0.95	1.07	0.85	4.66	5.03	5.60	4.27	4.66	5.03	5.60	4.27	ns
LVCMOS12_S8	0.90	0.95	1.07	0.85	3.17	3.62	4.31	3.01	3.17	3.62	4.31	3.01	ns
LVCMOS12_S12	0.90	0.95	1.07	0.85	2.31	2.60	3.04	2.35	2.31	2.60	3.04	2.35	ns
LVCMOS12_F4	0.90	0.95	1.07	0.85	4.11	4.38	4.80	3.77	4.11	4.38	4.80	3.77	ns
LVCMOS12_F8	0.90	0.95	1.07	0.85	1.97	2.56	3.47	2.10	1.97	2.56	3.47	2.10	ns
LVCMOS12_F12	0.90	0.95	1.07	0.85	1.62	1.79	2.05	1.73	1.62	1.79	2.05	1.73	ns
SSTL135_S	0.66	0.69	0.77	0.73	1.10	1.15	1.25	1.28	1.10	1.15	1.25	1.28	ns
SSTL15_S	0.66	0.71	0.80	0.77	1.10	1.15	1.24	1.24	1.10	1.15	1.24	1.24	ns
SSTL18_I_S	0.67	0.71	0.80	0.79	1.55	1.65	1.82	1.71	1.55	1.65	1.82	1.71	ns
SSTL18_II_S	0.67	0.71	0.80	0.79	1.10	1.15	1.24	1.24	1.10	1.15	1.24	1.24	ns
DIFF_SSTL135_S	0.64	0.71	0.83	0.75	1.10	1.15	1.25	1.28	1.10	1.15	1.25	1.28	ns
DIFF_SSTL15_S	0.70	0.75	0.84	0.81	1.10	1.15	1.24	1.24	1.10	1.15	1.24	1.24	ns
DIFF_SSTL18_I_S	0.72	0.77	0.87	0.83	1.51	1.60	1.76	1.61	1.51	1.60	1.76	1.61	ns
DIFF_SSTL18_II_S	0.72	0.77	0.87	0.83	1.06	1.11	1.19	1.19	1.06	1.11	1.19	1.19	ns
SSTL135_F	0.66	0.69	0.77	0.73	0.98	1.03	1.13	1.12	0.98	1.03	1.13	1.12	ns
SSTL15_F	0.66	0.71	0.80	0.77	0.97	1.02	1.12	1.13	0.97	1.02	1.12	1.13	ns
SSTL18_I_F	0.67	0.71	0.80	0.79	1.07	1.13	1.23	1.22	1.07	1.13	1.23	1.22	ns
SSTL18_II_F	0.67	0.71	0.80	0.79	0.97	1.01	1.09	1.11	0.97	1.01	1.09	1.11	ns
DIFF_SSTL135_F	0.64	0.71	0.83	0.75	0.98	1.03	1.13	1.12	0.98	1.03	1.13	1.12	ns
DIFF_SSTL15_F	0.70	0.75	0.84	0.81	0.97	1.02	1.12	1.13	0.97	1.02	1.12	1.13	ns
DIFF_SSTL18_I_F	0.72	0.77	0.87	0.83	1.03	1.08	1.18	1.17	1.03	1.08	1.18	1.17	ns
DIFF_SSTL18_II_F	0.72	0.77	0.87	0.83	0.94	0.98	1.07	1.08	0.94	0.98	1.07	1.08	ns

Table 16: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{IOTPHZ}	T input to Pad high-impedance	2.39	2.56	2.80	2.80	ns

Input/Output Logic Switching Characteristics

Table 17: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.46/ 0.01	0.51/ 0.01	0.72/ 0.01	0.40/ –0.07	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.57/ –0.15	0.66/ –0.15	1.07/ –0.15	0.88/ –0.35	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.01/ 0.25	0.02/ 0.26	0.02/ 0.30	0.01/ 0.33	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IDELAY)	0.02/ 0.25	0.02/ 0.26	0.02/ 0.30	0.01/ 0.33	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.10	0.11	0.13	0.14	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.15	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.39	0.42	0.48	0.54	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.39	0.42	0.49	0.55	ns
T_{ICKQ}	CLK to Q outputs	0.50	0.54	0.63	0.71	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.91	1.02	1.25	1.32	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.64	0.74	0.74	0.74	ns, Min

Table 18: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.64/ –0.14	0.67/ –0.14	0.80/ –0.14	0.60/ –0.18	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.30/ –0.08	0.32/ –0.08	0.48/ –0.08	0.21/ –0.10	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.35/ 0.12	0.41/ 0.12	0.76/ 0.12	0.62/ –0.25	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.65/ –0.14	0.69/ –0.14	0.84/ –0.14	0.60/ –0.18	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.31/ –0.08	0.32/ –0.08	0.48/ –0.08	0.22/ –0.10	ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.79	0.87	1.05	1.18	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.44	0.47	0.53	0.63	ns
T_{RQ_OLOGIC}	SR pin to OQ/TQ out	0.68	0.75	0.90	1.12	ns
T_{GSRQ_OLOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T_{RPW_OLOGIC}	Minimum Pulse Width, SR inputs	0.64	0.74	0.74	0.74	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 19: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.01/ 0.13	0.02/ 0.14	0.02/ 0.17	0.02/ 0.21	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.42/ –0.02	0.48/ –0.02	0.68/ –0.02	0.35/ –0.11	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	–0.11/ 0.31	–0.11/ 0.34	–0.11/ 0.38	–0.17/ 0.40	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	–0.02/ 0.12	–0.02/ 0.13	–0.02/ 0.16	–0.04/ 0.19	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IDELAY)(1)	–0.02/ 0.11	–0.02/ 0.13	–0.02/ 0.16	–0.03/ 0.19	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	–0.02/ 0.12	–0.02/ 0.13	–0.02/ 0.16	–0.04/ 0.19	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY)(1)	0.11/ 0.11	0.13/ 0.13	0.16/ 0.16	0.19/ 0.19	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.47	0.51	0.57	0.67	ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.19	0.20	0.23	0.25	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 20: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.40/ –0.05	0.43/ –0.05	0.60/ –0.05	0.44/ –0.25	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.65/ –0.14	0.69/ –0.14	0.83/ –0.14	0.60/ –0.25	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.29/ –0.14	0.32/ –0.14	0.37/ –0.14	0.46/ –0.25	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.30/ –0.02	0.32/ –0.02	0.48/ –0.02	0.21/ –0.15	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.44	0.49	0.81	0.70	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.31/ –0.08	0.32/ –0.08	0.48/ –0.08	0.22/ –0.15	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.38	0.40	0.45	0.54	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.44	0.47	0.53	0.63	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ Out	0.79	0.87	1.05	1.18	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 21: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.48	3.48	3.48	3.22	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.0(1)	200	200	200	200	MHz
	Attribute REFCLK frequency = 300.0(1)	300	300	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	56.16	56.16	56.16	56.16	ns
IDELAY						
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution	1/(32 x 2 x F_{REF})				ps
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±10	±10	±10	±10	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY	680	680	600	520	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin Setup/Hold with respect to C	0.12/ 0.11	0.15/ 0.13	0.20/ 0.15	0.14/ 0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin Setup/Hold with respect to C	0.11/ 0.15	0.13/ 0.17	0.15/ 0.21	0.10/ 0.23	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin Setup/Hold with respect to C	0.14/ 0.09	0.15/ 0.11	0.17/ 0.13	0.22 0.19	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See TRACE report for actual values.

I/O FIFO Switching Characteristics

Table 22: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T_{OFFCKO_DO}	RDCLK to Q outputs	0.35	0.45	0.45	0.81	ns
T_{CKO_FLAGS}	Clock to IO_FIFO Flags	0.44	0.58	0.58	0.55	ns
Setup/Hold						
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.64/ –0.09	0.80/ –0.08	0.80/ –0.08/	0.76/ –0.05	ns
T_{IFFCCK_WREN} /T_{IFFCKC_WREN}	WREN to WRCLK	0.53/ –0.07	0.69/ –0.07	0.69/ –0.07	0.70/ –0.05	ns
$T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$	RDEN to RDCLK	0.63/ –0.03	0.80/ –0.03	0.80/ –0.03	0.79/ –0.02	ns
Minimum Pulse Width						
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	1.29	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	1.29	ns
Maximum Frequency						
F_{MAX}	RDCLK and WRCLK	266	200	200	200	MHz

CLB Switching Characteristics

Table 23: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	0.15	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	0.41	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	0.65	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	1.51	ns, Max
T_{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	1.01	ns, Max
T_{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	0.98	ns, Max
T_{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	0.98	ns, Max
T_{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	1.08	ns, Max
T_{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	0.82	ns, Max
T_{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	0.99	ns, Max
T_{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	0.69	ns, Max
T_{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	0.86	ns, Max
T_{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	0.84	ns, Max
T_{OPCYA}	An input to COUT output	0.53	0.60	0.73	0.87	ns, Max
T_{OPCYB}	Bn input to COUT output	0.51	0.57	0.70	0.84	ns, Max
T_{OPCYC}	Cn input to COUT output	0.42	0.48	0.59	0.70	ns, Max

Table 23: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{OPCYD}	Dn input to COUT output	0.42	0.48	0.59	0.70	ns, Max
T_{AXCY}	AX input to COUT output	0.45	0.50	0.60	0.73	ns, Max
T_{BXCY}	BX input to COUT output	0.39	0.43	0.52	0.64	ns, Max
T_{CXCY}	CX input to COUT output	0.30	0.34	0.41	0.50	ns, Max
T_{DXCY}	DX input to COUT output	0.30	0.33	0.40	0.49	ns, Max
T_{BYP}	CIN input to COUT output	0.10	0.10	0.12	0.15	ns, Max
T_{CINA}	CIN input to AMUX output	0.41	0.45	0.55	0.66	ns, Max
T_{CINB}	CIN input to BMUX output	0.37	0.43	0.53	0.63	ns, Max
T_{CINC}	CIN input to CMUX output	0.33	0.37	0.44	0.53	ns, Max
T_{CIND}	CIN input to DMUX output	0.38	0.43	0.52	0.62	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	0.62	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	0.73	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D Flip Flops	0.07/ 0.12	0.09/ 0.14	0.11 0.18	0.11 0.20	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D Flip Flops	0.06/ 0.19	0.07/ 0.21	0.09/ 0.26	0.09/ 0.31	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D Flip Flops	0.59/ 0.08	0.66/ 0.09	0.81/ 0.11	0.97/ 0.12	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D Flip Flops	0.15/ 0.00	0.17/ 0.00	0.21/ 0.01	0.34/ –0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.38/ 0.03	0.43/ 0.04	0.53/ 0.05	0.62/ 0.05	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.28/ 0.17	0.31/ 0.19	0.38/ 0.23	0.45/ 0.27	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	0.83	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	0.83	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 24: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.98	1.09	1.32	1.54	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.37	1.53	1.86	2.18	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.54/ 0.28	0.60/ 0.30	0.72/ 0.35	0.96/ 0.40	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.27/ 0.55	0.30/ 0.60	0.37/ 0.70	0.43/ 0.71	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.69/ 0.18	0.77/ 0.21	0.94/ 0.26	1.11/ 0.29	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.38/ 0.10	0.43/ 0.10	0.53/ 0.12	0.62/ 0.13	ns, Min
T_{CECK_LRAM}/ T_{CKCE_LRAM}	CE input to CLK	0.39/ 0.10	0.44/ 0.10	0.53/ 0.11	0.63/ 0.12	ns, Min
Clock CLK						
T_{MPW_LRAM}	Minimum pulse width	0.70	0.82	1.00	0.82	ns, Min
T_{MCP}	Minimum clock period	1.40	1.64	2.00	2.00	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 25: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.19	1.21	1.30	1.89	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.58	1.65	1.84	2.53	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.09	1.14	1.27	1.68	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS_SHFREG}/ T_{WH_SHFREG}	WE input	0.37/ 0.10	0.37/ 0.11	0.37/ 0.13	0.59/ 0.13	ns, Min
T_{CECK_SHFREG}/ T_{CKCE_SHFREG}	CE input to CLK	0.37/ 0.10	0.37/ 0.11	0.37/ 0.13	0.60/ 0.12	ns, Min
T_{DS_SHFREG}/ T_{DH_SHFREG}	A – D inputs to CLK	0.33/ 0.34	0.35/ 0.35	0.40/ 0.39	0.54/ 0.47	ns, Min
Clock CLK						
T_{MPW_SHFREG}	Minimum pulse width	0.60	0.70	0.85	1.04	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.

Block RAM and FIFO Switching Characteristics

Table 26: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	2.10	2.24	2.46	3.24	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.73	0.81	0.94	1.11	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.77	3.20	3.84	5.30	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.73	0.81	0.94	1.11	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	2.61	2.88	3.30	3.76	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.16	1.28	1.46	1.56	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.76	0.87	1.05	1.02	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.94	1.02	1.15	1.30	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.78	0.85	0.94	1.10	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.56	2.95	3.55	4.90	ns, Max
	Clock CLK to BITERR (with output register)	0.68	0.76	0.89	1.05	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.75	0.88	1.07	1.15	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.84	0.93	1.08	1.29	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$	ADDR inputs[8]	0.45/ 0.31	0.49/ 0.33	0.57/ 0.36	0.77/ 0.36	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9]	0.58/ 0.60	0.65/ 0.63	0.74/ 0.67	0.92/ 0.32	ns, Min
$T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode[9]	0.20/ 0.29	0.22/ 0.34	0.25/ 0.41	0.29/ 0.32	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.50/ 0.43	0.55 0.46	0.63/ 0.50	0.78/ 0.37	ns, Min
$T_{RDCK\_DI\_ECCW}/T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only[9]	0.93/ 0.43	1.02/ 0.46	1.17/ 0.50	1.38/ 0.37	ns, Min
$T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode[9]	1.04/ 0.56	1.15/ 0.59	1.32/ 0.64	1.55/ 0.37	ns, Min
$T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.58/ 0.35	0.64/ 0.37	0.74/ 0.40	0.92/ 0.29	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.35/ 0.20	0.39/ 0.21	0.45/ 0.23	0.57/ 0.26	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.24/ 0.15	0.29/ 0.15	0.36/ 0.16	0.34/ 0.07	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.29/ 0.07	0.32/ 0.07	0.35/ 0.07	0.41/ 0.03	ns, Min

Table 26: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.32/ 0.42	0.34/ 0.43	0.36/ 0.46	0.40/ 0.21	ns, Min
$T_{RCCK\_WEA}/T_{RCKC\_WEA}$	Write Enable (WE) input (Block RAM only)	0.44/ 0.18	0.48/ 0.19	0.54/ 0.20	0.64/ 0.23	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.46/ 0.30	0.46/ 0.35	0.47/ 0.43	0.77/ 0.26	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.42/ 0.30	0.43/ 0.35	0.43/ 0.43	0.71/ 0.14	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers(10)	0.90	0.98	1.10	1.25	ns, Max
$T_{RREC\_RST}/T_{RREM\_RST}$	FIFO reset recovery and removal timing(11)	1.87/ –0.81	2.07/ –0.81	2.37/ –0.81	1.34/ –0.09	ns, Max
Maximum Frequency						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	509	460	388	315	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	509	460	388	315	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	447	404	339	268	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	467	418	345	273	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	467	418	345	273	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	405	362	297	226	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	509	460	388	315	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	410	365	297	215	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 27: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.26/ 0.12	0.30/ 0.13	0.37/ 0.14	0.45/ 0.14	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.33/ 0.15	0.38/ 0.16	0.45/ 0.18	0.60/ 0.19	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.17/ 0.17	0.20/ 0.19	0.24/ 0.21	0.34/ 0.29	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.25/ 0.18	0.32/ 0.20	0.42/ 0.22	0.54/ 0.23	ns
$T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.23/ 0.12	0.27/ 0.13	0.32/ 0.14	0.36/ 0.14	ns
$T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.25/ 0.15	0.29/ 0.16	0.36/ 0.18	0.41/ 0.19	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.40/ –0.01	2.76/ –0.01	3.29/ –0.01	4.31/ –0.07	ns
$T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$	{A, D} input to AD register CLK	1.29/ –0.02	1.48/ –0.02	1.76/ –0.02	2.29/ –0.27	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	4.02/ –0.28	4.60/ –0.28	5.48/ –0.28	6.95/ –0.48	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.93/ –0.73	4.50/ –0.73	5.35/ –0.73	6.73/ –1.68	ns
$T_{DSPDCK\_\{A, B\}\ \_PREG}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG}$	A or B input to P register CLK not using multiplier	1.73/ –0.28	1.98/ –0.28	2.35/ –0.28	2.80/ –0.48	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.54/ –0.26	1.76/ –0.26	2.10/ –0.26	2.54/ –0.45	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.32/ –0.15	1.51/ –0.15	1.80/ –0.15	2.13/ –0.25	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.35/ 0.06	0.42/ 0.08	0.52/ 0.11	0.64/ 0.11	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.28/ 0.10	0.34/ 0.11	0.42/ 0.13	0.49/ 0.16	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.36/ –0.03	0.43/ –0.03	0.52/ –0.03	0.68/ 0.14	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.17/ 0.18	0.21/ 0.20	0.27/ 0.23	0.45/ 0.29	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/ 0.01	0.43/ 0.01	0.53/ 0.01	0.63/ 0.00	ns

Table 27: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/ 0.11	0.46/ 0.13	0.55/ 0.15	0.63/ 0.40	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/ 0.10	0.08/ 0.11	0.09/ 0.12	0.13/ 0.11	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/ 0.07	0.50/ 0.08	0.59/ 0.09	0.67/ 0.08	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/ 0.22	0.23/ 0.24	0.27/ 0.28	0.28/ 0.35	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.27/ 0.01	0.30/ 0.01	0.35/ 0.01	0.43/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18	6.61	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.72	4.26	5.07	6.41	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier	1.53	1.75	2.08	2.48	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.33	1.53	1.82	2.22	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74	0.87	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54	7.03	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40	6.81	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41	2.88	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.58	1.81	2.15	2.62	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.65	4.19	5.00	6.40	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.37	1.57	1.88	2.44	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.38	0.44	0.53	0.63	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33	6.79	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21	2.84	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	1.11	1.28	1.52	1.82	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85	2.21	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.37	0.44	0.54	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69	0.84	ns

Table 27: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.68	1.93	2.31	2.73	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64	3.12	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.72	3.10	3.69	4.60	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02	4.99	ns
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	6.84	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.65	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.81	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	6.77	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	1.02	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	7.24	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	3.04	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	7.17	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	3.20	ns
Maximum Frequency						
F_{MAX}	With all registers used	628	550	464	363	MHz
F_{MAX_PATDET}	With pattern detector	531	465	392	310	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349	305	257	210	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317	277	233	191	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397	346	290	223	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397	346	290	223	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260	227	190	150	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241	211	177	140	MHz

Clock Buffers and Networks

Table 28: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	0.14/ 0.24	0.14/ 0.26	0.20/ 0.32	0.31/ 0.17	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.14/ 0.24	0.14/ 0.26	0.20/ 0.32	0.31/ 0.17	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.09	0.09	0.12	0.14	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628	550	464	394	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 29: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	0.96	1.06	1.36	1.50	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680	680	600	600	MHz

Table 30: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.55	0.58	0.76	1.08	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.20	0.23	0.36	0.57	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.74	0.81	0.95	0.96	ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	420	375	315	315	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 31: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BHCKO_O}	BUFH delay from I to O	0.11	0.11	0.15	0.16	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.21/ 0.14	0.23/ 0.15	0.27/ 0.22	0.35/ 0.08	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	628	550	464	394	MHz

Table 32: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.20	0.20	0.20	0.25	ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC7A100T	0.31	0.36	0.39	0.53	ns
		XC7A200T	0.49	0.54	0.59	0.76	ns
		XC7A350T	0.53	0.58	0.62	0.79	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.02	0.02	0.03	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.18	0.18	0.18	0.18	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 33: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$MMCM\_F_{INMAX}$	Maximum Input Clock Frequency	800	800	800	800	MHz
$MMCM\_F_{INMIN}$	Minimum Input Clock Frequency	10	10	10	10	MHz
$MMCM\_F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
$MMCM\_F_{INDUTY}$	Allowable Input Duty Cycle: 10—49 MHz	25	25	25	25	%
	Allowable Input Duty Cycle: 50—199 MHz	30	30	30	30	%
	Allowable Input Duty Cycle: 200—399 MHz	35	35	35	35	%
	Allowable Input Duty Cycle: 400—499 MHz	40	40	40	40	%
	Allowable Input Duty Cycle: >500 MHz	45	45	45	45	%
$MMCM\_F_{MIN\_PSCLK}$	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
$MMCM\_F_{MAX\_PSCLK}$	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
$MMCM\_F_{VCOMIN}$	Minimum MMCM VCO Frequency	600	600	600	600	MHz

Table 33: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$MMCM\_F_{VCOMAX}$	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
$MMCM\_F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical(1)	4.00	4.00	4.00	4.00	MHz
$MMCM\_T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs(2)	0.12	0.12	0.12	0.12	ns
$MMCM\_T_{OUTJITTER}$	MMCM Output Jitter(3)	Note 1				
$MMCM\_T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision(4)	0.20	0.20	0.20	0.25	ns
$MMCM\_T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	100	100	µs
$MMCM\_F_{OUTMAX}$	MMCM Maximum Output Frequency	800	800	800	800	MHz
$MMCM\_F_{OUTMIN}$	MMCM Minimum Output Frequency(5)(6)	4.69	4.69	4.69	4.69	MHz
$MMCM\_T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
$MMCM\_RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	ns
$MMCM\_F_{PFDMAX}$	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
$MMCM\_F_{PFDMIN}$	Minimum Frequency at the Phase Frequency Detector	10	10	10	10	MHz
$MMCM\_T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
MMCM Switching Characteristics Setup and Hold						
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and Hold of Phase Shift Enable	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.59	0.68	0.81	0.78	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR Setup/Hold	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI Setup/Hold	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN Setup/Hold	1.76/ 0.00	1.97/ 0.00	2.29/ 0.00	2.40/ 0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE Setup/Hold	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.65	0.72	0.99	0.70	ns, Max
F_{DCK}	DCLK frequency	200	200	200	100	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, $MMCM\_F_{OUTMIN}$ is 0.036 MHz.

PLL Switching Characteristics

Table 34: **PLL Specification**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F_{INMAX}	Maximum Input Clock Frequency	800	800	800	800	MHz
PLL_F_{INMIN}	Minimum Input Clock Frequency	19	19	19	19	MHz
PLL_$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable Input Duty Cycle: 19—49 MHz	25	25	25	25	%
	Allowable Input Duty Cycle: 50—199 MHz	30	30	30	30	%
	Allowable Input Duty Cycle: 200—399 MHz	35	35	35	35	%
	Allowable Input Duty Cycle: 400—499 MHz	40	40	40	40	%
	Allowable Input Duty Cycle: >500 MHz	45	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO Frequency	800	800	800	800	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO Frequency	2133	1866	1600	1600	MHz
PLL_$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical(1)	1.00	1.00	1.00	1.00	MHz
	High PLL Bandwidth at Typical(1)	4.00	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static Phase Offset of the PLL Outputs(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL Output Jitter(3)	Note 1				
PLL_$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision(4)	0.20	0.20	0.20	0.25	ns
PLL_$T_{LOCKMAX}$	PLL Maximum Lock Time	100	100	100	100	µs
PLL_F_{OUTMAX}	PLL Maximum Output Frequency	800	800	800	800	MHz
PLL_F_{OUTMIN}	PLL Minimum Output Frequency(5)	6.25	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
PLL_$RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
PLL_F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19	19	19	19	MHz
PLL_$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T_{PLLDCK_DADDR}/ T_{PLLCKD_DADDR}	DADDR Setup/Hold	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns, Min
T_{PLLDCK_DI}/ T_{PLLCKD_DI}	DI Setup/Hold	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns, Min
T_{PLLDCK_DEN}/ T_{PLLCKD_DEN}	DEN Setup/Hold	1.76/ 0.00	1.97/ 0.00	2.29/ 0.00	2.40/ 0.00	ns, Min
T_{PLLDCK_DWE}/ T_{PLLCKD_DWE}	DWE Setup/Hold	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.70	ns, Max

Table 34: **PLL Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F_{DCK}	DCLK frequency	200	200	200	100	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 35: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Clock-capable clock input and OUTFF *without* MMCM/PLL (near clock region)	XC7A100T	6.27	6.72	7.97	7.93	ns
		XC7A200T	6.65	7.11	8.39	8.42	ns
		XC7A350T	6.91	7.34	8.57	8.59	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 36: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF *without* MMCM/PLL (far clock region)	XC7A100T	6.58	7.01	8.34	8.37	ns
		XC7A200T	7.47	7.90	9.41	9.60	ns
		XC7A350T	7.67	8.07	9.51	9.70	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 37: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7A100T	2.71	1.60	1.76	2.81	ns
		XC7A200T	2.77	1.66	1.81	2.88	ns
		XC7A350T	2.80	1.69	1.82	2.89	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 38: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.							
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7A100T	1.34	1.27	1.43	2.26	ns
		XC7A200T	1.40	1.33	1.48	2.34	ns
		XC7A350T	1.43	1.36	1.49	2.35	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 39: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{ICKOFCS}$	Clock to out of I/O clock	6.19	6.74	8.03	7.93	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks	XC7A100T	2.34/ –0.53	2.88/ –0.53	3.12/ –0.53	1.77/ 0.35	ns
		XC7A200T	2.63/ –0.31	3.26/ –0.31	3.48/ –0.31	0.87/ 1.47	ns
		XC7A350T	2.99/ –0.47	3.69/ –0.47	4.05/ –0.47	0.85/ 1.56	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Table 41: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay clock-capable clock input and IFF(2) with MMCM	XC7A100T	1.72/ –0.31	2.62/ –0.31	3.13/ –0.31	1.92/ –0.28	ns
		XC7A200T	1.85/ –0.23	2.77/ –0.23	3.29/ –0.23	2.09/ –0.24	ns
		XC7A350T	1.84/ –0.23	2.76/ –0.23	3.29/ –0.23	2.09/ –0.23	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 42: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No Delay clock-capable clock input and IFF(2) with PLL	XC7A100T	2.42/ –0.44	2.93/ –0.44	3.47/ –0.44	2.24/ –0.68	ns
		XC7A200T	2.55/ –0.36	3.07/ –0.36	3.63/ –0.36	2.42/ –0.63	ns
		XC7A350T	2.55/ –0.36	3.07/ –0.36	3.63/ –0.36	2.42/ 0.00	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.40/ 1.33	–0.40/ 1.45	–0.40/ 1.70	–0.60/ 1.88	ns

Table 44: **Sample Window**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{SAMP}	Sampling Error at Receiver Pins(1)	0.61	0.67	0.72	0.72	ns
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	0.36	0.42	0.48	0.48	ns

Notes:

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

Table 45: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC7A100T	CSG324		ps
			FTG256		ps
			FGG484		ps
			FGG676		ps
		XC7A200T	SBG484		ps
			FBG484		ps
			FBG676		ps
			FFG1156		ps
		XC7A350T	FBG484		ps
			FBG676		ps
			FFG1156		ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

GTP Transceiver Specifications

GTP Transceiver DC Characteristics

Table 46: **GTP Transceiver Current Supply**

Symbol	Description	Typ(1)	Max	Units
$I_{MGTAVCC}$	MGTAVCC supply current for one GTP Quad (4 lanes)		Note 2	mA
$I_{MGTAVTT}$	MGTAVTT supply current for one GTP Quad (4 lanes)			mA

Notes:
1. Typical values are specified at nominal voltage, 25°C, at the maximum line rate.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 47: **GTP Transceiver Quiescent Supply Current(1)(2)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTP Quad (4 lanes)		Note 3	mA
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTP Quad (4 lanes)			mA

Notes:
1. Device powered and unconfigured.
2. GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. Typical values are specified at nominal voltage, 25°C.

GTP Transceiver DC Input and Output Levels

Table 48 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further details.

Table 48: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled		–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTT = 1.2V	–200	–	MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT = 1.2V	–	2/3 MGTAVTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	MGTAVTT – DV_{PPOUT}/4			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled		1/2 MGTAVTT			mV
R_{IN}	Differential input resistance			100		Ω
R_{OUT}	Differential output resistance			100		Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (Flip-chip packages)		–	–	10	ps
	Transmitter output pair (TXP and TXN) intra-pair skew (Wire-bond packages)		–	–	12	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG482: *7 Series FPGAs GTP Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

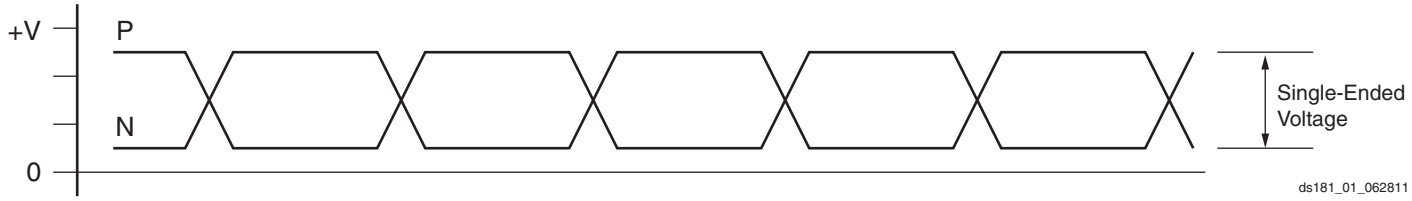

Figure 1: **Single-Ended Peak-to-Peak Voltage**

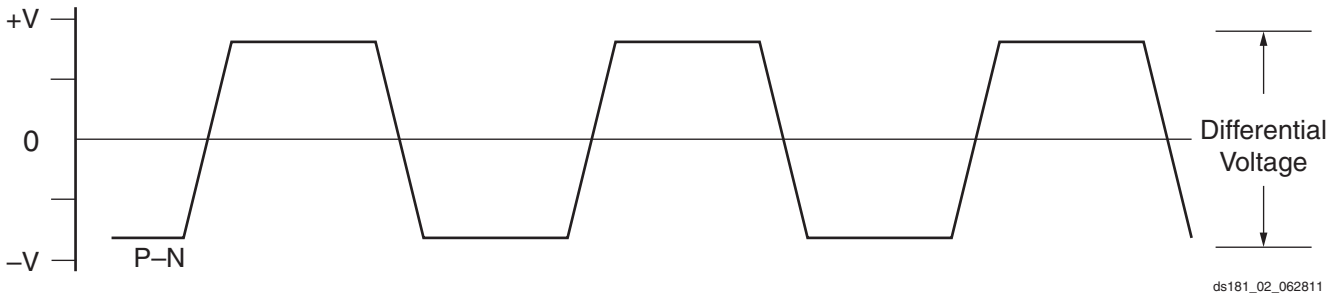

Figure 2: **Differential Peak-to-Peak Voltage**

Table 49 summarizes the DC specifications of the clock input of the GTP transceiver. Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further details.

Table 49: **GTP Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250		2000	mV
R_{IN}	Differential input resistance		100		Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further information.

Table 50: **GTP Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade				Units
			1.0V			0.9V	
			-3(1)	-2/-2L(1)	-1	-2L	
F_{GTPMAX}	Maximum GTP transceiver data rate		6.6	6.6	3.75	3.75	Gb/s
F_{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	0.500	Gb/s
$F_{GTPRANGE}$	PLL line rate range	1	3.2–6.6	3.2–6.6	3.2–3.75	3.2–3.75	Gb/s
		2	1.6–3.3	1.6–3.3	1.6–3.2	1.6–3.2	Gb/s
		4	0.8–1.65	0.8–1.65	0.8–1.6	0.8–1.6	Gb/s
		8	0.5–0.825	0.5–0.825	0.5–0.8	0.5–0.8	Gb/s
$F_{GTPPLLRANGE}$	GTP transceiver PLL frequency range		1.6–3.3	1.6–3.3	1.6–3.3	1.6–3.3	GHz

Notes:

1. F_{GTPMAX} is limited to 5.4 Gb/s in wire bond packages.

Table 51: **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$F_{GTPDRPCLK}$	GTPDRPCLK maximum frequency	156	156	125	125	MHz

Table 52: **GTP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{TXOUT}	TXUSERCLKOUT maximum frequency		60	–	660	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–		ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–		µs

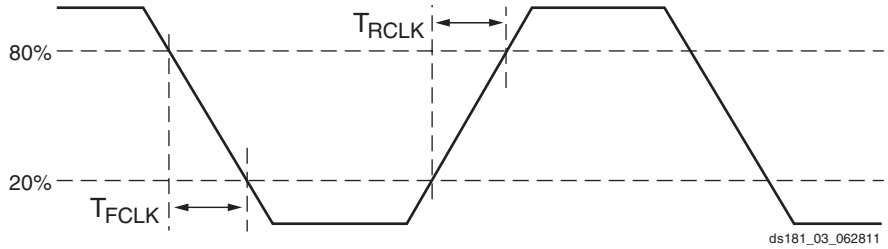

Figure 3: **Reference Clock Timing Parameters**

Table 53: **GTP Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
F_{GLK}	Reference clock frequency range		412.5	412.5	234.375	234.375	MHz
F_{RXOUT}	RXOUTCLKT maximum frequency		412.5	412.5	234.375	234.375	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.5	412.5	234.375	234.375	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.5	412.5	234.375	234.375	MHz

Notes:

1. Clocking must be implemented as described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 54: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK}$	User clock maximum frequency	250	250	250	250	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250	250	250	250	MHz
F_{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

XADC Specifications

Table 55: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, T_j = –40°C to 100°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±2	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±4	LSBs
Gain Error		Gain calibration disabled	–	–	±0.4	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.2	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio(2)	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion(2)	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	70	–	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs(3)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T_j = –40°C to 100°C.	–	–	±4	°C
		T_j = –55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to +100°C	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to +125°C	–	–	±2	%
Conversion Rate(4)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Table 55: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference[5]						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset errors are removed by enabling the XADC automatic offset calibration feature. All values provided are with this feature enabled.
2. Only specified for new BitGen option XADCEnhancedLinearity = ON.
3. See the ADC chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
4. See the Timing chapter in UG480: *7 Series FPGAs XADC User Guide* for a detailed description.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 56: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T_{PL}[1]	Program latency	5	5	5	5	ms, Max
T_{POR}[1]	Power-on reset (50ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1ms ramp rate time)	10/38	10/38	10/38	10/38	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250	250	250	250	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay	150	150	150	150	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency	100	100	100	70	MHz, Max
	Master CCLK frequency for AES encrypted x16	50	50	50	50	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration	3	3	3	3	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave CCLK frequency	100	100	100	70	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time	2.5	2.5	2.5	2.5	ns, Min
T_{EMCCKH}	External master CCLK High time	2.5	2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency	100	100	100	70	MHz, Max
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T_{CCO}	DOUT clock to out	8.0	8.0	8.0	9.0	ns, Max

Table 56: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	D[31:00] Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	10.0/0.0	12.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7.0	7.0	7.0	8.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback	8.0	8.0	8.0	10.0	ns, Max
F_{RBCCK}	Readback frequency	100	100	100	70	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup/Hold	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.0	7.0	7.0	8.5	ns, Max
F_{TCK}	TCK frequency	66	66	66	50	MHz, Max
BPI Master Flash Mode Programming Switching						
T_{BPICCO}(2)	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.5	8.5	8.5	10.0	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
SPI Master Flash Mode Programming Switching						
T_{SPIDCC}/T_{SPICCD}	D[03:00] Setup/Hold	3.0/0.0	3.0/0.0	3.0/0.0	3.0/0.0	ns, Min
T_{SPICCM}	MOSI clock to out	8.0	8.0	8.0	9.0	ns, Max
$T_{SPICCFC}$	FCS_B clock to out	8.0	8.0	8.0	9.0	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in UG470: *7 Series FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 57 lists the programming conditions specifically for eFUSE. For more information, see UG470: *7 Series FPGA Configuration User Guide*.

Table 57: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document:

Date	Version	Description
09/26/11	1.0	Initial Xilinx release.
11/07/11	1.1	Revised the V_{OCM} specification in Table 10. Updated the AC Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 11 and Table 12. Added MMCM_$T_{FBDELAY}$ while adding MMCM_ to the symbol names of a few specifications in Table 33 and PLL to the symbol names in Table 34. In Table 35 through Table 42, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 46.
02/13/12	1.2	Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the AC Switching Characteristics based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade. Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Updated the notes in Table 4. Added MGTAVCC and MGTAVTT power supply ramp times to Table 6. Rearranged Table 7, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 8 and Table 9. Revised the specifications in Table 10. Revised V_{IN} in Table 48. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the I/O FIFO Switching Characteristics table. Revised F_{TXIN} and F_{RXIN} in Table 53. Revised I_{CCADC} and updated Note 1 in Table 55. Revised DDR LVDS transmitter data width in Table 13. Removed notes from Table 23 as they are no longer applicable. Updated specifications in Table 56. Updated Note 1 in Table 32.
06/01/12	1.3	Reorganized entire data sheet including adding Table 39 and Table 43. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Updated Power-On/Off Power Supply Sequencing section with regards to GTP transceivers. In Table 7, updated many parameters including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 9. Updated V_{OL} in Table 10. Updated Table 13 and removed notes 2 and 3. Updated Table 14. Updated the AC Switching Characteristics based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document. In Table 26, updated Reset Delays section including Note 10 and Note 11. In Table 53, replaced F_{TXOUT} with F_{GLK}. Updated many of the XADC specifications in Table 55 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 56 to Table 33 and Table 34.

Notice of Disclaimer