Space-Grade Virtex-4QV FPGAs: DC and Switching Characteristics

DS680 (v2.0) April 12, 2010 **Product Specification**

Virtex-4QV FPGA Electrical Characteristics

Space-grade, radiation-tolerant Virtex®-4QV FPGAs are available in the -10 speed grade and qualified for military (T_j = –55° C to +125° C) operational temperatures.

Virtex-4QV FPGA DC and AC characteristics are specified for military temperatures only. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -10 speed grade military device are the same as for a -10 speed grade industrial device).

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Virtex-4QV FPGA data sheet is part of an overall set of documentation on the Virtex-4 family of FPGAs available on the Xilinx website:

- DS653, *Space-Grade Virtex-4QV Family Overview*
- UG070, *Virtex-4 FPGA User Guide*
- UG071, *Virtex-4 FPGA Configuration Guide*
- UG073, *XtremeDSP for Virtex-4 FPGAs*
- UG496, *Virtex-4QV FPGA Ceramic Packaging and Pinout Specifications*
- UG072, *Virtex-4 FPGA PCB Designer's Guide*

Virtex-4QV FPGA DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.75	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.05	V
V_{REF}	Input reference voltage	–0.3 to 3.75	V
V_{IN}	I/O input voltage relative to GND (all user and dedicated I/Os)	–0.75 to 4.05	V
	I/O input voltage relative to GND(3) (restricted to maximum of 100 user I/Os)(4)	–0.85 to 4.3	V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	–0.75 to V_{CCO} +0.5	V
V_{TS}	Voltage applied to 3-state 3.3V output(3) (all user and dedicated I/Os)	–0.75 to 4.05	V
	Voltage applied to 3-state 3.3V output(3) (restricted to maximum of 100 user I/Os)(4)	–0.85 to 4.3	V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	–0.75 to V_{CCO} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(2)	+220	°C
T_J	Maximum junction temperature(2)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the *Virtex-4QV FPGA Ceramic Packaging and Pinout Specifications* on the Xilinx website.
3. For 3.3V I/O operation, refer to the *Virtex-4 FPGA User Guide*, *Chapter 6, 3.3V I/O Design Guidelines, Table 6-38.*
4. For more flexibility in specific designs, a maximum of 100 user I/Os can be stressed beyond the normal spec for no more than 20% of a data period. There are no bank restrictions.

Table 2: **Recommended Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND	1.14	1.26	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	2.375	2.625	V
V_{CCO}(1,2,3,4,5))	Supply voltage relative to GND	1.14	3.45	V
V_{IN}	3.3V supply voltage relative to GND	GND – 0.20	3.45	V
	2.5V and below supply voltage relative to GND	GND – 0.20	V_{CCO} + 0.2	V
V_{BATT}(2)	Battery voltage relative to GND	1.0	3.6	V

Notes:

1. Configuration data is retained even if V_{CCO} drops to 0V.
2. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
3. For 3.3V I/O operation, refer to the *Virtex-4 FPGA User Guide*.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The configuration output supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.9			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0			V
I_{REF}	V_{REF} current per pin			10	µA
I_L	Input or output leakage current per pin (sample-tested)			10	µA
C_{IN}	Input capacitance (sample-tested)			10	pF
I_{RPU}(1)	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	5		200	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.0V	5		125	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	5		120	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	5		60	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	5		40	µA
I_{RPD}(1)	Pad pull-down (when selected) @ V_{IN} = V_{CCO}	5		100	µA
I_{BATT}(1)	Battery supply current		75		nA
P_{CPU}	Power dissipation of PowerPC® 405 processor block		0.45		mW/ MHz
n	Temperature diode ideality factor		1.02		n
r	Series resistance		2		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.

Table 4: **Quiescent Supply Current**

Symbol	Description	Device	Typ(1)	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XQR4VSX55	488	Note (4)	mA
		XQR4VFX60	365	Note (4)	mA
		XQR4VFX140	796	Note (4)	mA
		XQR4VLX200	880	Note (4)	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XQR4VSX55	3.00	Note (4)	mA
		XQR4VFX60	3.00	Note (4)	mA
		XQR4VFX140	5.00	Note (4)	mA
		XQR4VLX200	5.00	Note (4)	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XQR4VSX55	137	Note (4)	mA
		XQR4VFX60	120	Note (4)	mA
		XQR4VFX140	215	Note (4)	mA
		XQR4VLX200	225	Note (4)	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the Power Estimator or XPOWER tool.
4. Use the XPower™ Estimator (XPE) tool to calculate maximum static power for specific process, voltage, and temperature conditions.

Power-On Power Supply Requirements

Xilinx® FPGAs require a certain amount of supply current during power-on to ensure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The power supplies can be turned on in any sequence, though the specifications shown in Table 5 are for the recommended power-on sequence of V_{CCINT}, V_{CCAUX}, V_{CCO}. Xilinx does not specify the current for other power-on sequences.

Table 5 shows the maximum current required by Virtex-4 devices for proper power-on and configuration.

Once initialized and configured, use the XPOWER tool to estimate current drain on these supplies.

Table 5: **Maximum Power-On Current for Virtex-4QV Devices**

Device	I_{CCINT}		I_{CCAUX}		I_{CCO}		Units
	Typ(1)	Max(2)	Typ(1)	Max(2)	Typ(1)	Max(2)	
XQR4VSX55	520	5355	225	930	150	450	mA
XQR4VFX60	410	4680	220	1050	150	435	mA
XQR4VFX140	860	9540	450	1313	250	563	mA
XQR4VLX200	1020	8820	500	1313	250	600	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum values are specified under worst-case process, voltage, and military temperature conditions.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Unless otherwise noted, values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **Select I/O DC Input and Output Levels**

IOSTANDARD Attribute	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.2	0.8	2.0	3.45	0.4	2.4	Note(3)	Note(3)
LVCMOS33	–0.2	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	Note(3)	Note(6)
LVCMOS25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.4	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.4	V_{CCO} – 0.45	Note(4)	Note(6)
PCI33_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI66_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI-X(5)	–0.2	35% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
GTLP	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	–	0.6	–	36	–
GTL	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	–	0.4	–	32	–
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
HSTL IV(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	48	–8
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	0.5	V_{CCO} – 0.5	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	–	–

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. For more information on PCI33_3, PCI66_3, and PCIX, refer to the *Virtex-4 FPGA User Guide, SelectIO Resources, Chapter 6*.
6. LVCMOS15 4 mA, LVCMOS33 6 mA, LVCMOS33 8 mA have reduced drive strength (I_{OH}) by 20%.

LDT DC Specifications (LDT_25)

Table 8: **LDT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage(1,2)	R_T = 100Ω across Q and $\overline{Q}$ signals	495	600	750	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15		15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15		15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15		15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15		15	mV

Notes:

1. Recommended input maximum voltage not to exceed V_{CCO} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals			1.602	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.898			V
V_{ODIFF}	Differential Output Voltage(1,2) (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	550	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.100	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCO} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	380	–	820	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage(1,2) (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CC} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, for example, a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-4 FPGA User Guide*: *Chapter 6, SelectIO Resources*.

Table 11: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6		2.2	V
V_{IDIFF}	Differential Input Voltage(1,2)	0.100		1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCO} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

Interface Performance Characteristics

Table 12: **Interface Performances**

Description	Speed Grade
	-10
Networking Applications	
SFI-4.1 (SDR LVDS Interface)(5)	500 MHz
SPI-4.2 (DDR LVDS Interface)	800 Mb/s
Memory Interfaces	
DDR(1)	426 Mb/s
DDR2(2)	510 Mb/s
QDR II SRAM(3)	514 Mb/s
RLDRAM II(4)	524 Mb/s

Notes:

1. Performance defined using design implementation described in application note XAPP709: *DDR SDRAM Controller Using Virtex-4 FPGA Devices*.
2. Performance defined using design implementation described in application note XAPP702: *DDR2 Controller Using Virtex-4 Devices*.
3. Performance defined using design implementation described in application note XAPP703: *QDR II SRAM Interface for Virtex-4 Devices*.
4. Performance defined using design implementation described in application note XAPP710: *Synthesizable CIO DDR RLDRAM II Controller for Virtex-4 FPGAs*.
5. 644 MHz not supported for operating temperatures above 100°C.

Switching Characteristics

Switching characteristics are specified on a per-speed- grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Table 13 correlates the current status of each Virtex-4QV device with a corresponding speed specification version 1.67 designation.

Table 13: **Virtex-4QV Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XQR4VSX55			-10
XQ4RVFX60			-10
XQR4VFX140			-10
XQR4VLX200			-10

Because individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-4QV FPGAs.

PowerPC Processor Switching Characteristics

Consult UG018, *PowerPC 405 Processor Block Reference Guide* for further information.

Table 14: **PowerPC 405 Processor Clocks Absolute AC Characteristics**

Description	Speed Grade		Units
	-10		
	Min	Max	
Characteristics when APU *Not* Used			
CPMC405CLOCK frequency(1,4)	0	350	MHz
CPMDCRCLK(3)	0	350	MHz
CPMFCMCLK(3)	–	–	MHz
JTAGC405TCK frequency(2)	0	175	MHz
PLBCLK(3)	0	350	MHz
BRAMDSOCMCLK(3)	0	350	MHz
BRAMISOCMCLK(3)	0	350	MHz
Characteristics when APU Used			
CPMC405CLOCK frequency(1,4)	0	233	MHz
CPMDCRCLK(3)	0	233	MHz
CPMFCMCLK(3)	0	233	MHz
JTAGC405TCK frequency(2)	0	116.5	MHz
PLBCLK(3)	0	233	MHz
BRAMDSOCMCLK(3)	0	233	MHz
BRAMISOCMCLK(3)	0	233	MHz

Notes:

1. Worst-case DCM output clock jitter is included in these specifications.
2. The theoretical maximum frequency of this clock is one-half the CPMC405CLOCK. However, the achievable maximum is system dependent, and will be much less.
3. The theoretical maximum frequency of these clocks is equal to the CPMC405CLOCK. Integer clock ratios are required for the CPMC405CLOCK and BRAMDSOCMCLK, CPMC405CLOCK and BRAMISOCMCLK, CPMC405CLOCK and CPMDCRCLK, CPMC405CLOCK and CPMFCMCLK, and CPMC405CLOCK and PLBCLK. The integer ratios can be different for each interface. However, the achievable maximum is system dependent.
4. Maximum operating frequency of CPMC405CLOCK is specified with the input pin TIEC405DISOPERANDFWD connected to a logic 1.

Table 15: **Processor Block Switching Characteristics**

Description	Symbol	Speed Grade	Units
		-10	
Setup and Hold Relative to Clock (CPMC405CLOCK)			
Clock and Power Management control inputs	$T_{PPCDCK\_CORECKI}$ $T_{PPCCKD\_CORECKI}$	0.74 0.23	ns Min
Reset control inputs	$T_{PPCDCK\_RSTCHIP}$ $T_{PPCCKD\_RSTCHIP}$	0.74 0.23	ns Min
Debug control inputs	$T_{PPCDCK\_EXBUSHAK}$ $T_{PPCCKD\_EXBUSHAK}$	0.74 0.23	ns Min
Trace control inputs	T_{PPCDCK_TRCDIS} T_{PPCCKD_TRCDIS}	0.74 0.23	ns Min
External Interrupt Controller control inputs	$T_{PPCDCK\_CINPIRQ}$ $T_{PPCCKD\_CINPIRQ}$	1.40 0.23	ns Min
Clock to Out			
Clock and Power Management control outputs	$T_{PPCCKO\_CORESLP}$	1.74	ns Max
Reset control outputs	$T_{PPCCKO\_RSTCHIP}$	1.83	ns Max
Debug control outputs	$T_{PPCCKO\_DBGLDAPU}$	1.70	ns Max
Trace control outputs	$T_{PPCCKO\_TRCCYCLE}$	1.83	ns Max
Clock			
CPMC405CLOCK minimum pulse width, High	T_{CPWH}	1.43	ns Min
CPMC405CLOCK minimum pulse width, Low	T_{CPWL}	1.43	ns Min

Table 16: **Processor Block PLB Switching Characteristics**

Description	Symbol	Speed Grade	Units
		-10	
Setup and Hold Relative to Clock (PLBCLK)			
Processor Local Bus (ICU/DCU) control inputs	$T_{PPCDCK\_ICUBUSY}$ $T_{PPCCKD\_ICUBUSY}$	0.76 0.23	ns Min
Processor Local Bus (ICU/DCU) data inputs	$T_{PPCDCK\_ICURDDB}$ $T_{PPCCKD\_ICURDDB}$	1.15 0.23	ns Min
Clock to Out			
Processor Local Bus (ICU/DCU) control outputs	$T_{PPCCKO\_DCUABORT}$	2.05	ns Max
Processor Local Bus (ICU/DCU) address bus outputs	$T_{PPCCKO\_ICUABUS}$	2.13	ns Max
Processor Local Bus (ICU/DCU) data bus outputs	$T_{PPCCKO\_DCUWRDBUS}$	2.57	ns Max

Table 17: **Processor Block JTAG Switching Characteristics**

Description	Symbol	Speed Grade	Units
		-10	
Setup and Hold Relative to Clock (JTAGC405TCK)			
JTAG control inputs	T_{PPCDCK_JTGTDI} T_{PPCCKD_JTGTDI}	1.48 0.23	ns Min
JTAG reset input	$T_{PPCDCK\_JTGTRSTN}$ $T_{PPCCKD\_JTGTRSTN}$	0.74 0.23	ns Min
Clock to Out			
JTAG control outputs	T_{PPCCKO_JTGTDO}	2.14	ns Max

Table 18: **PowerPC 405 Data-Side On-Chip Memory Switching Characteristics**

Description	Symbol	Speed Grade	Units
		-10	
Setup and Hold Relative to Clock (BRAMDSOCMCLK)			
Data-Side On-Chip Memory data bus inputs	$T_{PPCDCK\_DSOCMRDDB}$ $T_{PPCCKD\_DSOCMRDDB}$	0.74 0.23	ns Min
Clock to Out			
Data-Side On-Chip Memory control outputs	$T_{PPCCKO\_BRAMBWR}$	2.65	ns Max
Data-Side On-Chip Memory address bus outputs	$T_{PPCCKO\_BRAMABUS}$	2.65	ns Max
Data-Side On-Chip Memory data bus outputs	$T_{PPCCKO\_IBRAMWRDBUS01}$	2.06	ns Max

Table 19: **PowerPC 405 Instruction-Side On-Chip Memory Switching Characteristics**

Description	Symbol	Speed Grade	Units
		-10	
Setup and Hold Relative to Clock (BRAMISOCMCLK)			
Instruction-Side On-Chip Memory data bus inputs	$T_{PPCDCK\_ISOCMRDDB}$ $T_{PPCCKD\_ISOCMRDDB}$	0.94 0.23	ns Min
Clock to Out			
Instruction-Side On-Chip Memory control outputs	$T_{PPCCKO\_IBRAMEN}$	3.88	ns Max
Instruction-Side On-Chip Memory address bus outputs	$T_{PPCCKO\_IBRAMRDABUS}$	2.13	ns Max
Instruction-Side On-Chip Memory data bus outputs	$T_{PPCCKO\_IBRAMWRDBUS}$	2.14	ns Max

Table 20: **Processor Block DCR Bus Switching Characteristics**

Description	Symbol	Speed Grade	Units
		-10	
Setup and Hold Relative to Clock (CPMDCRCLOCK)			
Device Control Register Bus control inputs	$T_{PPCDCK\_EXDCRACK}$ $T_{PPCCKD\_EXDCRACK}$	0.15 0.19	ns Min
Device Control Register Bus data inputs	$T_{PPCDCK\_EXDCRDBUSI}$ $T_{PPCCKD\_EXDCRDBUSI}$	1.02 0.27	ns Min
Clock to Out			
Device Control Register Bus control outputs	$T_{PPCCKO\_EXDCRRD}$	1.54	ns Max
Device Control Register Bus address bus outputs	$T_{PPCCKO\_EXDCRABUS}$	1.66	ns Max
Device Control Register Bus data bus outputs	$T_{PPCCKO\_EXDCRDBUSO}$	1.67	ns Max

Table 21: **Processor Block APU Interface Switching Characteristics**

Description	Symbol	Speed Grade	Units
		-10	
Setup and Hold Relative to Clock (CPMDFCMCLOCK)			
APU bus control inputs	$T_{PPCDCK\_DCDCREN}$ $T_{PPCCKD\_DCDCREN}$	0.42 0.23	ns Min
APU bus data inputs	T_{PPCDCK_RESULT} T_{PPCCKD_RESULT}	0.78 0.23	ns Min
Clock to Out			
APU bus control outputs	$T_{PPCCKO\_APUFCMDEC}$	2.00	ns Max
APU bus data outputs	T_{PPCCKO_RADATA}	2.00	ns Max

IOB Pad Input/Output/3-State Switching Characteristics

Table 22 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO™ input buffer technology.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 24, page 16 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (for example, a high-impedance state).

Table 22: **IOB Switching Characteristics(1,2)**

IOSTANDARD Attribute(1)	Speed Grade			Units
	-10			
	T_{IOPI}	T_{IOOP}	T_{IOTP}	
LVDS_25	1.28	1.85	1.85	ns
RSDS_25	1.28	1.85	1.85	ns
LVDSEXT_25	1.30	1.91	1.91	ns
LDT_25	1.28	1.82	1.82	ns
BLVDS_25	1.28	2.34	2.34	ns
ULVDS_25	1.28	1.83	1.83	ns
PCI33_3 (PCI, 33 MHz, 3.3V)	0.97	3.02	3.02	ns
PCI66_3 (PCI, 66 MHz, 3.3V)	0.97	2.72	2.72	ns
PCI-X	0.97	2.25	2.25	ns
GTL	1.63	2.03	2.03	ns
GTLP	1.68	2.03	2.03	ns
HSTL_I	1.64	2.35	2.35	ns
HSTL_II	1.64	2.13	2.13	ns
HSTL_III	1.64	2.22	2.22	ns
HSTL_IV	1.64	2.03	2.03	ns
HSTL_I _18	1.60	2.21	2.21	ns
HSTL_II _18	1.60	2.16	2.16	ns
HSTL_III _18	1.60	2.09	2.09	ns
HSTL_IV_18	1.60	2.06	2.06	ns
SSTL2_I	1.68	2.43	2.43	ns
SSTL2_II	1.68	2.16	2.16	ns
LVTTL, Slow, 2 mA	0.97	7.03	7.03	ns
LVTTL, Slow, 4 mA	0.97	5.04	5.04	ns
LVTTL, Slow, 6 mA	0.97	4.91	4.91	ns
LVTTL, Slow, 8 mA	0.97	4.91	4.91	ns
LVTTL, Slow, 12 mA	0.97	3.96	3.96	ns
LVTTL, Slow, 16 mA	0.97	3.46	3.46	ns
LVTTL, Slow, 24 mA	0.97	3.12	3.12	ns
LVTTL, Fast, 2 mA	0.97	4.86	4.86	ns
LVTTL, Fast, 4 mA	0.97	3.46	3.46	ns
LVTTL, Fast, 6 mA	0.97	3.00	3.00	ns

Table 22: **IOB Switching Characteristics(1,2) *(Cont'd)***

IOSTANDARD Attribute(1)	Speed Grade			Units
	-10			
	T_{IOPI}	T_{IOOP}	T_{IOTP}	
LVTTL, Fast, 8 mA	0.97	2.79	2.79	ns
LVTTL, Fast, 12 mA	0.97	2.47	2.47	ns
LVTTL, Fast, 16 mA	0.97	2.47	2.47	ns
LVTTL, Fast, 24 mA	0.97	2.20	2.20	ns
LVCMOS33, Slow, 2 mA	0.97	8.73	8.73	ns
LVCMOS33, Slow, 4 mA	0.97	6.09	6.09	ns
LVCMOS33, Slow, 6 mA	0.97	5.00	5.00	ns
LVCMOS33, Slow, 8 mA	0.97	3.95	3.95	ns
LVCMOS33, Slow, 12 mA	0.97	3.42	3.42	ns
LVCMOS33, Slow, 16 mA	0.97	2.49	2.49	ns
LVCMOS33, Slow, 24 mA	0.97	2.49	2.49	ns
LVCMOS33, Fast, 2 mA	0.97	7.44	7.44	ns
LVCMOS33, Fast, 4 mA	0.97	4.33	4.33	ns
LVCMOS33, Fast, 6 mA	0.97	3.55	3.55	ns
LVCMOS33, Fast, 8 mA	0.97	2.46	2.46	ns
LVCMOS33, Fast, 12 mA	0.97	2.27	2.27	ns
LVCMOS33, Fast, 16 mA	0.97	2.08	2.08	ns
LVCMOS33, Fast, 24 mA	0.97	2.08	2.08	ns
LVCMOS25, Slow, 2 mA	0.88	5.89	5.89	ns
LVCMOS25, Slow, 4 mA	0.88	5.02	5.02	ns
LVCMOS25, Slow, 6 mA	0.88	4.31	4.31	ns
LVCMOS25, Slow, 8 mA	0.88	4.31	4.31	ns
LVCMOS25, Slow, 12 mA	0.88	3.50	3.50	ns
LVCMOS25, Slow, 16 mA	0.88	3.31	3.31	ns
LVCMOS25, Slow, 24 mA	0.88	2.77	2.77	ns
LVCMOS25, Fast, 2 mA	0.88	3.89	3.89	ns
LVCMOS25, Fast, 4 mA	0.88	3.19	3.19	ns
LVCMOS25, Fast, 6 mA	0.88	2.81	2.81	ns
LVCMOS25, Fast, 8 mA	0.88	2.52	2.52	ns
LVCMOS25, Fast, 12 mA	0.88	2.43	2.43	ns
LVCMOS25, Fast, 16 mA	0.88	2.21	2.21	ns
LVCMOS25, Fast, 24 mA	0.88	2.13	2.13	ns
LVCMOS18, Slow, 2 mA	1.25	5.89	5.89	ns
LVCMOS18, Slow, 4 mA	1.25	4.35	4.35	ns
LVCMOS18, Slow, 6 mA	1.25	4.00	4.00	ns
LVCMOS18, Slow, 8 mA	1.25	3.76	3.76	ns
LVCMOS18, Slow, 12 mA	1.25	3.74	3.74	ns
LVCMOS18, Slow, 16 mA	1.25	3.55	3.55	ns
LVCMOS18, Fast, 2 mA	1.25	3.89	3.89	ns
LVCMOS18, Fast, 4 mA	1.25	3.02	3.02	ns
LVCMOS18, Fast, 6 mA	1.25	2.72	2.72	ns

Table 22: **IOB Switching Characteristics[1,2] *(Cont'd)***

IOSTANDARD Attribute[1]	Speed Grade			Units
	-10			
	T_{IOPI}	T_{IOOP}	T_{IOTP}	
LVCMOS18, Fast, 8 mA	1.25	2.52	2.52	ns
LVCMOS18, Fast, 12 mA	1.25	2.36	2.36	ns
LVCMOS18, Fast, 16 mA	1.25	2.27	2.27	ns
LVCMOS15, Slow, 2 mA	1.34	6.61	6.61	ns
LVCMOS15, Slow, 4 mA	1.34	4.88	4.88	ns
LVCMOS15, Slow, 6 mA	1.34	4.26	4.26	ns
LVCMOS15, Slow, 8 mA	1.34	4.26	4.26	ns
LVCMOS15, Slow, 12 mA	1.34	3.77	3.77	ns
LVCMOS15, Slow, 16 mA	1.34	3.53	3.53	ns
LVCMOS15, Fast, 2 mA	1.34	4.17	4.17	ns
LVCMOS15, Fast, 4 mA	1.34	3.32	3.32	ns
LVCMOS15, Fast, 6 mA	1.34	2.94	2.94	ns
LVCMOS15, Fast, 8 mA	1.34	2.71	2.71	ns
LVCMOS15, Fast, 12 mA	1.34	2.50	2.50	ns
LVCMOS15, Fast, 16 mA	1.34	2.43	2.43	ns
LVDCI_33	0.97	3.13	3.13	ns
LVDCI_25	0.88	3.02	3.02	ns
LVDCI_18	1.25	2.95	2.95	ns
LVDCI_15	1.34	2.93	2.93	ns
LVDCI_DV2_25	0.88	2.27	2.27	ns
LVDCI_DV2_18	1.25	2.28	2.28	ns
LVDCI_DV2_15	1.34	2.58	2.58	ns
GTL_DCI	1.51	2.03	2.03	ns
GTLP_DCI	1.23	2.03	2.03	ns
HSTL_I_DCI	1.64	2.35	2.35	ns
HSTL_II_DCI	1.64	2.13	2.13	ns
HSTL_III_DCI	1.64	2.22	2.22	ns
HSTL_IV_DCI	1.64	2.03	2.03	ns
HSTL_I_DCI_18	1.60	2.21	2.21	ns
HSTL_II_DCI_18	1.60	2.16	2.16	ns
HSTL_III_DCI_18	1.60	2.09	2.09	ns
HSTL_IV_DCI_18	1.60	2.06	2.06	ns
SSTL2_I_DCI	1.68	2.46	2.46	ns
SSTL2_II_DCI	1.68	2.45	2.45	ns
LVPECL_25	1.77	1.74	1.74	ns
SSTL18_I	1.68	2.54	2.54	ns
SSTL18_II	1.68	2.24	2.24	ns
SSTL18_I_DCI	1.68	2.32	2.32	ns
SSTL18_II_DCI	1.68	2.18	2.18	ns

Notes:

1. The I/O standard is selected in the Xilinx ISE® software tool using the IOSTANDARD attribute.
2. All I/O timing specifications are measured with V_{CCO} at -5% from nominal.

Table 23: **T_{IOOP} and T_{IOTP} Offset for 125°C Operation**

IOSTANDARD Attribute	Speed Grade			Units
	-10			
	I Grade	V Grade	Delta	
LVDS	1.85	2.23	0.38	ns
RSDS	1.85	2.23	0.38	ns
LVDSEXT	1.91	2.25	0.34	ns
LDT	1.82	2.23	0.41	ns
PCI33_3	3.02	3.26	0.24	ns
PCI66_3	2.72	3.26	0.54	ns
PCIX	2.25	2.49	0.24	ns
GTL	2.03	2.27	0.24	ns
GTLP	2.03	2.25	0.22	ns
HSTL_I	2.35	2.54	0.19	ns
HSTL_II	2.13	2.47	0.34	ns
HSTL_III	2.22	2.55	0.33	ns
HSTL_IV	2.03	2.43	0.40	ns
HSTL_I_18	2.21	2.43	0.22	ns
HSTL_II_18	2.16	2.39	0.23	ns
HSTL_III_18	2.09	2.40	0.31	ns
HSTL_IV_18	2.06	2.38	0.32	ns
SSTL2_I	2.43	2.46	0.03	ns
SSTL2_II	2.16	2.27	0.11	ns
LVTTL_S2	7.03	9.95	2.92	ns
LVTTL_S4	5.04	7.84	2.80	ns
LVTTL_S6	4.91	6.67	1.76	ns
LVTTL_S8	4.91	6.40	1.49	ns
LVTTL_S12	3.96	4.87	0.91	ns
LVTTL_S16	3.46	4.42	0.96	ns
LVTTL_S24	3.12	3.24	0.12	ns
LVTTL_F2	4.86	8.44	3.58	ns
LVTTL_F4	3.46	6.41	2.95	ns
LVTTL_F6	3.00	4.76	1.76	ns
LVTTL_F8	2.79	3.97	1.18	ns
LVTTL_F12	2.47	2.92	0.45	ns
LVTTL_F16	2.47	2.93	0.46	ns
LVTTL_F24	2.20	2.87	0.67	ns
LVCMOS33_S2	8.73	11.43	2.70	ns
LVCMOS33_S4	6.09	8.56	2.47	ns
LVCMOS33_S6	5.00	7.27	2.27	ns
LVCMOS33_S8	3.95	6.35	2.40	ns
LVCMOS33_S12	3.42	4.74	1.32	ns

Table 23: **T_{IOOP} and T_{IOTP} Offset for 125°C Operation *(Cont'd)***

IOSTANDARD Attribute	Speed Grade			Units
	-10			
	I Grade	V Grade	Delta	
LVCMOS33_S16	2.49	4.56	2.07	ns
LVCMOS33_S24	2.49	3.06	0.57	ns
LVCMOS33_F2	7.44	10.18	2.74	ns
LVCMOS33_F4	4.33	6.18	1.85	ns
LVCMOS33_F6	3.55	5.53	1.98	ns
LVCMOS33_F8	2.46	4.47	2.01	ns
LVCMOS33_F12	2.27	3.22	0.95	ns
LVCMOS33_F16	2.08	2.74	0.66	ns
LVCMOS33_F24	2.08	2.61	0.53	ns
LVCMOS25_S2	5.89	8.57	2.68	ns
LVCMOS25_S4	5.02	6.44	1.42	ns
LVCMOS25_S6	4.31	6.00	1.69	ns
LVCMOS25_S8	4.31	5.24	0.93	ns
LVCMOS25_S12	3.50	4.30	0.80	ns
LVCMOS25_S16	3.31	3.95	0.64	ns
LVCMOS25_S24	2.77	2.64	-0.13	ns
LVCMOS25_F2	3.89	7.97	4.08	ns
LVCMOS25_F4	3.19	4.99	1.80	ns
LVCMOS25_F6	2.81	3.92	1.11	ns
LVCMOS25_F8	2.52	3.29	0.77	ns
LVCMOS25_F12	2.43	2.43	0.00	ns
LVCMOS25_F16	2.21	2.39	0.18	ns
LVCMOS25_F24	2.13	2.39	0.26	ns
LVCMOS18_S2	5.89	8.68	2.79	ns
LVCMOS18_S4	4.35	7.31	2.96	ns
LVCMOS18_S6	4.00	5.66	1.66	ns
LVCMOS18_S8	3.76	5.11	1.35	ns
LVCMOS18_S12	3.74	4.59	0.85	ns
LVCMOS18_S16	3.55	3.89	0.34	ns
LVCMOS18_F2	3.89	8.34	4.45	ns
LVCMOS18_F4	3.02	5.99	2.97	ns
LVCMOS18_F6	2.72	4.35	1.63	ns
LVCMOS18_F8	2.52	3.66	1.14	ns
LVCMOS18_F12	2.36	2.80	0.44	ns
LVCMOS18_F16	2.27	2.70	0.43	ns
LVCMOS15_S2	6.61	9.21	2.60	ns
LVCMOS15_S4	4.88	7.75	2.87	ns
LVCMOS15_S6	4.26	6.14	1.88	ns

Table 23: **T_{IOOP} and T_{IOTP} Offset for 125°C Operation *(Cont'd)***

IOSTANDARD Attribute	Speed Grade			Units
	-10			
	I Grade	V Grade	Delta	
LVCMOS15_S8	4.26	6.18	1.92	ns
LVCMOS15_S12	3.77	4.77	1.00	ns
LVCMOS15_S16	3.53	4.07	0.54	ns
LVCMOS15_F2	4.17	8.32	4.15	ns
LVCMOS15_F4	3.32	6.53	3.21	ns
LVCMOS15_F6	2.94	4.69	1.75	ns
LVCMOS15_F8	2.71	3.90	1.19	ns
LVCMOS15_F12	2.50	2.92	0.42	ns
LVCMOS15_F16	2.43	2.84	0.41	ns
SSTL18_I	2.54	2.44	-0.10	ns
SSTL18_II	2.24	2.42	0.18	ns

Table 24: **IOB 3-State On Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade	Units
		-10	
T_{IOTPHZ}	T input to Pad high-impedance	1.12	ns

Ethernet MAC Switching Characteristics

Consult UG074, *Virtex-4 Embedded Tri-Mode Ethernet MAC User Guide* for further information.

Table 25: **Maximum Ethernet MAC Performance**

Description	Speed Grade	Units
	-10	
Ethernet MAC Maximum Performance	10/100/1000	Mb/s

Input/Output Logic Switching Characteristics

Table 26: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Setup/Hold			
T_{ICE1CK} / T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.79/–0.23	ns
T_{ICECK} / T_{ICKCE}	DLYCE pin setup/hold with respect to CLKDIV	0.23/0.16	ns
T_{IRSTCK} / T_{ICKRST}	DLYRST pin setup/hold with respect to CLKDIV	–0.02/0.54	ns
T_{IINCCK} / T_{ICKINC}	DLYINC pin setup/hold with respect to CLKDIV	0.01/0.51	ns
T_{ISRCK} / T_{ICKSR}	SR/REV pin setup/hold with respect to CLK	1.59/–0.56	ns
T_{IDOCK} / T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.34/–0.10	ns
T_{IDOCKD} / T_{IOCKDD}	D pin setup/hold with respect to CLK (IOBDELAY_TYPE = DEFAULT)	8.84/–5.99	ns
	D pin setup/hold with respect to CLK (IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)	1.09/–0.63	ns
Combinatorial			
T_{IDI}	D pin to O pin propagation delay, no Delay	0.24	ns
T_{IDID}	D pin to O pin propagation delay (IOBDELAY_TYPE = DEFAULT)	7.96	ns
	D pin to O pin propagation delay (IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)	0.99	ns
Sequential Delays			
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.71	ns
T_{IDLOD}	D pin to Q1 pin using flip-flop as a latch (IOBDELAY_TYPE = DEFAULT)	9.21	ns
	D pin to Q1 pin using flip-flop as a latch (IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)	1.45	ns
T_{ICKQ}	CLK to Q outputs	0.72	ns
T_{ICE1Q}	CE1 pin to Q1 using flip-flop as a latch, propagation delay	1.27	ns
T_{RQ}	SR/REV pin to OQ/TQ out	2.44	ns
T_{GSRQ}	Global set/reset to Q outputs	2.03	ns
Set/Reset			
T_{RPW}	Minimum pulse width, SR/REV inputs	0.70	ns, Min

Table 27: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Setup/Hold			
T_{ODCK} / T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.75/–0.22	ns
T_{OOCECK} / T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.77/–0.33	ns
T_{OSRCK} / T_{OCKSR}	SR/REV pin setup/hold with respect to CLK	1.42/–0.55	ns
T_{OTCK} / T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.75/–0.22	ns
T_{OTCECK} / T_{OCKTCE}	TCE pin setup/hold with respect to CLK	0.77/–0.33	ns
Combinatorial			
T_{ODQ}	D1 to OQ out	0.76	ns
T_{OTQ}	T1 to TQ out	0.76	ns
Sequential Delays			
T_{IOSRON}	REV pin to TQ out	1.64	ns
T_{OCKQ}	CLK to OQ/TQ out	0.59	ns
T_{RQ}	SR/REV pin to OQ/TQ out	1.64	ns
T_{GSRQ}	Global Set/Reset to Q outputs	2.03	ns
Set/Reset			
T_{RPW}	Minimum Pulse Width, SR/REV inputs	0.70	ns Min

Input Serializer/Deserializer Switching Characteristics

Table 28: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Setup/Hold for Control Lines			
$T_{ISCCK\_BITSLIP}$ / $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.40/–0.13	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin setup/hold with respect to CLK (for CE1)	0.69/–0.25	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin setup/hold with respect to CLKDIV (for CE2)	0.16/–0.02	ns
T_{ISCCK_DLYCE} / T_{ISCKC_DLYCE}	DLYCE pin setup/hold with respect to CLKDIV	0.23/0.16	ns
T_{ISCCK_DLYINC} / T_{ISCKC_DLYINC}	DLYINC pin setup/hold with respect to CLKDIV	0.01/0.51	ns
T_{ISCCK_DLYRST} / T_{ISCKC_DLYRST}	DLYRST pin setup/hold with respect to CLKDIV	–0.02/0.54	ns
T_{ISCCK_REV}	REV pin setup with respect to CLK	1.23	ns
T_{ISCCK_SR}	SR pin setup with respect to CLKDIV	0.92	ns
Setup/Hold for Data Lines			
T_{ISDCK_D} / T_{ISCKD_D}	D pin setup/hold with respect to CLK (IOBDELAY = IBUF or NONE)	0.34/–0.11	ns
	D pin setup/hold with respect to CLK (IOBDELAY = IFD or BOTH, IOBDELAY_TYPE = DEFAULT)	8.84/–6.51	ns
	D pin setup/hold with respect to CLK(1) (IOBDELAY = IFD or BOTH, IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)	1.08/–0.68	ns
T_{ISDCK_DDR} / T_{ISCKD_DDR}	D pin setup/hold with respect to CLK at DDR mode (IOBDELAY = IBUF or NONE)	0.34/–0.11	ns
	D pin setup/hold with respect to CLK at DDR mode (IOBDELAY = IFD or BOTH, IOBDELAY_TYPE = DEFAULT)	8.84/–6.51	ns
	D pin setup/hold with respect to CLK at DDR mode(1) (IOBDELAY = IFD or BOTH, IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)	1.08/–0.68	ns
Sequential Delays			
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.85	ns
Propagation Delays			
$T_{ISDO\_DO\_IOBDELAY\_IFD}$	D input to DO output pin (IOBDELAY = IFD)	0.24	ns
$T_{ISDO\_DO\_IOBDELAY\_NONE}$	D input to DO output pin (IOBDELAY = NONE)	0.24	ns
$T_{ISDO\_DO\_IOBDELAY\_BOTH}$	D input to DO output pin (IOBDELAY = BOTH, IOBDELAY_TYPE = DEFAULT)	7.96	ns
	D input to DO output pin(1) (IOBDELAY = BOTH, IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)	0.99	ns
$T_{ISDO\_DO\_IOBDELAY\_IBUF}$	D input to DO output pin (IOBDELAY = IBUF, IOBDELAY_TYPE = DEFAULT)	7.96	ns
	D input to DO output pin(1) (IOBDELAY = IBUF, IOBDELAY_TYPE = FIXED, IOBDELAY_VALUE = 0)	0.99	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE} / T_{ISCKC_CE} in TRCE report.

Input Delay Switching Characteristics

Table 29: **Input Delay Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
$T_{IDELAYRESOLUTION}$	IDELAY Chain Delay Resolution	75	ps
$T_{IDELAYTOTAL\_ERR}$	Cumulative delay at a given tap (3)	[(tap –1) x 75 +34] ±0.07[(tap –1) x 75 +34]	ps
$T_{IDELAYCTRLCO\_RDY}$	Reset to Ready for IDELAYCTRL (Maximum)	3.00	µs
$F_{IDELAYCTRL\_REF}$	REFCLK frequency	200	MHz
IDELAYCTRL_REF_PRECISION (2)	REFCLK precision	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	50.0	ns
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern	0	Note (1)
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)	10 ± 2	Note (1)

Notes:

1. Units in ps peak-to-peak per tap.
2. See the “REFCLK - Reference Clock” section (specific to IDELAYCTRL) in the *Virtex-4 FPGA User Guide:* Chapter 7, “SelectIO Logic Resources.”
3. This value accounts for tap 0, an anomaly in the tap chain with an average value of 34 ps.

Output Serializer/Deserializer Switching Characteristics

Table 30: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Setup/Hold			
$T_{OSDCK\_D} / T_{OSCKD\_D}$	D input setup/hold with respect to CLKDIV	0.50/–0.03	ns
$T_{OSDCK\_T} / T_{OSCKD\_T}$ (1)	T input setup/hold with respect to CLK	0.62/–0.16	ns
$T_{OSDCK\_T2} / T_{OSCKD\_T2}$ (1)	T input setup/hold with respect to CLKDIV	0.50/–0.03	ns
$T_{OSCCK\_OCE} / T_{OSCKC\_OCE}$	OCE input setup/hold with respect to CLK	0.64/0.03	ns
T_{OSCCK_S}	SR (Reset) input setup with respect to CLKDIV	0.96	ns
$T_{OSCCK\_TCE} / T_{OSCKC\_TCE}$	TCE input setup/hold with respect to CLK	0.64/0.03	ns
Sequential Delays			
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.59	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.59	ns
Combinatorial			
T_{OSDO_TTQ}	T input to TQ out	0.76	ns
T_{OSCO_OQ}	Asynchronous reset to OQ	1.64	ns
T_{OSCO_TQ}	Asynchronous reset to TQ	1.64	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as $T_{OSDCK\_T} / T_{OSCKD\_T}$ in TRCE report.

CLB Switching Characteristics

Table 31: **CLB Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Combinatorial Delays			
T_{ILO}	4-input function: F/G inputs to X/Y outputs	0.20	ns, max
T_{IF5}	5-input function: F/G inputs to F5 output	0.46	ns, max
T_{IF5X}	5-input function: F/G inputs to X output	0.57	ns, max
T_{IF6Y}	FXINA or FXINB inputs to YMUX output	0.39	ns, max
T_{INAFX}	FXINA input to FX output via MUXFX	0.27	ns, max
T_{INBFX}	FXINB input to FX output via MUXFX	0.26	ns, max
T_{BXX}	BX input to XMUX output	0.76	ns, max
T_{BYY}	BY input to YMUX output	0.56	ns, max
T_{BXCY}	BX input to C_{OUT} output – Getting into carry chain(2)	0.78	ns, max
T_{BYCY}	BY input to C_{OUT} output – Getting into carry chain(2)	0.63	ns, max
T_{BYP}	C_{IN} input to C_{OUT} output – Carry chain delay(2)	0.09	ns, max
T_{OPCYF}	F input to C_{OUT} output – Getting out from carry chain(2)	0.58	ns, max
T_{OPCYG}	G input to C_{OUT} output – Getting out from carry chain(2)	0.57	ns, max
Sequential Delays			
T_{CKO}	FF Clock CLK to XQ/YQ outputs	0.36	ns, max
T_{CKLO}	Latch Clock CLK to XQ/YQ outputs	0.48	ns, max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK			
T_{DICK}/T_{CKDI}	BX/BY inputs	0.47/–0.09	ns, min
T_{CECK}/T_{CKCE}	CE input	0.75/–0.16	ns, min
T_{FXCK}/T_{CKFX}	FXINA/FXINB inputs	0.54/–0.14	ns, min
T_{SRCK}/T_{CKSR}	SR/BY inputs (synchronous)	1.35/–0.73	ns, min
T_{CINCK}/T_{CKCIN}	C_{IN} Data Inputs (DI) – Getting out from carry chain(2)	0.67/–0.23	ns, min
Set/Reset			
T_{RPW}	Minimum Pulse Width, SR/BY inputs	0.70	ns, min
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	1.35	ns, max
F_{TOG}	Toggle Frequency (MHz) (for export control)	1028	MHz

Notes:

1. A zero “0” hold time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case,” but if a “0” is listed, there is no positive hold time.
2. These items are of interest for carry chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 32: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Sequential Delays			
T_{SHCKO}	Clock CLK to X outputs (WE active)	2.08	ns, max
$T_{SHCKOF5}$	Clock CLK to F5 output (WE active)	1.98	ns, max
Setup and Hold Times Before/After Clock CLK			
T_{DS} / T_{DH}	BX/BY data inputs (DI)	1.80/–0.88	ns, min
T_{AS} / T_{AH}	F/G address inputs	1.13/–0.29	ns, min
T_{WS} / T_{WH}	WE input (SR)	1.42/–0.47	ns, min
Clock CLK			
T_{WPH}	Minimum Pulse Width, High	0.69	ns, min
T_{WPL}	Minimum Pulse Width, Low	0.70	ns, min
T_{WC}	Minimum clock period to meet address write cycle time	0.98	ns, min

Notes:

1. A zero “0” hold time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case,” but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRCE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 33: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Sequential Delays			
T_{REG}	Clock CLK to X/Y outputs	2.57	ns, max
T_{REGXB}	Clock CLK to XB output via MC15 LUT output	2.04	ns, max
T_{REGYB}	Clock CLK to YB output via MC15 LUT output	2.17	ns, max
T_{CKSH}	Clock CLK to Shiftout	1.99	ns, max
T_{REGF5}	Clock CLK to F5 output	2.47	ns, max
Setup and Hold Times Before/After Clock CLK			
T_{WS} / T_{WH}	WE input (SR)	1.12/–0.62	ns, min
T_{DS} / T_{DH}	BX/BY data inputs (DI)	1.75/–1.11	ns, min
Clock CLK			
T_{WPH}	Minimum pulse width, High	0.69	ns, min
T_{WPL}	Minimum pulse width, Low	0.70	ns, min

Notes:

1. A zero “0” hold time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case,” but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 34: **Block RAM Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Sequential Delays			
T_{RCKO_DORA}	Clock CLK to DOUT output (without output register)(2)	2.10	ns, max
T_{RCKO_DOA}	Clock CLK to DOUT output (with output register)(3)	0.92	ns, min
Setup and Hold Times Before Clock CLK			
T_{RCCK_ADDR} / T_{RCKC_ADDR}	ADDR inputs	0.43/0.33	ns, min
T_{RDCK_DI} / T_{RCKD_DI}	DIN inputs(4)	0.23/0.33	ns, min
T_{RCCK_EN} / T_{RCKC_EN}	EN input(5)	0.52/0.33	ns, min
T_{RCCK_REGCE} / T_{RCKC_REGCE}	CE input of output register	0.32/0.33	ns, min
T_{RCCK_SSR} / T_{RCKC_SSR}	RST input	0.32/0.33	ns, min
T_{RCCK_WE} / T_{RCKC_WE}	WEN input	0.75/0.33	ns, min
Maximum Frequency			
F_{MAX}	Write first and no change mode	400.00	MHz
F_{MAX}	Read first mode	400.00	MHz

Notes:

1. A zero “0” hold time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case,” but if a “0” is listed, there is no positive hold time.
2. T_{RCKO_DORA} includes T_{RCKO_DOWA}, T_{RCKO_DOPAR}, and T_{RCKO_DOPAW} as well as the B port equivalent timing parameters.
3. T_{RCKO_DOA} includes T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
4. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
5. Xilinx block RAMs do not have asynchronous inputs on an enabled port address. During the time that a port is enabled, its addresses must be stable during the specified set-up time. Do not create an asynchronous input on an enabled port address.

Table 35: **FIFO Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Sequential Delays			
T_{FCKO_DO}	Clock CLK to DO output(2)	0.92	ns, max
T_{FCKO_FLAGS}	Clock CLK to FIFO flags outputs(3)	1.19	ns, max
$T_{FCKO\_POINTERS}$	Clock CLK to FIFO pointer outputs(4)	1.48	ns, max
Setup and Hold Times Before Clock CLK			
T_{FDCK_DI} / T_{FCKD_DI}	DI input(5)	0.23/0.33	ns, min
T_{FCCK_EN} / T_{FCKC_EN}	Enable inputs(6)	0.84/0.33	ns, min
Reset Delays			
T_{FCO_FLAGS}	Reset RST to FLAGS(7)	1.68	ns, max
Maximum Frequency			
F_{MAX}	FIFO in all modes	400.00	MHz

Notes:

1. A zero “0” hold time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case,” but if a “0” is listed, there is no positive hold time.
2. T_{FCKO_DO} includes parity output (T_{FCKO_DOP}).
3. T_{FCKO_FLAGS} includes these parameters: T_{FCKO_AEMPTY}, T_{FCKO_AFULL}, T_{FCKO_EMPTY}, T_{FCKO_FULL}, T_{FCKO_RDERR}, T_{FCKO_WRERR}.
4. $T_{FCKO\_POINTERS}$ includes both $T_{FCKO\_RDCOUNT}$ and $T_{FCKO\_WRCOUNT}$.
5. T_{FDCK_DI} includes parity inputs (T_{FDCK_DIP}).
6. T_{FCCK_EN} includes both WRITE and READ enable.
7. T_{FCO_FLAGS} includes these flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT and WRCOUNT.

XtremeDSP Switching Characteristics

Table 36: **XtremeDSP™ Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Setup and Hold of CE Pins			
T_{DSPCCK_CE} / T_{DSPCKC_CE}	Setup/hold of all CE inputs of the DSP48 slice	0.49/0.12	ns
T_{DSPCCK_RST} / T_{DSPCKC_RST}	Setup/hold of all RST inputs of the DSP48 slice	0.40/0.12	ns
Setup and Hold Times of Data			
$T_{DSPDCK\_\{AA, BB, CC\}}$ / $T_{DSPCKD\_\{AA, BB, CC\}}$	Setup/hold of {A, B, C} input to {A, B, C} register	0.32/0.29	ns
$T_{DSPDCK\_\{AM, BM\}}$ / $T_{DSPCKD\_\{AM, BM\}}$	Setup/hold of {A, B} input to M register	2.28/0.00	ns
Sequential Delays			
T_{DSPCKO_PP}	Clock to out from P register to P output	0.79	ns
T_{DSPCKO_PM}	Clock to out from M register to P output	2.98	ns
Combinatorial			
$T_{DSPDO\_\{AP, BP\}L}$	From {A, B} input to P output (LEGACY_MODE = MULT18X18)	4.41	ns
Maximum Frequency			
F_{MAX}	From {A, B} register to P register (LEGACY_MODE = MULT18X18)	253.94	MHz
	Fully Pipelined	400.00	MHz

Configuration Switching Characteristics

Table 37: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
Power-up Timing Characteristics			
T_{PL}	Program latency	0.5	µs/frame, max
T_{POR}	Power-on-reset	T_{PL} + 10	ms, max
T_{ICCK}	CCLK (output) delay	500	ns, min
$T_{PROGRAM}$	Program pulse width	400	ns, min
Master/Slave Serial Mode Programming Switching			
T_{DCC} / T_{CCD}	DIN setup/hold, slave mode	1.0/1.0	ns, min
T_{DSCK} / T_{SCKD}	DIN setup/hold, master mode	1.0/1.0	ns, min
T_{CCO}	DOUT	8.0	ns, max
T_{CCH}	High time	2.0	ns, min
T_{CCL}	Low time	2.0	ns, min
F_{CC_SERIAL}	Maximum frequency, master mode with respect to nominal CCLK.	80	MHz, max
F_{MCCTOL}	Frequency tolerance, master mode with respect to nominal CCLK.	±50	%
F_{MAX_SLAVE}	Slave mode external CCLK	80	MHz
SelectMAP Mode Programming Switching			
T_{SMDCC} / T_{SMCCD}	SelectMAP setup/hold	3.0/0.0	ns, min
T_{SMCSCC} / T_{SMCCCS}	CS_B setup/hold	2.0/0.5	ns, min
T_{SMCCW} / T_{SMWCC}	RDWR_B setup/hold	8.0/1.0	ns, min
T_{SMCKBY}	BUSY propagation delay	8.0	ns, max
$F_{CC\_SELECTMAP}$	Maximum frequency, master mode with respect to nominal CCLK.	80	MHz, max
F_{MCCTOL}	Frequency tolerance, master mode with respect to nominal CCLK.	±50	%
Boundary-Scan Port Timing Specifications			
T_{TAPTCK}	TMS and TDI setup time before TCK	1.5	ns, min
T_{TCKTAP}	TMS and TDI hold time after TCK	2.0	ns, min
T_{TCKTDO}	TCK falling edge to TDO output valid	8.0	ns, max
F_{TCK}	Maximum configuration TCK clock frequency	66	MHz, max
F_{TCKB}	Maximum Boundary-Scan TCK clock frequency	50	MHz, max

Table 37: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade	Units
		-10	
Dynamic Reconfiguration Port (DRP) for DCM			
CLKIN_FREQ_DLL_HF_MS_MAX	Maximum frequency for DCLK	400	MHz, max
D_DCMADV_DADDR_DCLK_SETUP/ D_DCMADV_DADDR_DCLK_HOLD	DADDR setup/hold	0.72/0.00	ns, max
D_DCMADV_DI_DCLK_SETUP/ D_DCMADV_DI_DCLK_HOLD	DI setup/hold	0.72/0.00	ns, max
D_DCMADV_DEN_DCLK_SETUP/ D_DCMADV_DEN_DCLK_HOLD	DEN setup/hold time	0.58/0.00	ns, max
D_DCMADV_DWE_DCLK_SETUP/ D_DCMADV_DWE_DCLK_HOLD	DWE setup/hold time	0.58/0.00	ns, max
D_DCMADV_DCLK_DO	CLK to out of DO(1)	0	ns, max
D_DCMADV_DCLK_DRDY	CLK to out of DRDY	0.92	ns, max

Notes:

1. DO holds until next DRP operation.

Master/Slave SelectMAP Parameters

Figure 1 is a generic timing diagram for data loading using SelectMAP. For other data loading diagrams, refer to the *Virtex-4 FPGA User Guide*.

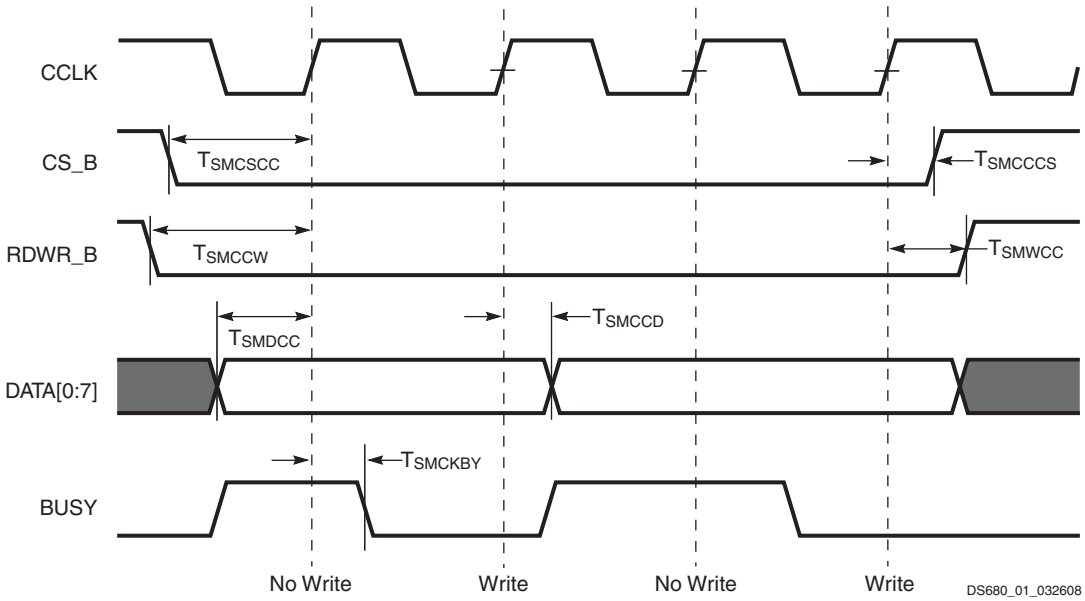

Figure 1: **SelectMAP Mode Data Loading Sequence (Generic)**

Clock Buffers and Networks

Table 38: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade	Units
		-10	
T_{BCCCK_CE} / T_{BCCKC_CE}(1)	CE pins setup/hold	0.35/0.00	ns
T_{BCCCK_S} / T_{BCCKC_S}(1)	S pins setup/hold	0.35/0.00	ns
T_{BCCKO_O}	BUFGCTRL delay	0.90	ns
Maximum Frequency			
F_{MAX}	Global clock tree	400	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.

DCM and PMCD Switching Characteristics

DCM in Maximum Range (MR) Mode is not supported for operation beyond industrial temperature range.

Table 39: **Operating Frequency Ranges for DCM in Maximum Speed (MS) Mode**

Symbol	Description	Speed Grade	Units
		-10	
Outputs Clocks (Low Frequency Mode)			
CLKOUT_FREQ_1X_LF_MS_MIN	CLK0, CLK90, CLK180, CLK270	32	MHz
CLKOUT_FREQ_1X_LF_MS_MAX		150	MHz
CLKOUT_FREQ_2X_LF_MS_MIN	CLK2X, CLK2X180	64	MHz
CLKOUT_FREQ_2X_LF_MS_MAX		300	MHz
CLKOUT_FREQ_DV_LF_MS_MIN	CLKDV	2	MHz
CLKOUT_FREQ_DV_LF_MS_MAX		100	MHz
CLKOUT_FREQ_FX_LF_MS_MIN	CLKFX, CLKFX180	32	MHz
CLKOUT_FREQ_FX_LF_MS_MAX		210	MHz
Input Clocks (Low Frequency Mode)			
CLKIN_FREQ_DLL_LF_MS_MIN	CLKIN (using DLL outputs)(1,3,4,5)	32	MHz
CLKIN_FREQ_DLL_LF_MS_MAX		150	MHz
CLKIN_FREQ_FX_LF_MS_MIN	CLKIN (using DFS outputs only)(2,3,4)	1	MHz
CLKIN_FREQ_FX_LF_MS_MAX		210	MHz
PSCLK_FREQ_LF_MS_MIN	PSCLK	1	KHz
PSCLK_FREQ_LF_MS_MAX		400	MHz
Outputs Clocks (High Frequency Mode)			
CLKOUT_FREQ_1X_HF_MS_MIN	CLK0, CLK90, CLK180, CLK270	150	MHz
CLKOUT_FREQ_1X_HF_MS_MAX		400	MHz
CLKOUT_FREQ_2X_HF_MS_MIN	CLK2X, CLK2X180	300	MHz
CLKOUT_FREQ_2X_HF_MS_MAX		400	MHz
CLKOUT_FREQ_DV_HF_MS_MIN	CLKDV	9.4	MHz
CLKOUT_FREQ_DV_HF_MS_MAX		267	MHz
CLKOUT_FREQ_FX_HF_MS_MIN	CLKFX, CLKFX180	210	MHz
CLKOUT_FREQ_FX_HF_MS_MAX		300	MHz

Table 39: **Operating Frequency Ranges for DCM in Maximum Speed (MS) Mode *(Cont'd)***

Symbol	Description	Speed Grade	Units
		-10	
Input Clocks (High Frequency Mode)			
CLKIN_FREQ_DLL_HF_MS_MIN	CLKIN (using DLL outputs)(1,3,4)	150	MHz
CLKIN_FREQ_DLL_HF_MS_MAX		400	MHz
CLKIN_FREQ_FX_HF_MS_MIN	CLKIN (using DFS outputs only)(2,3,4)	50	MHz
CLKIN_FREQ_FX_HF_MS_MAX		300	MHz
PSCLK_FREQ_HF_MS_MIN	PSCLK	1	KHz
PSCLK_FREQ_HF_MS_MAX		400	MHz

Notes:

1. DLL outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN_DIVIDE_BY_2 attribute these values should be doubled.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN_DIVIDE_BY_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).
5. The DCM must be reset if the clock input clock stops for more than 100 ms.

Table 40: **Input Clock Duty Cycle Input Tolerance**

Symbol	Description	Frequency Range	Value	Units
CLKIN_PSCLK_PULSE_RANGE_1	PSCLK only	< 1 MHz	25 – 75	%
CLKIN_PSCLK_PULSE_RANGE_1_50	PSCLK and CLKIN	1 – 50 MHz	25 – 75	%
CLKIN_PSCLK_PULSE_RANGE_50_100		50 – 100 MHz	30 – 70	%
CLKIN_PSCLK_PULSE_RANGE_100_200		100 – 200 MHz	40 – 60	%
CLKIN_PSCLK_PULSE_RANGE_200_400		200 – 400 MHz	45 – 55	%

Table 41: **Input Clock Tolerances**

Symbol	Description	Speed Grade	Units
		-10	
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)			
CLKIN_CYC_JITT_DLL_LF	CLKIN (using DLL outputs)(1)	±300	ps
CLKIN_CYC_JITT_FX_LF	CLKIN (using DFS outputs)(2)	±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)			
CLKIN_CYC_JITT_DLL_HF	CLKIN (using DLL outputs)(1)	±150	ps
CLKIN_CYC_JITT_FX_HF	CLKIN (using DFS outputs)(2)	±150	ps
Input Clock Period Jitter (Low Frequency Mode)			
CLKIN_PER_JITT_DLL_LF	CLKIN (using DLL outputs)(1)	±1.0	ns
CLKIN_PER_JITT_FX_LF	CLKIN (using DFS outputs)(2)	±1.0	ns
Input Clock Period Jitter (High Frequency Mode)			
CLKIN_PER_JITT_DLL_HF	CLKIN (using DLL outputs)(1)	±1.0	ns
CLKIN_PER_JITT_FX_HF	CLKIN (using DFS outputs)(2)	±1.0	ns
Feedback Clock Path Delay Variation			
CLKFB_DELAY_VAR_EXT	CLKFB off-chip feedback	±1.0	ns

Notes:

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. If both DLL and DFS outputs are used, follow the more restrictive specifications.

Output Clock Jitter

Table 42: **Output Clock Jitter**

Description	Symbol	Speed Grade	Units
		-10	
Clock Synthesis Period Jitter			
CLK0	CLKOUT_PER_JITT_0	±100	ps
CLK90	CLKOUT_PER_JITT_90	±150	ps
CLK180	CLKOUT_PER_JITT_180	±150	ps
CLK270	CLKOUT_PER_JITT_270	±150	ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X	±200	ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1	±150	ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2	±300	ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX	Note 1	ps

Notes:

1. Values for this parameter are available at www.xilinx.com.

Output Clock Phase Alignment

Table 43: **Output Clock Phase Alignment**

Description	Symbol	Speed Grade	Units
		-10	
Phase Offset Between CLKIN and CLKFB			
CLKIN / CLKFB	CLKIN_CLKFB_PHASE	±120	ps
Phase Offset Between Any DCM Outputs			
All CLK outputs	CLKOUT_PHASE	±200	ps
Duty Cycle Precision			
DLL outputs(1)	CLKOUT_DUTY_CYCLE_DLL(3,4)	±150	ps
DFS outputs(2)	CLKOUT_DUTY_CYCLE_FX(4)	±250	ps

Notes:

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION=TRUE.
4. The measured value includes the duty cycle distortion of the global clock tree.

Table 44: **Miscellaneous Timing Parameters**

Symbol	Description	Speed Grade	Units
		-10	
Time Required to Achieve LOCK			
T_LOCK_DLL_240	DLL output – Frequency range > 240 MHz(1)	20	µs
T_LOCK_DLL_120_240	DLL output – Frequency range 120 – 240 MHz(1)	63	µs
T_LOCK_DLL_60_120	DLL output – Frequency range 60 – 120 MHz(1)	225	µs
T_LOCK_DLL_50_60	DLL output – Frequency range 50 – 60 MHz(1)	325	µs
T_LOCK_DLL_40_50	DLL output – Frequency range 40 – 50 MHz(1)	500	µs
T_LOCK_DLL_30_40	DLL output – Frequency range 30 – 40 MHz(1)	900	µs
T_LOCK_DLL_24_30	DLL output – Frequency range 24 – 30 MHz(1)	1250	µs
T_LOCK_DLL_30	DLL output – Frequency range < 30 MHz(1)	1250	µs
T_LOCK_FX_MIN	DFS outputs(2)	10	ms
T_LOCK_FX_MAX		10	ms
T_LOCK_DLL_FINE_SHIFT	Multiplication factor for DLL lock time with Fine Shift	2	–
Fine Phase Shifting			
FINE_SHIFT_RANGE_MS	Absolute shifting range in maximum speed mode	7	ns
Delay Lines			
DCM_TAP_MS_MIN	Tap delay resolution (Min) in maximum speed mode	5	ps
DCM_TAP_MS_MAX	Tap delay resolution (Max) in maximum speed mode	40	ps

Table 44: **Miscellaneous Timing Parameters *(Cont'd)***

Symbol	Description	Speed Grade	Units
		-10	
Input Signal Requirements			
DCM_RESET(3)	Minimum duration that RST must be held asserted	200	ms
	Maximum duration that RST can be held asserted(4)	10	sec
DCM_INPUT_CLOCK_STOP	Maximum duration that CLKIN and CLKFB can be stopped(5,6)	100	ms

Notes:

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. CLKIN must be present and stable during the DCM_RESET.
4. This only applies to production step 1 LX and SX devices. For these devices, use the design solutions described in answer record 21127 for support of longer reset durations. Production step 2 LX and SX devices and all production FX devices do not have this requirement.
5. For production step 1 LX and SX devices, use the design solutions described in answer record 21127 for support of longer durations of stopped clocks. For production step 2 LX and SX devices and all production FX devices, the ISE software automatically inserts a small macro to support longer durations of stopped clocks.
6. For all stepping levels, once the input clock is toggling again and stable after being stopped, DCM must be reset.

Table 45: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Table 46: **DCM Switching Characteristics**

Symbol	Description	Speed Grade	Units
		-10	
T_{DMCCK_PSEN} / T_{DMCKC_PSEN}	PSEN setup/hold	1.07/0.00	ns
$T_{DMCCK\_PSINCDEC}$ / $T_{DMCKC\_PSINCDEC}$	PSINCDEC setup/hold	1.07/0.00	ns
T_{DMCKO_PSDONE}	Clock to out of PSDONE	0.69	ns

Table 47: **PMCD Switching Characteristic**

Symbol	Description	Speed Grade	Units
		-10	
T_{PMCCCK_REL} / T_{PMCCKC_REL}	REL setup/hold for all outputs	0.60/0.00	ns
$T_{PMCCO\_CLK\{A1,B,C,D\}}$	RST assertion to clock output deassertion	4.50	ns
$T_{PMCCKO\_CLK\{A1,B,C,D\}}$	Max clock propagation delay of PMCD for all outputs	5.20	ns
PMCD_CLK_SKEW	Max phase between all outputs assuming all inputs	±150	ps
CLKIN_FREQ_PMCD_CLKA_MAX	Max input/output frequency	400	MHz
CLKIN_PSCLK_PULSE_RANGE	Max duty-cycle input tolerance (same as DCM)	Note(1)	
PMCD_REL_HIGH_PULSE_MIN	Min pulse width for REL	1.25	ns
PMCD_RST_HIGH_PULSE_MIN	Min pulse width for RST	1.25	ns

Notes:

1. Refer to Table 40, page 28 parameter: CLKIN_PSCLK_PULSE_RANGE.

System-Synchronous Switching Characteristics

Virtex-4QV FPGA Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 48. Values are expressed in nanoseconds unless otherwise noted.

Table 48: **Global Clock Input-to-Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, With DCM**

Symbol	Description	Device	Speed Grade	Units
			-10	
LVCMOS25 Global Clock Input-to-Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM.(3)				
$T_{ICKOFDCM}$	Global Clock and OFF with DCM	XQR4VSX55	4.14	ns
		XQR4VFX60	3.96	ns
		XQR4VFX140	4.59	ns
		XQR4VLX200	4.46	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.
3. Clock to out has +320 ps offset for operation above 100° C.

Table 49: **Global Clock Input-to-Output Delay for LVCMOS25, 12 mA, Fast Slew Rate, Without DCM**

Symbol	Description	Device	Speed Grade	Units
			-10	
LVCMOS25 Global Clock Input-to-Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM.(2)				
T_{ICKOF}	Global Clock and OFF without DCM	XQR4VSX55	9.54	ns
		XQR4VFX60	9.11	ns
		XQR4VFX140	10.02	ns
		XQR4VLX200	10.14	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Clock to out has +250 ps offset for operation above 100° C

Virtex-4QV FPGA Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 50. Values are expressed in nanoseconds unless otherwise noted.

Table 50: **Global Clock Setup and Hold for LVCMOS25 Standard, With DCM**

Symbol	Description	Device	Speed Grade	Units
			-10	
Input Setup-and-Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1,4)				
T_{PSDCM}/T_{PHDCM}	No Delay Global Clock and IFF with DCM(2)	XQR4VSX55	1.73/–0.13	ns
		XQR4VFX60	1.53/0.12	ns
		XQR4VFX140	1.52/0.82	ns
		XQR4VLX200	1.76/0.41	ns

Notes:

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
   CLK0 DCM jitter
   IFF = input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.
4. Hold time has +200 ps offset for operation above 100° C.

Table 51: **Global Clock Setup and Hold for LVCMOS25 Standard, With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade	Units
			-10	
Example Data Input Setup-and-hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer.(1,3,4)				
T_{PSDCM_0}/T_{PHDCM_0}	No Delay Global Clock and IFF with DCM in Source-Synchronous Mode(2)	XQR4VSX55	–0.09/1.52	ns
		XQR4VFX60	–0.25/1.77	ns
		XQR4VFX140	–0.32/2.56	ns
		XQR4VLX200	0.00/2.06	ns

Notes:

1. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CLK0 DCM jitter. Package skew is not included in these measurements.
2. IFF = input flip-flop
3. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in "IOB Switching Characteristics(1,2)," page 11.
4. Setup time has +100 ps offset for operation above 100° C.

Table 52: **Global Clock Setup and Hold for LVCMOS25 Standard, Without DCM**

Symbol	Description	Device	Speed Grade	Units
			-10	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)				
T_{PSFD}/T_{PHFD}	Full Delay Global Clock and IFF without DCM(2)	XQR4VSX55	3.02/0.98	ns
		XQR4VFX60	3.58/0.62	ns
		XQR4VFX140	3.51/1.71	ns
		XQR4VLX200	4.32/0.82	ns

Notes:

1. Setup time is measured relative to the global clock input signal with the fastest route and the lightest load. Hold time is measured relative to the global clock input signal with the slowest route and heaviest load.
2. IFF = input flip-flop or latch
3. A zero “0” hold time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed best-case, but if a “0” is listed, there is no positive hold time.

ChipSync Source-Synchronous Technology Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-4QV FPGA source-synchronous transmitter and receiver data-valid windows.

Table 53: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade	Units
			-10	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	150	ps
T_{CKSKEW}	Global Clock Tree Skew(2)	XQR4VSX55	190	ps
		XQR4VFX60	190	ps
		XQR4VFX140	350	ps
		XQR4VLX200	350	ps
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	100	ps
	I/O clock tree skew across one clock region	All	50	ps
$T_{BUFIOSKEW}$	I/O clock tree skew across multiple clock regions	All	50	ps
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	250	ps
$T_{BUFIO\_MAX\_FREQ}$	I/O clock tree MAX frequency	All	500	MHz
$T_{BUFR\_MAX\_FREQ}$	Regional clock tree MAX frequency	All	250	MHz

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to the application.

Table 54: **Sample Window**

Symbol	Description	Device	Speed Grade	Units
			-10	
T_{SAMP}	Sampling Error at Receiver Pins(1)	All	550	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	All	450	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-4 FPGA DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-4 FPGA DDR input registers across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 55: **ChipSync™ Technology Pin-to-Pin Setup/Hold and Clock to Out**

Symbol	Description	Speed Grade	Units
		-10	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO			
T_{PSCS} / T_{PHCS}	Setup/hold of I/O clock across multiple clock regions	–0.44/1.17	ns
Pin-to-Pin Clock to Out Using BUFIO			
$T_{ICKOFCS}$	Clock-to-Out of I/O clock across multiple clock regions	5.02	ns

Production Stepping

The Virtex-4 FPGA stepping identification system denotes the capability improvement of production released devices. By definition, devices from one stepping are functional supersets of previous devices. Bitstreams compiled for a device with an earlier stepping are guaranteed to operate correctly in subsequent device steppings.

New device steppings can be shipped in place of earlier device steppings. Existing production designs are guaranteed on new device steppings. To take advantage of the capabilities of a newer device stepping, customers are able to order a new stepping version and compile a new bitstream.

Production devices are marked with a stepping version, with the exception of some step 1 devices. Designs should be compiled with a CONFIG STEPPING parameter set to a specific stepping version.

This parameter is set in the UCF file:

CONFIG STEPPING = “#”;

Where

= the stepping version

Table 56 shows the JTAG ID code by step.

Table 56: **JTAG ID Code by Step**

Device	ID Code	Stepping
XQR4VSX55	4	2
XQ4RVFX60	8	1
XQR4VFX140	4	1
XQR4VLX200	2 or 5	0 or 3

Current Production Virtex-4 FPGA Devices

Table 57 summarizes the current production device stepping.

Table 57: **Current Production Devices**

Device Stepping	Step 2
Example Ordering Code	XQR4VFX60-CF1144V
Device steppings shipped when ordered per Example Ordering Code	Step 1 or 2 only (see Table 56)
Capability Improvements	• T_{CONFIG} requirement is removed • DCM_RESET requirement is removed • DCM_INPUT_CLOCK_STOP requirement is removed by a macro (automatically inserted by ISE software)
CONFIG STEPPING parameter (must be set in UCF file)	“1”
Minimum Software Required	ISE 7.1i SP4
Minimum Speed Specification Required	1.58

Revision History

The following table shows the revision history for this document.

Date	Version	Revisions
03/28/08	1.0	Initial Xilinx release.
12/16/08	1.1	Changed occurrences of “hardened” to “tolerant”.
04/12/10	2.0	Changed document classification from Preliminary Product Specification to Product Specification. Changed product title to “Space-Grade Virtex-4QV FPGAs” and changed product name to “Virtex-4QV FPGA” throughout document. In the first paragraph of "Virtex-4QV FPGA Electrical Characteristics," added “radiation-tolerant” to the description of the Virtex-4QV FPGA. In Table 12, removed table notes referring to obsolete application notes. Added values for XQR4VFX140 device to Table 13, Table 48, Table 49, Table 50, Table 51, Table 52, Table 53, and Table 56. Added Critical Applications disclaimer.

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