Serial Configuration (Index 74h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
74h	Serial Configuration	SLOT 16	REGM 2	REGM 1	REGM 0	DRQEN	DLRQ 2	DLRQ 1	DLRQ 0	X	X	X	X	X	DRRQ 2	DRRQ 1	DRRQ 0	7000h

DRRQ0 Master ACÕ97 Codec DAC Right Request.

DRRQ1 Slave 1 Codec DAC Right Request.

DRRQ2 Slave 2 Codec DAC Right Request.

DLRQ0 Master ACÕ97 Codec DAC Left Request.

DLRQ1 Slave 1 Codec DAC Left Request.

DLRQ2 Slave 2 Codec DAC Left Request.

DRQEN Fills idle status slots with DAC request reads, and stuffs DAC requests into LSB of output address slot. (AC-Link Slot 1.)

REGM0 Master Codec Register Mask.

REGM1 Slave 1 Codec Register Mask.

REGM2 Slave 2 Codec Register Mask.

SLOT16 Enable 16-Bit Slots.

If your system uses only a single AD1819B, you can ignore the register mask and the slave 1/slave 2 request bits. If you write to this register, write ones to all of the register mask bits. The request bits are read-only.

The codec asserts each request bit when the corresponding DAC channel can accept data in the next frame. These bits are snapshots of the codec state taken when the current frame began (effectively, on the rising edge of SYNC), but they also take notice of DAC samples sent in the current frame.

If you set the DRQEN bit, the AD1819B will fill all otherwise unused AC-Link status address and data slots with the contents of register 74h. That makes it somewhat simpler to access the information, because you donÕt need to continually issue AC-Link read commands to get the register contents.

Also, the DAC requests are reflected in Slot 1, Bits (11 . . . 6). These bits are active Lo.

SLOT16 makes all AC-Link slots 16 bits in length, formatted into 16 slots.

Miscellaneous Control Bits (Index 76h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
76h	Misc Control Bits	DACZ	X	X	X	X	DLSR	X	ALSR	MODEN	SRX10D7	SRX8D7	X	X	DRSR	X	ARSR	0000h

ARSR ADC Right Sample Generator Select. Connects right ADC channel to SR0 or SR1.
0 = SR0 Selected.
1 = SR1 Selected.

DRSR DAC Right Sample Generator Select. Connects right DAC channel to SR0 or SR1.
0 = SR0 Selected.
1 = SR1 Selected.

SRX8D7 Multiply SR1 Rate by 8/7.

SRX10D7 Multiply SR1 Rate by 10/7. SRX10D7 and SRX8D7 are mutually exclusive; SRX10D7 has priority if both are set.

MODEN Modem Filter Enable (left channel only). Change only when DACs are powered down.

ALSR ADC Left Sample Generator Select. Connects left ADC channel to SR0 or SR1.
0 = SR0 Selected.
1 = SR1 Selected.

DLSR DAC Left Sample Generator Select. Connects left DAC channel to SR0 or SR1.
0 = SR0 Selected.
1 = SR1 Selected.

DACZ Zero-Fill (vs. repeat sample) if DAC is starved.

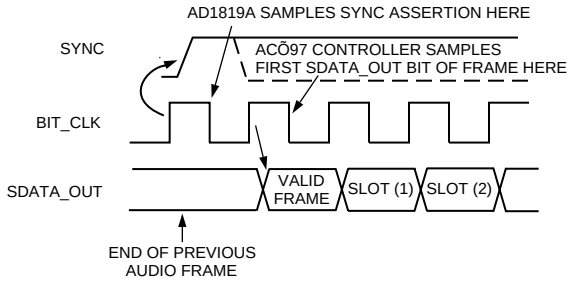


Figure 11. Start of an Audio Output Frame

SDATA_OUTÕs composite stream is MSB justified (MSB first) with all nonvalid slotsÕ bit positions stuffed with 0s by the ACÕ97 controller. The AD1819B ignores invalid slots.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the ACÕ97 controller always stuffs all trailing nonvalid bit positions of the 20-bit slot with 0s. The AD1819B ignores unused bits.

As an example, consider an 8-bit sample stream being played out to one of the AD1819BÕs DACs. The first 8-bit positions are presented to the DAC (MSB justified), followed by the next 12 bit positions, which are stuffed with 0s by the ACÕ97 controller.

When mono audio sample streams are output from the ACÕ97 controller, it is necessary that BOTH left and right stream time slots be filled with the same data.

Slot 1: Command Address Port

The command port is used to control features and request status (see Audio Input Frame Slots l and 2) for AD1819B functions including, but not limited to, mixer settings and power management (refer to the control register section of this specification).

The control interface architecture supports up to sixty-four 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid, odd register (01h, 03h, etc.) accesses are discouraged (defaulting to the preceding even byte boundaryÑi.e., a read to 01h will return the 16-bit contents of 00h). Note that shadowing of the control register file on the ACÕ97 controller is an option left open to the implementation of the ACÕ97 controller. The AD1819BÕs control register file is readable as well as writable.

Audio output frame Slot 1 communicates control register address, and write/read command information to AD1819B.

Command Address Port Bit Assignments:

Bit (19)	Read/Write Command	(1 = Read, 0 = Write)
Bit (18:12)	Control Register Index	(64 16-Bit Locations, Addressed On Even Byte Boundaries)
Bit (11:0)	Reserved	(Stuffed with 0s)

The first bit (MSB) sampled by the AD1819B indicates whether the current control transaction is a read or a write operation. The following 7-bit positions communicate the targeted control register address. The trailing 12-bit positions within the slot are reserved.

Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, Bit 19).

Bit (19:4)	Control Register Write Data	(Stuffed with 0s If Current Operation Is Not a Write)
Bit (3:0)	Reserved	(Stuffed with 0s)

If the current command port operation is not a write, the entire slot time should be stuffed with 0s by the ACÕ97 controller.

Slot 3: PCM Playback Left Channel

Audio output frame Slot 3 is the composite digital audio left playback stream. In a typical ÒGames CompatibleÓ PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the ACÕ97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20 bits is transferred, the ACÕ97 controller should stuff all trailing nonvalid bit positions within this time slot with 0s.

Slot 4: PCM Playback Right Channel

Audio output frame Slot 4 is the composite digital audio right playback stream. In a typical ÒGames CompatibleÓ PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the ACÕ97 controller or host processor) with music synthesis output samples. If a sample stream of resolutionless than 20 bits is transferred, the ACÕ97 controller should stuff all trailing nonvalid bit positions within this time slot with 0s.

MULTIPLE CODE CONFIGURATION

Setting Up Multiple Codecs

The AD1819B may be used with up to two additional AD1819 or AD1819B codecs. In order to configure the codecs as Master, Slave 1 or Slave 2, refer to the following table.

CS1	CS0	Configuration
0	0	Slave 1 Codec
0	1	Slave 2 Codec
1	0	Master Codec
1	1	ACÕ97 Mode Codec

0 = Ground; 1 = V_{DD}.

The XTAL_IN pin on the Slave Codecs ÒmustÓ be tied to ground and the CHAIN_IN pin ÒmustÓ be tied to ground on the last codec Slave 1 (on a 2-codec design) or Slave 2 (on a 3-codec design). See Figures 15, 16 and 17.

Configure the Codec Resources

Programing REGM (2:0) bits in the Serial Configuration Register (74h) allows the digital controller read write access to all the internal registers on each codec according to the following table.

REGM2	REGM1	REGM0	Read	Write
0	0	0	x	x
0	0	1	Master	Master
0	1	0	Slave 1	Slave 1
0	1	1	Master	Master, Slave 1
1	0	0	Slave 2	Slave 2
1	0	1	Master	Master, Slave 2
1	1	0	Slave 1	Slave 1, Slave 2
1	1	1	Master	Master, Slave 1, Slave 2

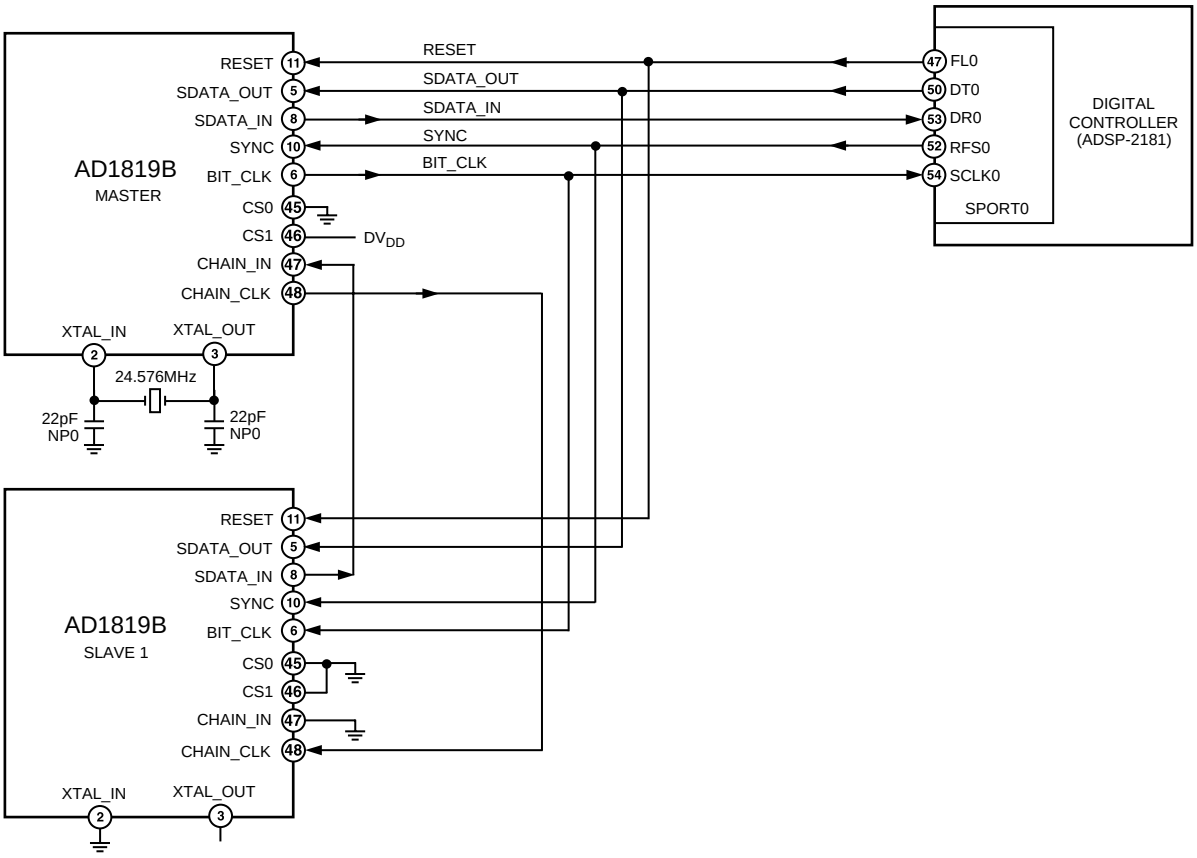
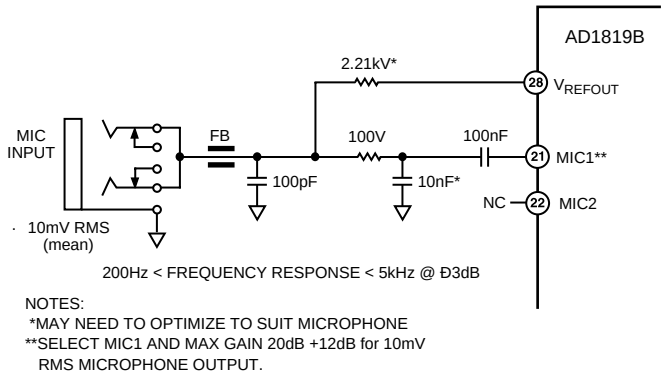


Figure 17. Two Codec System Example



NOTES:
*MAY NEED TO OPTIMIZE TO SUIT MICROPHONE
**SELECT MIC1 AND MAX GAIN 20dB +12dB for 10mV RMS MICROPHONE OUTPUT.

Figure 18. Microphone Input