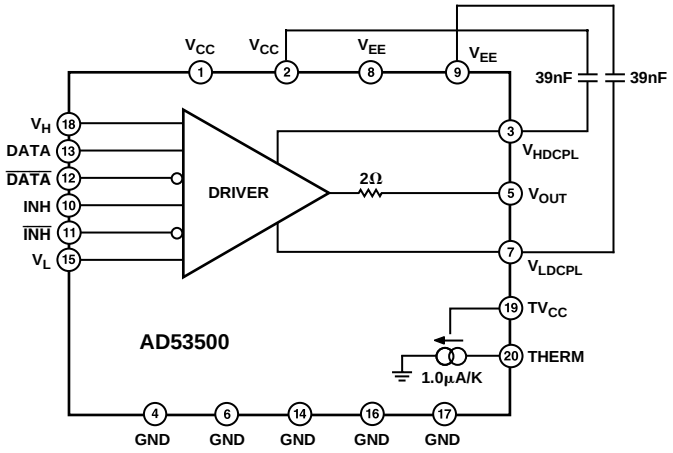
High Speed, High Current Capability Pin Driver

AD53500

FEATURES
–2 V to +6 V Output Range
2.5 Ω Output Resistance
2.5 ns Tr/Tf for a 3 V Step
300 MHz Toggle Rate
Can Drive 25 Ω Lines and Lower
Peak Dynamic Current Capability of 400 mA
Inhibit Leakage <1 μA
On-Chip Temperature Sensor

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems
Instrumentation and Characterization Equipment

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION:
The AD53500 is a complete high speed driver designed for use in digital or mixed signal test systems where high speed and high output drive capabilities are needed. Combining a high speed monolithic process and a unique surface mount package, this product attains superb electrical performance while preserving optimum packing densities and long-term reliability thanks to an ultrasmall 20-lead, PSOP package with built-in heat sink.

High and low reference levels can be set within a –2 V to +6 V range with low offset voltage and high gain accuracy. A 2.5 Ω output resistance allows use of an external backmatch resistor for application to 50 Ω, 25 Ω or other complex impedance load requirements. Without a backmatch resistor it is also capable of driving highly capacitive loads, typically achieving a rise/fall time of less than 10 ns with a 1000 pF capacitance. To test I/O devices, the pin driver can be switched into a high impedance state (Inhibit Mode), electrically removing the driver from the path. The pin driver leakage current in inhibit is typically less than 1 μA and output capacitance is typically less than 18 pF.

Transitions from HI/LO or to inhibit are controlled through the data and inhibit inputs. The input circuitry utilizes high-speed differential inputs with a common-mode range of –2 V to +5 V. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single-ended CMOS or TTL logic source or any combination over the common-mode range. The analog logic HI/LO inputs are equally easy to interface, typically requiring 50 μA of bias current.

REV. 0

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AD53500–SPECIFICATIONS

(All specifications are at T_J = +85°C ± 5°C, $+V_S$ = +10 V ± 3%, $-V_S$ = +6 V ± 3% unless otherwise noted. All temperature coefficients are measured over T_J = 75°C–95°C). (In test figures, voltmeter loading is 1 MΩ or greater, scope probe loading is 100 kΩ in parallel with 5 pF.) 39 nF capacitors must be connected between V_{CC} and V_{HDCPL} and between V_{EE} and V_{LDCPL}.

Parameter	Min	Typ	Max	Units	Test Conditions
DIFFERENTIAL INPUT CHARACTERISTICS (DATA to $\overline{DATA}$, INH to $\overline{INH}$)					
Common-Mode Input Voltage	–2		+5	Volts	
Differential Input Range		ECL or TTL			ECL = –0.8 V/–1.8 V, TTL = 0 V/5 V
Bias Current		±100		µA	V_{CM} = –2 V, +5 V
REFERENCE INPUTS					
Bias Currents	–50		+50	µA	V_L, V_H = 5 V
OUTPUT CHARACTERISTICS					
Logic High Range	+1		+6	Volts	DATA = H, V_L = –2 V, V_H = +1 V to +6 V
Logic Low Range	–2		+2	Volts	DATA = L, V_L = –2 V to +2 V, V_H = +6 V
Amplitude (V_H and V_L)	0.1		8	Volts	V_L = –0.05 V, V_H = +0.05 V and V_L = –2 V, V_H = +6 V
V_H, V_L Interaction	–10		+10	mV	100 mV Output Amplitude
Absolute Accuracy					
V_H Offset	–100		+100	mV	DATA = H, V_H = 0 V, V_L = –2 V
V_H Gain + Linearity Error		±0.3 ±5		% of V_H + mV	DATA = H, V_L = –2 V, V_H = +1 V to +6 V
V_L Offset	–100		+100	mV	DATA = L, V_L = 0 V, V_H = +6 V
V_L Gain + Linearity Error		±0.3 ±5		% of V_L + mV	DATA = L, V_L = –2 V to +2 V, V_H = +6 V
Offset TC, V_H or V_L		0.5		mV/°C	V_L, V_H = 0 V, +5 V and –2 V, 0 V
Output Resistance	1.5	2.5	5.5	Ω	V_H = +3 V, V_L = 0 V, I_{OUT} = 0, –30 mA, +30 mA
Dynamic Current Limit		400		mA	C_{BYP} = 39 nF, V_H = +5 V, V_L = 0 V C_{LOAD} = 1000 pF, Tr/Tf = 10 ns
Static Current Limit	60		180	mA	Output to –2 V, V_H = +6 V, V_L = –1 V,
	–180		–60	mA	DATA = H and Output to +6 V, V_H = +6 V, V_L = –2 V, DATA = L
DYNAMIC PERFORMANCE, DRIVE (V_H and V_L)					
Propagation Delay Time		2.5		ns	Measured at 50%, V_H = +400 mV, V_L = –400 mV
Propagation Delay TC		1		ps/°C	Measured at 50%, V_H = +400 mV, V_L = –400 mV
Delay Matching, Edge-to-Edge		100		ps	Measured at 50%, V_H = +400 mV, V_L = –400 mV
Rise and Fall Time					
1 V Swing		0.85		ns	Measured 20%–80%, V_L = 0 V, V_H = 1 V
3 V Swing		2.5		ns	Measured 10%–90%, V_L = 0 V, V_H = 3 V
5 V Swing		4.0		ns	Measured 10%–90%, V_L = 2 V, V_H = 3 V
Rise and Fall Time TC					
1 V Swing		±1		ps/°C	Measured 20%–80%, V_L = 0 V, V_H = 1 V
3 V Swing		±2		ps/°C	Measured 10%–90%, V_L = 0 V, V_H = 3 V
5 V Swing		±3		ps/°C	Measured 10%–90%, V_L = 0 V, V_H = 5 V
Overshoot, Undershoot and Preshoot		+5.0 +30		% of Step + mV	V_H–V_L = 0.5 V, 1 V, 3 V, 8 V
Settling Time					
to 15 mV		40		ns	V_L = 0 V, V_H = 0.5 V
to 4 mV		8		µs	V_L = 0 V, V_H = 0.5 V
Delay Change vs. Pulsewidth		100		ps	V_L = 0 V, V_H = 2 V, Pulsewidth = 2.5 ns/ Period = 10 ns and Pulsewidth = 30 ns/ Period = 120 ns
Minimum Pulsewidth					
3 V Swing		3.8		ns	V_L = 0 V, V_H = 3 V, Output = 2.7 V p-p, Measure at 50%
5 V Swing		5.5		ns	V_L = 0 V, V_H = 5 V, Output = 4.5 V p-p, Measure at 50%
Toggle Rate		300		MHz	V_L = –1.8 V, V_H = –0.8 V, V_{OUT} > 600 mV p-p

Parameter	Min	Typ	Max	Units	Test Conditions
DYNAMIC PERFORMANCE, INHIBIT					
Delay Time, Active to Inhibit	2		10	ns	Measured at 50%, V_H = +2 V, V_L = –2 V, 50 Ω Terminated to Ground
Delay Time, Inhibit to Active	2		10	ns	Measured at 50%, V_H = +2 V, V_L = –2 V, 50 Ω Terminated to Ground
I/O Spike		<200		mV, p-p	V_H = 0 V, V_L = 0 V
Output Leakage	–1.0		+1.0	µA	V_{OUT} = –2 V to +6 V
Output Capacitance		18		pF	Driver Inhibited
PSRR, Drive Mode		35		dB	V_S = V_S ± 3%
POWER SUPPLIES					
Total Supply Range		16		V	
Positive Supply		+10		V	
Negative Supply		–6		V	
Positive Supply Current		85	95	mA	
Negative Supply Current		88	98	mA	
Total Power Dissipation		1.37	1.54	W	
Temperature Sensor Gain Factor		1.0		µA/K	R_{LOAD} = 10 kΩ, V_{SOURCE} = +10 V

NOTES
Connecting or shorting the decoupling capacitors to ground will result in the destruction of the device.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage
- $+V_S$ to GND . . . . . +11 V
- $–V_S$ to GND . . . . . –7 V
- $+V_S$ to $–V_S$ . . . . . +18 V

Inputs
- DATA, $\overline{\text{DATA}}$, INH, $\overline{\text{INH}}$ . . . . . +5 V, –3 V
- DATA to $\overline{\text{DATA}}$, INH to $\overline{\text{INH}}$ . . . . . ±3 V
- V_H, V_L to GND . . . . . +7 V, –3 V
- V_H to V_L . . . . . +10 V, 0 V

Outputs
- V_{OUT} Short Circuit Duration to Ground . . . . . Indefinite[2]
- V_{OUT} Range in Inhibit Mode . . . . . See Figure 1
- V_{HDCPL} . . . . . Do Not Connect Except for Cap to V_{CC}[3]
- V_{LDCPL} . . . . . Do Not Connect Except for Cap to V_{EE}[3]
- THERM . . . . . +V_S, 0 V

Environmental
- Operating Temperature (Junction) . . . . . +175°C
- Storage Temperature . . . . . –65°C to +150°C
- Lead Temperature (Soldering, 10 sec)[4] . . . . . +260°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Output short circuit protection is guaranteed as long as proper heat sinking is employed to ensure compliance with the operating temperature limits.
[3]The V_{HDCPL} and V_{LDCPL} capacitors may be replaced by a low value resistor for higher dc-current drive capability.
[4]To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C ± 5°C (75°F ± 10°F) with relative humidity not to exceed 65%.

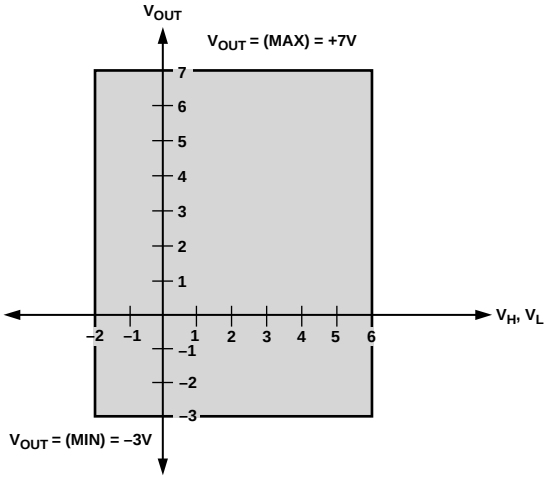


FIGURE 1 SHOWS THE MAXIMUM ALLOWABLE LIMITS FOR V_{OUT} AS A FUNCTION OF V_{HIGH} AND V_{LOW} WHEN THE DRIVER IS OPERATING IN INHIBIT MODE. THE LIMITS, AS STATED BEFORE, ARE MAXIMUM RATINGS ONLY, AND SHOULD NOT BE USED AS THE PART'S NORMAL OPERATING RANGE. THIS RANGE APPLIES ONLY TO SUPPLIES OF +V_S = +10V AND –V_S = –6V AND SHOULD BE DERATED PROPORTIONALLY FOR LOWER SUPPLIES.

V_{HIGH} / V_{LOW}

Figure 1. Absolute Maximum Ratings for V_{OUT}

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53500 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

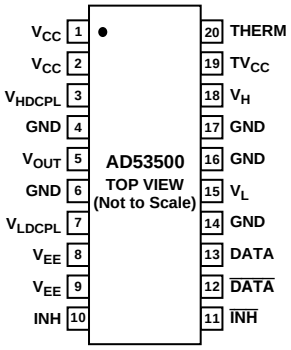


Table I. Pin Driver Truth Table

DATA	$\overline{DATA}$	INH	$\overline{INH}$	Output State
0	1	0	1	V_L
1	0	0	1	V_H
0	1	1	0	Hi-Z
1	0	1	0	Hi-Z

Table II. Package Thermal Characteristics

Air Flow, FM	θ_{JC}, °C/W	θ_{JA}, °C/W
50	3.28	49.1
400	3.91	33.74

PIN FUNCTION DESCRIPTIONS

Pin Name	Pin Number	Description
V_{CC}	1, 2	Positive Power Supply. Both pins should be connected to minimize inductance and allow maximum speed of operation. V_{CC} should be decoupled to GND with a low inductance 0.1 µF capacitor.
V_{EE}	8, 9	Negative Power Supply. Both pins should be connected to keep the inductance down and allow maximum speed of operation. V_{EE} should be decoupled to GND with a low inductance 0.1 µF capacitor.
GND	4, 6, 14, 16, 17	Device Ground. These pins should be connected to the circuit board's ground plane at the pins.
V_L	15	Analog input that sets the voltage level of a Logic 0 of the driver. Determines the driver output for $\overline{DATA}$ > DATA.
V_H	18	Analog input that sets the voltage level of a Logic 1 of the driver. Determines the driver output for DATA > $\overline{DATA}$.
V_{OUT}	5	The Driver Output.
V_{HDCPL}	3	Internal supply decoupling for the output stage. This pin is connected to V_{CC} through a 39 nF (minimum) capacitor.
V_{LDCPL}	7	Internal supply decoupling for the output stage. This pin is connected to V_{EE} through a 39 nF (minimum) capacitor.
INH, $\overline{INH}$	10, 11	Differential inputs that control the high impedance state of the driver. When INH > $\overline{INH}$, the driver goes into a high impedance state.
DATA, $\overline{DATA}$	13, 12	Differential inputs that determine the high and low state of the driver. Driver output is high for DATA > $\overline{DATA}$.
TV_{CC}	19	Temperature Sensor Startup Pin. This pin should be connected to V_{CC}.
THERM	20	Temperature sensor output pin. A resistor (10 kΩ) should be connected between THERM and V_{CC}. The approximate die temperature can be determined by measuring the current through the resistor. The typical scale factor is 1 µA/K.

ORDERING GUIDE

Model	Package Description	Shipment Method, Quantity Per Shipping Container	Package Option
AD53500JRP	20-Lead Power SOIC	Tube, 38 Pieces	RP-20

APPLICATION INFORMATION

Power Supply Distribution, Bypassing and Sequencing

The AD53500 draws substantial transient currents from its power supplies when switching between states and careful design of the power distribution and bypassing is key to obtaining specified performance. Supplies should be distributed using broad, low inductance traces or (preferably) planes in a multilayered board with a dedicated ground-plane layer. All of the device's power supply pins should be used to minimize the internal inductance presented by the part's bond wires. Each supply must be bypassed to ground with at least one 0.1 µF capacitor; chip-style capacitors are preferable as they minimize inductance. One or more 10 µF (or greater) Tantalum capacitors per board are also advisable to provide additional local energy storage.

The AD53500's current-limit circuitry also requires external bypass capacitors. Figure 2 shows a simplified schematic of the positive current-limit circuit. Excessive collector current in output transistor Q49 creates a voltage drop across the 5 Ω resistor, which turns on PNP transistor Q48. Q48 diverts the rising-edge slew current, shutting down the current mirror and removing the output stage's base drive. The V_{HDCPL} pin should be bypassed to the positive supply with a 0.039 µF capacitor, while the V_{LDCPL} pin (not shown) requires a similar capacitor to the negative supply. These capacitors ensure that the AD53500 does not current-limit during normal output transitions up its full 8 V rated step size. Both capacitors must have minimum-length connections to the AD53500. Here again, chip capacitors are ideal.

Several points about the current-limit circuitry should be noted. First, the limiting currents are not tightly controlled, as they are functions of both absolute transistor V_{BE} and junction temperature; higher dc output current is available at lower junction temperatures. Second, it is essential to connect the V_{HDCPL} capacitor to the positive supply (and the V_{LDCPL} capacitor to the negative supply)—failure to do so causes considerable thermal stress in the current-limiting resistor(s) during normal supply sequencing and may ultimately cause them to fail, rendering the part nonfunctional. Finally, the AD53500 may appear to function normally for small output steps (less than 3 V or so) if one or both of these caps is absent, but it may exhibit excessive rise or fall times for steps of larger amplitude.

The AD53500 does not require special power-supply sequencing. However, good design practice dictates that digital and analog control signals not be applied to the part before the supplies are stable. Violating this guideline will not normally destroy the part, but the active inputs can draw considerable current until the main supplies are applied.

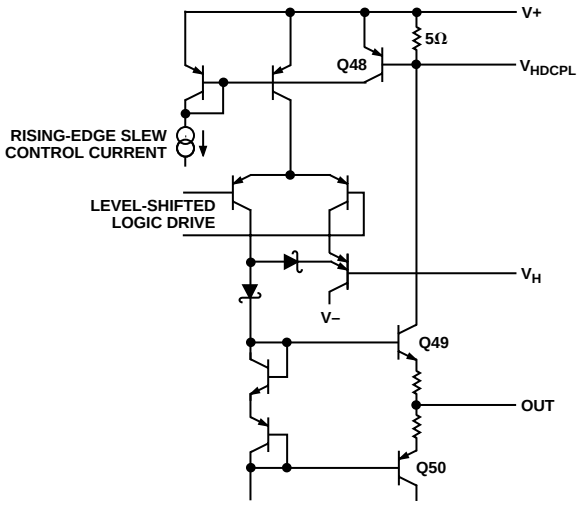


Figure 2. Simplified Schematic of the AD53500 Output Stage and Positive Current-Limit Circuitry

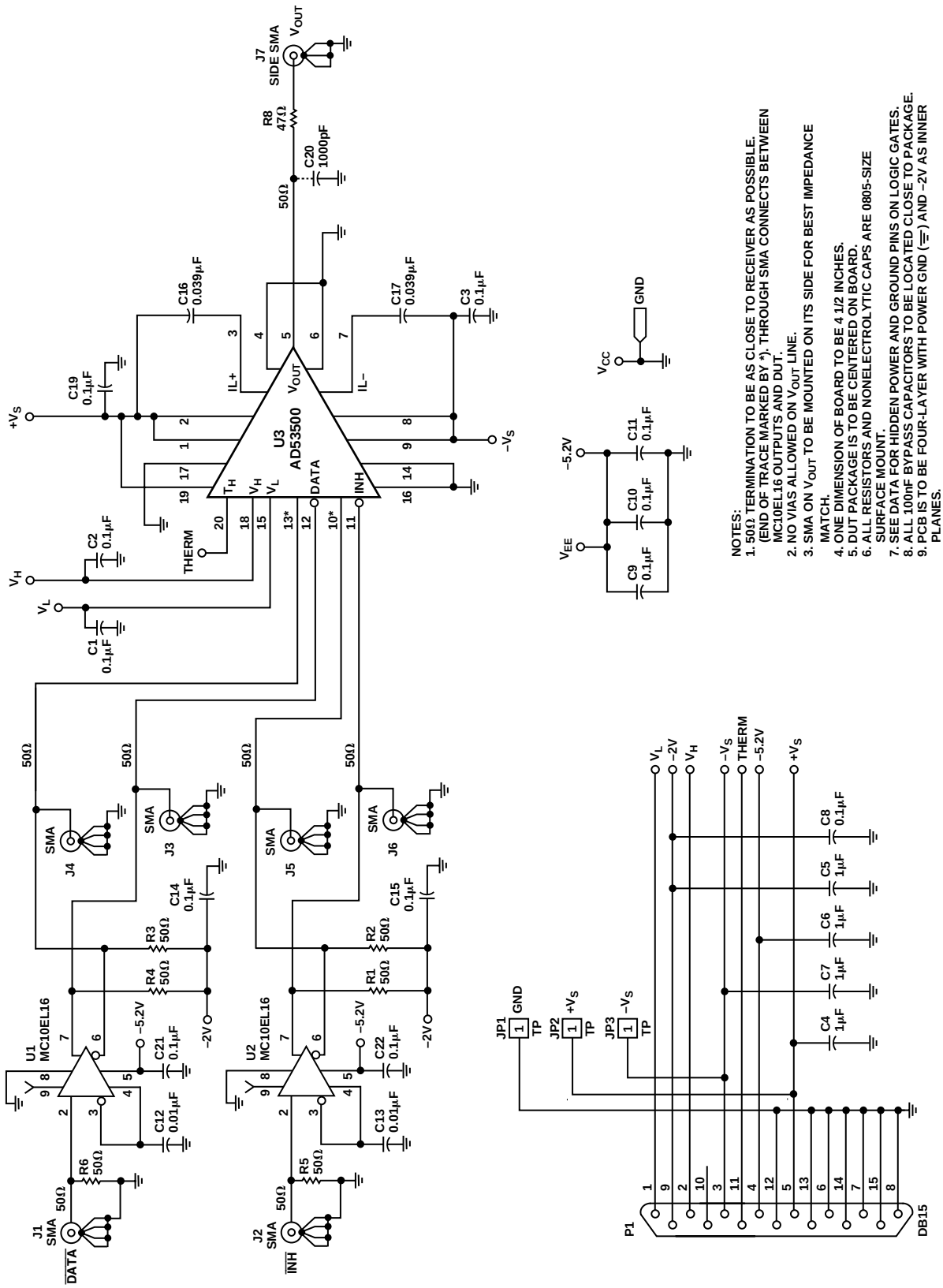
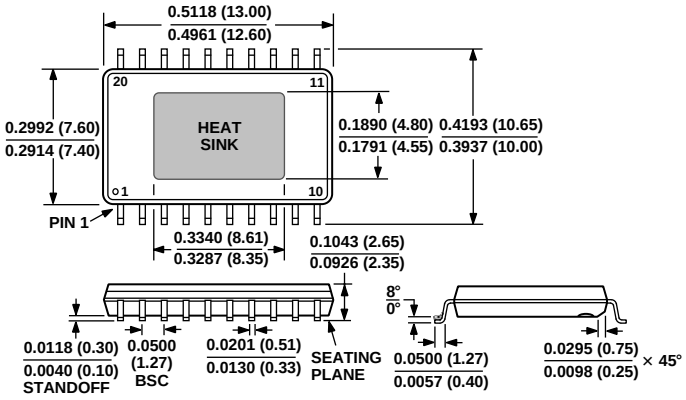


Figure 3. Evaluation Board Schematic

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Thermally Enhanced Small Outline Package (PSOP)
(RP-20)



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