

### 1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at [www.analog.com/AD561](http://www.analog.com/AD561)

### 2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
<b>AD561-703D</b>	Low Cost 10-Bit Monolithic D/A Converter
<b>AD561-713D</b>	Radiation Tested, Low Cost 10-Bit Monolithic D/A Converter

### 2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
D	GDIP2-T16	16-Lead sidebraced dual-in-line package

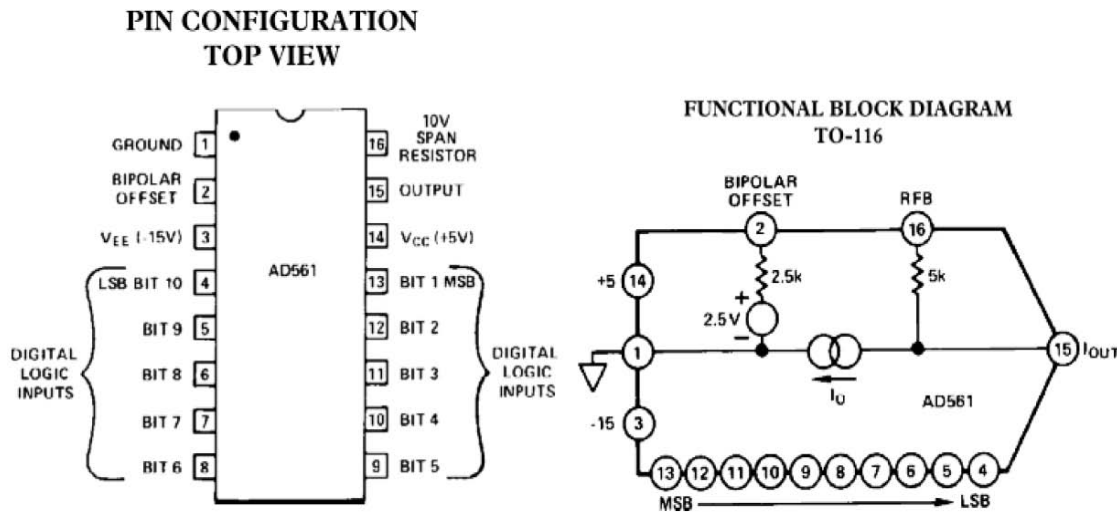


Figure 1 - Terminal connections.

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Rev. F

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### 3.0 Absolute Maximum Ratings. ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Operating Temperature Range.....	-55°C to +125°C
Storage Temperature Range.....	-65°C to +150°C
Power Dissipation .....	500mW
Lead Temperature (Soldering, 60 sec.) .....	+300°C
Maximum Junction Temperature ( $T_J$ ) .....	+175°C
Supply Voltage.....	$\pm 16.5\text{V}$
Digital Input Voltage ( $V_{IN}$ ) .....	$V_{CC}$ to Ground
Output Voltage Compliance ( $V_{OUT}$ ).....	-2V to +10V
10V Span Resistor to Ground.....	$V_{CC}$ to $V_{EE}$

### 3.1 Thermal Characteristics:

Thermal Resistance, Sidebraced (D) Package

Junction-to-Case ( $\Theta_{JC}$ ) = 30°C/W Max

Junction-to-Ambient ( $\Theta_{JA}$ ) = 100°C/W Max

### 4.0 Electrical Table:

**TABLE I**

Parameter See notes at end of table	Symbol	Conditions (Note 1/)	Sub-group	Limit Min	Limit Max	Units
Relative Accuracy	RA	All Bits with + or - Errors on	1		½	LSB
Differential Nonlinearity	DNL	Major carry transitions	1, 2, 3		1	
Gain Error	$A_E$	With fixed 25Ω resistor	1		$\pm ½$	%FS
Gain Error TC	$TCA_E$		2, 3		$\pm 60$	ppm of FS /°C
Unipolar Offset Error	$V_{OS}$	Note 2	1		$\pm 0.05$	%FS
Unipolar Error TC	$TCV_{OS}$				$\pm 10$	ppm of FS /°C
Bipolar Zero Error	$B_{PZE}$	With 10Ω resistor	1		$\pm 3.5$	LSB
Bipolar Zero Error TC	$TCB_{PZE}$		2, 3		$\pm 20$	ppm of FS /°C
Output Current	$I_{OUT}$	Digital inputs at logic "1"	1	1.5	2.4	mA
Power Supply Gain Sensitivity	PSS1	$V_{CC}$ , +4.5V to +5.5V $V_{CC}$ , 13.5V to +16.5V	1		$\pm 10$	ppm of FS %
	PSS2	$V_{EE}$ , -10.8V to -13.2V $V_{EE}$ , - 13.2V to -16.5V	1		$\pm 25$	
Power Supply Current 2/	$I_{CC}$	$V_{CC}$ , +4.5V to +16.5V	1		10	mA
	$I_{EE}$	$V_{EE}$ , -10.8V to -16.5V	1		16	
Power Dissipation	PD		1		500	mW
Digital Input High Voltage	$V_{IH}$		1	2.0		V
Digital Input Low Voltage	$V_{IL}$		1		0.8	
Digital Input High Current	$I_{IH}$	Digital "1" = 15V	1		$\pm 100$	nA
Digital Input Low Current	$I_{IL}$	Digital "0" = 0V	1		$\pm 25$	μA

#### TABLE I NOTES:

1/  $V_{CC} = +5\text{V}$ ,  $V_{EE} = -15\text{V}$ , unless otherwise specified.

2/ Also tested in CMOS mode.  $V_{CC} = +15\text{V}$ ,  $V_{EE} = -15\text{V}$ ,  $V_{IH} = 10.5\text{V}$ ,  $V_{IL} = 4.5\text{V}$ .

#### 4.1 Electrical Test Requirements:

<b>Table II</b>	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3 <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Deltas excluded from PDA

2/ See table III for delta parameters and limits.

#### 4.2 Table III. Lifetest / Burn-in delta limits.

<b>Table III</b>				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
I <sub>CC</sub>	10	10	±3	mA
I <sub>EE</sub>	16	16	±3	mA
B <sub>PZE</sub>	±3.5	±3.5	±2	LSB

#### 5.0 Life Test/Burn-In Circuit:

- 5.1 HTRB is not applicable for this drawing.
- 5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
- 5.3 Steady state life test is per MIL-STD-883 Method 1005.

# AD561

Rev	Description of Change	Date
A	Initiate	June 30, 2000
B	Correct Typo's in Table I. No limits changed. Update Table III.	June 29, 2001
C	Update web address. Delete subgroups 4, 5, & 6 from Table II as they are not on Table I.	Feb. 20, 2002
D	Update web address. Delete Burn-in Circuit.	Jun. 20, 2003
E	Correct Typo's in 2.1 Case Outline, Descriptive designator. Change from GDIP1-T16 to GDIP2-T16.	Nov. 18, 2003
F	Update header/footer & add to 1.0 Scope description.	Feb. 21, 2008