



# DI CMOS Analog Switches with Data Latches

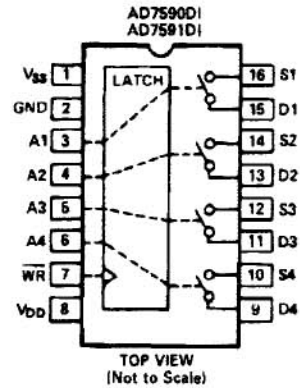
## AD7590DI/AD7591DI/AD7592DI

### FEATURES

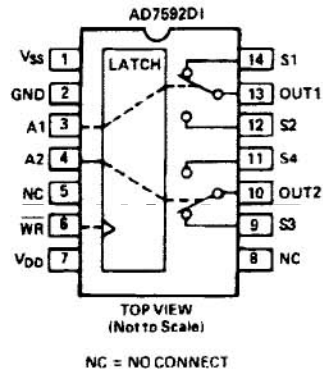
- SCR Latch-Proof
- Overvoltage-Proof:  $\pm 25V$
- Low  $R_{ON}$ :  $60\Omega_{typ}$
- Buffered Switch Logic
- TTL, CMOS Compatible
- Monolithic Dielectrically-Isolated CMOS
- Pin Compatible with AD7510DI Series

### FUNCTIONAL BLOCK DIAGRAMS

#### 16-Pin DIP



#### 14-Pin DIP



### GENERAL DESCRIPTION

The AD7590DI, AD7591DI and AD7592DI are a family of protected (latch-proof) dielectrically isolated CMOS switches featuring overvoltage protection up to  $\pm 25V$  above the power supplies. Microprocessor interfacing is facilitated by the provision of on-chip data latches.

The AD7590DI and AD7591DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the switch control logic is inverted. The AD7592DI has two independent SPDT switches packaged in a 14-pin DIP.

### CONTROL LOGIC (WR HELD LOW)

AD7590DI: Switch "ON" for Address "HIGH"

AD7591DI: Switch "ON" for Address "LOW"

AD7592DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

### REV. A

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# AD7590DI/AD7591DI/AD7592DI—SPECIFICATIONS ( $V_{DD} = 15V$ , $V_{SS} = -15V$ unless otherwise noted)

Parameter	Model	$T_A = +25^\circ\text{C}$ (K, B, T)	$T_A =$ 0 to $+70^\circ\text{C}$ (K) $-25^\circ\text{C}$ to $+85^\circ\text{C}$ (B)	$-55^\circ\text{C}$ to $+125^\circ\text{C}$ (T)	Units	Test Conditions/Comments
<b>ANALOG SWITCH</b>						
Analog Signal Range	All	$\pm 10$	$\pm 10$	$\pm 10$	Volts	
$R_{ON}^1$	All	60	60	60	$\Omega$ typ	$-10V \leq V_S \leq +10V$ , $I_{DS} = 1mA$ ; Test Circuit 1
	All	90	120	150	$\Omega$ max	
$R_{ON}$ Match <sup>2</sup>	All	2	2	2	$\Omega$ typ	$V_S = 0$ , $I_{DS} = 1mA$
$R_{ON}$ Match Drift <sup>2</sup>	All	0.01	0.01	0.01	$\Omega/^\circ\text{C}$ typ	$V_S = 0$ , $I_{DS} = 1mA$
$I_{1, OFF}^1$	AD7590DI	0.5	0.5	0.5	nA typ	Test Circuit 2
	AD7591DI	5	50	200	nA max	
$I_S OFF^1$	All	0.5	0.5	0.5	nA typ	Test Circuits 2 & 4
	All	5	50	200	nA max	
$I_D (I_S) ON^1$	All	0.5	0.5	0.5	nA typ	Test Circuit 3
	All	5	50	200	nA max	
$I_{OUT}^1$	AD7592DI	1	1	1	nA typ	Test Circuit 4
	All	10	100	400	nA max	
$C_S (C_D) OFF^3$	All	10	10	10	pF typ	
$C_S (C_D) ON^3$	All	30	30	30	pF typ	
$C_{DS} (C_{S-OUT})^3$	All	1	1	1	pF typ	
$C_{DD} (C_{SS})^3$	All	0.5	0.5	0.5	pF typ	
$C_{OUT}^3$	AD7592DI	40	40	40	pF typ	
<b>DIGITAL CONTROL</b>						
$V_{IN1}^1$	All	0.8	0.8	0.8	V max	
$V_{INH}^1$	All	2.4	2.4	2.4	V min	
$C_{IN}^3$	All	7	7	7	pF typ	
$I_{INL}$ or $I_{INH}^{1,4}$	All	1	1	1	$\mu\text{A}$ max	$V_{IN} = 0$ or $V_{DD}$
<b>DYNAMIC CHARACTERISTICS</b>						
$t_{ON}^2$	AD7590DI	250	380	380	ns max	Test Circuit 5
	AD7591DI	400	500	500	ns max	
$t_{OFF}^2$	AD7590DI	400	500	500	ns max	Test Circuit 5
	AD7591DI	250	380	380	ns max	
$t_{TRANSITION}^2$	AD7592DI	350	450	450	ns max	Test Circuit 6
Write Pulse-Width ( $t_{WR}$ ) <sup>2</sup>	All	250	300	400	ns min	See Figure 1
Address Setup Time ( $t_{AS}$ ) <sup>2</sup>	All	300	300	400	ns min	See Figure 1
Address Hold Time ( $t_{AH}$ ) <sup>2</sup>	All	20	30	40	ns min	See Figure 1
Off Isolation <sup>3</sup> (Analog Input to Analog Output)	All	-85	-85	-85	dB typ	$A$ , $\overline{WR} = 0.8V$ ; $V_S = 10V$ (Pk-Pk); $f = 1kHz$ , $R_L = 10k\Omega$
Crosstalk <sup>3</sup> (Digital Input to Analog Output)	All	5	5	5	mV peak, typ	$R_L = 1M\Omega$ , $C_L = 15pF$ ; $V_{INH} = 3V$ , $V_{INL} = 0V$ ; $t_{RISE} = t_{FALL} = 20ns$ ; $\overline{WR}$ held HIGH
$Q_{INJ}^3$ (Charge Injection)	All	55	55	55	pC typ	Test Circuit 7
<b>POWER SUPPLY</b>						
$I_{DD}^1$	All	1	1.5	2	mA max	Digital Inputs = $V_{INL}$ or $V_{INH}$
$I_{SS}$	All	1	1	1	mA max	

## NOTES

<sup>1</sup>100% tested.

<sup>2</sup>Guaranteed, not production tested.

<sup>3</sup>Typical values for information only, not subject to test.

<sup>4</sup>Inputs are MOS gates typical current less than 10nA.

Specifications subject to change without notice.

## TIMING AND CONTROL SEQUENCE

Figure 1 shows the timing sequence for latching the switch address inputs. The latches are level sensitive and, therefore, while  $\overline{WR}$  is held low the latches are transparent and the switches respond to the address inputs. The digital inputs are latched on the rising edge of  $\overline{WR}$ .

NOTE: All digital input signals rise and fall times measured from 10% to 90% of 3V.  $t_R = t_F = 20ns$ .

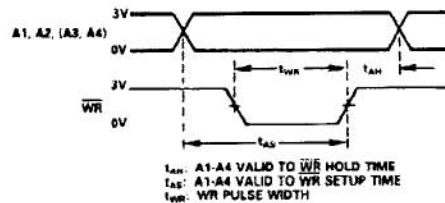


Figure 1. Timing and Control Sequence

# AD7590DI/AD7591DI/AD7592DI

## ABSOLUTE MAXIMUM RATINGS\*

( $T_A = +25^\circ\text{C}$  unless otherwise noted)

$V_{DD}$ to GND	+17V
$V_{SS}$ to GND	-17V
<b>Overvoltage at <math>V_D</math> (<math>V_S</math>), One Switch Only</b>	
(1 $\mu\text{s}$ surge)	$V_{DD} + 25\text{V}$ or $V_{SS} - 25\text{V}$
(Continuous)	$V_{DD} + 20\text{V}$ or $V_{SS} - 20\text{V}$
or 20mA, Whichever Occurs First	
Switch Current ( $I_{DS}$ , Continuous)	50mA
Switch Current ( $I_{DS}$ , Surge)	150mA
1ms Duration, 10% Duty Cycle	
Digital Input Voltage Range	-0.3V to $V_{DD} + 0.3\text{V}$
<b>Power Dissipation (Any Package)</b>	
Up to $+75^\circ\text{C}$	450mW
Derates above $+75^\circ\text{C}$ by	6mW/ $^\circ\text{C}$
Storage Temperature	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
<b>Operating Temperature</b>	
Plastic (KN Versions)	0 to $+70^\circ\text{C}$
Cerdip (BQ Versions)	$-25^\circ\text{C}$ to $+85^\circ\text{C}$
Cerdip (TQ Versions)	$-55^\circ\text{C}$ to $+125^\circ\text{C}$

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Option <sup>2</sup>
AD7590DIKN	$0^\circ\text{C}$ to $+70^\circ\text{C}$	N-16
AD7590DIKP	$0^\circ\text{C}$ to $+70^\circ\text{C}$	P-20A
AD7590DIBQ	$-25^\circ\text{C}$ to $+85^\circ\text{C}$	Q-16
AD7590DITQ	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	Q-16
AD7591DIKN	$0^\circ\text{C}$ to $+70^\circ\text{C}$	N-16
AD7591DIKP	$0^\circ\text{C}$ to $+70^\circ\text{C}$	P-20A
AD7591DIBQ	$-25^\circ\text{C}$ to $+85^\circ\text{C}$	Q-16
AD7591DITQ	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	Q-16
AD7592DIKN	$0^\circ\text{C}$ to $+70^\circ\text{C}$	N-14
AD7592DIKP	$0^\circ\text{C}$ to $+70^\circ\text{C}$	P-20A
AD7592DIBQ	$-25^\circ\text{C}$ to $+85^\circ\text{C}$	Q-14
AD7592DITQ	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	Q-14

### NOTES

<sup>1</sup>To order MIL-STD-883C, Class B processed parts, add /883B to part number. Refer to the Analog Devices Military Products Databook (1990) for military data sheet.

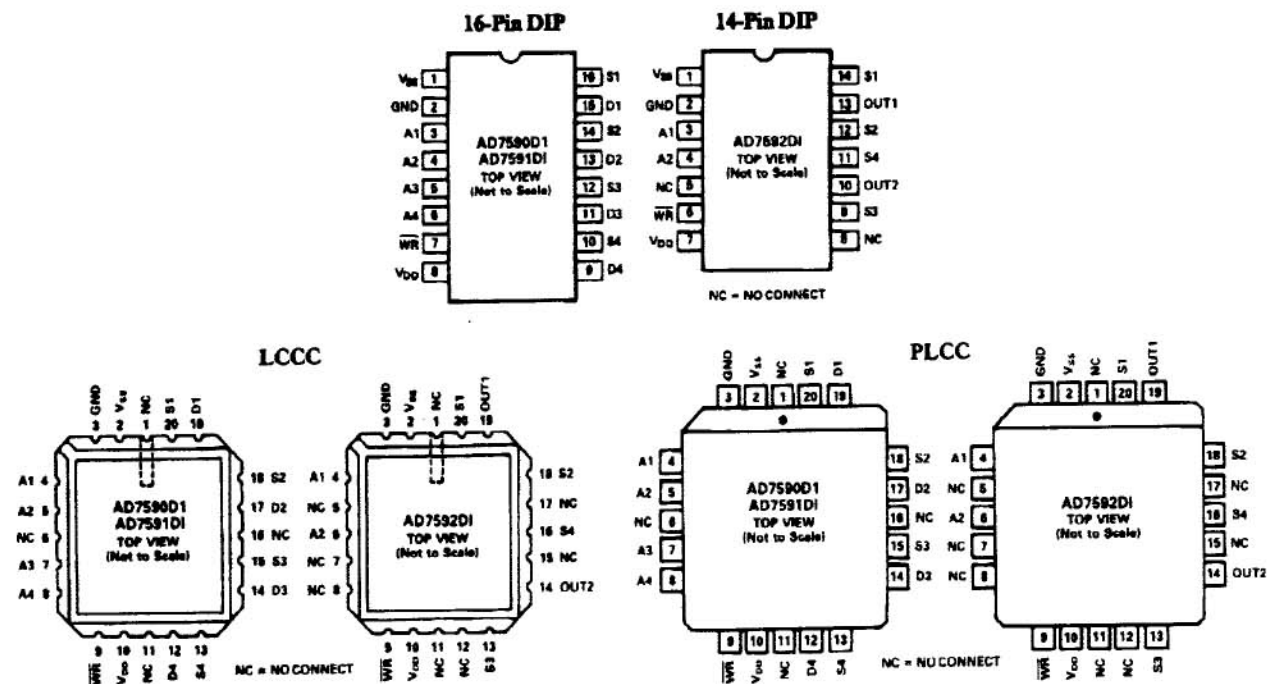
<sup>2</sup>N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier Q = Cerdip. For Hermetic Surface Mount package, contact your local sales office.

### CAUTION:

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



## PIN CONFIGURATIONS



# AD7590DI/AD7591DI/AD7592DI

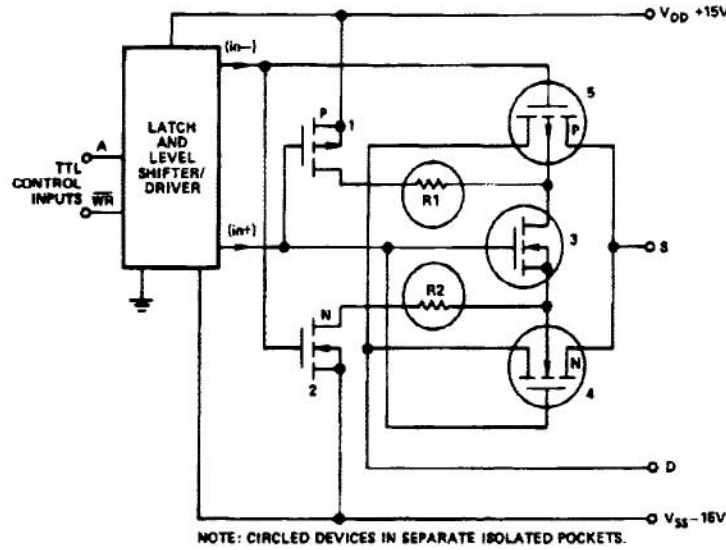


Figure 2. Typical Output Switch Circuitry of AD7590DI Series

## CIRCUIT DESCRIPTION

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as  $R_{ON}$  or leakage, or provided only limited protection in the event of overvoltage.

The AD7590DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 2. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is  $V_{DD}$  and (in-) is  $V_{SS}$  from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 is "ON". Hence, the backgates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. The circled devices are located in separate dielectrically isolated pockets. Floating the output switch backgates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter  $R_{ON}$  versus  $V_S$  response.

For an "OFF" switch, device number 3 is "OFF," and the backgates of devices 4 and 5 are tied through  $1k\Omega$  resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D (OUT) terminal which exceeds  $V_{DD}$  or  $V_{SS}$ , the S- or D-to-backgate diode is forward biased; however, R1 and R2 provide current limiting action to the supplies.

An equivalent circuit of the output switch element in Figure 3 shows that, indeed, the  $1k\Omega$  limiting resistors are in series with the backgates of the P- and N-channel output devices – not in series with the signal path between the S and D terminals.

It is possible to turn on an "OFF" switch by applying a voltage in excess of  $V_{DD}$  or  $V_{SS}$  to the S or D terminal. If a positive stress voltage is applied to the S or D terminal which exceeds  $V_{DD}$  by a threshold, then the P-channel (device 5) will turn on creating a low impedance path between the S and D terminals. A similar situation exists for negative stress voltages which exceed  $V_{SS}$ . In this case the N-channel provides the low impedance path between the S and D terminals. The limiting factor on the overvoltage protection is the power dissipation of the package and is  $\pm 20V$  continuous (or 20mA whichever occurs first) above the supply voltages.

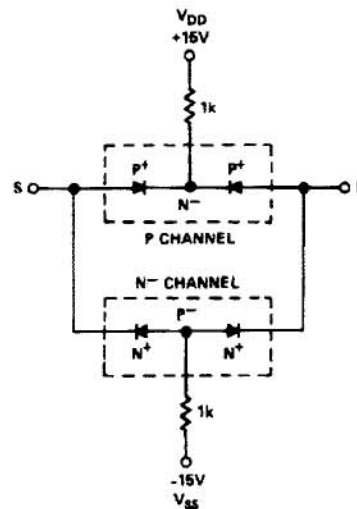
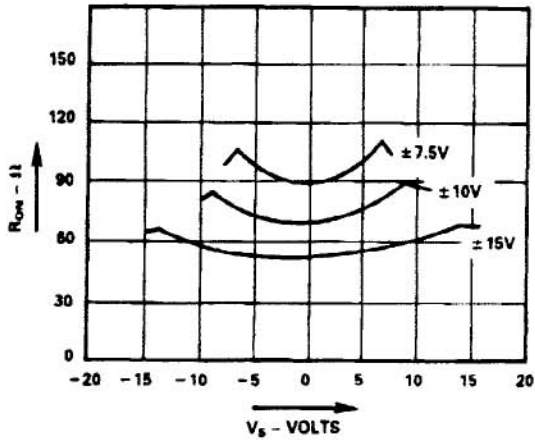
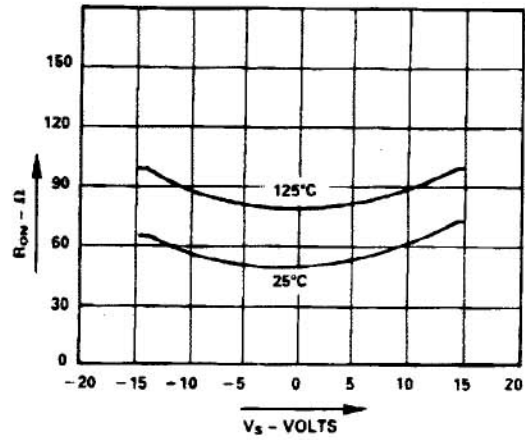


Figure 3. AD7590DI Series Output Switch Diode-Equivalent-Circuit

Typical Performance Characteristics and Test Circuits

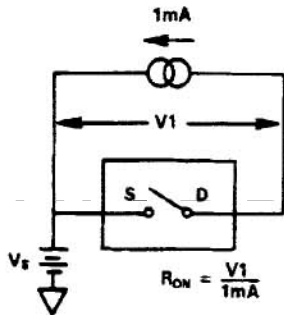


$R_{ON}$  AS A FUNCTION OF  $V_D$  ( $V_S$ ) FOR DIFFERENT SUPPLY VOLTAGES

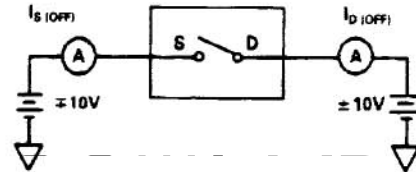


$R_{ON}$  AS A FUNCTION OF  $V_S$  ( $V_D$ ) FOR DIFFERENT TEMPERATURES

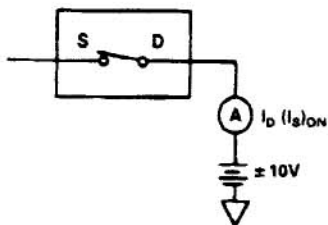
TEST CIRCUIT 1



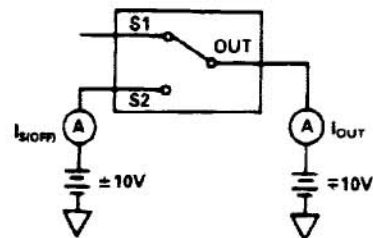
TEST CIRCUIT 2 (AD7590DI, AD7591DI)



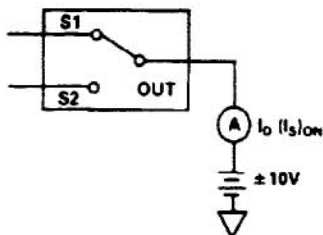
TEST CIRCUIT 3



TEST CIRCUIT 4 (AD7592DI ONLY)



a. AD7590DI, AD7591DI



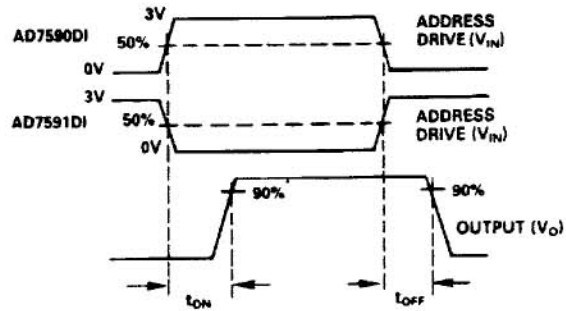
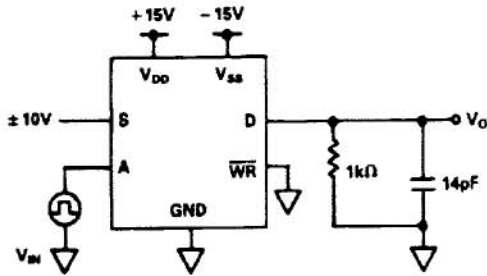
b. AD7592

# AD7590DI/AD7591DI/AD7592DI

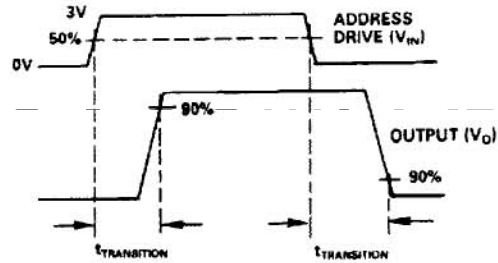
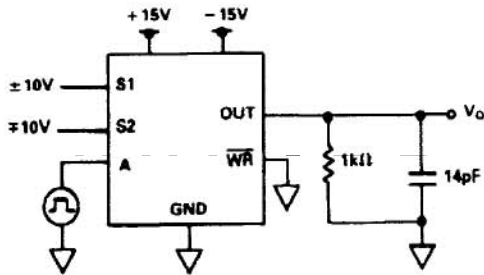
## Typical Switching Characteristics and Test Circuits

Note: All digital input signal rise and fall times measured from 10% to 90% of 3V.  $t_r = t_f = 20\text{ns}$ .

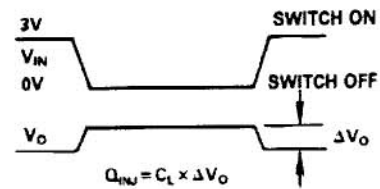
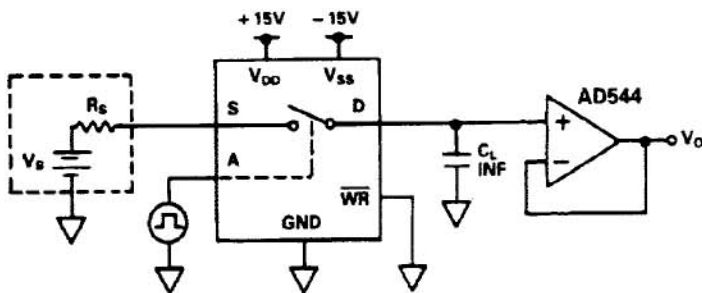
**TEST CIRCUIT 5**  
SWITCHING TIME OF AD7590DI AND AD7591DI,  $t_{ON}$ ,  $t_{OFF}$



**TEST CIRCUIT 6**  
SWITCHING TIME OF AD7592DI,  $t_{TRANSITION}$



**TEST CIRCUIT 7**  
CHARGE INJECTION

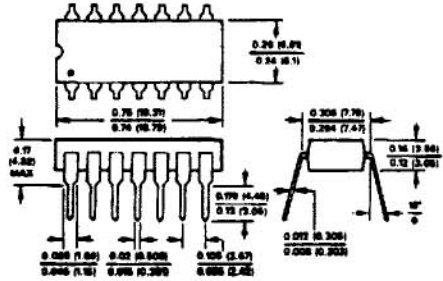


# AD7590DI/AD7591DI/AD7592DI

## MECHANICAL INFORMATION OUTLINE DIMENSIONS

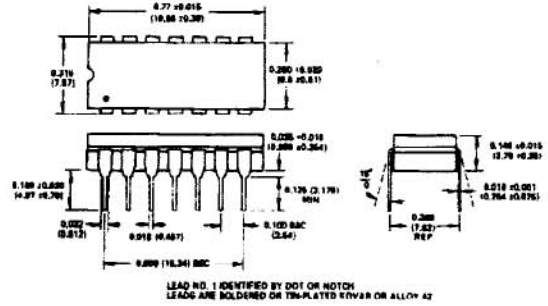
Dimensions shown in inches and (mm).

### 14-PIN PLASTIC DIP (SUFFIX N)



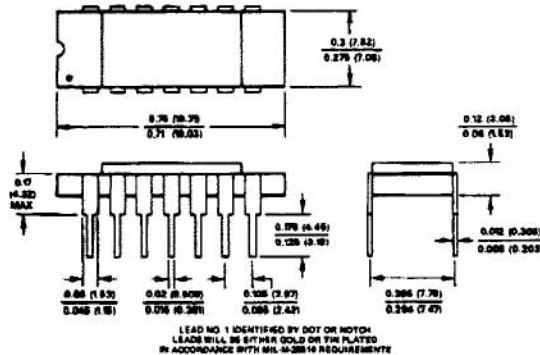
AD7592DI

### 14-PIN CERDIP PACKAGE (SUFFIX Q)



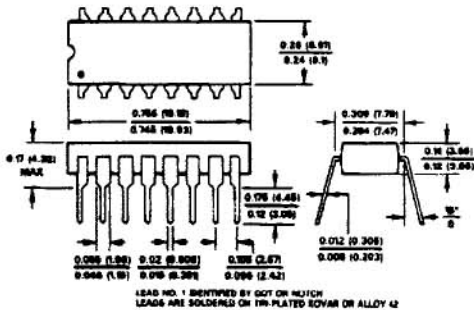
AD7592DI

### 14-PIN CERAMIC DIP\*



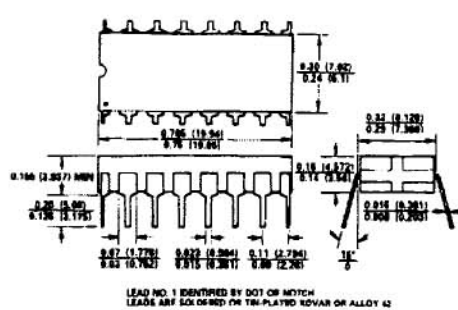
AD7592DI

### 16-PIN PLASTIC DIP (SUFFIX N)



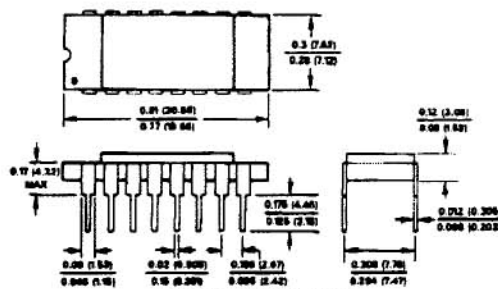
AD7590DI, AD7591DI

### 16-PIN CERDIP PACKAGE (SUFFIX Q)



AD7590DI, AD7591DI

### 16-PIN CERAMIC DIP\*



AD7590DI, AD7591DI

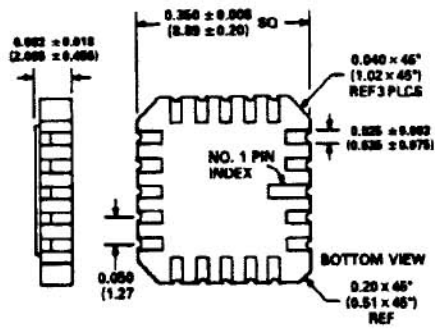
\*ANALOG DEVICES RESERVES THE RIGHT TO SHIP CERAMIC PACKAGES IN LIEU OF CERDIP PACKAGES.

# AD7590DI/AD7591DI/AD7592DI

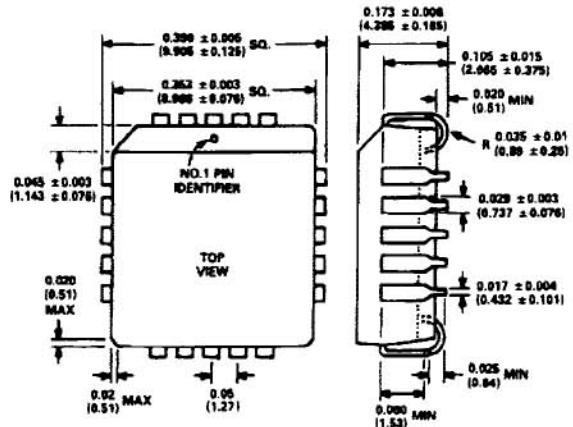
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

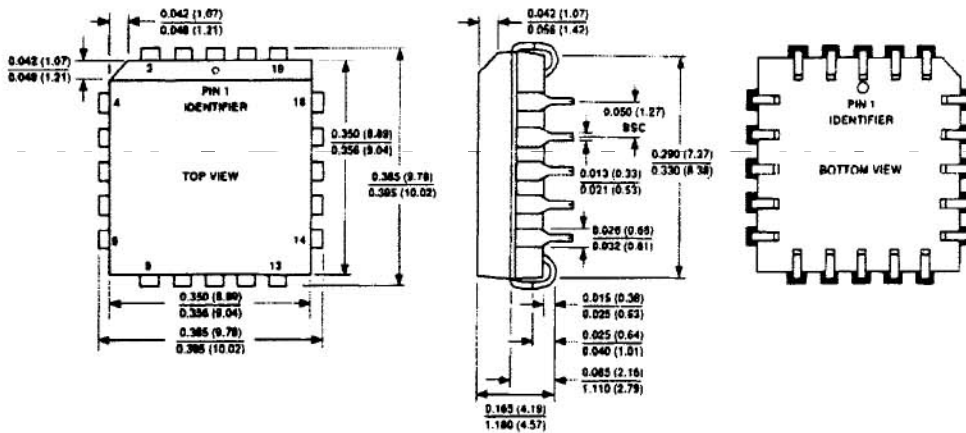
### 20-TERMINAL LEADLESS CERAMIC CHIP CARRIER (SUFFIX E)



### 20-TERMINAL PLASTIC LEADED CHIP CARRIER (SUFFIX P)



### PLCC (P-20A)



C517c-21-11/86

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