

### FEATURES

**33 V supply range**  
**Fully specified at +12 V, ±15 V**  
**130 Ω on resistance**  
**No  $V_L$  supply required**  
**3 V logic-compatible inputs**  
**Rail-to-rail operation**  
**16-lead TSSOP and 16-lead SOIC**  
**Typical power consumption: <0.03 μW**

### APPLICATIONS

**Signal switching**  
**Battery-powered systems**  
**Communication systems**  
**Audio/video signal routing**

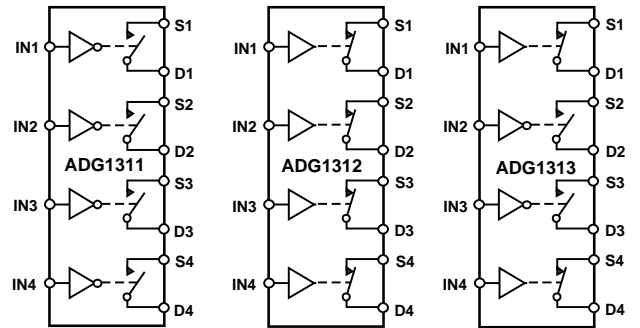
### GENERAL DESCRIPTION

The ADG1311/ADG1312/ADG1313 are monolithic CMOS devices containing four independently selectable switches designed on a CMOS process.

The ADG1311/ADG1312/ADG1313 contain four independent single-pole/single-throw (SPST) switches. The ADG1311 and ADG1312 differ only in that the digital control logic is inverted. The ADG1311 switches are turned on with Logic 0 on the appropriate control input, while Logic 1 is required for the ADG1312. The ADG1313 has two switches with digital control logic similar to the ADG1311; the logic is inverted on the other two switches. The ADG1313 exhibits break-before-make switching action for use in multiplexer applications.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

### FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 1 INPUT

Figure 1.

05676-001

### PRODUCT HIGHLIGHTS

- 3 V logic-compatible digital inputs:  $V_{IH} = 2.0$  V,  $V_{IL} = 0.8$  V.
- No  $V_L$  logic power supply required.
- 16-lead TSSOP and SOIC packages.

#### Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

**TABLE OF CONTENTS**

Features .....	1	Absolute Maximum Ratings .....	5
Applications.....	1	ESD Caution.....	5
Functional Block Diagram .....	1	Pin Configuration and Function Descriptions.....	6
General Description .....	1	Terminology .....	7
Product Highlights .....	1	Typical Performance Characteristics .....	8
Specifications.....	3	Test Circuits.....	10
Dual Supply .....	3	Outline Dimensions .....	12
Single Supply .....	4	Ordering Guide .....	12

**REVISION HISTORY**

10/05—Revision 0: Initial Version

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 1.**

Parameter	Y Version <sup>1</sup>		Unit	Test Conditions/Comments
	25°C	-40°C to +105°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		$V_{DD}$ to $V_{SS}$	V	
On Resistance ( $R_{ON}$ )	130	230	$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$ ; Figure 10
	200		$\Omega$ max	$V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	5		$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$
	10		$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	25		$\Omega$ typ	$V_S = -5\text{ V}/0\text{ V}/+5\text{ V}$ ; $I_S = -1\text{ mA}$
	65		$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage, $I_S$ (Off)	$\pm 10$		nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ ; Figure 11
Drain Off Leakage, $I_D$ (Off)	$\pm 10$		nA typ	$V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ ; Figure 11
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 10$		nA typ	$V_S = V_D = \pm 10\text{ V}$ ; Figure 12
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.0	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	2.5		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	105		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	125	180	ns max	$V_S = +10\text{ V}$ ; Figure 13
$t_{OFF}$	40		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	50	60	ns max	$V_S = +10\text{ V}$ ; Figure 13
Break-Before-Make Time Delay, $t_D$ (ADG1313 Only)	25		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		10	ns min	$V_{S1} = V_{S2} = 10\text{ V}$ ; Figure 14
Charge Injection	2		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Figure 15
Off Isolation	80		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Figure 16
Channel-to-Channel Crosstalk	90		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Figure 17
-3 dB Bandwidth	600		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Figure 18
$C_S$ (Off)	5		pF typ	
$C_D$ (Off)	5		pF typ	
$C_D$ , $C_S$ (On)	10		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ Digital inputs = 0 V or $V_{DD}$
		1.0	$\mu\text{A}$ max	
$I_{DD}$	220		$\mu\text{A}$ typ	Digital inputs = 5 V
		320	$\mu\text{A}$ max	
$I_{SS}$	0.001		$\mu\text{A}$ typ	Digital inputs = 0 V or $V_{DD}$
		1.0	$\mu\text{A}$ max	
$I_{SS}$	0.001		$\mu\text{A}$ typ	Digital inputs = 5 V
		1.0	$\mu\text{A}$ max	

<sup>1</sup> Temperature range for Y Version is -40°C to +105°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

# ADG1311/ADG1312/ADG1313

## SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 2.

Parameter	Y Version <sup>1</sup>		Unit	Test Conditions/Comments
	25°C	–40°C to +105°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	325	520	$\Omega$ typ	$V_S = 0\text{ V} - 10\text{ V}$ , $I_S = -1\text{ mA}$ ; Figure 10
	500		$\Omega$ max	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	10		$\Omega$ typ	$V_S = 0\text{ V} - 10\text{ V}$ , $I_S = -1\text{ mA}$
	15		$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	65		$\Omega$ typ	$V_S = +3\text{ V}/+6\text{ V}/+9\text{ V}$ , $I_S = -1\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage, $I_S$ (Off)	$\pm 10$		nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$
Drain Off Leakage, $I_D$ (Off)	$\pm 10$		nA typ	$V_S = +1\text{ V}/+10\text{ V}$ , $V_D = +10\text{ V}/+1\text{ V}$ ; Figure 11
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 10$		nA typ	$V_S = +1\text{ V}/+10\text{ V}$ , $V_D = +10\text{ V}/+1\text{ V}$ Figure 11
				$V_S = V_D = +1\text{ V}$ or $+10\text{ V}$ ; Figure 12
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.0	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	3		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	120		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	155	210	ns max	$V_S = 8\text{ V}$ ; Figure 13
$t_{OFF}$	45		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	65	80	ns max	$V_S = 8\text{ V}$ ; Figure 13
Break-Before-Make Time Delay, $t_D$ (ADG1313 Only)	50	10	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			ns min	$V_{S1} = V_{S2} = 8\text{ V}$ ; Figure 14
Charge Injection	2		pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Figure 15
Off Isolation	80		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Figure 16
Channel-to-Channel Crosstalk	90		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Figure 17
–3 dB Bandwidth	500		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Figure 18
$C_S$ (Off)	5		pF typ	
$C_D$ (Off)	5		pF typ	
$C_D$ , $C_S$ (On)	10		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$
		1.0	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	220		$\mu\text{A}$ typ	Digital inputs = 5 V
		320	$\mu\text{A}$ max	

<sup>1</sup> Temperature range for Y Version is –40°C to +105°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

**Table 3.**

Parameter	Rating
V <sub>DD</sub> to V <sub>SS</sub>	35 V
V <sub>DD</sub> to GND	−0.3 V to +25 V
V <sub>SS</sub> to GND	+0.3 V to −25 V
Analog Inputs <sup>1</sup>	V <sub>SS</sub> − 0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND − 0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current per Channel, S or D	25 mA
Operating Temperature Range Automotive	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ <sub>JA</sub> Thermal Impedance (4-layer board)	112°C/W
16-Lead SOIC, θ <sub>JA</sub> Thermal Impedance	77°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. ADG1311/ADG1312 Truth Table**

ADG1311 INx	ADG1312 INx	Switch Condition
0	1	On
1	0	Off

**Table 5. ADG1313 Truth Table**

ADG1313 INx	Switch 1, 4	Switch 2, 3
0	Off	On
1	On	Off

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# ADG1311/ADG1312/ADG1313

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

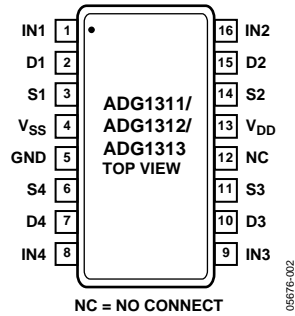


Figure 2. SOIC/TSSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Logic Control Input.
2	D1	Drain Terminal. Can be an input or output.
3	S1	Source Terminal. Can be an input or output.
4	V <sub>SS</sub>	Most Negative Power Supply Potential.
5	GND	Ground (0 V) Reference.
6	S4	Source Terminal. Can be an input or output.
7	D4	Drain Terminal. Can be an input or output.
8	IN4	Logic Control Input.
9	IN3	Logic Control Input.
10	D3	Drain Terminal. Can be an input or output.
11	S3	Source Terminal. Can be an input or output.
12	NC	No Connection.
13	V <sub>DD</sub>	Most Positive Power Supply Potential.
14	S2	Source Terminal. Can be an input or output.
15	D2	Drain Terminal. Can be an input or output.
16	IN2	Logic Control Input.

## TERMINOLOGY

### $I_{DD}$

The positive supply current.

### $I_{SS}$

The negative supply current.

### $V_D$ ( $V_S$ )

The analog voltage on Terminal D and Terminal S.

### $R_{ON}$

The ohmic resistance between D and S.

### $R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

### $I_S$ (Off)

The source leakage current with the switch off.

### $I_D$ (Off)

The drain leakage current with the switch off.

### $I_D, I_S$ (On)

The channel leakage current with the switch on.

### $V_{INL}$

The maximum input voltage for Logic 0.

### $V_{INH}$

The minimum input voltage for Logic 1.

### $I_{INL}$ ( $I_{INH}$ )

The input current of the digital input.

### $C_S$ (Off)

The off switch source capacitance, measured with reference to ground.

### $C_D$ (Off)

The off switch drain capacitance, measured with reference to ground.

### $C_D, C_S$ (On)

The on switch capacitance, measured with reference to ground.

### $C_{IN}$

The digital input capacitance.

### $t_{ON}$

The delay between applying the digital control input and the output switching on. See Figure 13.

### $t_{OFF}$

The delay between applying the digital control input and the output switching off. See Figure 13.

### Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

### Off Isolation

A measure of unwanted signal coupling through an off switch.

### Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### Bandwidth

The frequency at which the output is attenuated by 3 dB.

### On Response

The frequency response of the on switch.

### Insertion Loss

The loss due to the on resistance of the switch.

TYPICAL PERFORMANCE CHARACTERISTICS

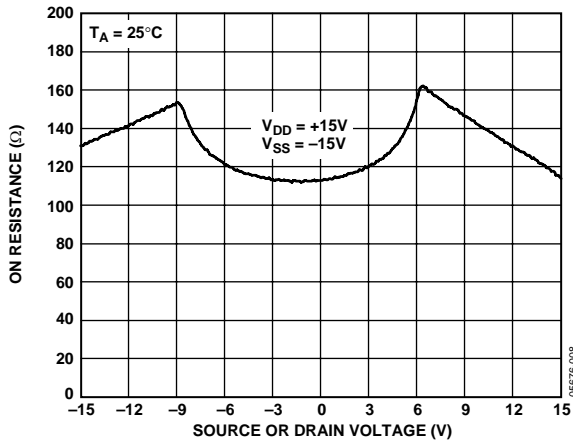


Figure 3. On Resistance as a Function of  $V_D$  ( $V_s$ ) for Dual Supply

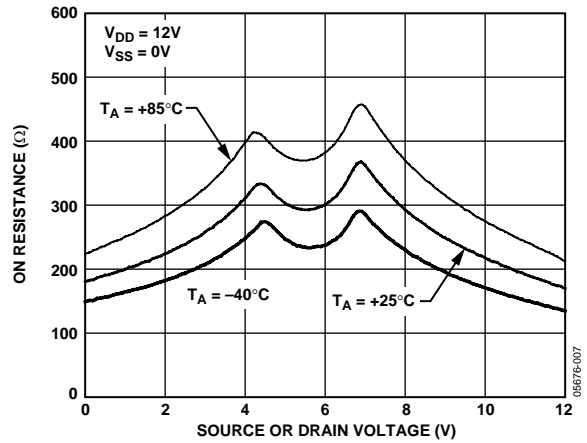


Figure 6. On Resistance as a Function of  $V_D$  ( $V_s$ ) for Different Temperatures, Single Supply

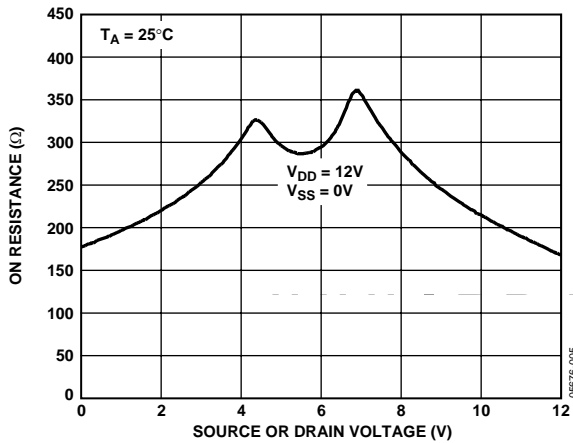


Figure 4. On Resistance as a Function of  $V_D$  ( $V_s$ ) for Single Supply

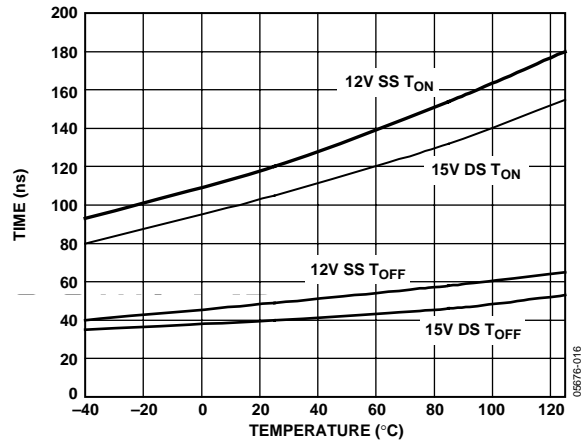


Figure 7.  $T_{ON}/T_{OFF}$  Times vs. Temperature

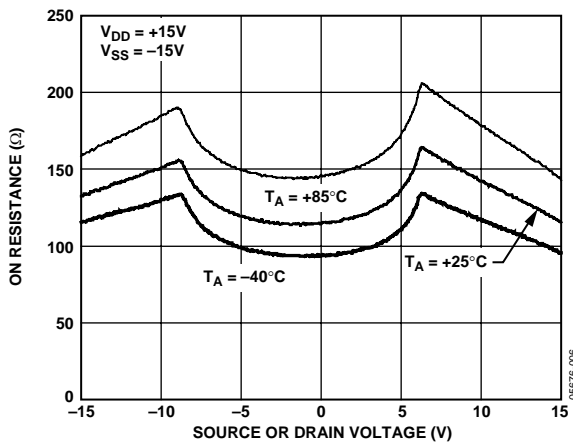


Figure 5. On Resistance as a Function of  $V_D$  ( $V_s$ ) for Different Temperatures, Dual Supply

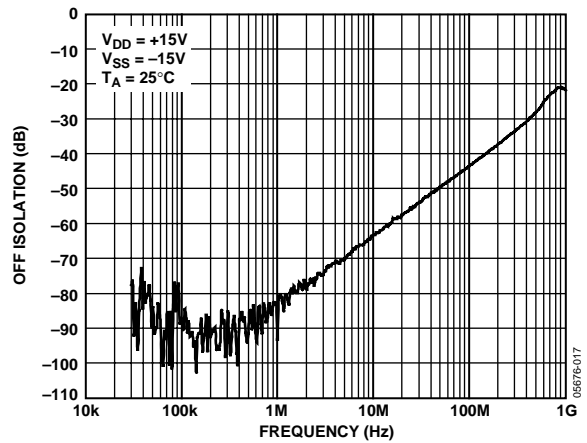


Figure 8. Off Isolation vs. Frequency



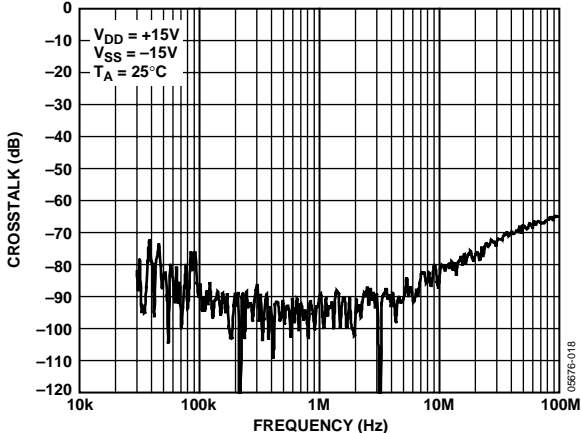


Figure 9. Crosstalk vs. Frequency

## TEST CIRCUITS

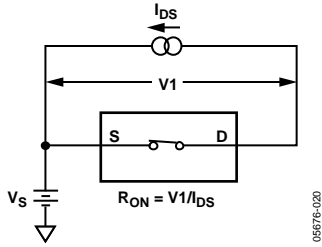


Figure 10. Test Circuit 1—On Resistance

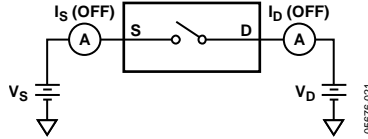


Figure 11. Test Circuit 2—Off Leakage

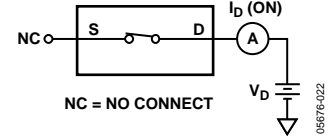


Figure 12. Test Circuit 3—On Leakage

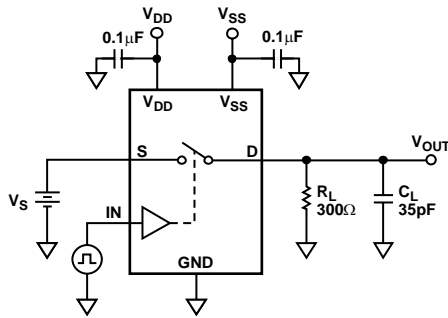


Figure 13. Test Circuit 4—Switching Times

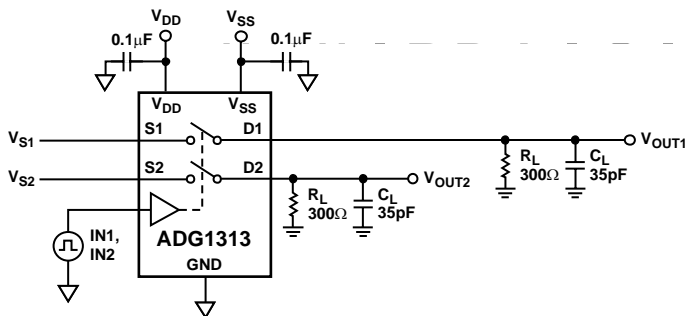
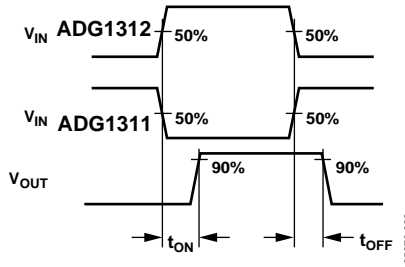


Figure 14. Test Circuit 5—Break-Before-Make Time Delay

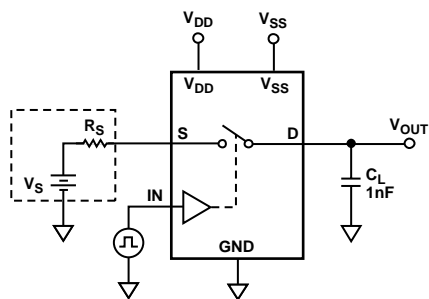
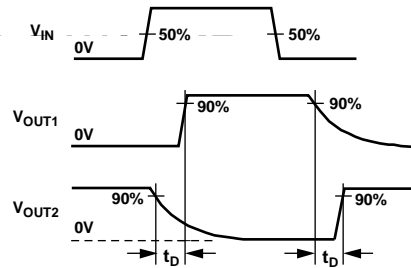
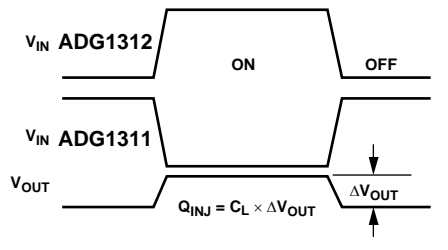


Figure 15. Test Circuit 6—Charge Injection



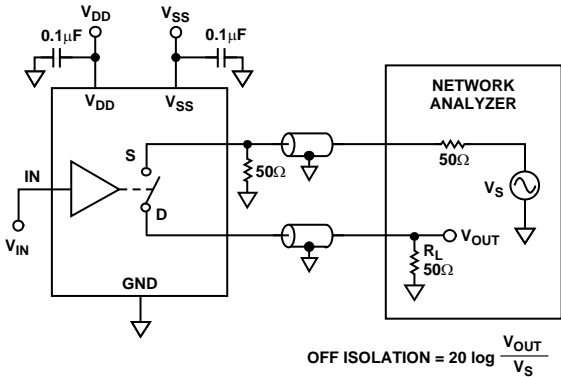


Figure 16. Test Circuit 7—Off Isolation

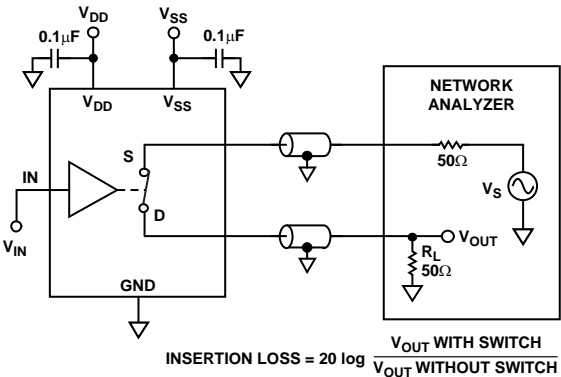


Figure 18. Test Circuit 9—Bandwidth

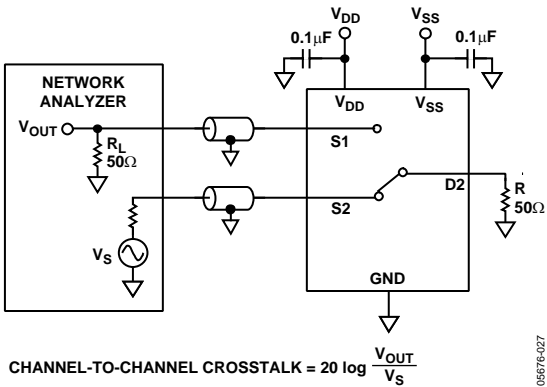
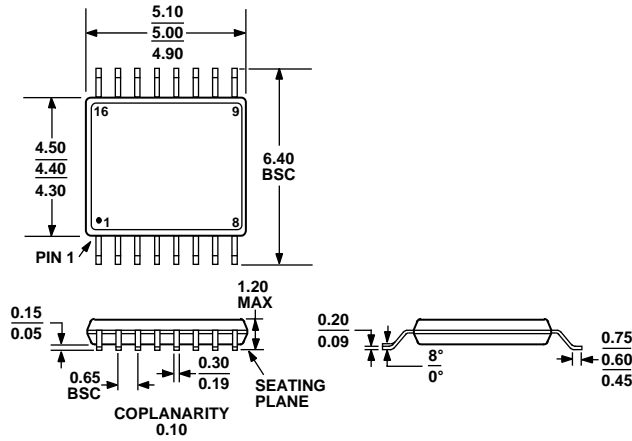


Figure 17. Test Circuit 8—Channel-to-Channel Crosstalk

# ADG1311/ADG1312/ADG1313

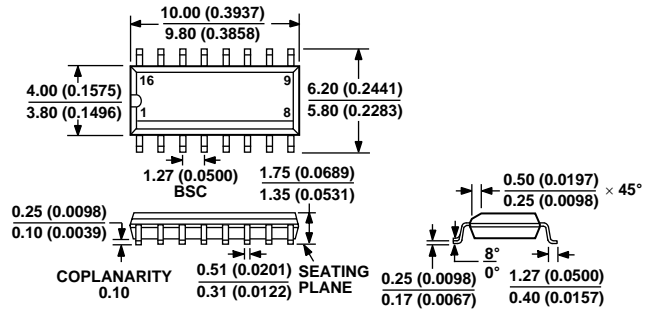
## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 19. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 20. 16-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-16)

Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1311YRUZ <sup>1</sup>	-40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1311YRUZ-REEL7 <sup>1</sup>	-40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1311YRZ <sup>1</sup>	-40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1311YRZ-REEL7 <sup>1</sup>	-40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1312YRUZ <sup>1</sup>	-40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1312YRUZ-REEL7 <sup>1</sup>	-40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1312YRZ <sup>1</sup>	-40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1312YRZ-REEL7 <sup>1</sup>	-40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1313YRUZ <sup>1</sup>	-40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1313YRUZ-REEL7 <sup>1</sup>	-40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1313YRZ <sup>1</sup>	-40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG1313YRZ-REEL7 <sup>1</sup>	-40°C to +105°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16

<sup>1</sup> Z = Pb-free part.