

### FEATURES

- 1  $\Omega$  on resistance
- 0.2  $\Omega$  on resistance flatness
- Up to 430 mA continuous current
- Fully specified at +12 V,  $\pm 15$  V,  $\pm 5$  V
- No  $V_L$  supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 8-lead MSOP and 8-lead, 3 mm  $\times$  2 mm LFCSP packages

### APPLICATIONS

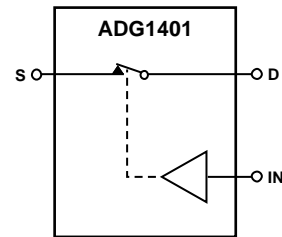
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communication systems
- Relay replacements

### GENERAL DESCRIPTION

The ADG1401/ADG1402 contain a single-pole/single-throw (SPST) switch. Figure 1 shows that with a logic input of 1, the switch of the ADG1401 is closed and that of the ADG1402 is open. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

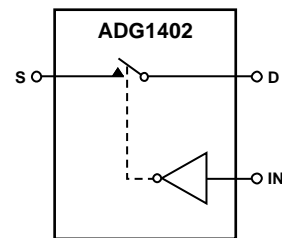
The *i*CMOS<sup>®</sup> (industrial CMOS) modular manufacturing process combines high voltage, complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has achieved. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and a reduced package size.

### FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 1 INPUT

Figure 1. ADG1401 Functional Block Diagram



SWITCHES SHOWN FOR A LOGIC 1 INPUT

Figure 2. ADG1402 Functional Block Diagram

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. The *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

### PRODUCT HIGHLIGHTS

1. 1.3  $\Omega$  maximum on resistance at 25°C.
2. Minimum distortion.
3. 3 V logic-compatible digital inputs:  $V_{INH} = 2.0$  V,  $V_{INL} = 0.8$  V.
4. No  $V_L$  logic power supply required.
5. 8-lead MSOP and 8-lead, 3 mm  $\times$  2 mm LFCSP packages.

#### Rev. 0

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## REVISION HISTORY

10/09—Revision 0: Initial Version

# SPECIFICATIONS

## ±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	1			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 20
	1.3	1.6	1.8	$\Omega$ max	$V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
On Resistance Flatness, $R_{FLAT(ON)}$	0.2			$\Omega$ typ	$V_S = \pm 10\text{ V}$ ; $I_S = -10\text{ mA}$
	0.23	0.26	0.3	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.05$			nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
	$\pm 0.4$	$\pm 3$	$\pm 150$	nA max	$V_S = \pm 10\text{ V}$ , $V_D = \pm 10\text{ V}$ ; see Figure 21
Drain Off Leakage, $I_D$ (Off)	$\pm 0.05$			nA typ	$V_S = \pm 10\text{ V}$ , $V_D = \pm 10\text{ V}$ ; see Figure 21
	$\pm 0.4$	$\pm 3$	$\pm 150$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.2$			nA typ	$V_S = V_D = \pm 10\text{ V}$ ; see Figure 22
	$\pm 1$	$\pm 3$	$\pm 150$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	4			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	120			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	150	185	215	ns max	$V_S = 10\text{ V}$ ; see Figure 23
$t_{OFF}$	120			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	150	175	200	ns max	$V_S = 10\text{ V}$ ; see Figure 23
Charge Injection	-12			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 24
Off Isolation	-58			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 25
Total Harmonic Distortion + Noise	0.008			% typ	$R_L = 10\text{ k}\Omega$ , $5\text{ V rms}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ ; see Figure 27
-3 dB Bandwidth	120			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
Insertion Loss	0.08			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
$C_S$ (Off)	36			pF typ	$f = 1\text{ MHz}$ , $V_S = 0\text{ V}$
$C_D$ (Off)	41			pF typ	$f = 1\text{ MHz}$ , $V_S = 0\text{ V}$
$C_D$ , $C_S$ (On)	187			pF typ	$f = 1\text{ MHz}$ , $V_S = 0\text{ V}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.002			$\mu\text{A}$ typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
			1.0	$\mu\text{A}$ max	Digital inputs = $0\text{ V}$ or $V_{DD}$
$I_{DD}$	60			$\mu\text{A}$ typ	Digital inputs = $5\text{ V}$
			95	$\mu\text{A}$ max	
$I_{SS}$	0.002			$\mu\text{A}$ typ	Digital inputs = $0\text{ V}$ , $5\text{ V}$ , or $V_{DD}$
			1.0	$\mu\text{A}$ max	
$V_{DD}/V_{SS}$			$\pm 4.5/\pm 16.5$	V min/max	Ground = $0\text{ V}$

<sup>1</sup> Guaranteed by design, not subject to production test.

# ADG1401/ADG1402

## +12 V SINGLE SUPPLY

$V_{DD} = +12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	2			$\Omega$ typ	$V_S = 0\text{ V}$ to 10 V, $I_S = -10\text{ mA}$ ; see Figure 20
	2.4	2.9	3.2	$\Omega$ max	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance Flatness, $R_{FLAT(ON)}$	0.6			$\Omega$ typ	$V_S = 0\text{ V}$ to 10 V, $I_S = -10\text{ mA}$
	0.68	0.8	0.85	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.05$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.4$	$\pm 3$	$\pm 150$	nA max	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 21
Drain Off Leakage, $I_D$ (Off)	$\pm 0.05$			nA typ	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 21
	$\pm 0.4$	$\pm 3$	$\pm 150$	nA max	
Channel On Leakage, $I_D, I_S$ (On)	$\pm 0.2$			nA typ	$V_S = V_D = 1\text{ V}$ or 10 V; see Figure 22
	$\pm 1$	$\pm 3$	$\pm 150$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	4			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	180			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	235	295	335	ns max	$V_S = 8\text{ V}$ ; see Figure 23
$t_{OFF}$	140			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	185	215	260	ns max	$V_S = 8\text{ V}$ ; see Figure 23
Charge Injection	57			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 24
Off Isolation	-58			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 25
-3 dB Bandwidth	82			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
Insertion Loss	0.15			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
$C_S$ (Off)	61			pF typ	$f = 1\text{ MHz}$ , $V_S = 6\text{ V}$
$C_D$ (Off)	68			pF typ	$f = 1\text{ MHz}$ , $V_S = 6\text{ V}$
$C_D, C_S$ (On)	181			pF typ	$f = 1\text{ MHz}$ , $V_S = 6\text{ V}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$
			1.0	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	60			$\mu\text{A}$ typ	Digital inputs = 5 V
			95	$\mu\text{A}$ max	
$V_{DD}$			5/16.5	V min/max	Ground = 0 V, $V_{SS} = 0\text{ V}$

<sup>1</sup> Guaranteed by design, not subject to production test.

**±5 V DUAL SUPPLY**

$V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 3.**

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	2.3			$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$ ; see Figure 20
	2.7	3.3	3.7	$\Omega$ max	$V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$
On Resistance Flatness, $R_{FLAT(ON)}$	0.65			$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.72	0.85	0.9	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$			nA typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$
	$\pm 0.4$	$\pm 3$	$\pm 150$	nA max	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ ; see Figure 21
Drain Off Leakage, $I_D$ (Off)	$\pm 0.02$			nA typ	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ ; see Figure 21
	$\pm 0.4$	$\pm 3$	$\pm 150$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.1$			nA typ	$V_S = V_D = \pm 4.5\text{ V}$ ; see Figure 22
	$\pm 1$	$\pm 3$	$\pm 150$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	4			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	290			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	375	460	520	ns max	$V_S = 3\text{ V}$ ; see Figure 23
$t_{OFF}$	235			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	305	365	405	ns max	$V_S = 3\text{ V}$ ; see Figure 23
Charge Injection	145			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 24
Off Isolation	-58			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 25
Total Harmonic Distortion + Noise	0.02			% typ	$R_L = 10\text{ k}\Omega$ , 5 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 27
-3 dB Bandwidth	79			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 26
Insertion Loss	0.14			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
$C_S$ (Off)	52			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	58			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	198			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$
			1.0	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{SS}$	0.001			$\mu\text{A}$ typ	Digital inputs = 0 V or $V_{DD}$
			1.0	$\mu\text{A}$ max	
$V_{DD}/V_{SS}$			$\pm 4.5/\pm 16.5$	V min/max	Ground = 0 V

<sup>1</sup> Guaranteed by design, not subject to production test.

# ADG1401/ADG1402

## CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, S or D <sup>1</sup>					
±15 V Dual Supply					$V_{DD} = +13.5\text{ V}, V_{SS} = -13.5\text{ V}$
8-Lead MSOP ( $\theta_{JA} = 206^\circ\text{C/W}$ )	275	190	125	mA maximum	
8-Lead LFCSP ( $\theta_{JA} = 50.8^\circ\text{C/W}$ )	430	275	160	mA maximum	
+12 V Single Supply					$V_{DD} = 10.8\text{ V}, V_{SS} = 0\text{ V}$
8-Lead MSOP ( $\theta_{JA} = 206^\circ\text{C/W}$ )	255	180	120	mA maximum	
8-Lead LFCSP ( $\theta_{JA} = 50.8^\circ\text{C/W}$ )	355	235	145	mA maximum	
±5 V Dual Supply					$V_{DD} = +4.5\text{ V}, V_{SS} = -4.5\text{ V}$
8-Lead MSOP ( $\theta_{JA} = 206^\circ\text{C/W}$ )	250	175	120	mA maximum	
8-Lead LFCSP ( $\theta_{JA} = 50.8^\circ\text{C/W}$ )	340	225	140	mA maximum	

<sup>1</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 5.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	35 V
$V_{DD}$ to GND	-0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to -25 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)	
8-Lead MSOP (4-Layer Board)	500 mA
8-Lead LFCSP	700 mA
Continuous Current per Channel, S or D	Data in Table 4 + 15%
Operating Temperature Range	
Industrial	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	260°C

<sup>1</sup> Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

Table 6. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead MSOP (4-Layer Board)	206	44	°C/W
8-Lead LFCSP	50.8		°C/W

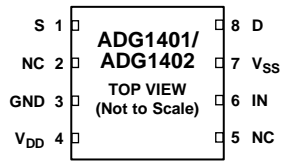
## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG1401/ADG1402

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**  
 1. EXPOSED PAD TIED TO SUBSTRATE,  $V_{SS}$ .  
 2. NC = NO CONNECT.

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Figure 3. ADG1401/ADG1402 Pin Configuration

Table 7. ADG1401/ADG1402 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S	Source Terminal. This pin can be an input or output.
2	NC	No Connect.
3	GND	Ground (0 V) Reference.
4	$V_{DD}$	Most Positive Power Supply Potential.
5	NC	No Connect.
6	IN	Logic Control Input.
7	$V_{SS}$	Most Negative Power Supply Potential.
8	D	Drain Terminal. This pin can be an input or output.
	EPAD	Exposed pad tied to substrate, $V_{SS}$ , for LFCSP package.

Table 8. ADG1401/ADG1402 Truth Table

ADG1401 IN	ADG1402 IN	Switch Condition
1	0	On
0	1	Off



# TYPICAL PERFORMANCE CHARACTERISTICS

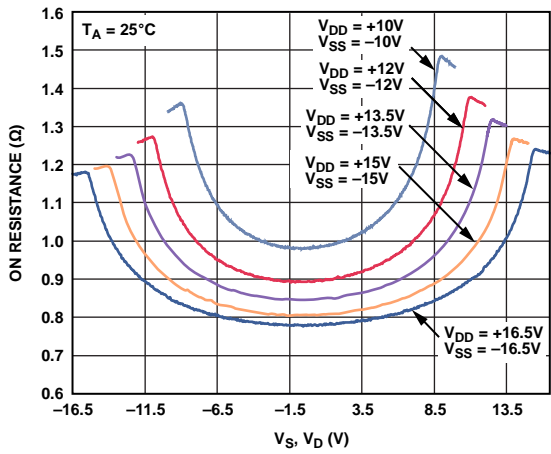


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

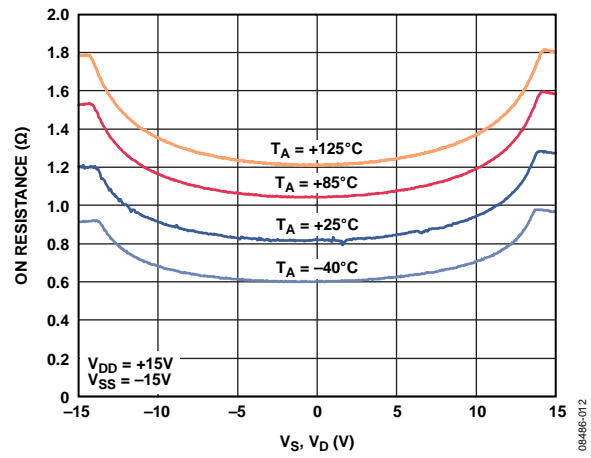


Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures,  $\pm 15$  V Dual Supply

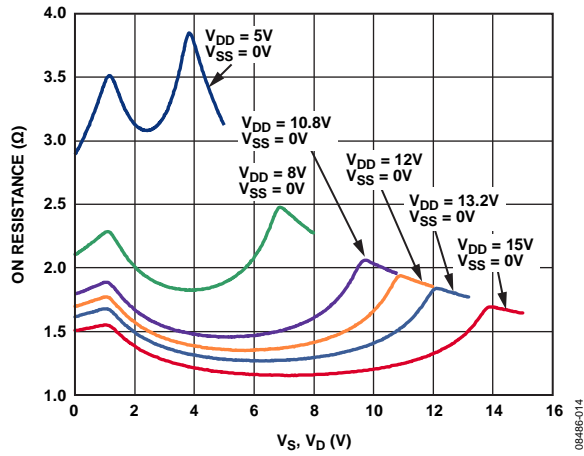


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

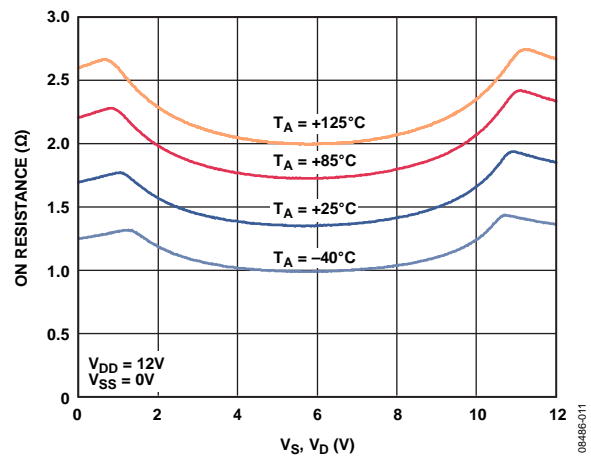


Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, +12 V Single Supply

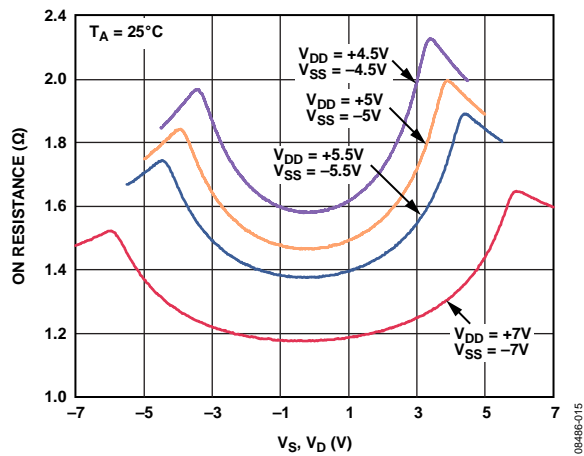


Figure 6. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

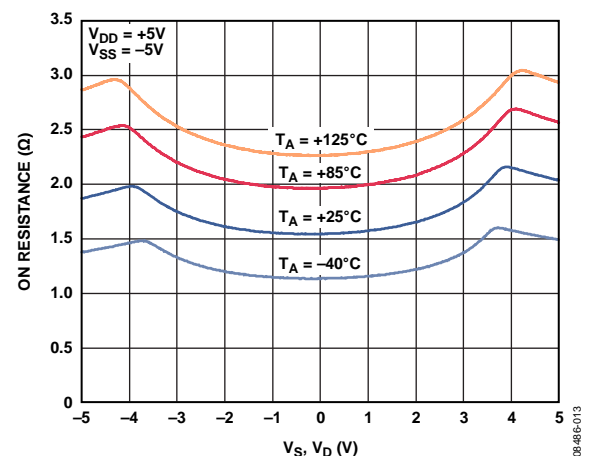


Figure 9. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures,  $\pm 5$  V Dual Supply

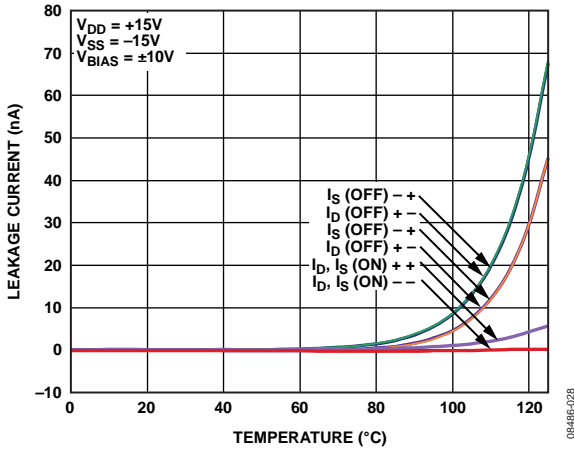


Figure 10. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

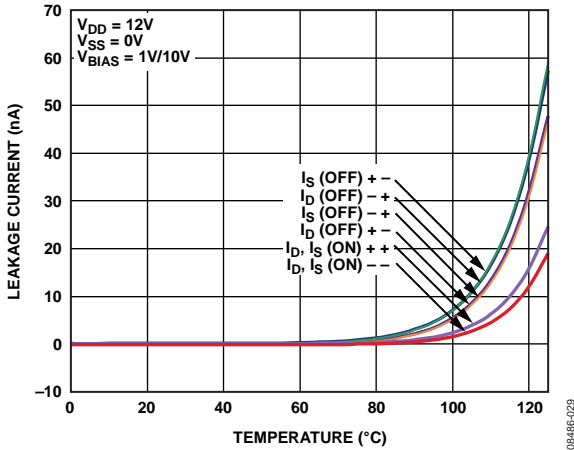


Figure 11. Leakage Currents as a Function of Temperature, +12 V Single Supply

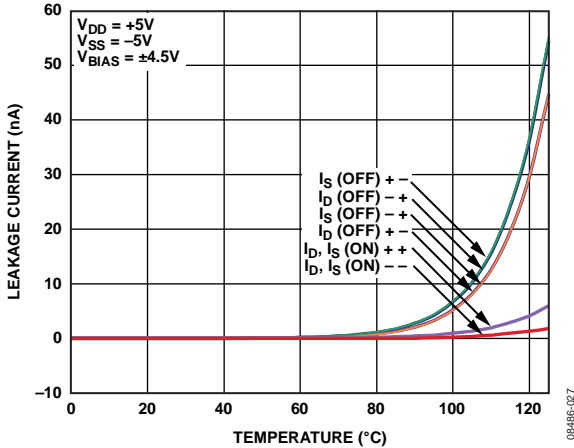


Figure 12. Leakage Currents as a Function of Temperature, ±5 V Dual Supply

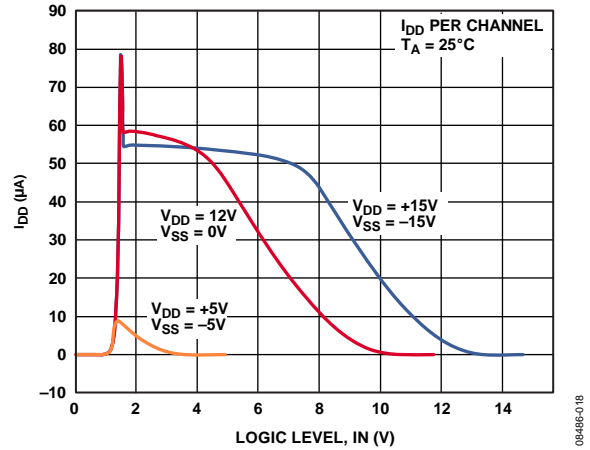


Figure 13.  $I_{DD}$  vs. Logic Level

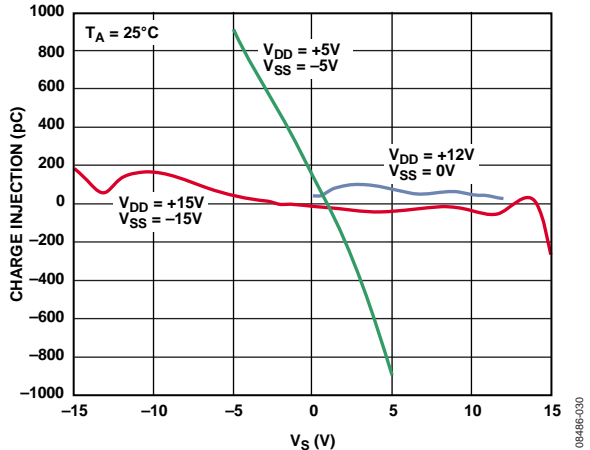


Figure 14. Charge Injection vs. Source Voltage

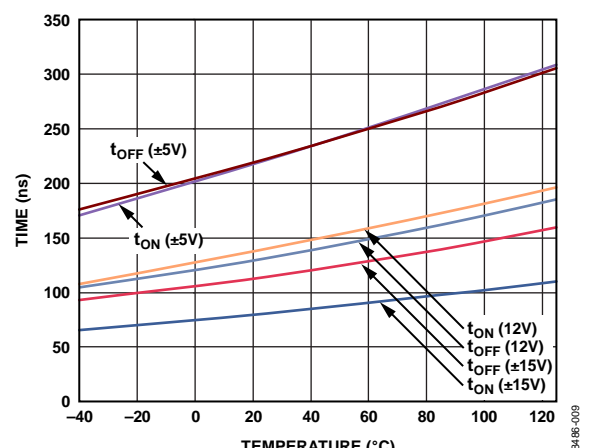


Figure 15.  $t_{ON}/t_{OFF}$  Times vs. Temperature

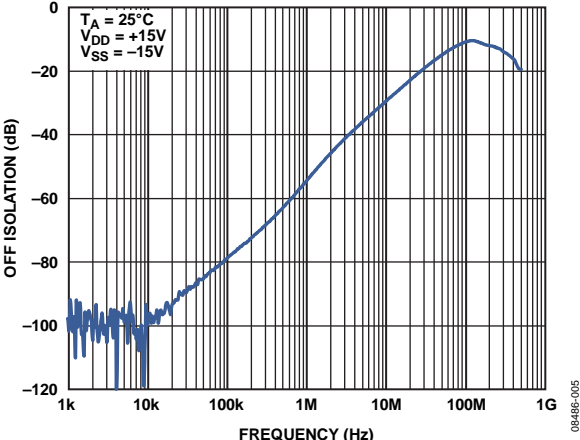


Figure 16. Off Isolation vs. Frequency

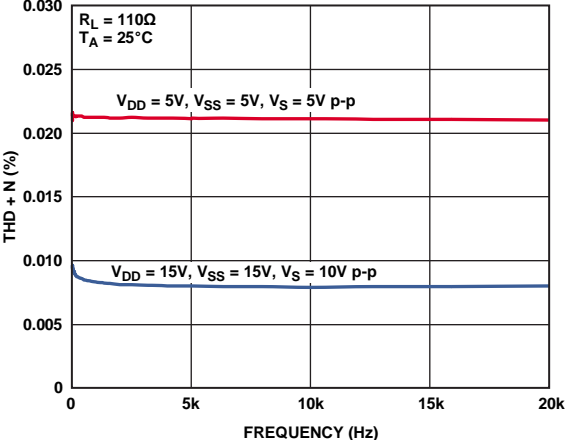


Figure 18. THD + N vs. Frequency

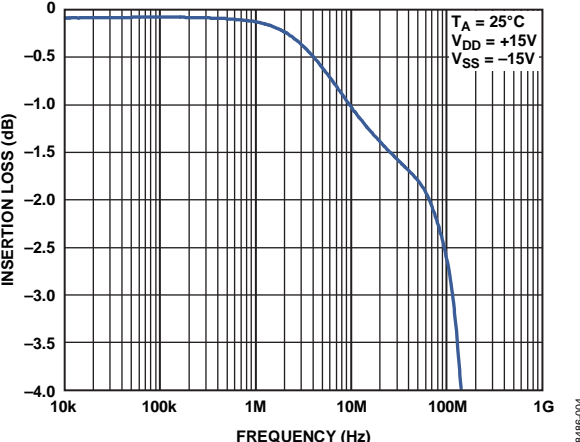


Figure 17. On Response vs. Frequency

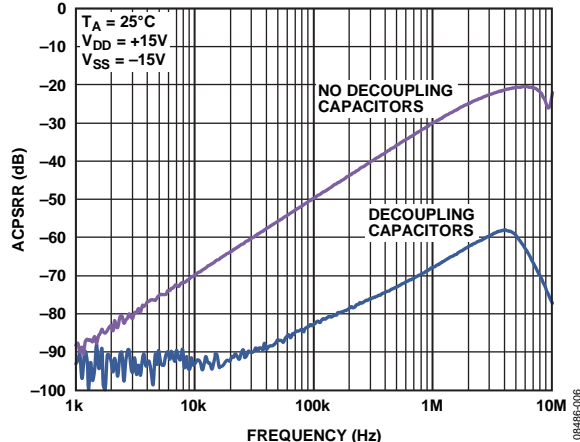


Figure 19. ACPSRR vs. Frequency

## TEST CIRCUITS

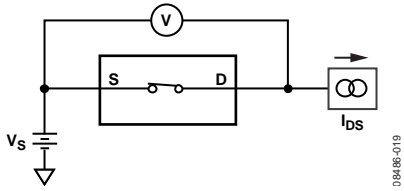


Figure 20. On Resistance

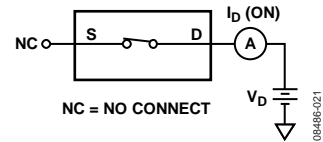


Figure 22. On Leakage

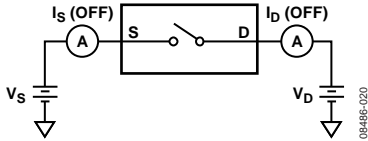


Figure 21. Off Leakage

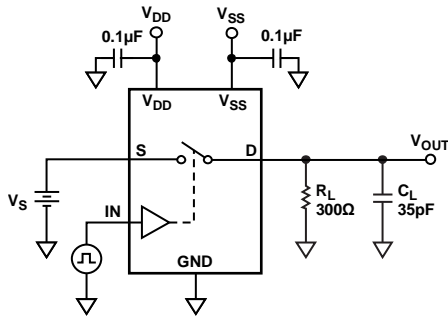


Figure 23. Switching Times,  $t_{ON}$  and  $t_{OFF}$

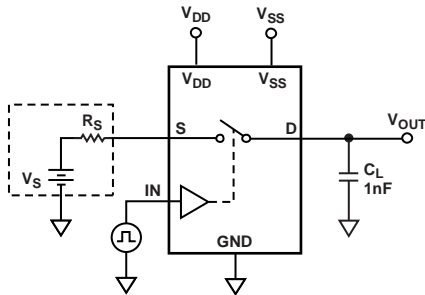
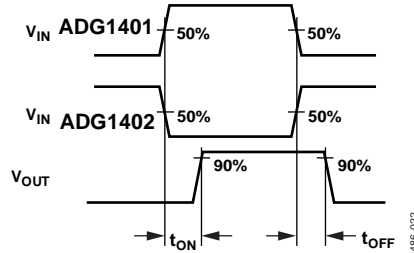
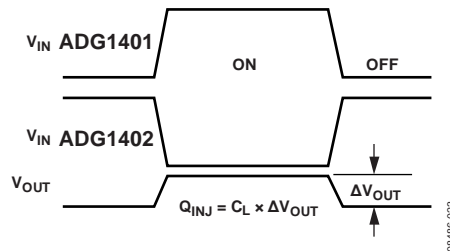


Figure 24. Charge Injection



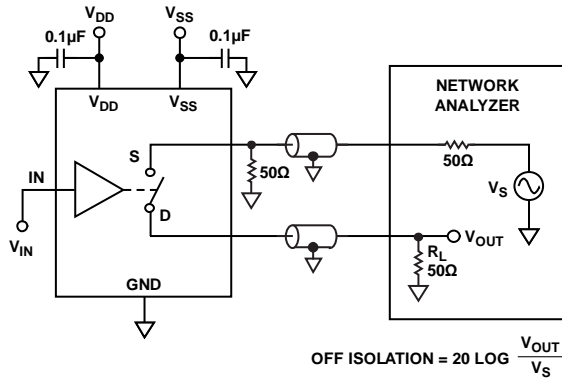


Figure 25. Off Isolation

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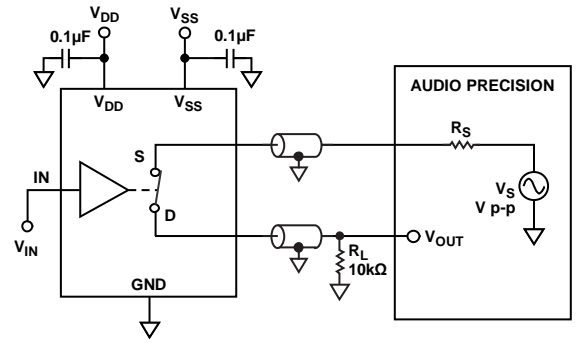


Figure 27. THD + N

08486-026

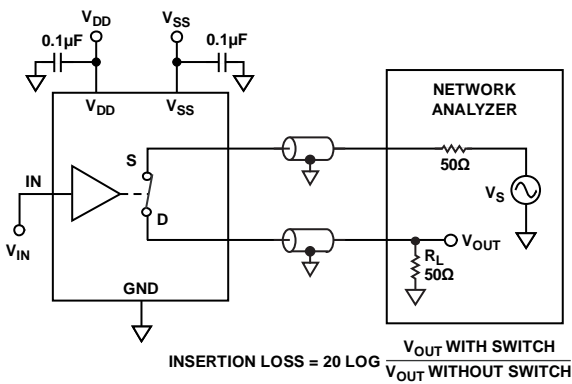


Figure 26. Bandwidth

08486-025

## TERMINOLOGY

**I<sub>DD</sub>**

The positive supply current.

**I<sub>SS</sub>**

The negative supply current.

**V<sub>D</sub> (V<sub>S</sub>)**

The analog voltage on Terminal D and Terminal S.

**R<sub>ON</sub>**

The ohmic resistance between Terminal D and Terminal S.

**R<sub>FLAT (ON)</sub>**

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

**I<sub>S</sub> (Off)**

The source leakage current with the switch off.

**I<sub>D</sub> (Off)**

The drain leakage current with the switch off.

**I<sub>D</sub>, I<sub>S</sub> (On)**

The channel leakage current with the switch on.

**V<sub>INL</sub>**

The maximum input voltage for Logic 0.

**V<sub>INH</sub>**

The minimum input voltage for Logic 1.

**I<sub>INL</sub> (I<sub>INH</sub>)**

The input current of the digital input.

**C<sub>S</sub> (Off)**

The off switch source capacitance, measured with reference to ground.

**C<sub>D</sub> (Off)**

The off switch drain capacitance, measured with reference to ground.

**C<sub>D</sub>, C<sub>S</sub> (On)**

The on switch capacitance, measured with reference to ground.

**C<sub>IN</sub>**

The digital input capacitance.

**t<sub>ON</sub>**

Delay time between the 50% and 90% points of the digital input and switch on condition. See Figure 23.

**t<sub>OFF</sub>**

Delay time between the 50% and 90% points of the digital input and switch off condition. See Figure 23.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching. See Figure 24.

**Off Isolation**

A measure of unwanted signal coupling through an off switch. See Figure 25.

**Bandwidth**

The frequency at which the output is attenuated by 3 dB. See Figure 26.

**On Response**

The frequency response of the on switch.

**Insertion Loss**

The loss due to the on resistance of the switch. See Figure 26.

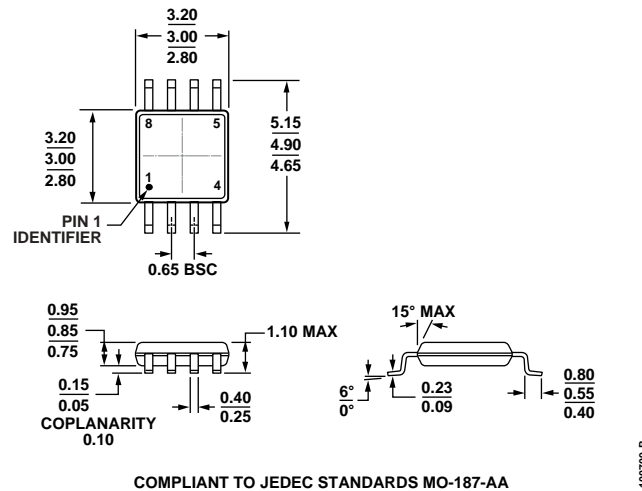
**THD + N**

The ratio of the harmonic amplitude plus noise of the signal to the fundamental. See Figure 27.

**AC Power Supply Rejection Ratio (ACPSRR)**

ACPSRR measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the ACPSRR. See Figure 19.

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 28. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

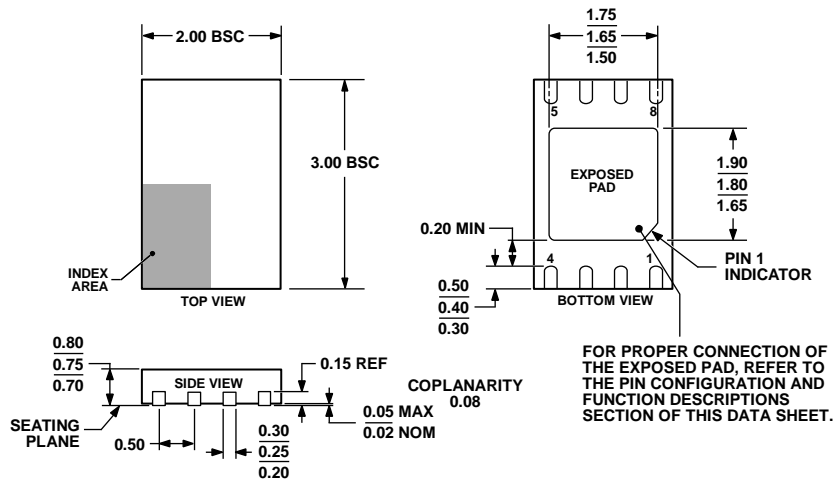


Figure 29. 8-Lead Lead Frame Chip Scale Package [LFCSP\_WD] 3 mm x 2 mm Body, Very Very Thin, Dual Lead (CP-8-4)

Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG1401BRMZ <sup>1</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S2T
ADG1401BRMZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S2T
ADG1401BCPZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-4	2Y
ADG1402BRMZ <sup>1</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S2U
ADG1402BRMZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S2U
ADG1402BCPZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-4	1F

<sup>1</sup> Z = RoHS Compliant Part.

**ADG1401/ADG1402**

**NOTES**