High Speed quad SPST CMOS analog switch

ADG201HS

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/ADG201

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
ADG201-803Q	High speed quad SPST CMOS analog switch

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
Q	GDIP1-T16	16-Lead ceramic dual-in-line package (CERDIP)

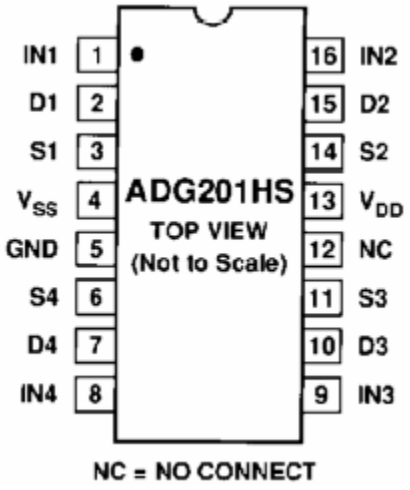

Figure 1 - Terminal connections.

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3.0 Absolute Maximum Ratings. 1/ (T_A = 25°C, unless otherwise noted)

V_{DD} to V_{SS} 44V
V_{DD} to GND ..... -0.3V, 25V
V_{SS} to GND 2/ ..... +0.3V, -25V
Analog Inputs 3/
Voltage at S, D ..... V_{SS} -2V to V_{DD} +2V
or 20mA, whichever comes first
Current at S, D 20mA
Continuous Current, S or D 20mA
Pulsed Current, S or D (1mS Duration, 10% duty cycle) 70mA
Digital Inputs 3/
Voltage at IN, WR ..... V_{SS} - 4V to V_{DD} +4V
or 20mA, whichever comes first
Current at IN 20mA
Power dissipation 470mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Notes:

1/ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2/ If V_{SS} is open circuited with V_{DD} and GND applied, the V_{SS} pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V_{SS} to GND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.

3/ Overvoltage at IN, S, or D will be clamped by diodes. Current should be limited to 20mA (see above).

3.1 Thermal Characteristics:

Thermal Resistance, cerdip (Q) Package

Junction-to-Case (Θ_{JC}) = 35°C/W Max

Junction-to-Ambient (Θ_{JA}) = 120°C/W Max

4.0 Electrical Table: See notes at end of table

Table I

Parameter	Symbol	Conditions 1/	Sub-group	Limit 2/ Min	Limit 2/ Max	Units
Analog Signal range	V_S	3/	4		±15	V
On resistance	$R_{DS(ON)}$	V_S = ±10V, I_D=1mA, V_{IN} = 0.8V	1		50	Ohm
			2, 3		75	
Source OFF leakage current	$I_{S(OFF)}$	V_D=±14V, V_S=±14V, V_{IN} =2.4V	1		±1.0	nA
			2, 3		±60	
Drain OFF leakage current	$I_{D(OFF)}$	V_D=±14V, V_S=±14V, V_{IN} =2.4V	1		±1.0	
			2, 3		±60	
Channel ON leakage current	$I_{D(ON)}$	V_D = V_S = ±14V, V_{IN} = 0.8V	1		±1.0	
			2, 3		±60	
Low level input voltage 4/	V_{IL}		7, 8		0.8	V
High level input voltage 4/	V_{IH}		7, 8	2.4		
Input leakage current (low)	I_{IL}	V_{IN} under test = 1.0V, All other V_{IN} = 16.5V	1, 2, 3		±1.0	µA
Input leakage current (high)	I_{IH}	V_{IN} under test = 16.5V, All other V_{IN} = 1.0V, V_S = ±17V	1, 2, 3		±1.0	
Positive supply current	I+	V_{IN}=3.0V or 0.8V for all switches	1, 2, 3		10	mA
Negative supply current	I-	V_{IN}=2.4V or 0.8V for all switches	1, 2, 3		-6	
Switch on time	t_{ON}	R_L = 1KΩ, C_L=35pF, V_{IH}=+3V, V_{IL}=0V, V_S = ±10V see figure 3	9		50	nS
			10, 11		65	
Switch off time	t_{OFF}	R_L = 1KΩ, C_L=35pF, V_{IH}=+3V, V_{IL}=0V, V_S = ±10V see figure 3	9		50	
			10, 11		65	

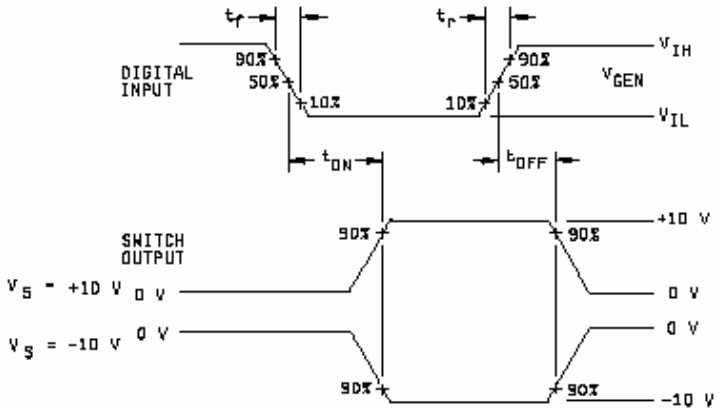
TABLE I NOTES:

1/ V+ = +15V, V- = -15V, unless otherwise specified

2/ The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.

3/ These parameters may not be tested, but shall be guaranteed to the limits specified in table I herein.

4/ Test not required if applied as a forcing function.



NOTE: Rise time and fall time ≤ 20 ns.

FIGURE 3. Test circuit and switching waveforms.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 7, 8 1/ 2/
Group A Test Requirements	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters	1, 7 2/
Group D end-point electrical parameters	1, 7
Group E end-point electrical parameters	na

1/ PDA applies to subgroup 1. Exclude Deltas from PDA.
2/ See Table III for delta measure parameters and limits.

4.2 Table III. Burn-in test delta limits.

Table III.				
TEST TITLE	BURN-IN LIMIT	LIFE TEST LIMIT	DELTA LIMIT	UNITS
$R_{DS(ON)}$	50	65	±15	Ω
$I_{D(OFF)}$	±1	±2	±1	nA
$I_{S(ON)} + I_{D(ON)}$	±1	±2	±1	nA

5.0 Life Test/Burn-In:

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B or C.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

6.0 MIL-STD-38535 QMLV exceptions:

6.1 Full WLA per MIL-STD-883 TM 5007 is not available for this product fabricated in a QMLQ wafer process facility. SEM Inspection only is available per MIL-STD-883, TM2018.

Rev	Description of Change	Date
A	Initiate	July 30, 2001
B	Update web address	Feb. 18, 2002
C	Update web address	June 20, 2003
D	Clarify SEM vs. WLA availability for QMLQ fab process	Nov. 8, 2007
E	Update header/footer & add to 1.0 Scope description.	Feb. 26,2008