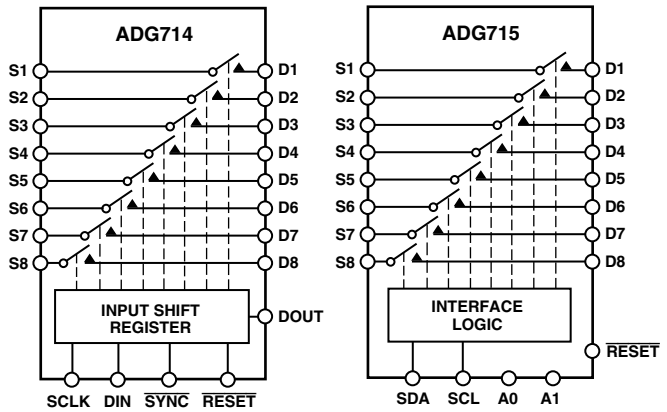
CMOS, Low Voltage Serially Controlled, Octal SPST Switches

ADG714/ADG715

FEATURES
ADG714 SPI™/QSPI™/MICROWIRE™-Compatible Interface
ADG715 I²C™-Compatible Interface
2.7 V to 5.5 V Single Supply
±2.5 V Dual Supply
2.5 Ω On Resistance
0.6 Ω On Resistance Flatness
100 pA Leakage Currents
Octal SPST
Power-On Reset
Fast Switching Times
TTL/CMOS-Compatible
Small TSSOP Package

APPLICATIONS
Data Acquisition Systems
Communication Systems
Relay Replacement
Audio and Video Switching

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG714/ADG715 are CMOS, octal SPST (single-pole, single-throw) switches controlled via either a 2- or 3-wire serial interface. On resistance is closely matched between switches and very flat over the full signal range. Each switch conducts equally well in both directions and the input signal range extends to the supplies. Data is written to these devices in the form of 8 bits, each bit corresponding to one channel.

The ADG714 uses a 3-wire serial interface that is compatible with SPI , QSPI, and MICROWIRE and most DSP interface standards. The output of the shift register DOUT enables a number of these parts to be daisy chained.

The ADG715 uses a 2-wire serial interface that is compatible with the I²C interface standard. The ADG715 has four hard wired addresses, selectable from two external address pins (A0 and A1). This allows the 2 LSBs of the 7-bit slave address to be set by the user. A maximum of four of these devices may be connected to the bus.

On power-up of these devices, all switches are in the OFF condition, and the internal registers contain all zeros.

Low power consumption and operating supply range of 2.7 V to 5.5 V make this part ideal for many applications. These parts may also be supplied from a dual ±2.5 V supply. The ADG714 and ADG715 are available in a small 24-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. 2- or 3-wire serial interface
2. Single/dual supply operation. The ADG714 and ADG715 are fully specified and guaranteed with 3 V, 5 V, and ±2.5 V supply rails.
3. Low on resistance, typically 2.5 Ω
4. Low leakage
5. Power-on reset
6. Small 24-lead TSSOP package

REV. B

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ADG714/ADG715–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
	4.5	5	Ω max	
On Resistance Match Between Channels (ΔR_{ON})		0.4	Ω typ	
		0.8	Ω max	V_S = 0 V to V_{DD}, I_S = 10 mA
On Resistance Flatness ($R_{FLAT(ON)}$)	0.6		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V
	±0.1	±0.3	nA max	
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V
	±0.1	±0.3	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 1 V, or 4.5 V
	±0.1	±0.3	nA max	
DIGITAL INPUTS (SCLK, DIN, $\overline{SYNC}$, A0, A1)				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance[2]	3		pF typ	
DIGITAL OUTPUT ADG714 DOUT[2]				
Output Low Voltage		0.4	V max	I_{SINK} = 6 mA
C_{OUT} Digital Output Capacitance	4		pF typ	
DIGITAL INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7 V_{DD}	V min	
		V_{DD} + 0.3	V max	
Input Low Voltage, V_{INL}		–0.3	V min	
		0.3 V_{DD}	V max	
I_{IN}, Input Leakage Current	0.005		μA typ	V_{IN} = 0 V to V_{DD}
		±1	μA max	
V_{HYST}, Input Hysteresis	0.05 V_{DD}		V min	
C_{IN}, Input Capacitance	6		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON} ADG714	20		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		32	ns max	
t_{ON} ADG715	95		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		140	ns max	
t_{OFF} ADG714	8		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		15	ns max	
t_{OFF} ADG715	85		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		130	ns max	
Break-Before-Make Time Delay, t_D	8		ns typ	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF
		1	ns min	
Charge Injection	±3		pC typ	V_S = 2 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	–60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel-to-Channel Crosstalk	–70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
–3 dB Bandwidth	155		MHz typ	R_L = 50 Ω, C_L = 5 pF
C_S (OFF)	11		pF typ	
C_D (OFF)	11		pF typ	
C_D, C_S (ON)	22		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 5.5 V
		20	μA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ±10%, V_{SS} = 0 V, GND = 0 V unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6		Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
	11	12	Ω max	
On Resistance Match Between Channels (ΔR_{ON})		0.4	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
		1.2	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)		3.5	Ω typ	V_S = 0 V to V_{DD}, I_S = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V
	±0.1	±0.3	nA max	
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V
	±0.1	±0.3	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V, or 3 V
	±0.1	±0.3	nA max	
DIGITAL INPUTS (SCLK, DIN, $\overline{SYNC}$, A0, A1)				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance[2]	3		pF typ	
DIGITAL OUTPUT ADG714 DOUT[2]				
Output Low Voltage		0.4	V max	I_{SINK} = 6 mA
C_{OUT} Digital Output Capacitance	4		pF typ	
DIGITAL INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7 V_{DD}	V min	
		V_{DD} + 0.3	V max	
Input Low Voltage, V_{INL}		–0.3	V min	
		0.3 V_{DD}	V max	
I_{IN}, Input Leakage Current	0.005		μA typ	V_{IN} = 0 V to V_{DD}
		±1	μA max	
V_{HYST}, Input Hysteresis	0.05 V_{DD}		V min	
C_{IN}, Input Capacitance	6		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON} ADG714	35		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		65	ns max	
t_{ON} ADG715	130		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		200	ns max	
t_{OFF} ADG714	11		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		20	ns max	
t_{OFF} ADG715	115		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		180	ns max	
Break-Before-Make Time Delay, t_D	8		ns typ	V_S = 2 V, R_L = 300 Ω, C_L = 35 pF
		1	ns min	
Charge Injection	±2		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	–60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel-to-Channel Crosstalk	–70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
–3 dB Bandwidth	155		MHz typ	R_L = 50 Ω, C_L = 5 pF
C_S (OFF)	11		pF typ	
C_D (OFF)	11		pF typ	
C_D, C_S (ON)	22		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or 3.3 V
		20	μA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG714/ADG715–SPECIFICATIONS[1]

DUAL SUPPLY (V_{DD} = +2.5 V ± 10%, V_{SS} = 2.5 V ± 10%, GND = 0 V unless otherwise noted.)

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
	4.5	5	Ω max	
On Resistance Match Between Channels (ΔR_{ON})		0.4	Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
		0.8	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.6		Ω typ	V_S = V_{SS} to V_{DD}, I_{DS} = 10 mA
		1	Ω max	
LEAKAGE CURRENTS				V_{DD} = +2.75 V, V_{SS} = –2.75 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = +2.25 V/–1.25 V, V_D = –1.25 V/+2.25 V
	±0.1	±0.3	nA max	
Drain OFF Leakage I_D (OFF)	±0.01		nA typ	V_S = +2.25 V/–1.25 V, V_D = –1.25 V/+2.25 V
	±0.1	±0.3	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = +2.25 V/–1.25 V
	±0.1	±0.3	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.7	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance[2]	3		pF typ	
DIGITAL OUTPUT ADG714 DOUT[2]				
Output Low Voltage		0.4	V max	I_{SINK} = 6 mA
C_{OUT} Digital Output Capacitance	4		pF typ	
DIGITAL INPUTS (SCL, SDA)[2]				
Input High Voltage, V_{INH}		0.7 V_{DD}	V min	
		V_{DD} + 0.3	V max	
Input Low Voltage, V_{INL}		–0.3	V min	
		0.3 V_{DD}	V max	
I_{IN}, Input Leakage Current	0.005		μA typ	V_{IN} = 0 V to V_{DD}
		±1	μA max	
V_{HYST}, Input Hysteresis	0.05 V_{DD}		V min	
C_{IN}, Input Capacitance	6		pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage		0.4	V max	I_{SINK} = 3 mA
		0.6	V max	I_{SINK} = 6 mA
DYNAMIC CHARACTERISTICS[2]				
t_{ON} ADG714	20		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		32	ns max	
t_{ON} ADG715	133		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		200	ns max	
t_{OFF} ADG714	8		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		18	ns max	
t_{OFF} ADG715	124		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		190	ns max	
Break-Before-Make Time Delay, t_D	8		ns typ	V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF
		1	ns min	
Charge Injection	±3		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	–60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel-to-Channel Crosstalk	–70		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
–3 dB Bandwidth	155		MHz typ	R_L = 50 Ω, C_L = 5 pF
C_S (OFF)	11		pF typ	
C_D (OFF)	11		pF typ	
C_D, C_S (ON)	22		pF typ	
POWER REQUIREMENTS				V_{DD} = +2.75 V, V_{SS} = –2.75 V
I_{DD}	15		μA typ	Digital Inputs = 0 V or 3.3 V
		25	μA max	
I_{SS}	15		μA typ	
		25	μA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG714 TIMING CHARACTERISTICS[1, 2] (V_{DD} = 2.7 V to 5.5 V. All specifications –40°C to +85°C unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
f_{SCLK}	30	MHz max	SCLK Cycle Frequency
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	0	ns min	$\overline{SYNC}$ to SCLK Rising Edge Setup Time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge
t_8	33	ns min	Minimum $\overline{SYNC}$ High Time
t_9[3]	20	ns max	SCLK Rising Edge to DOUT Valid

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3]C_L = 20 pF, R_L = 1 kΩ.

Specifications subject to change without notice.

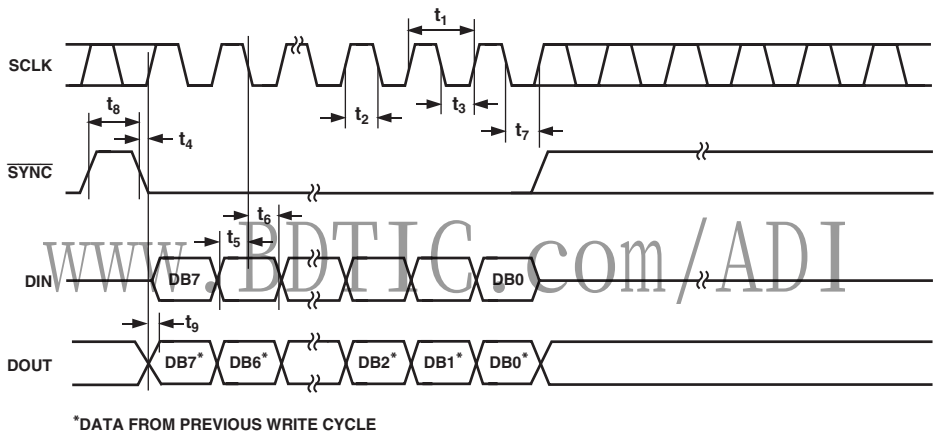


Figure 1. 3-Wire Serial Interface Timing Diagram

ADG715 TIMING CHARACTERISTICS[1] (V_{DD} = 2.7 V to 5.5 V. All specifications –40°C to +85°C unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
f_{SCL}	400	kHz max	SCL Clock Frequency
t_1	2.5	µs min	SCL Cycle Time
t_2	0.6	µs min	t_{HIGH}, SCL High Time
t_3	1.3	µs min	t_{LOW}, SCL Low Time
t_4	0.6	µs min	$t_{HD, STA}$, Start/Repeated Start Condition Hold Time
t_5	100	ns min	$t_{SU, DAT}$, Data Setup Time
t_6[2]	0.9	µs max	$t_{HD, DAT}$, Data Hold Time
	0	µs min	
t_7	0.6	µs min	$t_{SU, STA}$, Setup Time for Repeated Start
t_8	0.6	µs min	$t_{SU, STO}$, Stop Condition Setup Time
t_9	1.3	µs min	t_{BUF}, Bus Free Time Between a STOP Condition and a Start Condition
t_{10}	300	ns max	t_R, Rise Time of Both SCL and SDA When Receiving
	$20 + 0.1C_b$[3]	ns min	
t_{11}	250	ns max	t_F, Fall Time of SDA When Receiving
t_{11}	300	ns max	t_F, Fall Time of SDA When Transmitting
	$0.1C_b$[3]	ns min	
C_b	400	pF max	Capacitive Load for Each Bus Line
t_{SP}[4]	50	ns max	Pulsewidth of Spike Suppressed

NOTES
[1]See Figure 2.
[2]A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[3]C_b is the total capacitance of one bus line in pF. t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD}.
[4]Input filtering on both the SCL and SDA inputs suppress noise spikes that are less than 50 ns.

Specifications subject to change without notice.

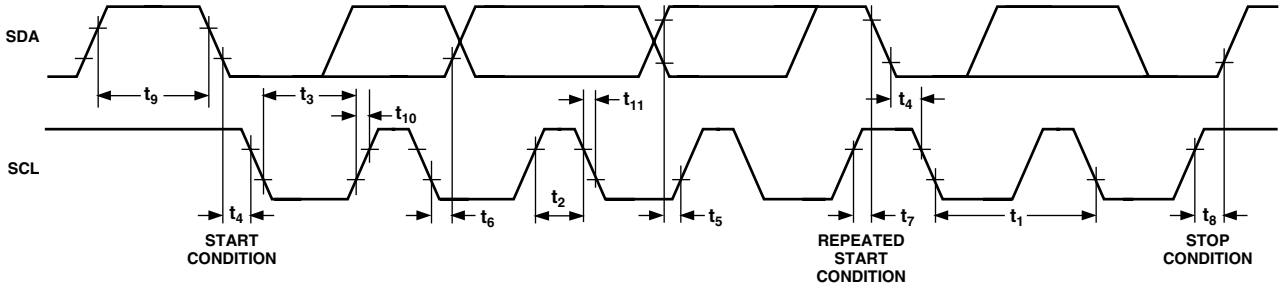


Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = 25°C unless otherwise noted.)

V_{DD} to V_{SS} . . . . . 7 V
V_{DD} to GND . . . . . –0.3 V to +7 V
V_{SS} to GND . . . . . +0.3 V to –3.5 V
Analog Inputs[2] . . . . . V_{SS} –0.3 V to V_{DD} +0.3 V
or 30 mA, Whichever Occurs First
Digital Inputs[2] . . . . . –0.3 V to V_{DD} +0.3 V
or 30 mA, Whichever Occurs First
Peak Current, S or D . . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Continuous Current, S or D . . . . . 30 mA
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C

TSSOP Package
θ_{JA} Thermal Impedance . . . . . 128°C/W
θ_{JC} Thermal Impedance . . . . . 42°C/W
Lead Temperature, Soldering (10 sec) . . . . . 300°C
Infrared Reflow (20 sec) . . . . . 235°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

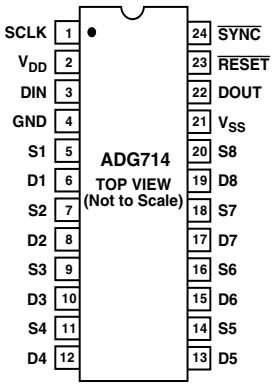
ORDERING GUIDE

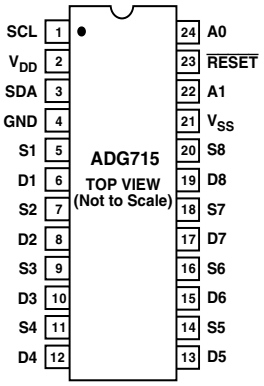
Model	Temperature Range	Interface	Package Description	Package Option
ADG714BRU	–40°C to +85°C	SPI/QSPI/MICROWIRE	TSSOP	RU-24
ADG715BRU	–40°C to +85°C	I²C-Compatible	TSSOP	RU-24

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG714/ADG715 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS
24-Lead TSSOP





ADG714 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz.
2	V_{DD}	Positive Analog Supply Voltage.
3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4	GND	Ground Reference
5, 7, 9, 11, 14, 16, 18, 20	Sx	Source. May be an input or output.
6, 8, 10, 12, 13, 15, 17, 19	Dx	Drain. May be an input or output.
21	V_{SS}	Negative Analog Supply Voltage. For single supply operation this should be tied to GND.
22	DOUT	Serial Data Output. This allows a number a parts to be daisy chained. Data is clocked out of the input shift register on the rising edge of SCLK. DOUT is an open-drain output that should be pulled to the supply with an external pull-up resistor.
23	$\overline{\text{RESET}}$	Active Low Control Input. Clears the input register and turns all switches to the OFF condition.
24	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clocks. Taking $\overline{\text{SYNC}}$ high updates the switches.

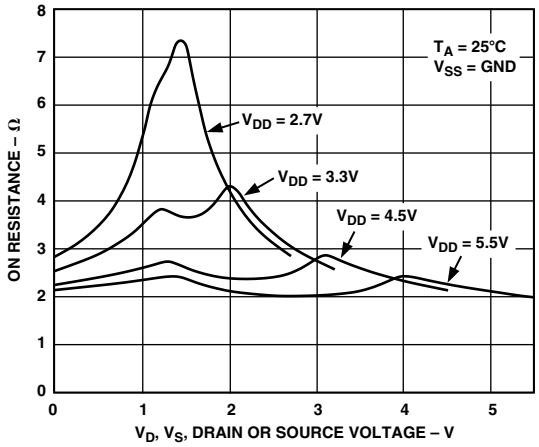
ADG715 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 8-bit input shift register. Clock rates of up to 400 kbit/s can be accommodated with this 2-wire serial interface.
2	V_{DD}	Positive Analog Supply Voltage
3	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 8-bit input shift register during the write cycle and used to readback one byte of data during the read cycle. It is a bidirectional open-drain data line which should be pulled to the supply with an external pull-up resistor.
4	GND	Ground Reference
5, 7, 9, 11, 14, 16, 18, 20	Sx	Source. May be an input or output.
6, 8, 10, 12, 13, 15, 17, 19	Dx	Drain. May be an input or output.
21	V_{SS}	Negative Analog Supply Voltage. For single supply operation this should be tied to GND.
22	A1	Address Input. Sets the second least significant bit of the 7-bit slave address.
23	$\overline{\text{RESET}}$	Active Low Control Input. Clears the input register and turns all switches to the OFF condition.
24	A0	Address Input. Sets the least significant bit of the 7-bit slave address.

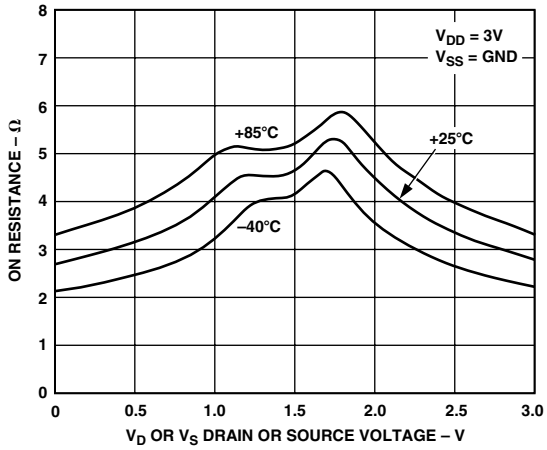
TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply in a dual supply application. In single supply applications, this should be tied to ground.
I_{DD}	Positive Supply Current
I_{SS}	Negative Supply Current
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
R_{ON}	Ohmic resistance between D and S
ΔR_{ON}	On resistance match between any two channels, i.e., R_{ON} max–R_{ON} min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D and S
C_S (OFF)	"OFF" Switch Source Capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" Switch Drain Capacitance. Measured with reference to ground.
C_D, C_S (ON)	"ON" Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance
t_{ON}	Delay time between loading new data to the shift register and selected switches switching on.
t_{OFF}	Delay time between loading new data to the shift register and selected switches switching off.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Bandwidth	The frequency at which the output is attenuated by –3 dBs.
On Response	The frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the switch. Insertion Loss = 20 $\log_{10}$ (V_{OUT} with switch/ V_{OUT} without switch.
V_{INL}	Maximum input voltage for Logic 0.
V_{INH}	Minimum input voltage for Logic 1.
I_{INL}(I_{INH})	Input current of the digital input.
I_{DD}	Positive Supply Current

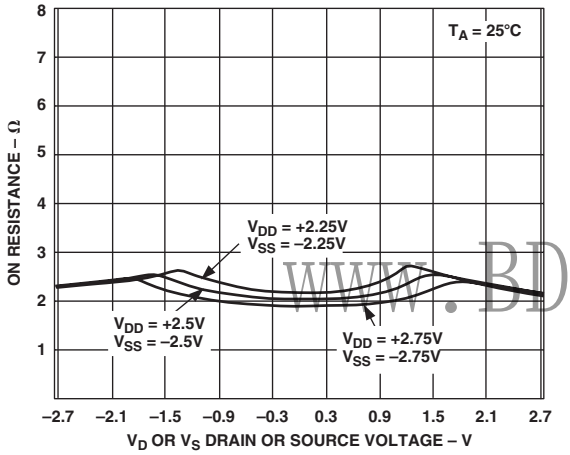
ADG714/ADG715–Typical Performance Characteristics



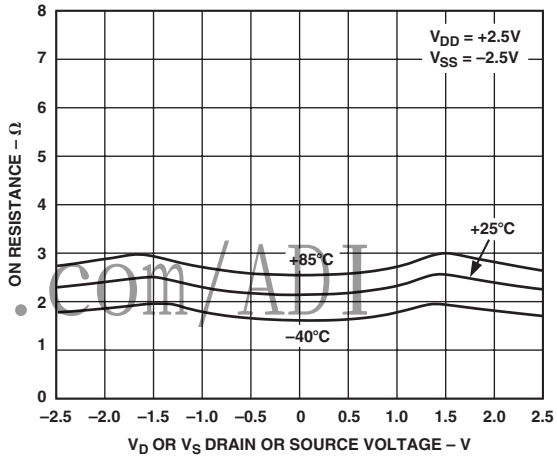
TPC 1. On Resistance as a Function of V_D (V_S) Single Supply



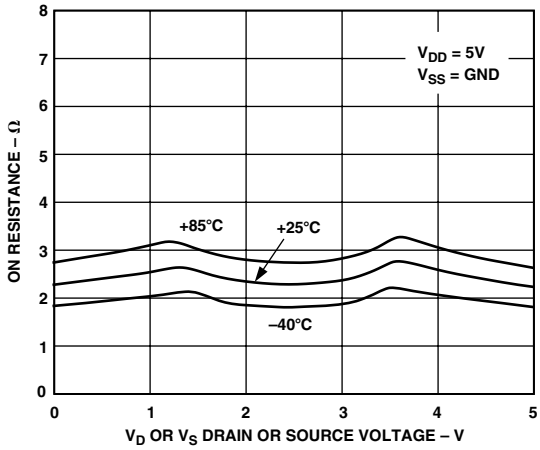
TPC 4. On Resistance as a Function of V_D (V_S) for Different Temperatures; V_{DD} = 3 V



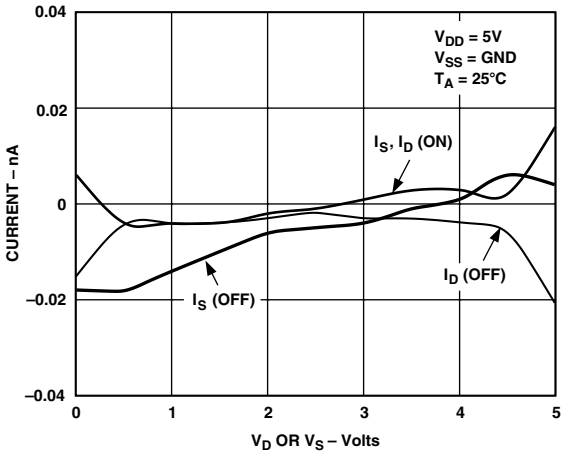
TPC 2. On Resistance as a Function of V_D (V_S); Dual Supply



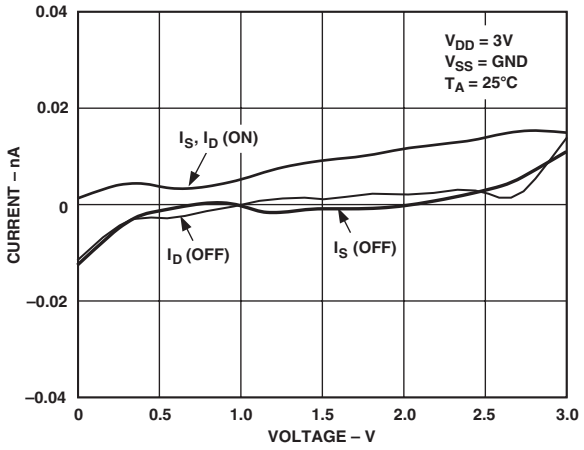
TPC 5. On Resistance as a Function of V_D (V_S) for Different Temperatures; Dual Supply



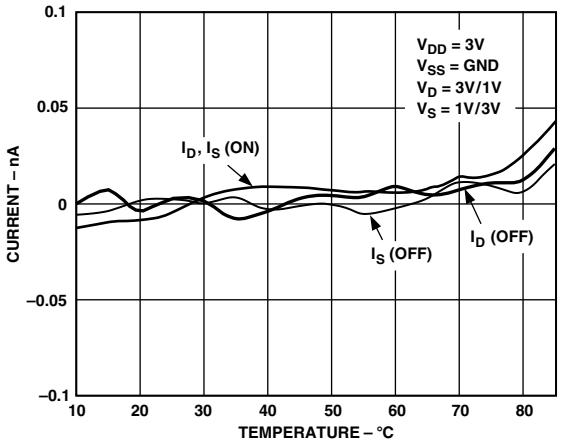
TPC 3. On Resistance as a Function of V_D (V_S) for Different Temperatures; V_{DD} = 5 V



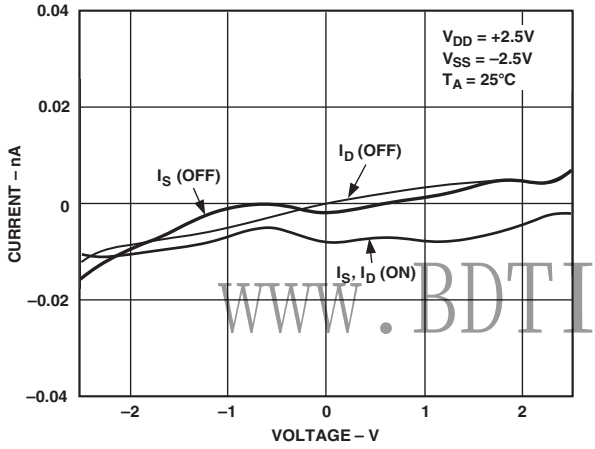
TPC 6. Leakage Currents as a Function of V_D (V_S)



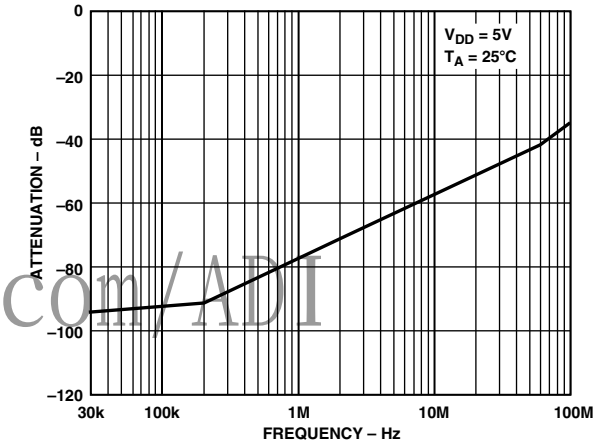
TPC 7. Leakage Currents as a Function of V_D (V_S)



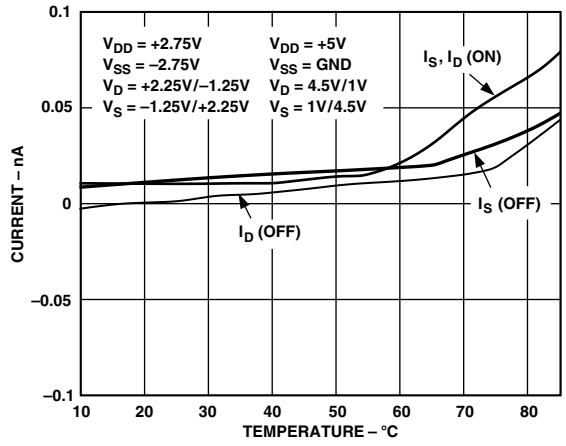
TPC 10. Leakage Currents as a Function of Temperature



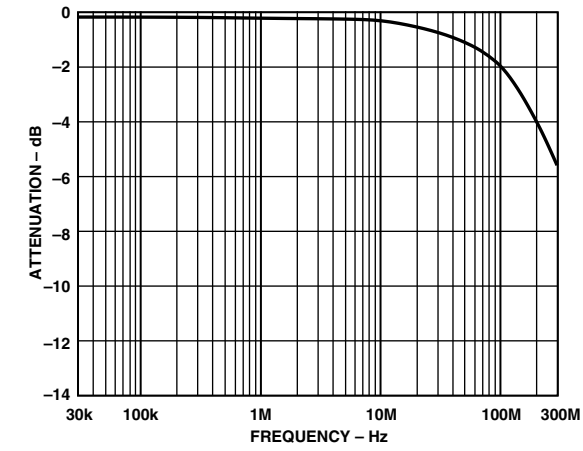
TPC 8. Leakage Currents as a Function of V_D (V_S) Dual Supply



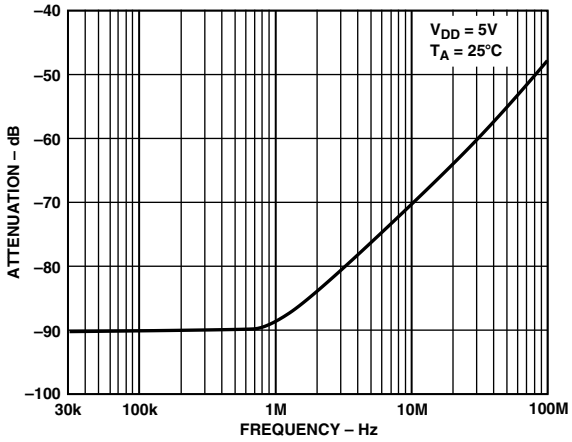
TPC 11. Off Isolation vs. Frequency



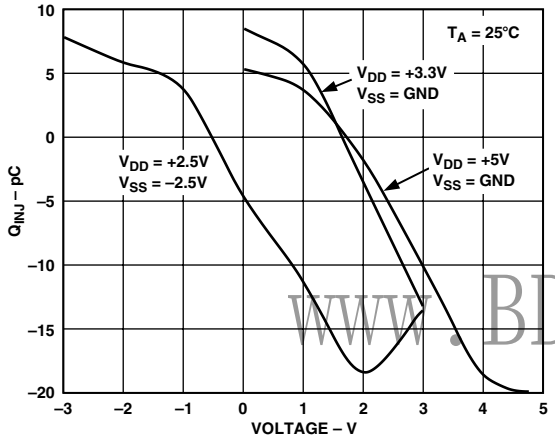
TPC 9. Leakage Currents as Function of Temperature



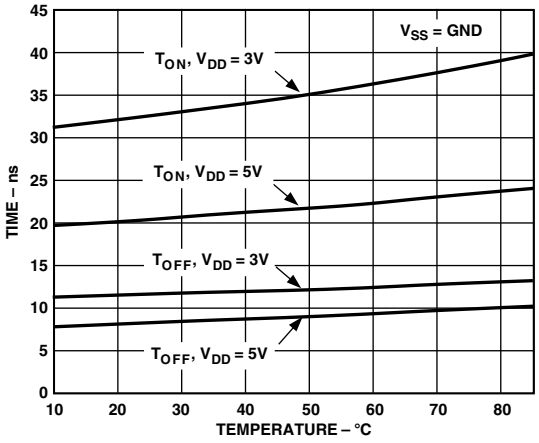
TPC 12. On Response vs. Frequency



TPC 13. Crosstalk vs. Frequency



TPC 14. Charge Injection vs. Source/Drain Voltage



TPC 15. T_{ON}/T_{OFF} Times vs. Temperature for ADG714

GENERAL DESCRIPTION

The ADG714 and ADG715 are serially controlled, octal SPST switches, controlled by either a 2- or 3-wire interface. Each bit of the 8-bit serial word corresponds to one switch of the part. A Logic 1 in the particular bit position turns on the switch, while a Logic 0 turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all, or none of the switches ON.

When changing the switch conditions, a new 8-bit word is written to the input shift register. Some of the bits may be the same as the previous write cycle, as the user may not wish to change the state of some switches. To minimize glitches on the output of these switches, the part cleverly compares the state of switches from the previous write cycle. If the switch is already in the ON condition, and is required to stay ON, there will be minimal glitches on the output of the switch.

POWER-ON RESET

On power-up of the device, all switches will be in the OFF condition and the internal shift register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

3-Wire Serial Interface

The ADG714 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN), that is compatible with SPI, QSPI, MICROWIRE interface standards and most DSPs. Figure 1 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit shift register via DIN under the control of the $\overline{SYNC}$ and SCLK signals. Data may be written to the shift register in more or less than eight bits. In each case the shift register retains the last eight bits that were written.

When $\overline{SYNC}$ goes low, the input shift register is enabled. Data from DIN is clocked into the shift register on the falling edge of SCLK. Each bit of the 8-bit word corresponds to one of the eight switches. Figure 3 shows the contents of the input shift register. Data appears on the DOUT pin on the rising edge of SCLK suitable for daisy chaining, delayed of course by eight bits. When all eight bits have been written into the shift register, the $\overline{SYNC}$ line is brought high again. The switches are updated with the new configuration and the input shift register is disabled. With $\overline{SYNC}$ held high, the input shift register is disabled, so further data or noise on the DIN line will have no effect on the shift register.

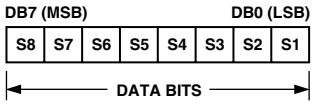


Figure 3. Input Shift Register Contents

SERIAL INTERFACE

2-Wire Serial Interface

The ADG715 is controlled via an I^2C-compatible serial bus. This device is connected to the bus as a slave device (no clock is generated by the switch).

The ADG715 has a 7-bit slave address. The five MSBs are 10010 and the two LSBs are determined by the state of the A0 and A1 pins.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte that consists of the 7-bit slave address followed by a R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master will read from the slave device. However, if the R/$\overline{W}$ bit is low, the master will write to the slave device.

2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master will pull the SDA line high during the tenth clock pulse to establish a STOP condition. In read mode, the master will issue a no acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse and then high during the tenth clock pulse to establish a STOP condition.

See Figure 4 for a graphical explanation of the serial interface.

A repeated write function gives the user flexibility to update the matrix switch a number of times after addressing the part only once. During the write cycle, each data byte will update the configuration of the switches. For example, after the matrix switch has acknowledged its address byte, and received one data byte, the switches will update after the data byte; if another data byte is written to the matrix switch while it is still the addressed slave device, this data byte will also cause a switch configuration update. Repeat read of the matrix switch is also allowed.

Input Shift Register

The input shift register is eight bits wide. Figure 3 illustrates the contents of the input shift register. Data is loaded into the device as an 8-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 2. The 8-bit word consists of eight data bits, each controlling one switch. MSB (Bit 7) is loaded first.

Write Operation

When writing to the ADG715, the user must begin with an address byte and R/$\overline{W}$ bit, after which the switch will acknowledge that it is prepared to receive data by pulling SDA low. This address byte is followed by the 8-bit word. The write operation for the switch is shown in the Figure 4.

READ Operation

When reading data back from the ADG715, the user must begin with an address byte and R/$\overline{W}$ bit, after which the switch will acknowledge that it is prepared to transmit data by pulling SDA low. The readback operation is a single byte that consists of the eight data bits in the input register. The read operation for the part is shown in Figure 5.

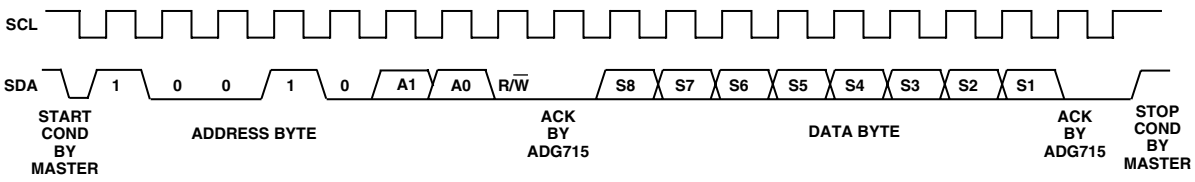


Figure 4. ADG715 Write Sequence

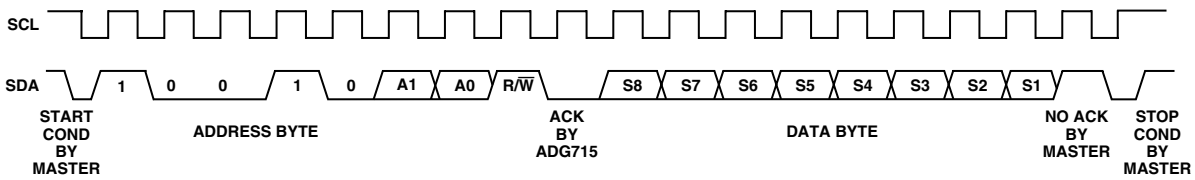


Figure 5. ADG715 Readback Sequence

APPLICATIONS

Multiple Devices On One Bus

Figure 6 shows four ADG715 devices on the same serial bus. Each has a different slave address since the state of their A0 and A1 pins is different. This allows each switch to be written to or read from independently.

Daisy-Chaining Multiple ADG714s

A number of ADG714 switches may be daisy-chained simply by using the DOUT pin. Figure 7 shows a typical implementation. The $\overline{\text{SYNC}}$ pin of all three parts in the example are tied together. When $\overline{\text{SYNC}}$ is brought low, the input shift registers of all parts are enabled, data is written to the parts via DIN, and clocked through the shift registers. When the transfer is complete, $\overline{\text{SYNC}}$ is brought high and all switches are updated simultaneously. Further shift registers may be added in series.

Power Supply Sequencing

When using CMOS devices, care must be taken to ensure correct power-supply sequencing. Incorrect power-supply sequencing can result in the device being subjected to stresses beyond those maximum ratings listed in the data sheet. Digital and analog inputs should always be applied after power supplies and ground. In dual supply applications, if digital or analog inputs may be applied to the device prior to the V_{DD} and V_{SS} supplies, the addition of a Schottky diode connected between V_{SS} and GND will ensure that the device powers on correctly. For single supply operation, V_{SS} should be tied to GND as close to the device as possible.

Decoding Multiple ADG714s Using an ADG739

The dual 4-channel ADG739 multiplexer can be used to multiplex a single chip select line to provide chip selects for up to four

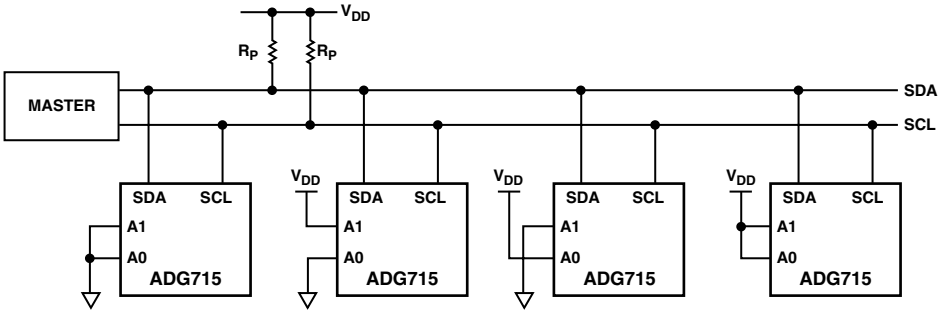


Figure 6. Multiple ADG715s On One Bus

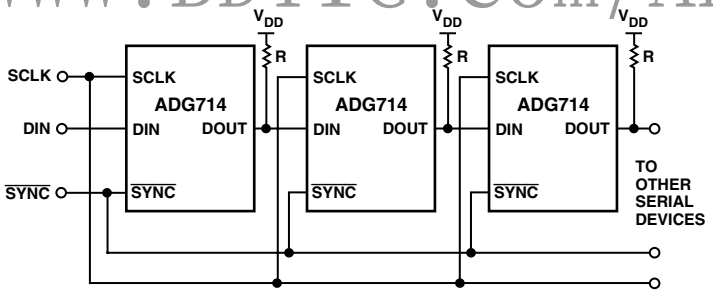


Figure 7. Multiple ADG714 Devices in a Daisy-Chained Configuration

devices on the SPI bus. Figure 8 illustrates the ADG739 and multiple ADG714s in such a typical configuration. All devices receive the same serial clock and serial data, but only one device will receive the $\overline{\text{SYNC}}$ signal at any one time. The ADG739 is a serially controlled device also. One bit programmable pin of the microcontroller is used to enable the ADG739 via $\overline{\text{SYNC2}}$, while another bit programmable pin is used as the chip select for the other serial devices, $\overline{\text{SYNC1}}$. Driving $\overline{\text{SYNC2}}$ low enables changes to be made to the addressed serial devices. By bringing $\overline{\text{SYNC1}}$ low, the selected serial device hanging from the SPI bus will be enabled and data will be clocked into its shift register on the falling edges of SCLK. The convenient design of the matrix switch allows for different combinations of the four serial devices to be addressed at any one time. If more devices need to be addressed via one chip select line, the ADG738 is an 8-channel device and would allow further expansion of the chip select scheme. There may be some digital feedthrough from the digital input lines because SCLK and DIN are permanently connected to each device. Using a burst clock will minimize the effects of digital feedthrough on the analog channels.

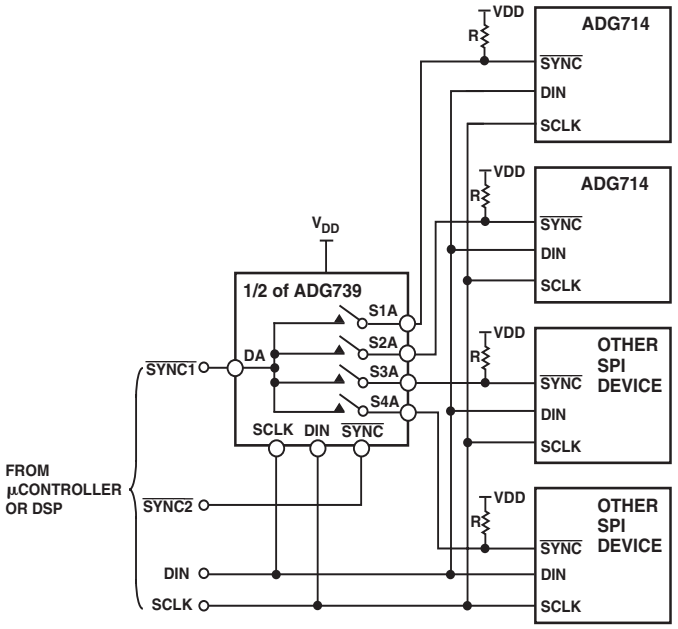
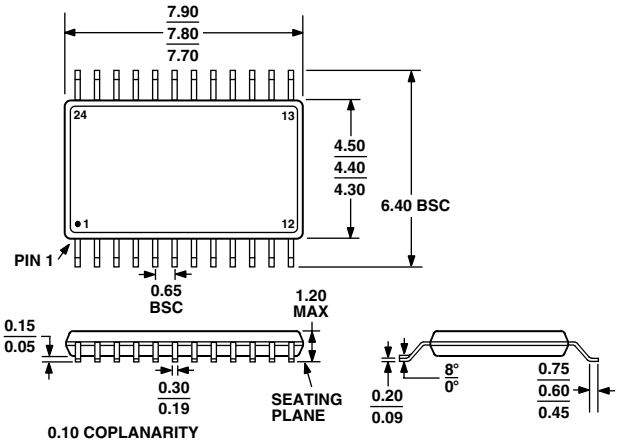


Figure 8. Addressing Multiple ADG714s Using an ADG739

OUTLINE DIMENSIONS

24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AD

C00043–0–11/02(B)

Revision History

Location	Page

11/02—Data Sheet changed from REV. A to REV. B.

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