3-Channel Digital Potentiometer with Nonvolatile Memory

ADN2860

FEATURES

- 3 channels:
  - Dual 512-position
  - Single 128-position
- 25 kΩ or 250 kΩ full-scale resistance
- Low temperature coefficient:
  - Potentiometer divider 15 ppm/°C
  - Rheostat mode 35 ppm/°C
- Nonvolatile memory retains wiper settings
- Permanent memory write protection
- Linear increment/decrement
- ±6 dB increment/decrement
- I²C-compatible serial interface
- 2.7 V to 5.5 V single-supply operation
- ±2.25 V to ±2.75 V dual-supply operation
- Power-on reset time
- 256 bytes general-purpose user EEPROM
- 11 bytes RDAC user EEPROM
- GBIC and SFP compliant EEPROM
- 100-year typical data retention at T_A = 55°C

APPLICATIONS

- Laser diode drivers
- Optical amplifiers
- TIA gain setting
- TEC controller temperature setpoint

FUNCTIONAL BLOCK DIAGRAM

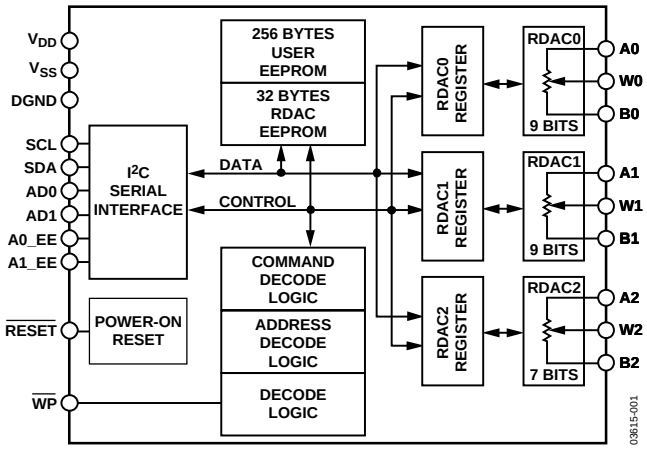

Figure 1.

GENERAL DESCRIPTION

The ADN2860 provides dual 512-position and single 128-position, digitally controlled variable resistors[1] (VR) in a single 4 mm × 4 mm LFCSP package. This device performs the same electronic adjustment function as a potentiometer, trimmer, or variable resistor. Each VR offers a completely programmable value of resistance between the A terminal and the wiper, or the B terminal and the wiper. The fixed A-to-B terminal resistance of 25 kΩ or 250 kΩ has a 1% channel-to-channel matching tolerance and a nominal temperature coefficient of 35 ppm/°C.

Wiper position programming, EEPROM[2] reading, and EEPROM writing are conducted via the standard 2-wire I²C interface. Previous default wiper position settings can be stored in memory, and refreshed upon system power-up.

Additional features of the ADN2860 include preprogrammed linear and logarithmic increment/decrement wiper changing. The actual resistor tolerances are stored in EEPROM so that the actual end-to-end resistance is known, which is valuable for calibration in precision applications.

The ADN2860 EEPROM, channel resolution, and package size conform to GBIC and SFP specifications. The ADN2860 is available in a 4 mm × 4 mm, 24-lead LFCSP package. All parts are guaranteed to operate over the extended industrial temperature range −40°C to +85°C.

[1] The terms programmable resistor, variable resistor, RDAC, and digital potentiometer are used interchangeably.
[2] The terms nonvolatile memory, EEMEM, and EEPROM are used interchangeably.

Rev. A

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REVISION HISTORY

11/04—Rev. 0 to Rev. A
Changes to Ordering Guide 20

7/04—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

Single supply: V_{DD} = 2.7 V to 5.5 V and −40°C < T_A < +85°C, unless otherwise noted.
Dual supply: V_{DD} = +2.25 V or +2.75 V, V_{SS} = −2.25 V or −2.75 V, and −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS, RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]						
	R-DNL	R_{WB}, 7-bit channel	−0.75		+0.75	LSB
		R_{WB}, 9-bit channels	−2.5		+2.5	LSB
Resistor Integral Nonlinearity[2]						
	R-INL	R_{WB}, 7-bit channel	−0.5		+0.5	LSB
	R-INL	R_{WB}, 9-bit channels, V_{DD} = 5.5 V	−2.0		+2.0	LSB
	R-INL	R_{WB}, 9-bit channels, V_{DD} = 2.7 V	−4.0		+4.0	LSB
Resistance Temperature Coefficent	$(\Delta R_{WB}/R_{WB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V, I_W = 1 V/R_{WB}		100	150	Ω
		V_{DD} = 3 V, I_W = 1 V/R_{WB}		250	400	Ω
Channel Resistance Matching	$\Delta R_{AB1}/\Delta R_{AB2}$	Ch 1 and Ch 2 R_{WB}, Dx = 0x1FF		0.1		%
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$	Dx = 0x3FF	−15		+15	%
DC CHARACTERISTICS, POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[3]						
	DNL	7-bit channel	−0.5		+0.5	LSB
	DNL	9-bit channels	−2.0		+2.0	LSB
Integral Nonlinearity[3]						
	INL	7-bit channel	−0.5		+0.5	LSB
	INL	9-bit channels	−2.0		+2.0	LSB
Voltage Divider Temperature Coefficent	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	7-bit channel/9-bit channels, code = full scale	−1/−2.75		0/0	LSB
Zero-Scale Error	V_{WZSE}	7-bit channel/9-bit channels, code = zero scale	0/0		1/2.0	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[4]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[5] Ax, Bx	$C_{A,B}$	f = 1 kHz, measured to GND, code = half scale		85		pF
Capacitance[5] Wx	C_W	f = 1 kHz, measured to GND, code = half scale		95		pF
Common-Mode Leakage Current[5, 6]	I_{CM}	$V_W = V_{DD}/2$		0.01	1	µA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V, V_{SS} = 0 V	2.4			V
		V_{DD}/V_{SS} = +2.7 V/0 V or V_{DD}/V_{SS} = ±2.5 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 5 V, V_{SS} = 0 V			0.8	V
		V_{DD}/V_{SS} = +2.7 V/0 V or V_{DD}/V_{SS} = ±2.5 V			0.6	V
Output Logic High (SDA)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to V_{DD} = 5 V, V_{SS} = 0 V	4.9			V
Output Logic Low	V_{OL}	$R_{PULL-UP}$ = 2.2 kΩ to V_{DD} = 5 V, V_{SS} = 0 V			0.4	V
$\overline{WP}$ Leakage Current	$I_{\overline{WP}}$	$\overline{WP} = V_{DD}$			9	µA
A0 Leakage Current	I_{A0}	A0 = GND			3	µA

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
Input Leakage Current (Excluding $\overline{WP}$ and A0)	I_I	V_{IN} = 0 V or V_{DD}			±1	µA
Input Capacitance[5]	C_I			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{SS} = 0 V		5	15	µA
Negative Supply Current	I_{SS}	$V_{IH} = V_{DD}$ or V_{IL} = GND, V_{DD} = 2.5 V, V_{SS} = −2.5 V		−5	−15	µA
EEMEM Data Storing Mode Current	I_{DD_STORE}	$V_{IH} = V_{DD}$ or V_{IL} = GND		35		mA
EEMEM Data Restoring Mode Current	$I_{DD\_RESTORE}$	$V_{IH} = V_{DD}$ or V_{IL} = GND		2.5		mA
Power Dissipation[7]	P_{DISS}	$V_{IH} = V_{DD}$ = 5 V or V_{IL} = GND		25	75	µW
Power Supply Sensitivity[5]	P_{SS}	ΔV_{DD} = 5 V ± 10%		0.01	0.025	%/%

[1] Typical represents average readings at 25°C, V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V.
[4] Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.
[5] Guaranteed by design and not subject to production test.
[6] Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

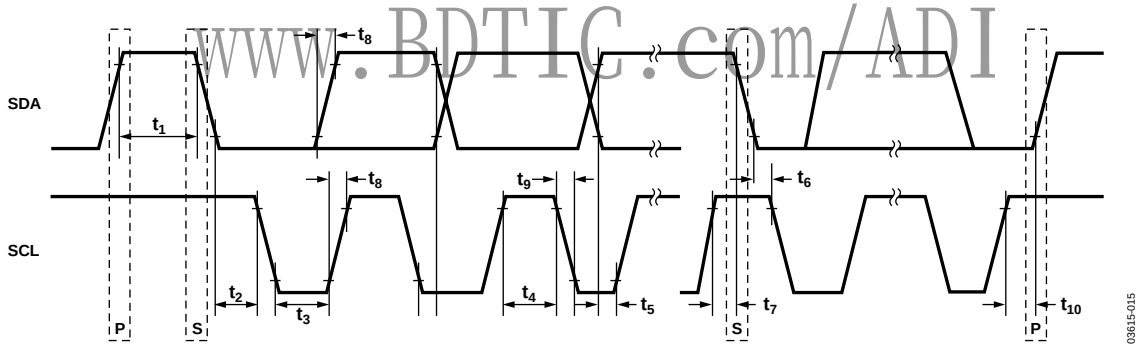


Figure 2. I²C Timing Diagram

ELECTRICAL CHARACTERISTICS

Single Supply: V_{DD} = 3 V to 5.5 V and −40°C < T_A < +85°C, unless otherwise noted.
Dual Supply: V_{DD} = +2.25 V or +2.75 V, V_{SS} = −2.25 V or −2.75 V, and −40°C < T_A < +85°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[2, 3]						
Bandwidth −3 dB	BW	V_{DD}/V_{SS} = ±2.5 V, R_{AB} = 25 kΩ/250 kΩ.		125/12		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz.		0.05		%
V_W Settling Time	t_S	$V_A = V_{DD}$, V_B = 0 V, V_W = 0.50% error band, code = 0x000 to 0x100, R_{AB} = 25 kΩ/250 kΩ.		4/36		µs
Resistor Noise Spectral Density	e_{N_WB}	R_{AB} = 25 kΩ/250 kΩ, T_A = 25°C.		14/45		nV√Hz
Digital Crosstalk	C_T	$V_A = V_{DD}$, V_B = 0 V, measure VW with adjacent RDAC making full-scale change.		−80		dB
Analog Crosstalk	C_{AT}	Signal input at A0 and measure output at W1, f = 1 kHz.		−72		dB
INTERFACE TIMING CHARACTERISTICS (Apply to All Parts)[4, 5]						
SCL Clock Frequency	f_{SCL}				400	kHz
t_{BUF} Bus Free Time between Stop and Start	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated.	600			ns
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6		50	µs
$t_{SU;STA}$ Setup Time for Start Condition	t_5		600			ns
$t_{HD;DAT}$ Data Hold Time	t_6				900	ns
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_R Rise Time of Both SDA and SCL Signals	t_8				300	ns
t_F Fall Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for Stop Condition	t_{10}		600			ns
EEMEM Data Storing Time	t_{EEMEM_STORE}			26		ms
EEMEM Data Restoring Time at Power-On	$t_{EEMEM\_RESTORE1}$			360		µs
EEMEM Data Restoring Time on Restore Command or Reset Operation	$t_{EEMEM\_RESTORE2}$			360		µs
EEMEM Data Rewritable Time	$t_{EEMEM\_REWRITE}$		540			µs
FLASH/EE MEMORY RELIABILITY						
Endurance[6]			100			kcycles
Data Retention[7]		55°C.		100		years

[1] Typical represents average readings at 25°C, V_{DD} = 5 V.
[2] All dynamic characteristics use V_{DD} = 5 V.
[3] Guaranteed by design and not subject to production test.
[4] Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.
[5] See Figure 2 for the location of measured values.
[6] Endurance is qualified to 100,000 cycles as per JEDEC Std. 22 Method A117 and measured at −40°C, +25°C, and +85°C. Typical endurance at 25°C is 700,000 cycles.
[7] Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V, +7 V
V_{SS} to GND	+0.3 V, −7 V
V_{DD} to V_{SS}	7 V
V_A, V_B, V_W to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
I_A, I_B, I_W	
Intermittent[1]	±20 mA
Continuous	±2 mA
Digital Inputs and Output Voltage to GND	−0.3 V, V_{DD} + 0.3 V
Operating Temperature Range[2]	−40°C to +85°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C
Thermal Resistance Junction-to-Ambient θ_{JA},	
LFCSP-24	32°C/W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] Includes programming of nonvolatile memory.
[2] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

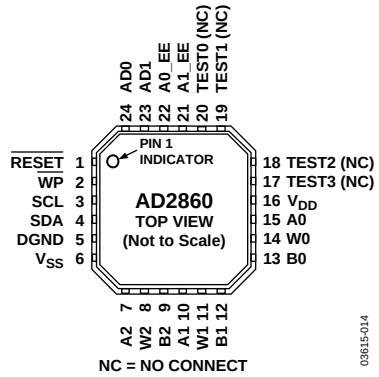


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Resets the scratchpad register with current contents of the EEMEM register. Factory defaults to midscale before any programming.
2	$\overline{\text{WP}}$	Write Protect. When active low, $\overline{\text{WP}}$ prevents any changes to the present register contents, except that $\overline{\text{RESET}}$ and Commands 1 and 8 still refresh the RDAC register from EEMEM.
3	SCL	Serial Input Register Clock. Shifts in one bit at a time upon the positive clock edges.
4	SDA	Serial Data Input. Shifts in one bit at a time upon the positive edges. The MSB is loaded first.
5	DGND	Ground. Logic ground reference.
6	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications.
7	A2	A Terminal of RDAC2.
8	W2	Wiper Terminal of RDAC2.
9	B2	B Terminal of RDAC2.
10	A1	A Terminal of RDAC1.
11	W1	Wiper Terminal of RDAC1.
12	B1	B Terminal of RDAC1.
13	B0	B Terminal of RDAC0.
14	W0	Wiper Terminal of RDAC0.
15	A0	A Terminal of RDAC0.
16	V_{DD}	Positive Power Supply.
17	TEST3	Test Pin 3. Do not connect.
18	TEST2	Test Pin 2. Do not connect.
19	TEST1	Test Pin 1. Do not connect.
20	TEST0	Test Pin 0. Do not connect.
21	A1_EE	I^2C Device Address 1 for EEMEM.
22	A0_EE	I^2C Device Address 0 for EEMEM.
23	AD1	I^2C Device Address 1 for RDAC.
24	AD0	I^2C Device Address 0 for RDAC.

TYPICAL PERFORMANCE CHARACTERISTICS

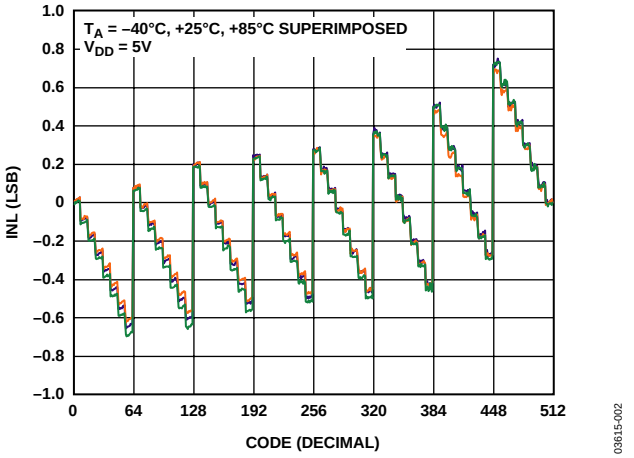


Figure 4. INL—9-Bit RDAC

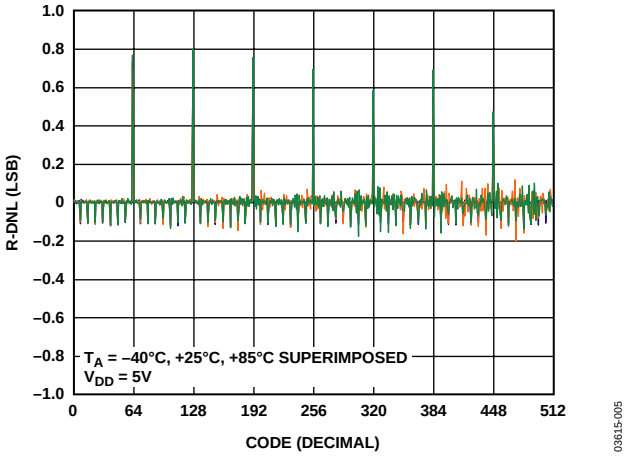


Figure 7. R-DNL—9-Bit RDAC

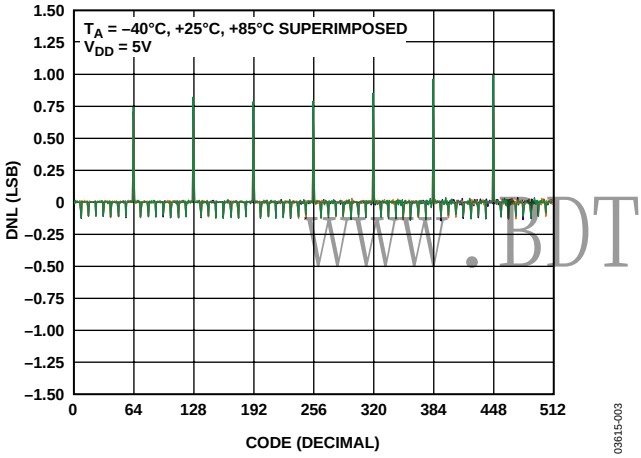


Figure 5. DNL—9-Bit RDAC

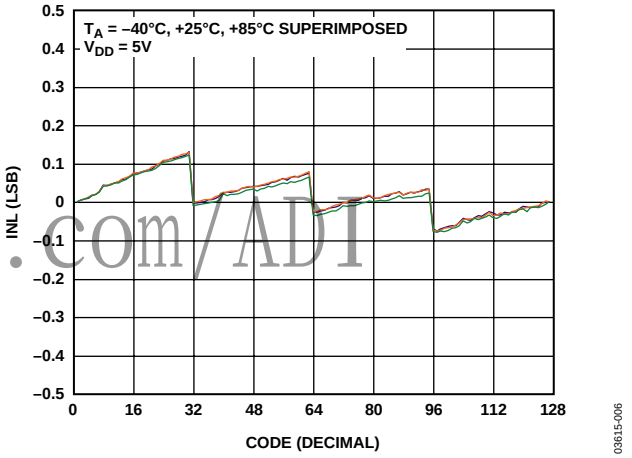


Figure 8. INL—7-Bit RDAC

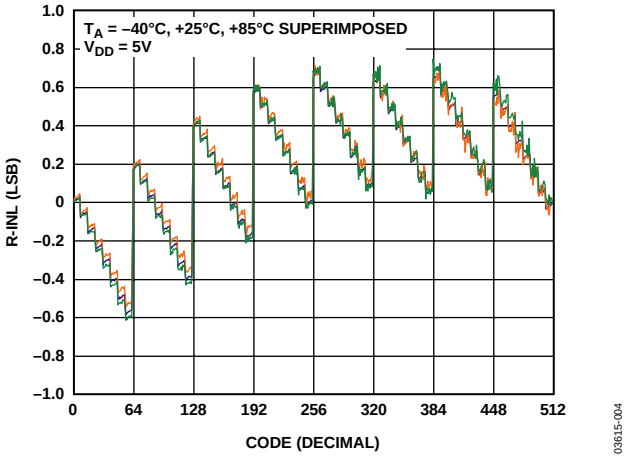


Figure 6. R-INL—9-Bit RDAC

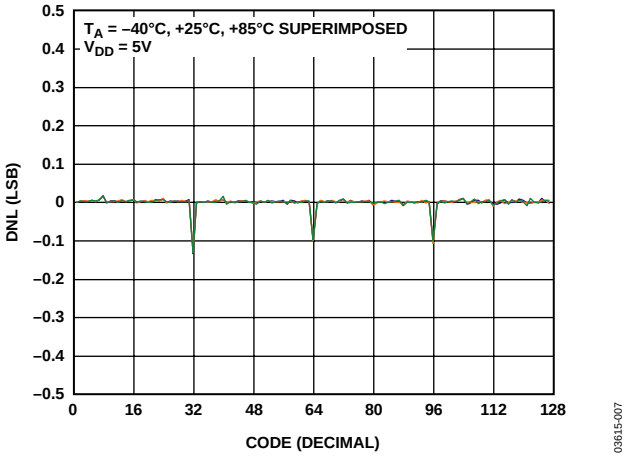


Figure 9. DNL—7-Bit RDAC

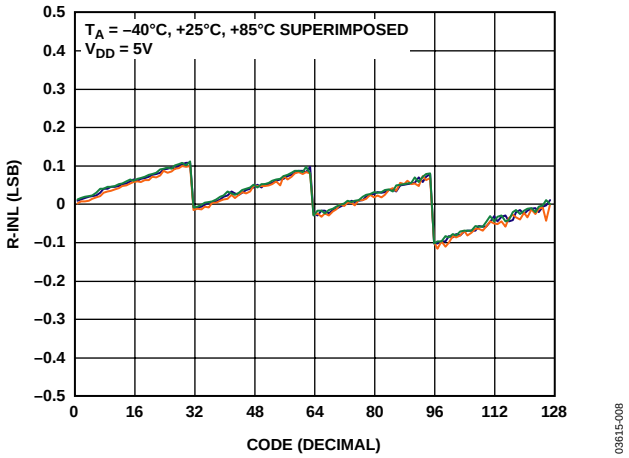


Figure 10. R-INL—7-Bit RDAC

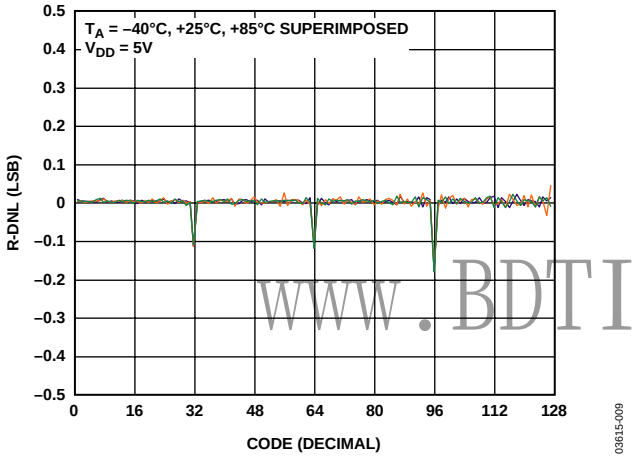


Figure 11. R-DNL—7-Bit RDAC

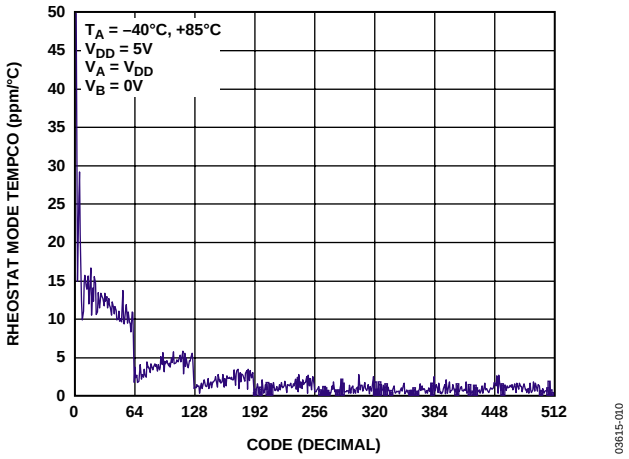


Figure 12. Temperature Coefficient (Rheostat Mode)

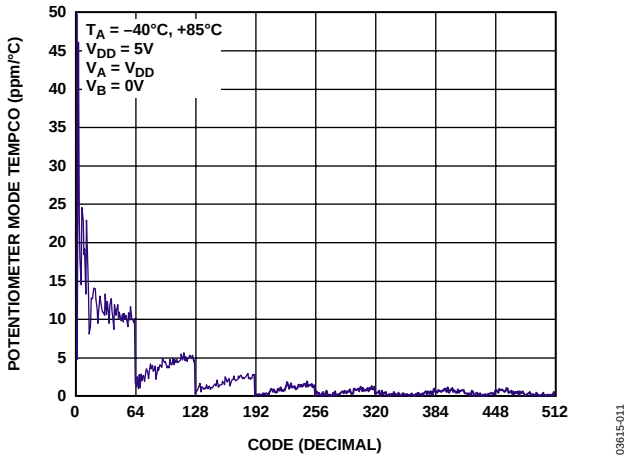


Figure 13. Temperature Coefficient (Potentiometer Mode)

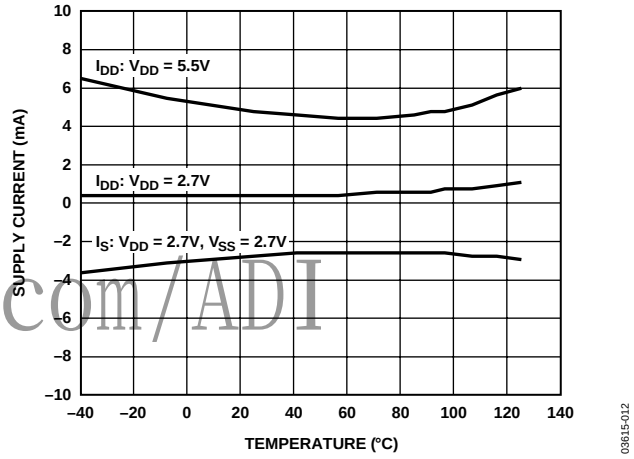


Figure 14. Supply Current vs. Temperature

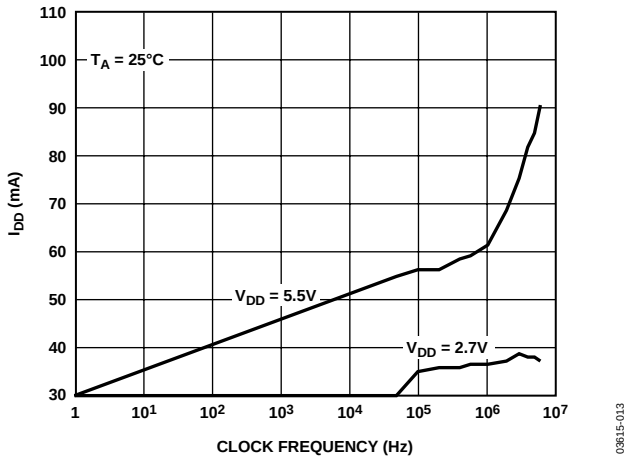


Figure 15. Supply Current vs. Clock Frequency

INTERFACE DESCRIPTIONS

I²C INTERFACE

All control and access to both EEPROM memory and the RDAC registers are conducted via a standard 2-wire I²C interface. Figure 2 shows the timing characteristics of the I²C bus. Figure 16 and Figure 17 illustrate standard transmit and receive bus signals in the I²C interface.

These figures use the following legend:

From master to slave

From slave to master

S = Start condition

P = Stop condition

A = Acknowledge (SDA low)

$\overline{A}$ = Not acknowledge (SDA high)

R/$\overline{W}$ = Read enable at high and write enable at low

Figure 16. I²C—Master Transmitting Data to Slave

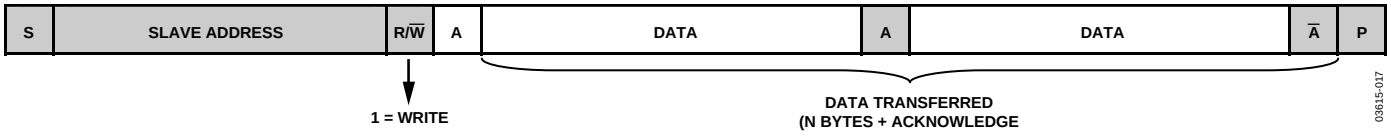


Figure 17. I²C—Master Reading Data from Slave

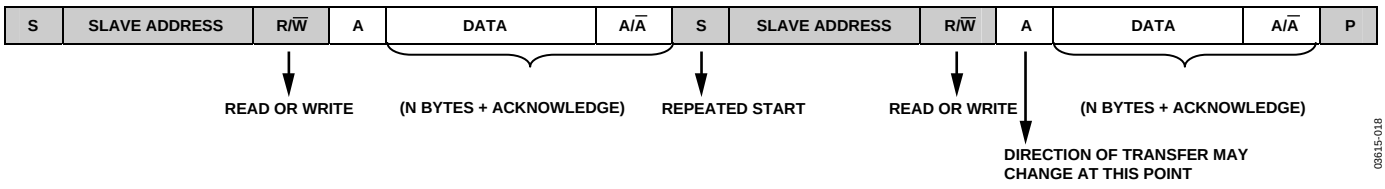


Figure 18. Combined Transmit/Read

EEPROM INTERFACE

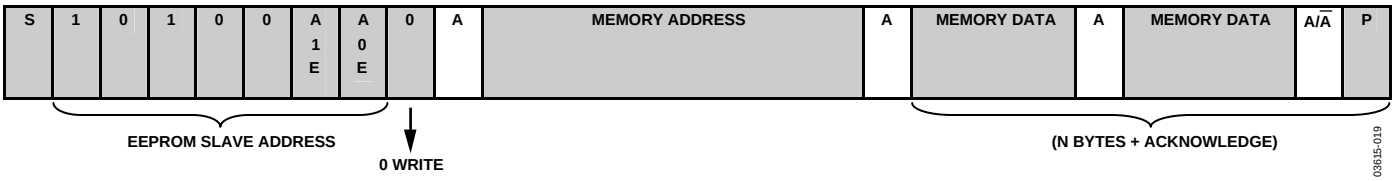


Figure 19. EEPROM Write

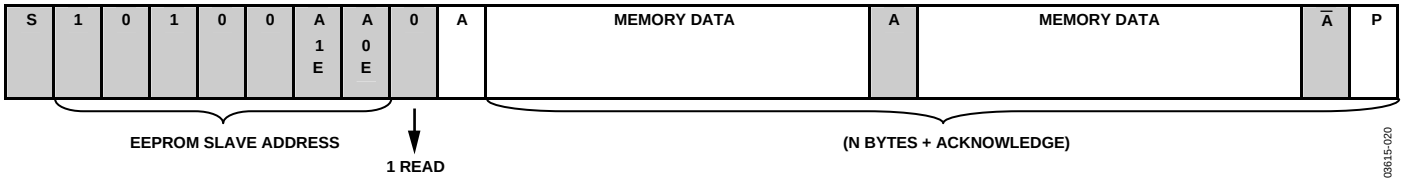


Figure 20. EEPROM Current Read

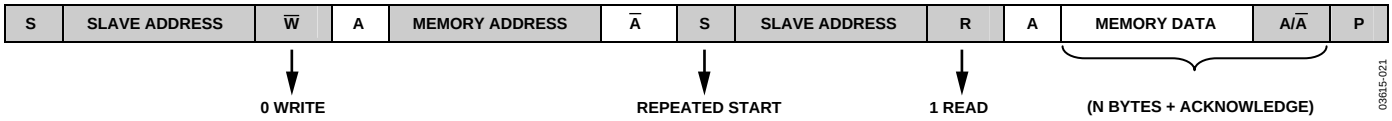


Figure 21. EEPROM Random Read

The 256 bytes of EEPROM memory provided in the ADN2860 are organized into 16 pages of 16 bytes each. The word size of each memory location is one byte wide.

The I²C slave address of the EEPROM is 10100(A1E)(A0E), where A1E and A0E are external pin-programmable address bits. The 2-pin programmable address bits allow a total of four ADN2860 devices to be controlled by a single I²C master bus, each having its own EEPROM.

An internal 8-bit address counter for the EEPROM is automatically incremented following each read or write operation. For read operations, the address counter is incremented after each byte is read, and the counter rolls over from Address 255 to 0.

For write operations, the address counter is incremented after each byte is written. The counter rolls over from the highest address of the current page to the lowest address of the current page. For example, writing two bytes beginning at Address 31 causes the counter to roll back to Address 16 after the first byte is written; then the address increments to 17 after the second byte is written.

EEPROM Write

Each write operation issued to the EEPROM programs between 1 byte and 16 bytes (one page) of memory. Figure 19 shows the EEPROM write interface. The number of bytes of data, N, that the user wants to send to the EEPROM is unrestricted. If more than 16 bytes of data are sent in a single write operation, the address counter rolls back to the beginning address, and the previously sent data is overwritten.

EEPROM Write-Acknowledge Polling

After each write operation, an internal EEPROM write cycle begins. During the EEPROM internal write cycle, the I²C interface of the device is disabled. It is necessary to determine if the internal write cycle is complete and whether the I²C interface is enabled. To do so, execute I²C interface polling by sending a start condition, followed by the EEPROM slave address plus the desired R/$\overline{W}$ bit. If the ADN2860 I²C interface responds with an ACK, the write cycle is complete and the interface is ready to proceed with further operations. Otherwise, the I²C interface must be polled again to determine whether the write cycle has been completed.

EEPROM Read

The ADN2860 EEPROM provides two different read operations, shown in Figure 20 and Figure 21. The number of bytes, N, read from the EEPROM in a single operation is unrestricted. If more than 256 bytes are read, the address counter rolls back to the start address, and data previously read is read again.

Figure 20 shows the EEPROM current read operation. This operation does not allow an address location to be specified, and reads data beginning at the current address location stored in the internal address counter.

A random read operation is shown in Figure 21. This operation changes the address counter to the specified memory address by performing a *dummy write* and then performing a read operation beginning at the new address counter location.

EEPROM Write Protection

Setting the $\overline{\text{WP}}$ pin to logic low protects the EEPROM memory from future write operations. In this mode, EEPROM read operations and RDAC register loading operate normally.

RDAC I²C INTERFACE

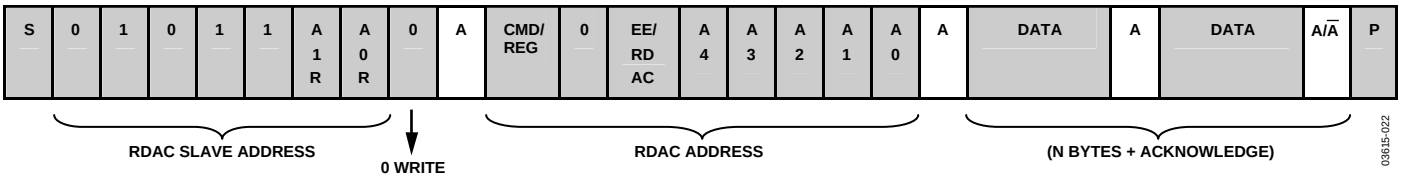


Figure 22. RDAC Write

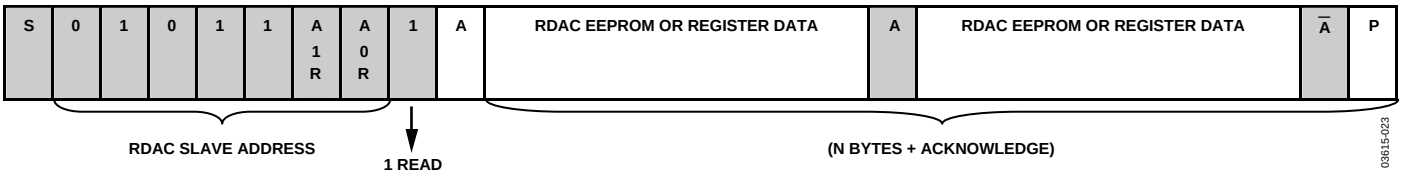


Figure 23. RDAC Current Read

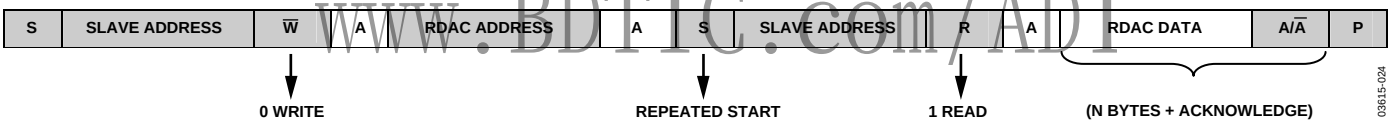


Figure 24. RDAC Random Read

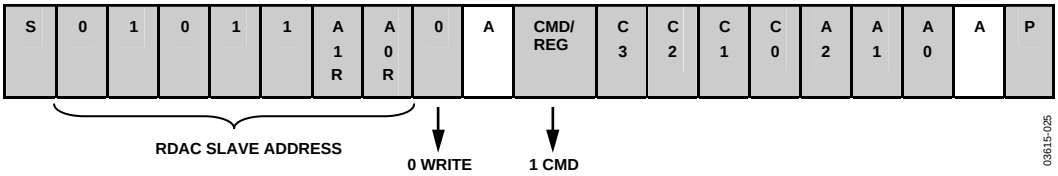


Figure 25. RDAC Shortcut Commands

Table 5. RDAC Register Addresses (CMD/$\overline{\text{REG}}$ = 0, EE/$\overline{\text{RDAC}}$ = 0)

A4	A3	A2	A1	A0	RDAC	Byte Description
0	0	0	0	0	RDAC0	(D7)(D6)(D5)(D4)(D3)(D2)(D1)(D0)—RDAC0 8 LSBs
0	0	0	0	1	RDAC0	(X)(X)(X)(X)(X)(X)(X)(D8)—RDAC0 MSB
0	0	0	1	0	RDAC1	(D7)(D6)(D5)(D4)(D3)(D2)(D1)(D0)—RDAC1 8 LSBs
0	0	0	1	1	RDAC1	(X)(X)(X)(X)(X)(X)(X)(D8)—RDAC1 MSB
0	0	1	0	0	RDAC2	(X)(D6)(D5)(D4)(D3)(D2)(D1)(D0)—RDAC2 7 bits
0	0	1	0	1		Reserved
		…to…				
1	1	1	1	1		

Table 6. RDAC R/$\overline{W}$ EEPROM Addresses (CMD/ $\overline{REG}$ = 0, EE/$\overline{RDAC}$ = 1)

A4	A3	A2	A1	A0	Byte Description
0	0	0	0	0	RDAC0 8 LSBs
0	0	0	0	1	RDAC0 MSB
0	0	0	1	0	RDAC1 8 LSBs
0	0	0	1	1	RDAC1 MSB
0	0	1	0	0	RDAC2 7 bits
0	0	1	0	1	11 bytes RDAC user EEPROM
		…to…			
0	1	1	1	1	

Table 7. RDAC Command Table (CMD/$\overline{REG}$ = 1)

C3	C2	C1	C0	Command Description
0	0	0	0	NOP.
0	0	0	1	Restore EEPROM to RDAC.[1]
0	0	1	0	Store RDAC to EEPROM.[2]
0	0	1	1	Decrement RDAC 6 dB.
0	1	0	0	Decrement all RDACs 6 dB.
0	1	0	1	Decrement RDAC one step.
0	1	1	0	Decrement all RDACs one step.
0	1	1	1	Reset. Restore EEPROM to all RDACs.[2]
1	0	0	0	Increment RDAC 6 dB.
1	0	0	1	Increment all RDACs 6 dB.
1	0	1	0	Increment RDAC one step.
1	0	1	1	Increment all RDACs one step.
1	1	0	0	Reserved.
	…to…			
1	1	1	1	

[1] Command leaves the device in the EEPROM read power state. Issue the NOP command to return the device to the idle state.
[2] Command requires acknowledge polling after execution.

RDAC Interface Operation

Each programmable resistor wiper setting is controlled by specific RDAC registers, as shown in Table 5. Each RDAC register corresponds to an EEPROM memory location, which provides nonvolatile wiper storage functionality.

RDAC registers and their corresponding EEPROM memory locations are programmed and read independently from each other. The RDAC register is refreshed by the EEPROM locations, either with a hardware reset via Pin 1, or by issuing one of the various RDAC register load commands shown in the Table 7.

RDAC Write

Setting the wiper position requires an RDAC write operation, shown in Figure 22. RDAC write operations follow a format similar to the EEPROM write interface. The only difference between an RDAC write and an EEPROM write operation is the use of an RDAC address byte in place of the memory address used in the EEPROM write operation. The RDAC address byte is described in detail in Table 5 and Table 6.

As with the EEPROM write operation, any RDAC EEPROM (Shortcut Command 2) write operation disables the I²C interface during the internal write cycle. Acknowledge polling, as described in the EEPROM Interface section, is required to determine whether the write cycle is complete.

RDAC Read

The ADN2860 provides two RDAC read operations. The first, shown in Figure 23, reads the contents of the current RDAC address counter. Figure 24 illustrates the second read operation, which allows users to specify which RDAC register to read by first issuing a dummy write command to change the RDAC address pointer, and then proceeding with the RDAC read operation at the new address location.

The read-only RDAC EEPROM memory locations can also be read by using the address and bits specified in Table 6.

RDAC Shortcut Commands

Eleven shortcut commands are provided for easy manipulation of RDAC registers and their corresponding EEPROM memory locations. These commands are shown in Table 9. A more detailed discussion about the RDAC shortcut commands can be found in the Theory of Operation section.

The interface for issuing an RDAC shortcut command is shown in Figure 25. All shortcut commands require acknowledge polling to determine whether the command has finished executing.

RDAC Resistor Tolerance

The end-to-end resistance tolerance for each RDAC channel is stored in read-only memory during factory production. This information is read by using the address and bits specified in Table 8.

Tolerance values are stored in percentage form. Figure 26 shows the format of the tolerance data stored in memory. Each stored tolerance uses two memory locations. The first location stores the integer portion, while the second location stores the decimal portion.

The resistance tolerance is stored in sign-magnitude format. The MSB of the first memory location designates the sign (0 = +, 1 = −) and the remaining 7 LSBs are designated for the integer portion of the tolerance. All eight bits of the second memory location are represented by the decimal portion of the tolerance value.

Table 8. Addresses for Reading Tolerance (CMD/$\overline{\text{REG}}$ = 0, EE/$\overline{\text{RDAC}}$ = 1, A4 = 1)

A4	A3	A2	A1	A0	Data Byte Description
1	1	0	0	0	Sign and 7-bit integer values of RDAC0 tolerance (read only)
1	1	0	0	1	8-bit decimal value of RDAC0 tolerance (read only)
1	1	0	1	0	Sign and 7-bit integer values of RDAC1 tolerance (read only)
1	1	0	1	1	8-bit decimal value of RDAC1 tolerance (read only)
1	1	1	0	0	Sign and 7-bit integer values of RDAC2 tolerance (read only)
1	1	1	0	1	8-bit decimal value of RDAC2 tolerance (read only)

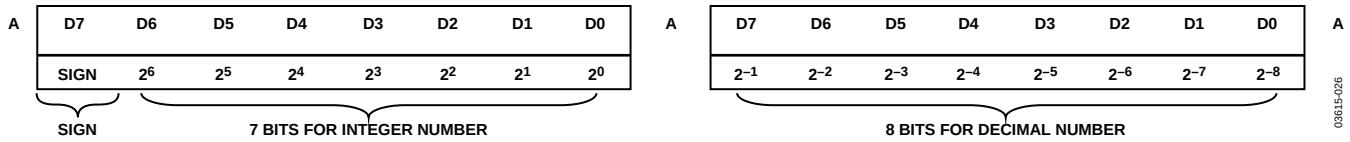


Figure 26. Format of Stored Tolerance in Sign Magnitude with Bit Position Descriptions (Unit is in %, Only Data Bytes Shown)

THEORY OF OPERATION

The ADN2860 digital potentiometer operates as a true variable resistor. The RDAC register contents determine the resistor wiper position. The RDAC register acts like a scratchpad register, allowing unlimited resistance setting changes. RDAC register contents are changed using the ADN2860's serial I²C interface. See the RDAC I2C Interface section for the format of the data words and commands to program the RDAC registers.

Each RDAC register has a corresponding EEPROM memory location, which provides nonvolatile storage of resistor wiper position settings. The ADN2860 provides commands to store the RDAC register contents to their respective EEPROM memory locations. During subsequent power-on sequences, the RDAC registers are automatically loaded with the stored values.

Saving data from an RDAC register to EEPROM memory takes approximately 25 ms and consumes 35 mA.

In addition to moving data between RDAC registers and EEPROM memory, the ADN2860 provides other shortcut commands.

Table 9. ADN2860 Shortcut Commands

No.	Function
1	Restore EEPROM setting to RDAC[1]
2	Store RDAC register contents to EEPROM[2]
3	Decrement RDAC 6 dB (shift data bits right)
4	Decrement all RDACs 6 dB (shift all data bits right)
5	Decrement RDAC one step
6	Decrement all RDACs one step
7	Reset EEPROM setting to RDAC[2]
8	Increment RDAC 6 dB (shift data bits left)
9	Increment all RDACs 6 dB (shift all data bits left)
10	Increment RDAC one step
11	Increment all RDACs one step

[1] Command leaves the device in the EEPROM read power state. Issue the NOP command to return the device to the idle state.
[2] Command requires acknowledge polling after execution.

LINEAR INCREMENT AND DECREMENT COMMANDS

The increment and decrement commands (Commands 10, 11, 5, and 6) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to send only an increment or decrement command to the ADN2860. The adjustment can be directed to an individual RDAC or to all three RDACs.

LOGARITHMIC TAPER MODE ADJUSTMENT (±6 dB/STEP)

The ADN2860 accommodates logarithmic taper adjustment of the RDAC wiper position(s) by shifting the register contents left/right for increment/decrement operations. Commands 8, 9, 3, and 4 are used to logarithmically increment or decrement the wiper positions individually or change all three channel settings at the same time.

Incrementing the wiper position by +6 dB doubles the RDAC register value, whereas decrementing by −6 dB halves it. Internally, the ADN2860 uses a shift register to shift the bits left and right to achieve a logarithmic increment or decrement.

Nonideal ±6 dB step adjustment occurs under certain conditions. Table 10 illustrates how the shifting function affects the data bits of an individual RDAC. Each row going down the table represents a successive shift operation. Note that the left-shift commands (Commands 10 and 11) were modified such that if the data in the RDAC register equals 0 and the data is shifted, the RDAC register is set to Code 1. Similarly, if the data in the RDAC register is greater than or equal to midscale and the data is left shifted, the data in the RDAC register is automatically set to full scale. This makes the left-shift function as close as possible to a logarithmic adjustment.

The right-shift commands (Commands 3 and 4) are ideal only if the LSB is a 0 (ideal logarithmic = no error). If the LSB is 1, the right-shift function generates a linear half LSB error.

Table 10. RDAC Register Contents after ±6 dB Step Adjustments

Left Shift (+6 dB/Step)	Right Shift (−6 dB/Step)
0 0000 0000	1 1111 1111
0 0000 0001	0 1111 1111
0 0000 0010	0 0111 1111
0 0000 0100	0 0011 1111
0 0000 1000	0 0001 1111
0 0001 0000	0 0000 1111
0 0010 0000	0 0000 0111
0 0100 0000	0 0000 0011
0 1000 0000	0 0000 0001
1 0000 0000	0 0000 0000
1 1111 1111	0 0000 0000
1 1111 1111	

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each right-shift command (Commands 3 and 4) execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. Figure 26 shows a plot of Log_Error, that is, 20 × Log10(error/code), for the ADN2860.

USING ADDITIONAL INTERNAL NONVOLATILE EEPROM

The ADN2860 contains additional internal user EEPROM for saving constants and other data. The user EEPROM I²C data-word follows the same format as the general-purpose EEPROM memory shown in Figure 19 and Figure 20. User EEPROM memory addresses are shown in Table 6.

To support the use of multiple EEPROM modules on a single I²C bus, the ADN2860 features two external addressing pins, Pins 21 and 22 (A1_EE and A0_EE), to manually set the address of the EEPROM included with the ADN2860. This feature ensures that the correct EEPROM memory is accessed when using multiple memory modules on a single I²C bus.

DIGITAL INPUT/OUTPUT CONFIGURATION

All digital inputs are ESD protected. Digital inputs are high impedance and can be driven directly from most digital sources. The $\overline{\text{RESET}}$ digital input pin does not have an internal pull-up resistor. Therefore, the user should place a pull-up resistor from $\overline{\text{RESET}}$ to V_{DD} if the function is not used. The $\overline{\text{WP}}$ pin has an internal pull-down resistor. If not driven by an external source, the ADN2860 defaults to a write-protected state. ESD protection of the digital inputs is shown in Figure 27.

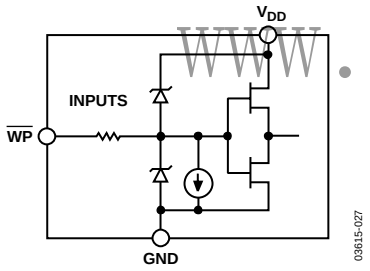


Figure 27. Equivalent $\overline{WP}$ ESD Protection

MULTIPLE DEVICES ON ONE BUS

Figure 28 shows four ADN2860 devices on the same serial bus. Each has a different slave address because the state of their AD0 and AD1 pins are different. This allows independent reading and writing to each RDAC within each device.

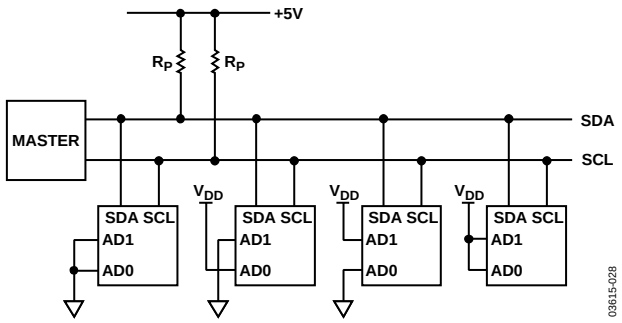


Figure 28. Multiple ADN2860 Devices on a Single Bus

LEVEL SHIFT FOR BIDIRECTIONAL COMMUNICATION

While most legacy systems operate at one voltage, adding a new component might require a different voltage. When two systems transmit the same signal at two different voltages, use a level shifter to allow the systems to communicate.

For example, a 3.3 V microcontroller (MCU) can be used along with a 5 V digital potentiometer. A level shifter is required to enable bidirectional communication.

Figure 29 shows one of many possible techniques to properly level-shift signals between two devices. M1 and M2 are N-channel FETs (2N7002). If V_{DD} falls below 2.5 V, use low threshold N-channel FETs (FDV301N) for M1 and M2.

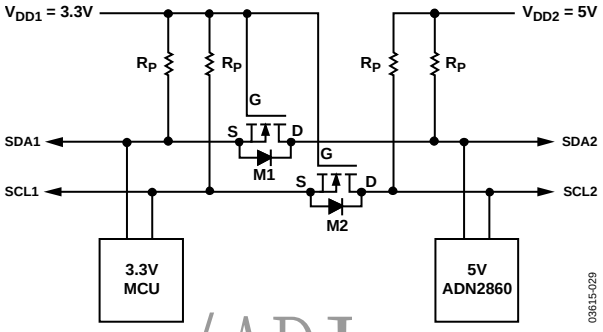


Figure 29. Level Shifting for Different Voltage Devices on an I²C Bus

TERMINAL VOLTAGE OPERATION RANGE

The ADN2860 positive V_{DD} and negative V_{SS} power supply inputs define the boundary conditions for proper 2-terminal programmable resistance operation. Supply signals on Terminals W and B that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes of the ADN2860.

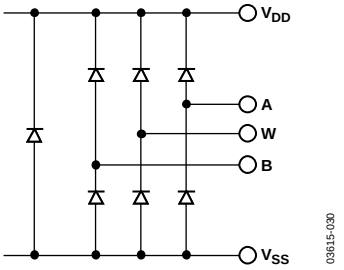


Figure 30. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the ADN2860 is used as a digital ground reference and needs to be tied to the common ground of the PCB. Reference the digital input control signals to the ADN2860 ground pin and satisfy the logic levels defined in Table 1 and Table 2.

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at the A, B, and W terminals (Figure 30), it is important to power V_{DD}/V_{SS} before applying voltage to the A, B, and W terminals. Otherwise, the diode is forward biased such that V_{DD}/V_{SS} are powered unintentionally, which affects the rest of the circuit. The ideal power-up sequence is as follows: GND, V_{DD}, V_{SS}, digital inputs, and $V_{A/B/W}$. The order of powering V_A, V_B, V_W, and the digital inputs is not important, as long as they are powered after V_{DD}/V_{SS}.

LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to use compact, minimum-lead-length layout design. Make the leads to the input as direct as possible with a minimum conductor length. Make sure that ground paths have low resistance and low inductance.

It is also a good practice to bypass the power supplies with quality capacitors. Use low equivalent series resistance (ESR) 1 µF to 10 µF tantalum or electrolytic capacitors at the supplies to minimize any transient disturbance and filter low frequency ripple. Figure 31 illustrates the basic supply-bypassing configuration for the ADN2860.

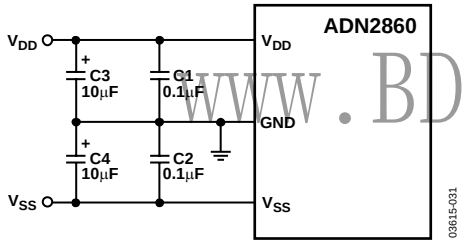


Figure 31. Power Supply Bypassing

Solder the slug on the bottom of the LFCSP package to a floating pad to improve thermal dissipation. Do not connect the slug to a ground plane on the PCB.

RDAC STRUCTURE

The patent pending RDAC contains a string of equal resistor segments with an array of analog switches. The switches together act as the wiper connection.

The ADN2860 has two RDACs with 512 connection points, allowing it to provide better than 0.2% progammability resolution. The ADN2860 also contains a third RDAC with 128-step resolution.

Figure 32 shows an equivalent structure of the connections between the two terminals that make up one channel of an RDAC. The SW_B switch is always on, while one of switches SW(0) to SW($2^N - 1$) may or may not be on at any given time, depending on the resistance position decoded from the data bits in the RDAC register.

Since the switches are nonideal, there is a 100 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature; lower supply voltages and higher temperatures result in higher wiper resistances. Consideration of wiper resistance dynamics is important in applications in which accurate prediction of output resistance is required.

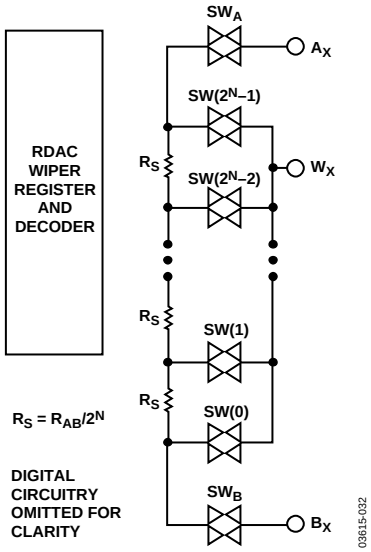


Figure 32. Equivalent RDAC Structure

CALCULATING THE PROGRAMMABLE RESISTANCE

The nominal resistance of the RDAC between the A and B terminals is available in 25 kΩ or 250 kΩ. The final two or three digits of the part number determine the nominal resistance value, for example, 25 kΩ = 25 and 250 kΩ = 250.

The following discussion describes the calculation of resistance $R_{WB}(d)$ at different codes of a 25 kΩ part for RDAC0. The 9-bit data-word in the RDAC latch is decoded to select one of the 512 possible settings.

The first wiper connection starts at the B terminal for data 0x000. $R_{WB}(0)$ is 100 Ω of the wiper resistance and is independent of the full-scale resistance. The second connection is the first tap point where $R_{WB}(1)$ becomes 48.8 Ω + 100 = 148.8 Ω for data 0x001. The third connection is the next tap point representing $R_{WB}(2)$ = 97.6 + 100 = 197.6 Ω for data 0x002, and so on. Each LSB data-value increase moves the wiper up the resistor ladder until the last tap point is reached at $R_{WB}(511)$ = 25,051 Ω. See Figure 32 for a simplified diagram of the equivalent RDAC circuit.

These general equations determine the programmed output resistance between terminals W and B.

For RDAC0 and RDAC1:

$$R_{WB}(D) = \frac{D}{512} \times R_{AB} + R_W \quad (1)$$

For RDAC2:

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + R_W \quad (2)$$

where:
D is the decimal equivalent of the data contained in the RDAC register.
R_W is the wiper resistance.

The output resistance values in Table 11 are set for the given RDAC latch codes with V_{DD} = 5 V, which applies to R_{AB} = 25 kΩ digital potentiometers.

Table 11. R_{WB} at Selected Codes for R_{WB_FS} = 25 kΩ

D (DEC)	R_{WB}(d) (Ω)	Output State
511	25051	Full scale
256	12600	Midscale
1	148.8	1 LSB
0	100	Zero scale (wiper contact resistance)

Note that in the zero-scale condition, a finite wiper resistance of 100 Ω is present. To avoid degradation or possible destruction of the internal switches, care should be taken to limit the current flow between Terminals W and B to no more than 20 mA intermittently or 2 mA continuously.

Channel-to-channel R_{WB} matching is better than 0.1%. The change in R_{WB} with temperature has a 35 ppm/°C temperature coefficient.

Like the mechanical potentiometer that the RDAC replaces, the ADN2860 parts are totally symmetrical. The resistance between the W wiper and the A terminal also produces a digitally controlled complementary resistance, R_{WA}. When R_{WA} is used, the B terminal can be floating or tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general transfer equations for this operation are as follows:

For RDAC0 and RDAC1:

$$R_{WB}(D) = \frac{512 - D}{512} \times R_{AB} + R_W \quad (3)$$

For RDAC2:

$$R_{WB}(D) = \frac{128 - D}{128} \times R_{AB} + R_W \quad (4)$$

For example, the following RDAC latch codes set the corresponding output resistance values, which apply to R_{AB} = 25 kΩ digital potentiometers.

Table 12. R_{WA}(d) at Selected Codes for R_{AB} = 25 kΩ

D (DEC)	R_{WA}(d) (Ω)	Output State
511	148.8	Full scale
256	12600	Midscale
1	25051	1 LSB
0	25100	Zero scale

The typical distribution of R_{AB} from channel to channel is ±0.1% within the same package. Device-to-device matching is lot dependent, with a worst-case variation of ±15%. R_{AB} temperature coefficient is 35 ppm/°C.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer can be configured to generate an output voltage at the wiper terminal, which is proportional to the input voltages applied to the A and B terminals. Connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper that can vary between 0 V to 5 V. Each LSB of voltage is equal to the voltage applied across the A and B terminals divided by the 2^N position resolution of the potentiometer divider.

Since the ADN2860 can operate from dual supplies, the general equations defining the output voltage at V_W with respect to ground for any given input voltages applied to the A and B terminals are as follows:

For RDAC0 and RDAC1:

$$V_W(D) = \frac{D}{512} \times V_{AB} + V_B \quad (5)$$

For RDAC2:

$$V_W(D) = \frac{D}{128} \times V_{AB} + V_B \quad (6)$$

Equation 5 assumes that V_W is buffered to null the effect of wiper resistance. Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. In this mode, the output voltage is dependent on the ratio of the internal resistors, not on the absolute value; therefore, the drift improves to 15 ppm/°C. There is no voltage polarity restriction between the A, B, and W terminals as long as the terminal voltage (V_{TERM}) stays within $V_{SS} < V_{TERM} < V_{DD}$.

APPLICATIONS

LASER DIODE DRIVER (LDD) CALIBRATION

The ADN2860 can be used with any laser diode driver. Its high resolution, compact footprint, and superior temperature drift characteristics make it ideal for optical parameter setting.

The ADN2841 is a 2.7 Gbps laser diode driver that uses a unique control algorithm to manage both the laser average power and extinction ratio after initial factory calibration. It stabilizes the laser data transmission by continuously monitoring its optical power and by correcting the variations caused by temperature and the laser degradation over time. In the ADN2841, the I_{MPD} monitors the laser diode current. Through its dual-loop power and extinction ratio control, calibrated by the ADN2860, the internal driver controls the bias current, I_{BIAS}, and, consequently, the average power. It also regulates the modulation current, I_{MODP}, by changing the modulation current linearly with slope efficiency. Any changes in the laser threshold current or slope efficiency are, therefore, compensated. As a result, this optical supervisory system minimizes the laser characterization efforts, enabling designers to apply comparable lasers from multiple sources.

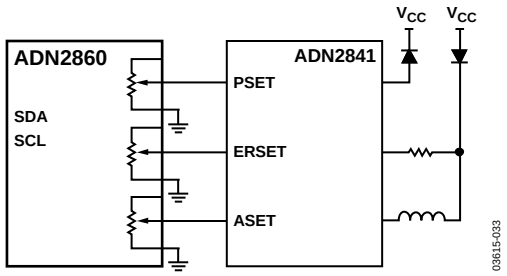
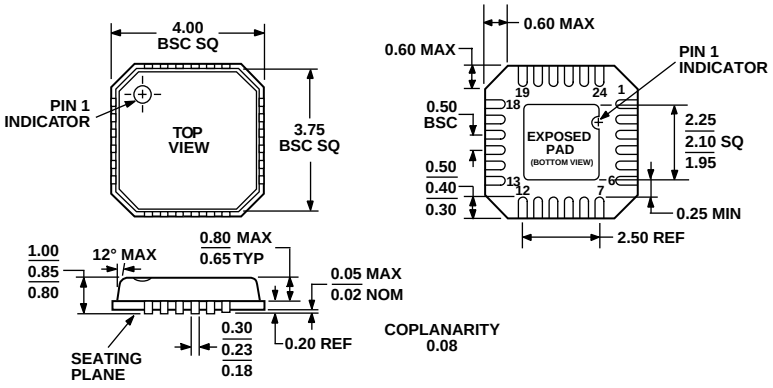


Figure 33. Optical Supervisory System

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2

Figure 34. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body
(CP-24-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Full Container Quantity	R_{AB} (kΩ)
ADN2860ACPZ25-RL7[1]	−40°C to +85°C	Lead Frame Chip Scale Package	CP-24-1	1,500	25
ADN2860ACPZ250-RL7[1]	−40°C to +85°C	Lead Frame Chip Scale Package	CP-24-1	1,500	250
ADN2860-EVAL		Evaluation Board			

[1] Z = Pb-free part.