500 mA PWM Step-Down DC-DC with Synchronous Rectifier

ADP3051

FEATURES

Current mode control for simple loop compensation
Input voltage range: 2.7 V to 5.5 V
Output voltage range: 0.8 V to 5.5 V
Tri-Mode™ operation for high efficiency
550 kHz PWM operating frequency
High accuracy over line, load, and temperature
Micropower shutdown mode
Space-saving MSOP-8 package

APPLICATIONS

Li-ion powered handhelds
MP3 players
PDAs and palmtops
Consumer electronics

GENERAL DESCRIPTION

The ADP3051 is a low noise, current mode, pulse width modulator (PWM) step-down converter capable of supplying over 500 mA to output voltages as low as 0.8 V. This device integrates a low resistance power switch and synchronous rectifier, providing excellent efficiency over the entire output voltage range and eliminating the need for a large and costly external Schottky rectifier. Its 550 kHz switching frequency permits the use of small external components.

Current mode control and external compensation allow the regulator to be easily optimized for a wide range of operating conditions. The ADP3051 operates at a constant 550 kHz frequency at medium to heavy loads; it smoothly transitions into Tri-Mode operation to save power at light loads. A pin-controlled micropower shutdown mode is also included.

The ADP3051's 2.7 V to 5.5 V input operating range makes it ideal for both battery-powered applications as well as those with 3.3 V or 5 V supply buses. It is available in a space-saving, 8-lead MSOP package.

TYPICAL APPLICATION CIRCUIT

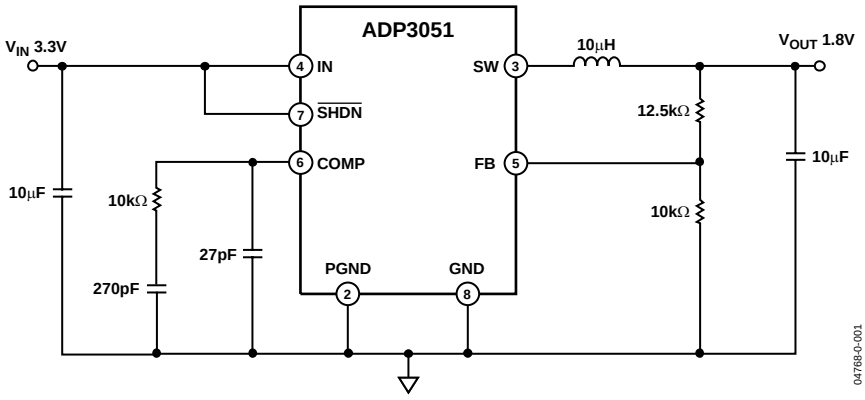

Figure 1.

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REVISION HISTORY

6/04—Revision 0: Initial Version

SPECIFICATIONS[1]

V_{IN} = 3.6 V @ T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY					
Input Voltage Range		2.7		5.5	V
Quiescent Supply Current	V_{FB} = 1.0 V		180	300	µA
Shutdown Supply Current	$\overline{SHDN}$ = 0 V		10	25	µA
PWM COMPARATOR					
Minimum Duty Ratio			0		%
Maximum Duty Ratio			100		%
OSCILLATOR					
Oscillator Frequency	$V_{COMP} \geq$ 1.5 V, V_{OUT} = 0.7 V	410	550	690	kHz
Foldback Frequency	V_{OUT} < 0.3 V		200		kHz
OUTPUT STAGE					
On Resistance, N Channel	I_{SW} = 150 mA		150		mΩ
Switch Leakage Current, N Channel	V_{IN} = 5.0 V, V_{SW} = 0 V		1		µA
On Resistance, P Channel	FB = GND		190		mΩ
Switch Leakage Current, P Channel	V_{SW} = 5.0 V		1		µA
Current Limit Threshold		680	1000	1320	mA
ERROR AMPLIFIER					
Feedback Regulation Voltage	T_A = 25°C	783	800	821	mV
		770		830	mV
Feedback Input Bias Current			5		nA
Current Sense Gain			2.9		Ω
Transconductance			0.32		mS
Maximum Sink Current			33		µA
Maximum Source Current			33		µA
UNDERVOLTAGE LOCKOUT					
Undervoltage Lockout Threshold	V_{IN} rising	1.9		2.6	V
Undervoltage Lockout Hysteresis			55		mV
$\overline{SHDN}$ INPUT THRESHOLD VOLTAGES					
Input High Threshold Voltage	Referenced to IN			−0.5	V
Input Low Threshold Voltage		0.4			V

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN, $\overline{SHDN}$, COMP, SW, FB to GND	–0.3 V to +6 V
SW to IN	–6 V to +0.3 V
PGND to GND	–0.3 V to +0.3 V
Operating Ambient Temperature	–40°C to +85°C
Operating Junction Temperature	–40°C to +125°C
Storage Temperature	–65°C to +150°C
θ_{JA}, 2-Layer (SEMI standard board)	159°C/W
θ_{JA}, 4-Layer (JEDEC standard board)	116°C/W
Lead Temperature Range	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

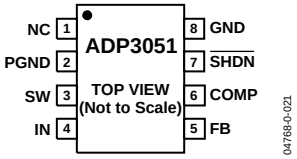


Figure 2. 8-Lead MSOP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. Not internally connected.
2	PGND	Power Ground. Connect PGND to GND at a single point. Use separate power ground and quiet ground planes for the power and sensitive analog circuitry, respectively. See the Circuit Board Layout Considerations section.
3	SW	Switching Output. SW connects to the drain of the internal power switch and synchronous rectifier. Connect the output inductor between SW and the load.
4	IN	Power Source Input. IN is the source of the high side P-channel MOSFET switch, and supplies the internal power to the ADP3051. Bypass IN to GND with a 0.1 µF or greater ceramic capacitor, placed as close as possible to IN.
5	FB	Feedback Voltage Sense Input. FB senses the output voltage. To set the output voltage, connect a resistive voltage divider from the output voltage to FB. The feedback threshold is 0.8 V. See the Setting the Output Voltage section.
6	COMP	Feedback Loop Compensation Node. COMP is the output of the internal transconductance error amplifier. Place a series RC network from COMP to GND to compensate the regulator. See the Compensation Design section.
7	$\overline{\text{SHDN}}$	Shutdown Input. Drive $\overline{\text{SHDN}}$ low to turn off the ADP3051; drive $\overline{\text{SHDN}}$ to within 0.5 V of V_{IN} to turn on the ADP3051. See the Shutdown section.
8	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, V_{OUT} = 3.3V, circuit of Figure 20, component values of Table 4, T_A = 25°C, unless otherwise specified.

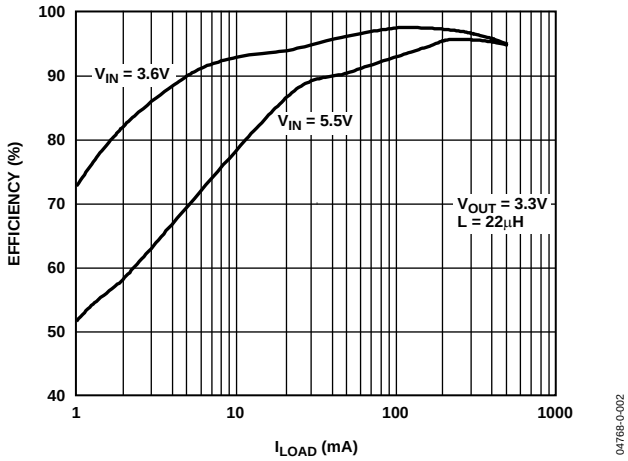


Figure 3. Output Efficiency vs. Load Current, V_{OUT} = 3.3 V

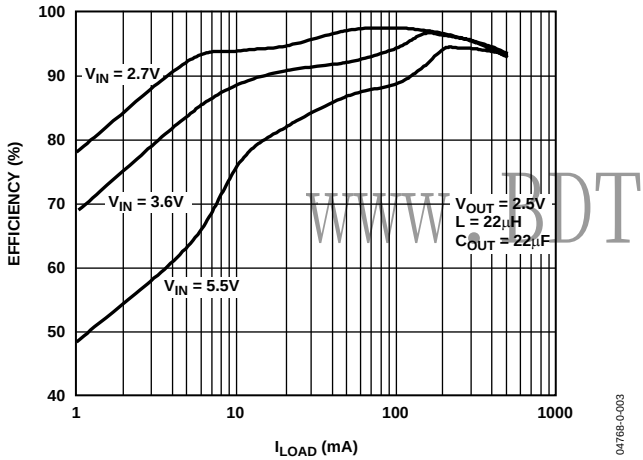


Figure 4. Output Efficiency vs. Load Current, V_{OUT} = 2.5 V

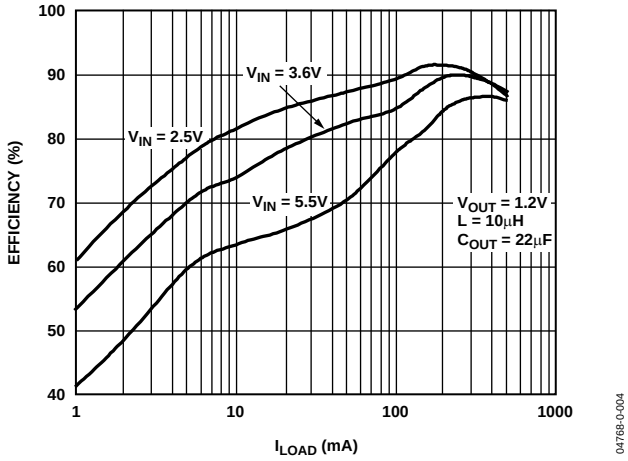


Figure 5. Output Efficiency vs. Load Current, V_{OUT} = 1.2 V

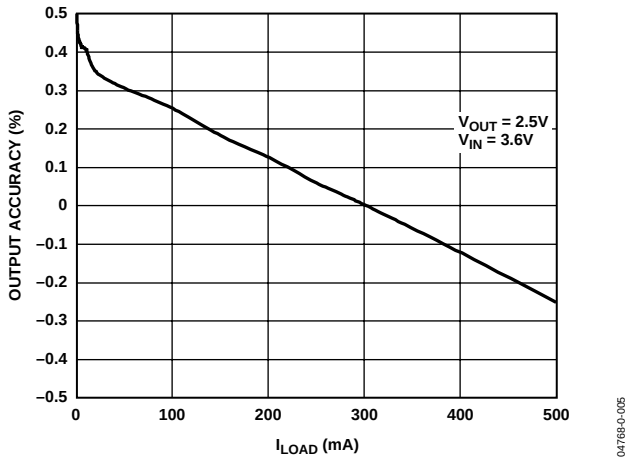


Figure 6. Output Voltage Error vs. Load Current

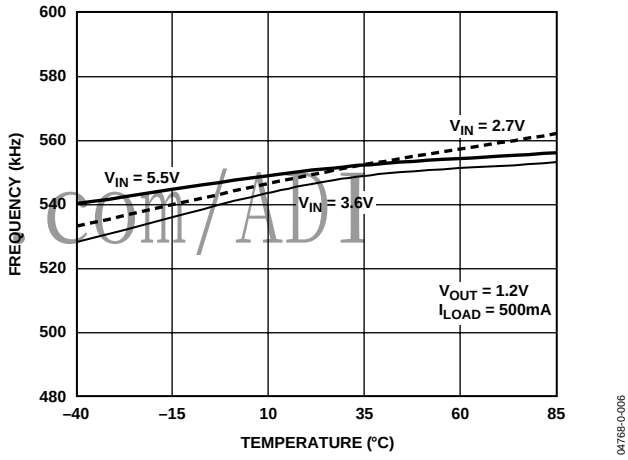


Figure 7. Oscillator Frequency vs. Temperature

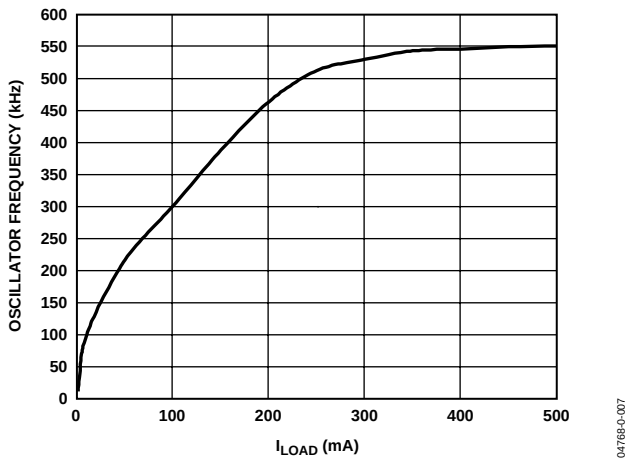
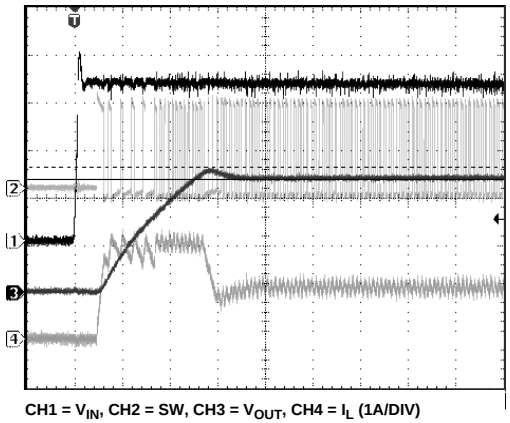
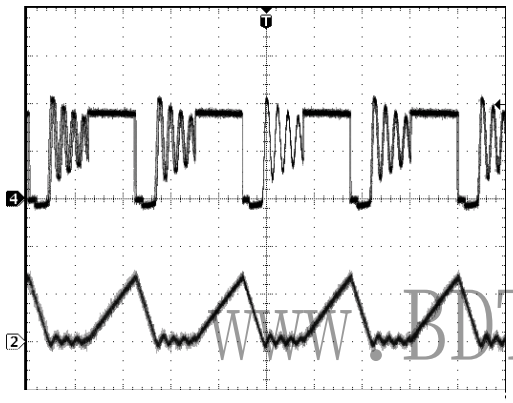


Figure 8. Oscillator Frequency vs. Load Current, V_{IN} = 3.6 V, V_{OUT} = 1.2 V



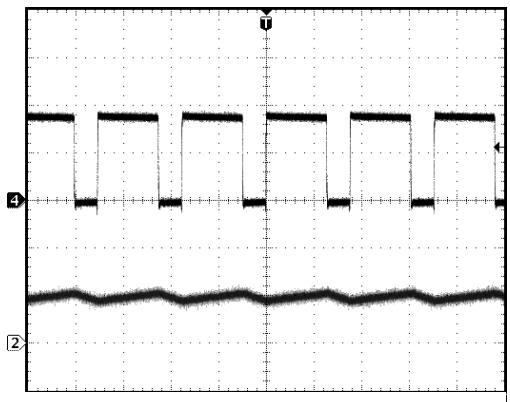
CH1 = V_{IN}, CH2 = SW, CH3 = V_{OUT}, CH4 = I_L (1A/DIV)
V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{LOAD} = 500mA

Figure 9. Start-Up Behavior



CH2 = I_L (100mA/DIV), CH4 = SW
V_{IN} = 3.6V, V_{OUT} = 2.5V, L = 22µH, I_{OUT} = 50mA

Figure 10. Light Load Switching Waveforms

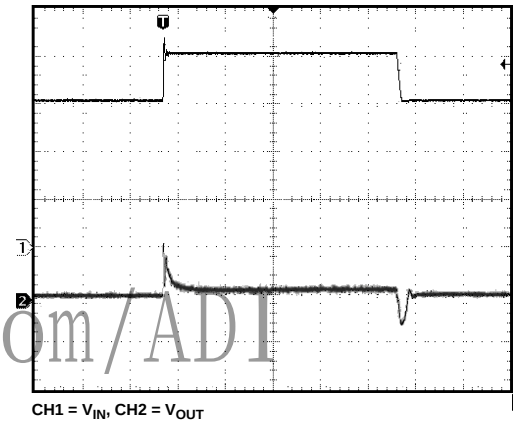


CH2 = I_L (500mA/DIV), CH4 = SW
V_{IN} = 3.6V, V_{OUT} = 2.5V, L = 22µH, I_{OUT} = 500mA

Figure 11. Heavy Load Switching Waveforms

CH1 = COMP, CH3 = V_{OUT}, CH4 = I_{LOAD} (50mA TO 490mA)
V_{IN} = 3.6V, V_{OUT} = 2.5V, C_{OUT} = 22µF, C_C = 150pF, R_C = 100kΩ

Figure 12. Load Transient Response



CH1 = V_{IN}, CH2 = V_{OUT}
V_{IN} = 3V TO 4V, V_{OUT} = 2.5V, I_{LOAD} = 500mA

Figure 13. Line Transient Response

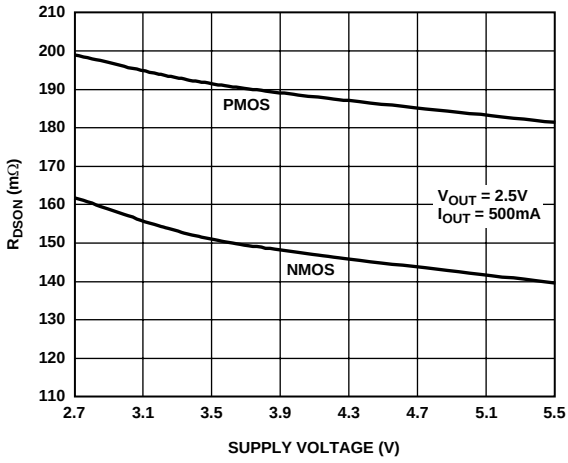


Figure 14. Switch On Resistance vs. Input Voltage

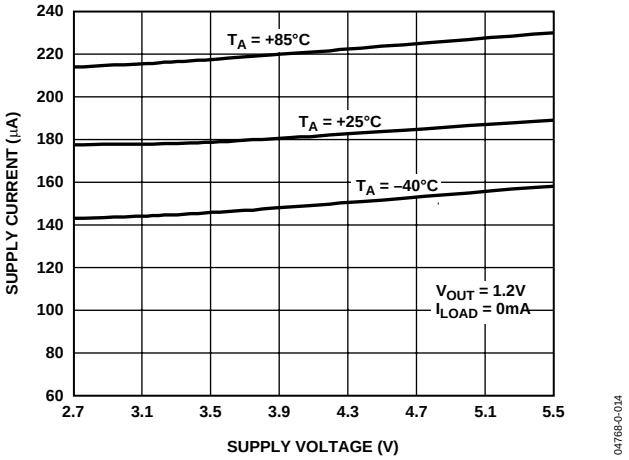


Figure 15. Quiescent Current vs. Input Voltage

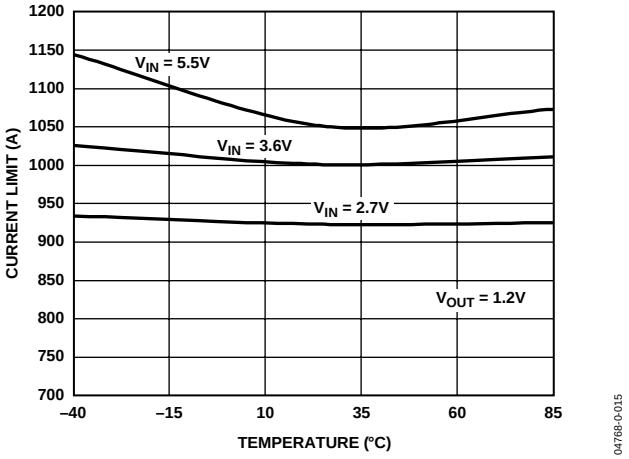


Figure 16. Current Limit vs. Input Voltage, V_{OUT} = 1.2 V

THEORY OF OPERATION

The ADP3051 is a monolithic current mode buck converter with an integrated high-side switch and low-side synchronous rectifier. It operates with input voltages between 2.7 V and 5.5 V, regulates an output voltage down to 0.8 V, and supplies more than 500 mA of load current. The ADP3051 features patented Tri-Mode technology to operate in fixed frequency PWM mode at medium to heavy loads. This improves light-load efficiency by smoothly transitioning into a variable frequency PWM mode, and into a single-pulse, current-limited variable frequency mode at very light loads.

PWM CONTROL MODE

At moderate to high output currents, the ADP3051 operates in a fixed frequency, peak current control mode to regulate the output voltage. At the beginning of each cycle, the P-channel output switch turns on and remains on until the inductor current exceeds the threshold set by the voltage at COMP. When the P-channel switch turns off, the N-channel synchronous rectifier turns on for the remainder of the cycle, after which the cycle repeats.

In current mode, two cascaded control loops combine to regulate the output voltage. The outer voltage control loop senses the voltage at FB and compares it to the internal 0.8 V reference. The internal transconductance amplifier forces a current at COMP proportional to the voltage difference between the reference and FB. By selecting the components between COMP and GND, the frequency characteristics of the control system give a stable regulation system.

The inner peak-current control loop monitors the current flowing through the P-channel MOSFET and converts that to a voltage. This voltage is internally compared to the voltage at COMP, which sets inductor peak current. The error amplifier, and thus the output voltage, controls the inductor peak current to regulate the output voltage. An internally generated slope compensation circuit ensures that the inner current control loop maintains stable operation over the entire input and output voltage range.

TRI-MODE OPERATION

The ADP3051 features patented Tri-Mode technology which allows fixed-frequency, current mode, PWM operation at medium and heavy loads; smoothly transitions to variable frequency PWM operation to improve light-load efficiency; and operates in a single-pulse, current-limited variable frequency mode at very light loads. These three modes work together to provide high efficiency over a wide range of load current conditions without the frequency jitter, increased output voltage ripple, and audible noise generation exhibited by other light-load control schemes.

The ADP3051's internal oscillator is a key component of its Tri-Mode operation. Under medium-heavy load conditions, the oscillator operates at a constant 550 kHz. Under light-load conditions, the oscillator frequency is decreased to minimize switching losses, thus improving light-load efficiency. At very light loads, the oscillator is disabled and the ADP3051 switches only as required to supply the load current for good light-load efficiency.

In addition to Tri-Mode operation, the ADP3051 operates in the 200 kHz frequency foldback mode when the voltage at FB is below 0.3 V for enhanced control of the inductor current under short-circuit and startup conditions. See the Short-Circuit Protection and Recovery section.

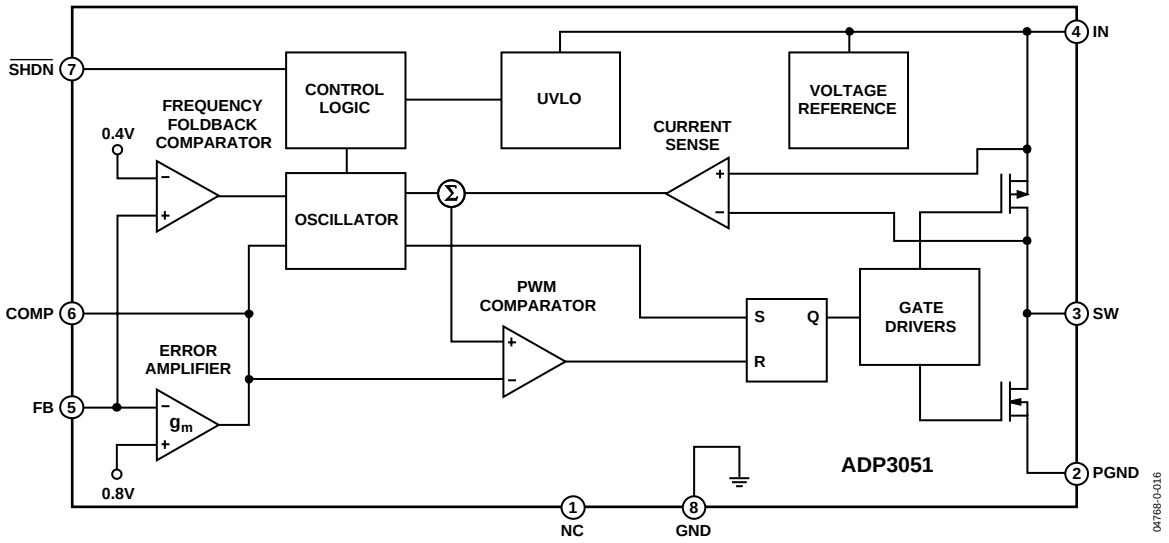


Figure 17. Simplified Block Diagram

100% DUTY CYCLE OPERATION

The ADP3051 is capable of operating at 100% duty cycle, allowing it to regulate output voltages that are very close to the input voltage. In 100% duty cycle operation, the P-channel switch remains continuously on, and the dropout voltage is simply the output current multiplied by the on resistance of the internal switch and inductor, typically 200 mV at full loads (500 mA).

SHUTDOWN

The ADP3051 is enabled and disabled via its $\overline{\text{SHDN}}$ input. $\overline{\text{SHDN}}$ easily interfaces to open-drain and three-state logic GPIOs. To enable the ADP3051, drive $\overline{\text{SHDN}}$ to within 0.5 V of the voltage at IN; to disable the ADP3051, drive $\overline{\text{SHDN}}$ below 0.4 V. The circuit of Figure 18 shows a simple means of driving $\overline{\text{SHDN}}$ to the proper high and low input states in cases where no open-drain or three-state GPIO is available.

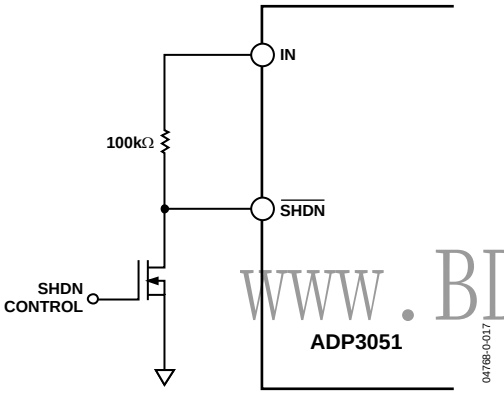


Figure 18. Shutdown Control Circuit

UNDERVOLTAGE LOCKOUT (UVLO)

The ADP3051 includes an internal undervoltage lockout (UVLO) circuit that turns off the converter if the input voltage drops below the 2.2 V UVLO threshold. This prevents uncontrolled behavior if the input voltage drops below the 2.7 V minimum allowable voltage range. The UVLO circuit includes 55mV of hysteresis to prevent oscillation at the UVLO threshold.

SHORT-CIRCUIT PROTECTION AND RECOVERY

When starting up or when the output is short circuited, the low voltage drop across the synchronous rectifier may allow the inductor current to run away because it rises more during the on time than it falls during the off time. To protect against this, the ADP3051 automatically initiates a frequency foldback operation when the voltage at FB drops below 0.3 V, allowing the ADP3051 to maintain control of the inductor current under these conditions.

When operating at higher input voltages (for example, from a 5 V bus), the ADP3051 may exhibit output voltage overshoot upon startup or after release of an overload condition (see Figure 9). In such cases, the ADP3051's limited COMP slew rate can slow its recovery as the output approaches regulation, allowing the output voltage to overshoot. If overshoot cannot be tolerated in an application, the COMP voltage can be limited by placing a Zener diode from COMP to GND, as shown in Figure 19.

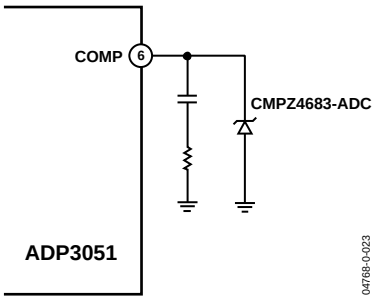


Figure 19. COMP Zener Clamp to Prevent Short-Circuit Recovery Output Voltage Overshoot

APPLICATIONS

RECOMMENDED COMPONENTS

External component selection for the application circuit shown in Figure 20 depends on the load current requirements. Certain tradeoffs between different performance parameters can also be made. Recommended external component values are given in Table 4.

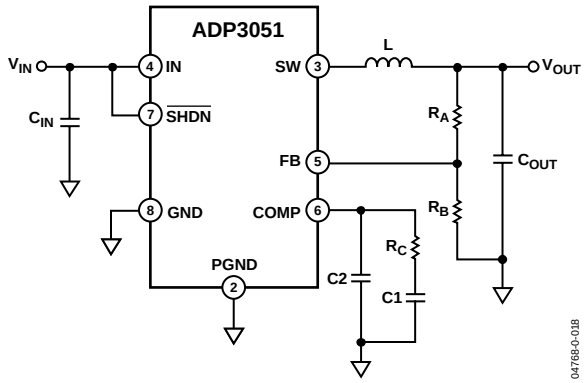


Figure 20. Typical Application Circuit

DESIGN PROCEDURE

For applications where specific performance is required, component combinations other than those listed in Table 4 may be more appropriate. A design procedure for selecting the components is provided in the following sections.

Setting the Output Voltage

The regulated output voltage of the ADP3051 is set by selecting the resistive voltage divider formed by R_A and R_B (see Figure 21). The voltage divider drops the output voltage to the voltage at FB by the equation

$$V_{OUT} = V_{FB}\left(1+\frac{R_A}{R_B}\right)$$

Where V_{OUT} is the output voltage and V_{FB} is the 0.8 V feedback regulation threshold. R_B controls the voltage divider current, I_{DIV}, which is calculated by

$$I_{DIV} = \frac{V_{FB}}{R_B}$$

Using higher divider current increases accuracy due to the 5 nA FB input bias current. With R_B = 100 kΩ, the accuracy is degraded by 0.0625%.

For a given R_B, choose the value of R_A to set the output voltage by the equation

$$R_A = R_B\left(\frac{V_{OUT}}{V_{FB}}-1\right)$$

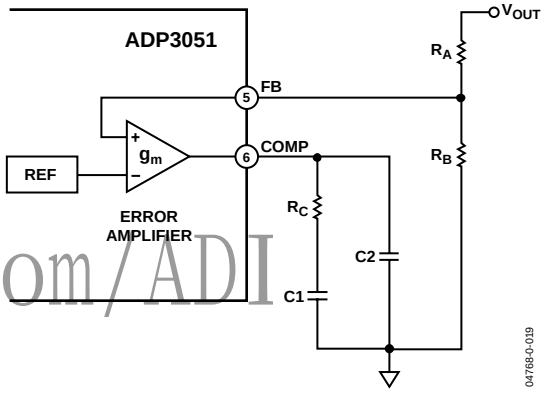


Figure 21. Typical Compensation Network

Table 4. Recommended External Components for Popular Input/Output Voltage Conditions (Based on I_{LOAD} = 500 mA Max and a 60 kHz Crossover Frequency)

V_{IN}	V_{OUT}	L (µH)	C_{OUT} (µF)	C_{IN} (µF)	R_A (kΩ)	R_B (kΩ)	R_C (kΩ)	C1 (pF)	C2 (pF)
2.5	1.0	6.8	10	10	2.5	10	4.7	470	47
	1.8	6.8	10	10	12.5	10	10	270	27
3.6	1.0	6.8	10	10	2.5	10	4.7	470	47
	1.8	8.2	10	10	12.5	10	10	270	27
	2.5	8.2	10	10	21.3	10	15	180	18
5.0	1.0	8.2	10	10	2.5	10	5.7	470	47
	1.8	10	10	10	12.5	10	10	270	27
	2.5	10	10	10	21.3	10	15	180	18
	3.3	12	10	10	31.3	10	18	150	15

Inductor Selection

The ADP3051's high switching frequency allows the use of a physically small inductor. The inductor ripple current is determined by

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

Where ΔI_L is the peak-to-peak inductor ripple current and f_{SW} is the switching frequency. As a guideline, the inductor peak-to-peak current ripple is typically set to be one-third the maximum dc load current. Using this guideline and solving for L,

$$L = \frac{3 \times V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOAD(MAX)}}$$

Simplifying for the known constants

$$L = 5\,\mu\text{H} \times \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times I_{LOAD(MAX)}}$$

It is important to ensure that the inductor is capable of handling the maximum peak inductor current, I_{LPK}, determined by

$$I_{LPK} = I_{LOAD(MAX)} + \left(\frac{\Delta I_L}{2}\right)$$

Finally, the ADP3051's internal slope compensation is designed to ensure stability of the inner current mode control loop when the inductor is chosen so that the down-slope of the inductor current is less than 320 mA/µs

$$L \geq \frac{V_{OUT}}{320\ \text{mA}/\mu\text{s}}$$

OUTPUT CAPACITOR SELECTION

The output capacitor should be chosen to meet output voltage ripple requirements for the application. Output voltage ripple is a function of the inductor ripple current and the impedance of the output capacitor at the switching frequency. The magnitude of the capacitive impedance is

$$X_{COUT} = \frac{1}{2\pi \times C_{OUT} \times f_{SW}}$$

For capacitors with relatively large capacitance or high equivalent series resistance (ESR), e.g., tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency; therefore, the output ripple voltage is mainly a function of ESR. In this case, the output capacitor should be chosen based on the ESR by the equation

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{\Delta I_L}$$

Where V_{RIPPLE} is the peak-to-peak output ripple voltage and ESR_{COUT} is the output capacitor ESR. For capacitors with relatively small capacitance and/or resistance, the capacitance dominates the output voltage ripple. In this case, choose the output capacitor by the capacitance using the equation

$$C_{OUT} \geq \frac{V_{IN}}{(2\pi \times f_{SW}) 2 \times L \times V_{RIPPLE}}$$

$$C_{OUT} \geq \frac{\Delta I_L}{8 f_{SW} \Delta V_{OUT}}$$

Multilayer ceramic (MLC), tantalum, OS-CON, or similar low ESR capacitors are recommended. Table 5 lists some vendors that make suitable capacitors.

Table 5. Capacitor Suppliers

Manufacturer	Capacitor Type	Contact Info
AVX	Tantalum	www.avxcorp.com
Murata	MLCC	www.murata.com
Sanyo	OS-CON	www.sanyovideo.com
Taiyo-Yuden	MLCC	www.t-yuden.com

Input Capacitor Selection

The input capacitor reduces input voltage ripple caused by switch currents. Select an input capacitor capable of withstanding the rms input current

$$I_{CIN(RMS)} \geq I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

Where $I_{CIN(RMS)}$ is the rms ripple rating of the input capacitor. As with the output capacitor, a low ESR capacitor is recommended to help to minimize input voltage ripple.

Compensation Design

The ADP3051's external compensation network allows designers to easily optimize the part's performance for a particular application with just a series RC network (R_C and C1 of Figure 21) from COMP to GND typically required to compensate the regulator.

The dc loop gain is given by the equation

$$A_{VDC} = \frac{V_{FB} \times G_{EA} \times R_{OEA} \times R_{LOAD}}{V_{OUT} \times R_{CS}}$$

where:
V_{FB} is the feedback voltage regulation threshold, 0.8 V.
G_{EA} is the error amplifier transconductance, 320 µs.
R_{OEA} is the error amplifier output impedance (10 MΩ).
R_{CS} is the 2.9 Ω current sense gain.
R_{LOAD} is the equivalent output resistance, equal to the output voltage divided by the load current.

The system has three poles and a zero that dominate its frequency response. The first compensation pole is given by

$$f_{PC1} = \frac{1}{2\pi \times R_{OEA} \times C1}$$

The output pole is given by

$$f_{POUT} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}}$$

If used, the optional second compensation pole is given by

$$f_{PC2} = \frac{1}{2\pi \times R_C \times C2}$$

Finally, the zero can be calculated as

$$f_{ZC} = \frac{1}{2\pi \times R_C \times C1}$$

Note that the dc loop gain is the inverse of the output load current, while the output pole, f_{POUT}, is proportional to the load current. Thus, the crossover frequency, which is proportional to the product of the dc loop gain and the output pole frequency, remains the same.

To choose the compensation components, first choose the regulator loop crossover frequency (the frequency where the loop gain drops to 1 V/V or 0 dB). To determine the desired crossover frequency, chose it for about one-tenth of the switching frequency or 60 kHz. The required compensation resistor, R_C, can be determined from the equation

$$R_C = \frac{2\pi \times f_C \times V_{OUT} \times R_{CS} \times C_{OUT}}{V_{REF} \times G_{EA}}$$

Where f_C is the crossover frequency. To make sure the phase margin is suitable, choose the first compensation capacitor to set the zero frequency to one-fourth the crossover frequency, or

$$C1 = \frac{4}{2\pi \times f_C \times R_C}$$

An optional second compensation capacitor reduces the high frequency gain to reduce the high frequency noise. If used, choose the second compensation capacitor to set the second compensation pole to the switching frequency, or

$$C2 = \frac{1}{2\pi \times f_{SW} \times R_C}$$

CIRCUIT BOARD LAYOUT CONSIDERATIONS

A good circuit board layout aids in extracting the most performance from the ADP3051. Poor circuit layout degrades the output ripple and the electromagnetic interference (EMI) or electromagnetic compatibility (EMC) performance.

The evaluation board layout of Figure 24 is optimized for the ADP3051. Use this layout for best performance. If this layout needs changing, use the following guidelines:

1. Use separate analog and power ground planes. Connect the sensitive analog circuitry (such as compensation and voltage divider components) to analog ground; connect the power components (such as input and output bypass capacitors) to power ground. Connect the two ground planes together near the load to reduce the effects of voltage dropped on circuit board traces.
2. Locate C_{IN} as close to the IN pin as possible, and use separate input bypass capacitors for the analog and power grounds indicated in Guideline 1.
3. Route the high current path from C_{IN}, through L, to the SW and PGND pins as short as possible.
4. Route the high current path from C_{IN} through L and C_{OUT} as short as possible.
5. Keep high current traces as short and as wide as possible.
6. Place the feedback resistors as close as possible to the FB pin to prevent noise pickup.
7. Place the compensation components as close as possible to the COMP pin.
8. Avoid routing high impedance traces, such as FB and COMP, near the high current traces and components or near the switch node (SW).
9. If high impedance traces are routed near high current and/or the SW node, place a ground plane shield between the traces.

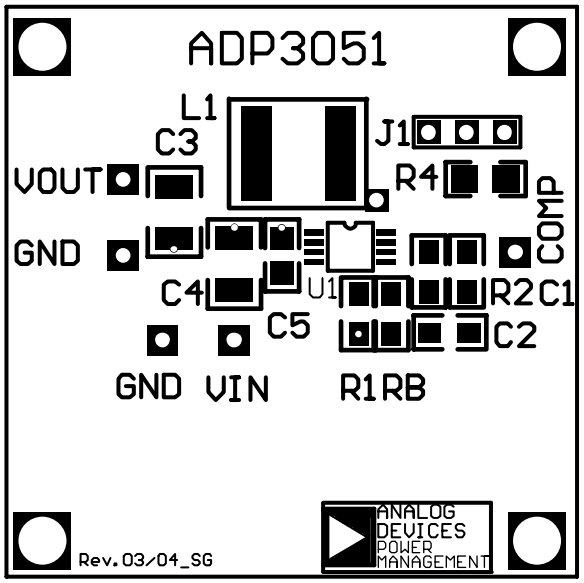


Figure 22. Sample Application Circuit Board Layout (Silkscreen Layer)

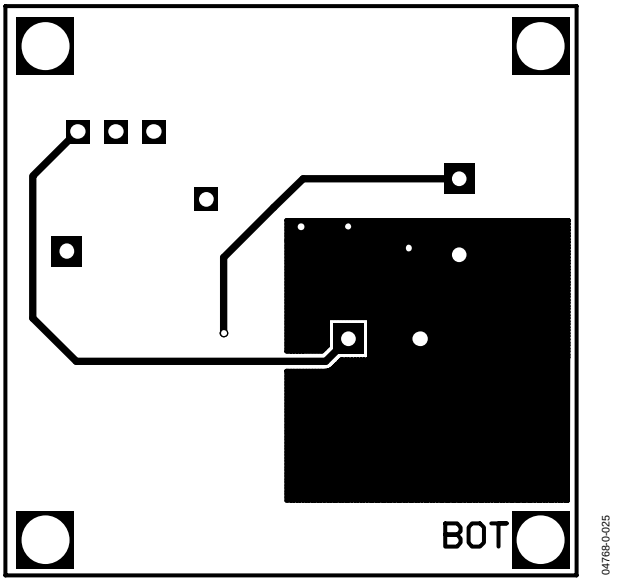


Figure 24. Sample Application Circuit Board Layout (Bottom Layer)

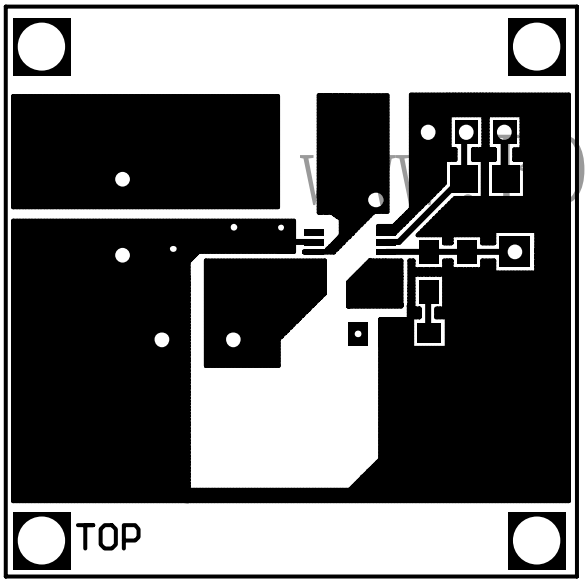


Figure 23. Sample Application Circuit Board Layout (Top Layer)

OUTLINE DIMENSIONS

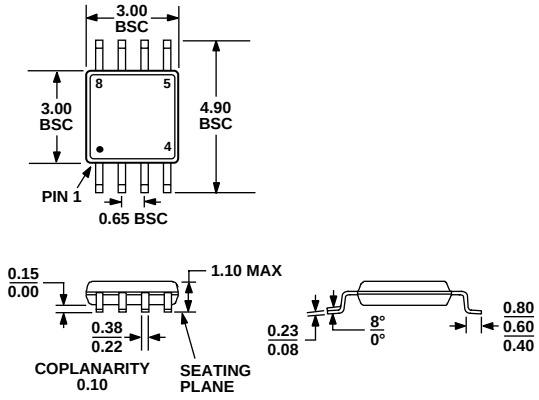


Figure 25. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline	Branding
ADP3051ARMZ-REEL7[1]	–40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	P3A

[1] Z = Pb-free part.

NOTES

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