
SPI Automotive Temperature Serial EEPROMs
128k (16,384 x 8) and 256k (32,768 x 8)

DATASHEET

Features

- Serial Peripheral Interface (SPI) compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
 - Data sheet describes Mode 0 operation
- Medium-voltage and standard-voltage operation
 - $V_{CC} = 2.5V$ to 5.5V
- Extended temperature range $-40^{\circ}C$ to $125^{\circ}C$
- 5MHz clock rate
- 64 byte page mode
- Block write protection
 - Protect 1/4, 1/2, or entire array
- Write Protect (\overline{WP}) pin and Write Disable instructions for both hardware and software data protection
- Self-timed write cycle (5ms max)
- High reliability
 - Endurance: one million write cycles
 - Data retention: 100 years
- 8-lead JEDEC SOIC and 8-lead TSSOP packages

Description

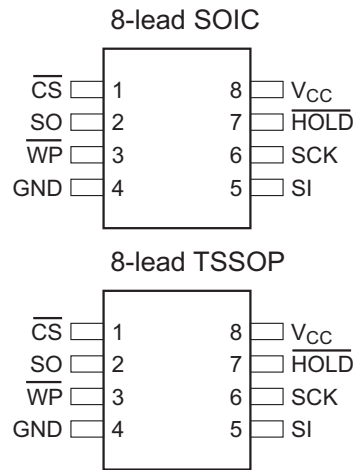
The Atmel® AT25128B/256B provides 131072/262144 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM) organized as 16384/32768 words of eight bits each. The device is optimized for use in many automotive applications where low-power and low-voltage operation are essential. The AT25128B/256B is available in space-saving 8-lead JEDEC SOIC and 8-lead TSSOP packages.

AT25128B/256B is enabled through the Chip Select pin (\overline{CS}) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate erase cycle is required before write.

Block write protection is enabled by programming the Status Register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the \overline{WP} pin to protect against inadvertent write attempts to the Status Register. The \overline{HOLD} pin may be used to suspend any serial communication without resetting the serial sequence.

Figure 1. Pin Configurations

Pin Name	Function
$\overline{\text{CS}}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
$\overline{\text{WP}}$	Write Protect
$\overline{\text{HOLD}}$	Suspends Serial Input

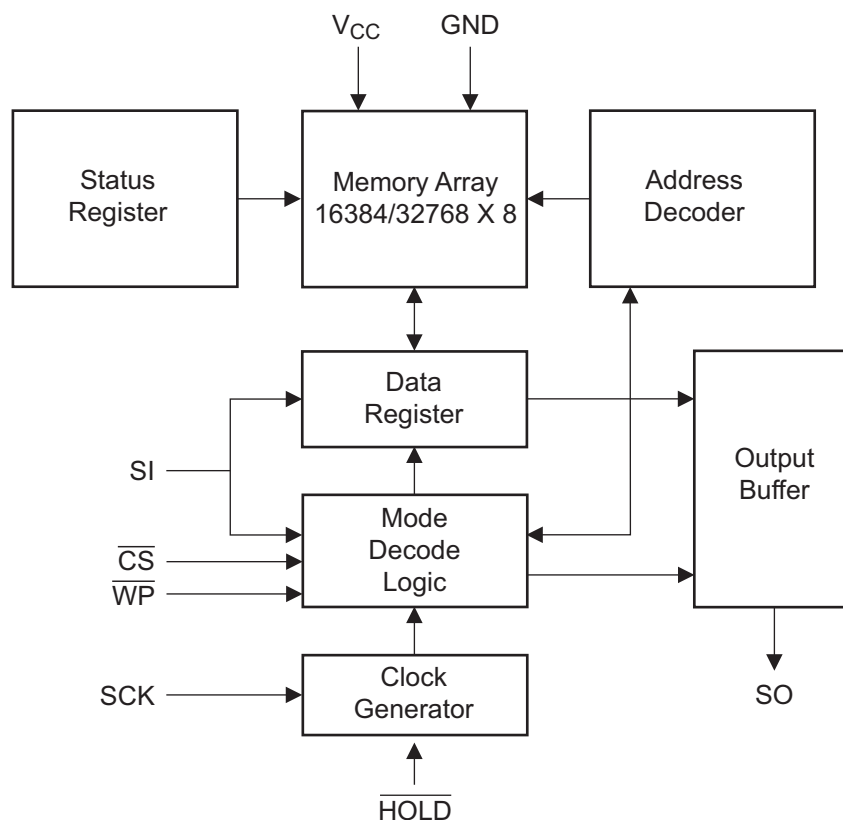


1. Absolute Maximum Ratings*

Operating Temperature	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Block Diagram



3. Electrical Characteristics

3.1 Pin Capacitance⁽¹⁾

Applicable at these conditions, unless otherwise noted. $T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = +5.0\text{V}$.

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	$V_{OUT} = 0\text{V}$
C_{IN}	Input Capacitance (\overline{CS} , SCK, SI, \overline{WP} , \overline{HOLD})	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

3.2 DC Characteristics

Applicable over recommended operating range from: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +2.5\text{V}$ to $+5.5\text{V}$.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		2.5		5.5	V
I_{CC1}	Supply Current	$V_{CC} = 5.0\text{V}$ at 5MHz, SO = Open, Read			6.0	mA
I_{CC2}	Supply Current	$V_{CC} = 5.0\text{V}$ at 1MHz, SO = Open, Read, Write			3.0	mA
I_{CC3}	Supply Current	$V_{CC} = 5.0\text{V}$ at 5MHz, SO = Open, Read, Write			7.0	mA
I_{SB1}	Standby Current	$V_{CC} = 2.5\text{V}$, $\overline{CS} = V_{CC}$		0.2	10.0	μA
I_{SB2}	Standby Current	$V_{CC} = 5.0\text{V}$, $\overline{CS} = V_{CC}$		2.0	13.0	μA
I_{IL}	Input Leakage	$V_{IN} = 0\text{V}$ to V_{CC}	-3.0		3.0	μA
I_{OL}	Output Leakage	$V_{IN} = 0\text{V}$ to V_{CC}	-3.0		3.0	μA
$V_{IL}^{(1)}$	Input Low-voltage		-0.6		$V_{CC} \times 0.3$	V
$V_{IH}^{(1)}$	Input High-voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL1}	Output Low-voltage	$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			0.4	V
V_{OH1}	Output High-voltage				$V_{CC} - 0.8$	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

3.3 AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$, $CL = 1$ TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	2.5–5.5	0	5.0	MHz
t_{RI}	Input Rise Time	2.5–5.5		2	μs
t_{FI}	Input Fall Time	2.5–5.5		2	μs
t_{WH}	SCK High Time	2.5–5.5	40		ns
t_{WL}	SCK Low Time	2.5–5.5	40		ns
t_{CS}	$\overline{\text{CS}}$ High Time	2.5–5.5	80		ns
t_{CSS}	$\overline{\text{CS}}$ Setup Time	2.5–5.5	80		ns
t_{CSH}	$\overline{\text{CS}}$ Hold Time	2.5–5.5	80		ns
t_{SU}	Data In Setup Time	2.5–5.5	5		ns
t_{H}	Data In Hold Time	2.5–5.5	20		ns
t_{HD}	$\overline{\text{Hold}}$ Setup Time	2.5–5.5	40		ns
t_{CD}	$\overline{\text{Hold}}$ Hold Time	2.5–5.5	40		ns
t_{V}	Output Valid	2.5–5.5	0	40	ns
t_{HO}	Output Hold Time	2.5–5.5	0		ns
t_{LZ}	$\overline{\text{Hold}}$ to Output Low Z	2.5–5.5	0	40	ns
t_{HZ}	$\overline{\text{Hold}}$ to Output High Z	2.5–5.5		80	ns
t_{DIS}	Output Disable Time	2.5–5.5		80	ns
t_{WC}	Write Cycle Time	2.5–5.5		5	ms
Endurance ⁽¹⁾	5.0V, 25°C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

4. Serial Interface Description

Master: The device that generates the serial clock.

Slave: Because the Serial Clock pin (SCK) is always an input, AT25128B/256B always operates as a slave.

Transmitter/Receiver: AT25128B/256B has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

Serial Opcode: After the device is selected with \overline{CS} going low, the first byte will be received. This byte contains the opcode that defines the operations to be performed.

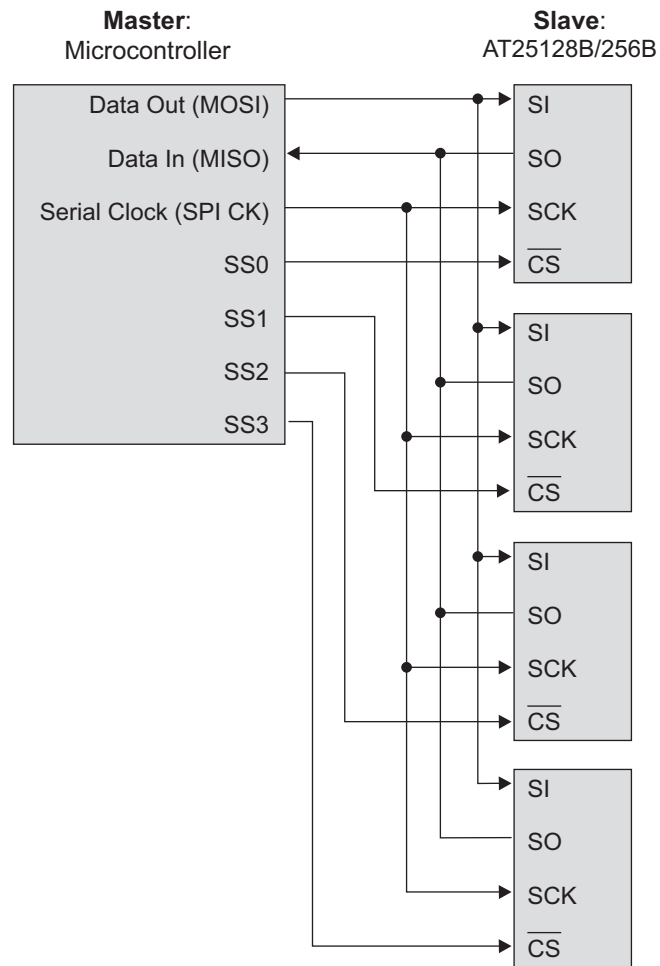
Invalid Opcode: If an invalid opcode is received, no data will be shifted into AT25128B/256B, and the Serial Output pin (SO) will remain in a high impedance state until the falling edge of \overline{CS} is detected again. This will reinitialize the serial communication.

Chip Select: AT25128B/256B is selected when the \overline{CS} pin is low. When the device is not selected, data will not be accepted via the SI pin, and the Serial Output pin (SO) will remain in a high impedance state.

Hold: The \overline{HOLD} pin is used in conjunction with the \overline{CS} pin to select AT25128B/256B. When the device is selected and a serial sequence is underway, \overline{HOLD} can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the \overline{HOLD} pin must be brought low while the SCK pin is low. To resume serial communication, the \overline{HOLD} pin is brought high while the SCK pin is low (SCK may still toggle during \overline{HOLD}). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

Write Protect: The Write Protect pin (\overline{WP}) will allow normal read/write operations when held high. When the WP pin is brought low and WPEN bit is one, all write operations to the Status Register are inhibited. \overline{WP} going low while \overline{CS} is still low will interrupt a write to the Status Register. If the internal write cycle has already been initiated, \overline{WP} going low will have no effect on any write operation to the Status Register. The \overline{WP} pin function is blocked when the WPEN bit in the Status Register is zero. This will allow the user to install AT25128B/256B in a system with the \overline{WP} pin tied to ground and still be able to write to the Status Register. All \overline{WP} pin functions are enabled when the WPEN bit is set to one.

Figure 4-1. SPI Serial Interface



5. Functional Description

AT25128B/256B is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

AT25128B/256B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in [Table 5-1](#). All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low CS transition.

Table 5-1. Instruction Set for the Atmel AT25128B/256B

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X010	Write Data to Memory Array

Write Enable (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

Write Disable (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the \overline{WP} pin.

Read Status Register (RDSR): The Read Status Register instruction provides access to the Status Register. The Ready/Busy and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the block write protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 5-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	\overline{RDY}

Table 5-3. Read Status Register Bit Definition

Bit	Definition
Bit 0 (\overline{RDY})	Bit 0 = 0 (\overline{RDY}) indicates the device is ready. Bit 0 = 1 indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1 = 0 indicates the device is not write-enabled. Bit 1 = 1 indicates the device is write-enabled.
Bit 2 (BP0)	See Table 5-4 on page 9 .
Bit 3 (BP1)	See Table 5-4 on page 9 .
Bits 4 – 6 are zeros when device is not in an internal write cycle.	
Bit 7 (WPEN)	See Table 5-5 on page 9 .

Note: 1. Bits 0 - 7 are ones during the internal write cycle.

Write Status Register (WRSR): The WRSR instruction allows the user to select one of four levels of protection. AT25128B/256B is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read-only. The block write protection levels and corresponding Status Register control bits are shown in [Table 5-4](#).

Bits BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, t_{WC} , RDSR).

Table 5-4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected	
	BP1	BP0	Atmel AT25128B	Atmel AT25256B
0	0	0	None	None
1 (1/4)	0	1	3000 – 3FFF	6000 – 7FFF
2 (1/2)	1	0	2000 – 3FFF	4000 – 7FFF
3 (All)	1	1	0000 – 3FFF	0000 – 7FFF

The WRSR instruction also allows the user to enable or disable the Write Protect (\overline{WP}) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the \overline{WP} pin is low and the WPEN bit is one. Hardware write protection is disabled when either the \overline{WP} pin is high or the WPEN bit is zero. When the device is hardware write protected, writes to the Status Register, including the block protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory that are not block-protected.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to zero as long as the \overline{WP} pin is held low.

Table 5-5. WPEN Operation

WPEN	\overline{WP}	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writeable	Writeable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writeable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writeable	Writeable

Read Sequence (READ): Reading the AT25128B/256B via the Serial Output (SO) pin requires the following sequence. After the \overline{CS} line is pulled low to select a device, the read opcode is transmitted via the SI line followed by the byte address to be read (A15–A0, see [Table 5-6](#)). Upon completion, any data on the SI line will be ignored. The data (D7–D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the \overline{CS} line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address, allowing the entire memory to be read in one continuous read cycle.

Write Sequence (WRITE): In order to program the AT25128B/256B, two separate instructions must be executed. First, the device **must be write enabled** via the WREN instruction. Then a Write (WRITE) instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write instruction requires the following sequence. After the \overline{CS} line is pulled low to select the device, the WRITE opcode is transmitted via the SI line followed by the byte address (A15–A0) and the data (D7–D0) to be programmed (See Table 5-6). Programming will start after the \overline{CS} pin is brought high. The low-to-high transition of the \overline{CS} pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a Read Status Register (RDSR) instruction. If Bit 0 = one, the write cycle is still in progress. If Bit 0 = zero, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

AT25128B/256B is capable of a 64-byte page write operation. After each byte of data is received, the five low-order address bits are internally incremented by one; the high-order bits of the address will remain constant. If more than 64 bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. AT25128B/256B is automatically returned to the write disable state at the completion of a write cycle.

Note: If the device is not Write Enabled (WREN), the device will ignore the write instruction and will return to the standby state, when \overline{CS} is brought high. A new \overline{CS} falling edge is required to reinitiate the serial communication.

Table 5-6. Address Key

Address	Atmel AT25128B	Atmel AT25256B
AN	A13–A0	A14–A0
Don't Care Bits	A15–A14	A15

6. Timing Diagrams

Figure 6-1. Synchronous Data Timing (for Mode 0)

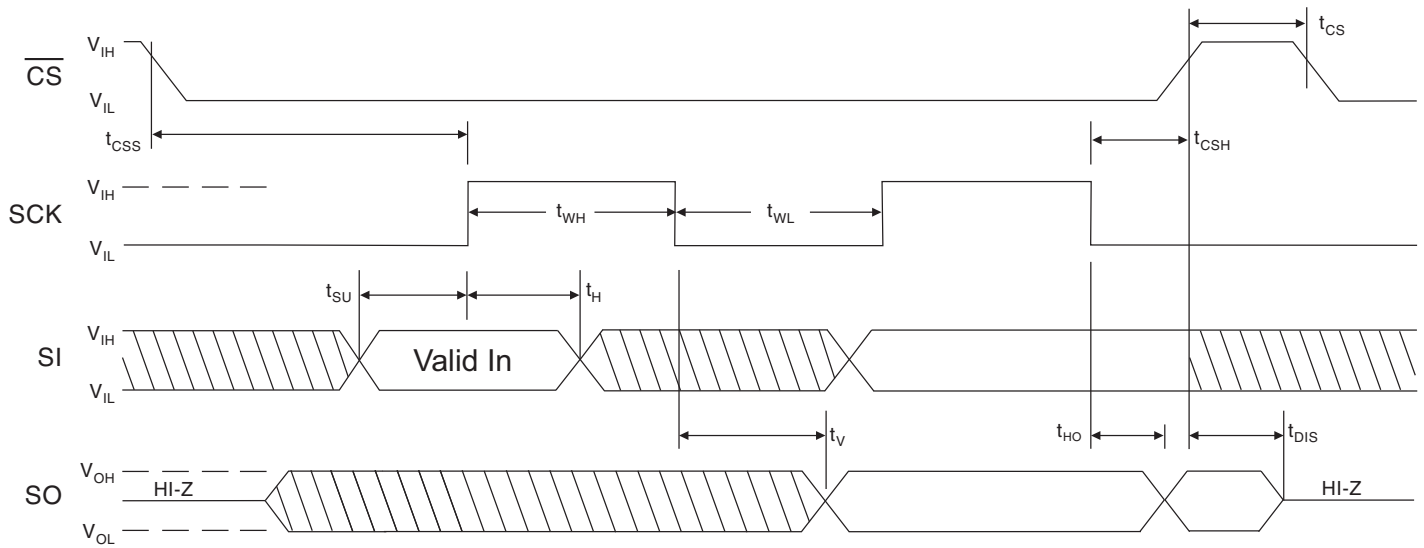


Figure 6-2. WREN Timing

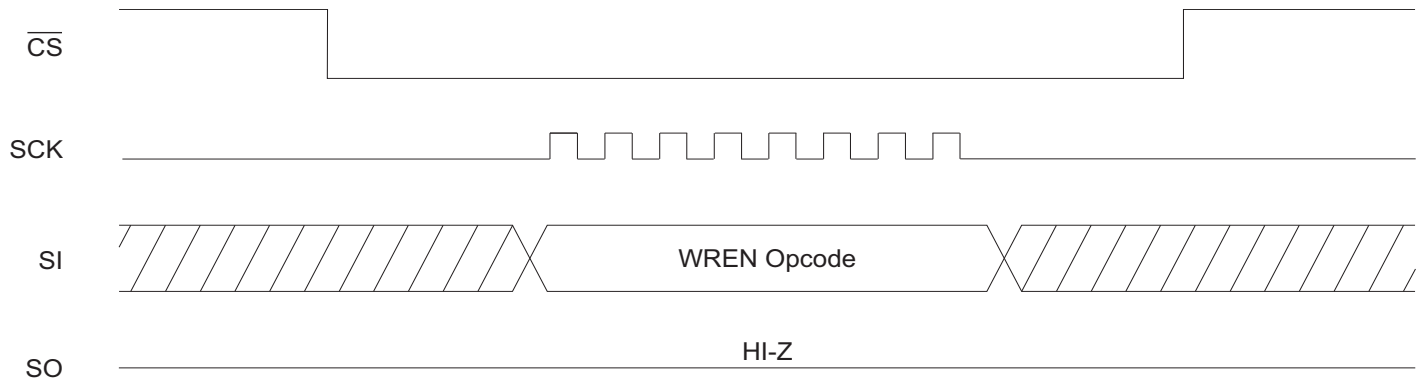


Figure 6-3. WRDI Timing

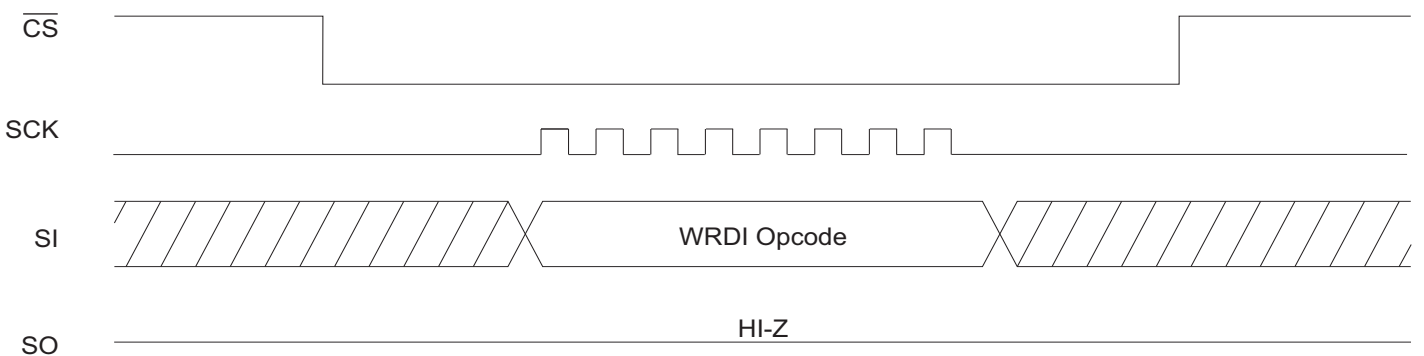


Figure 6-4. RDSR Timing

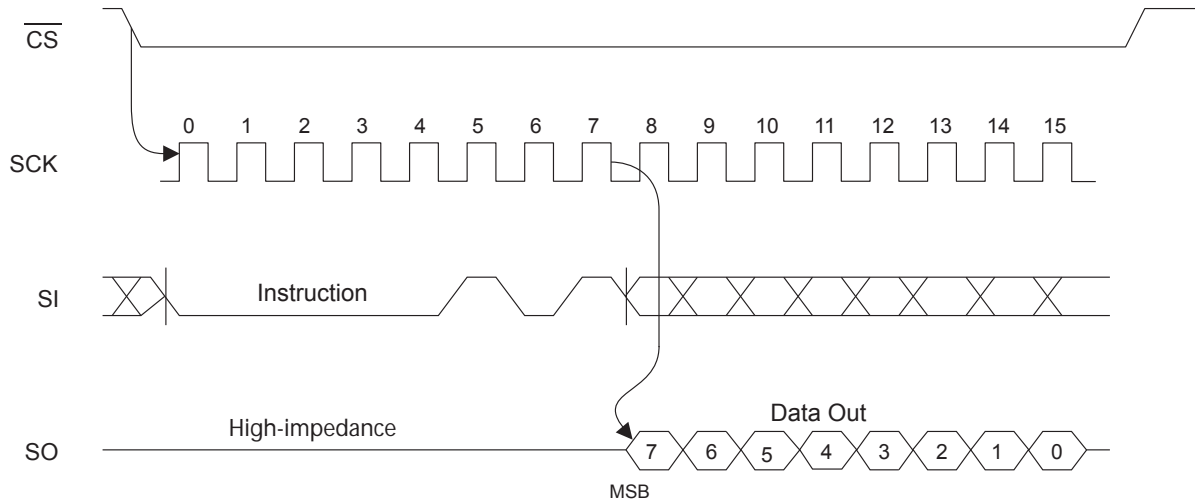


Figure 6-5. WRSR Timing

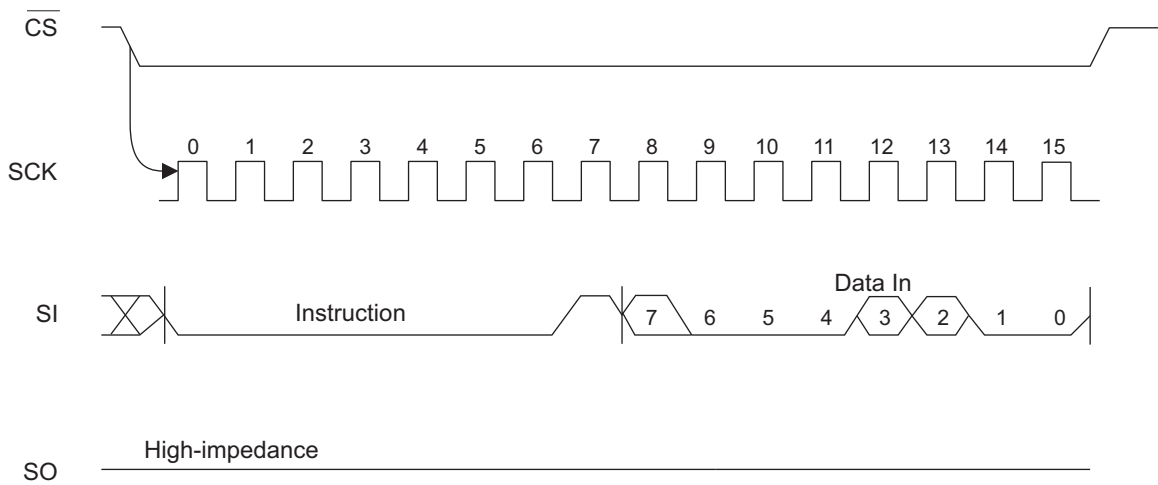


Figure 6-6. Read Timing

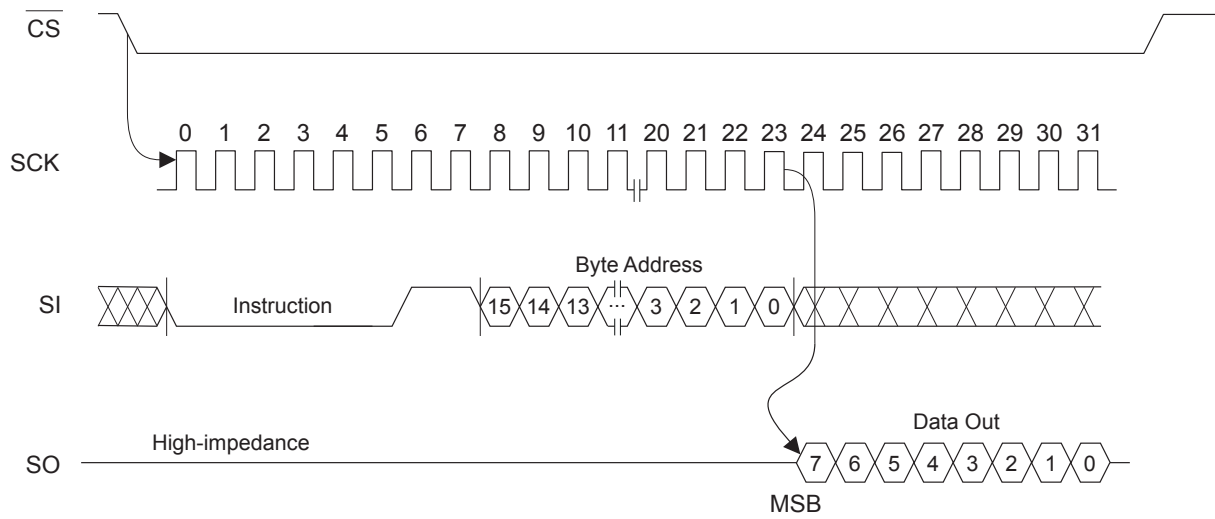


Figure 6-7. Write Timing

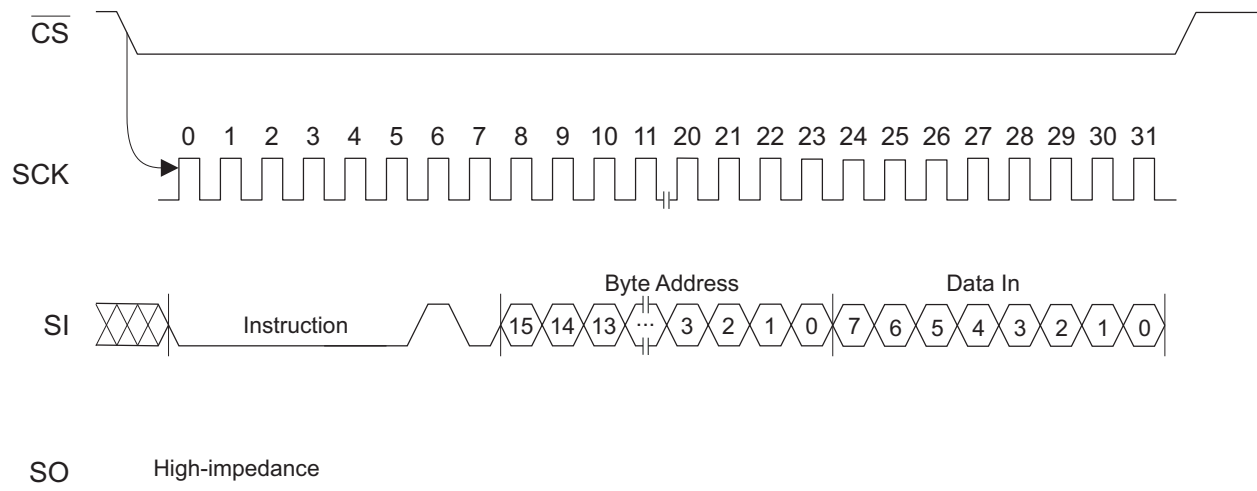
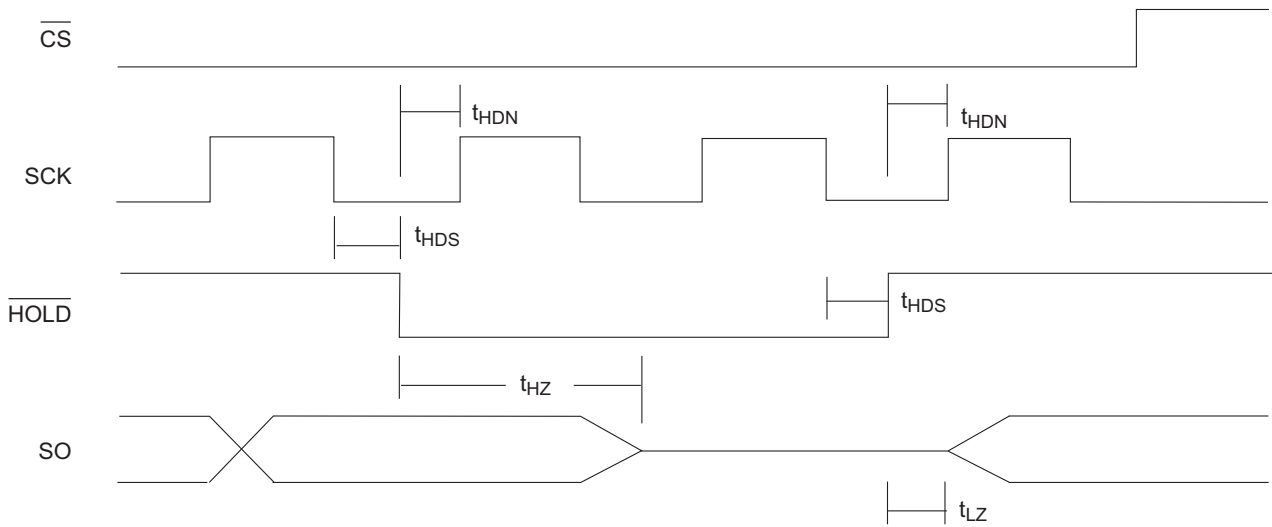


Figure 6-8. $\overline{\text{HOLD}}$ Timing

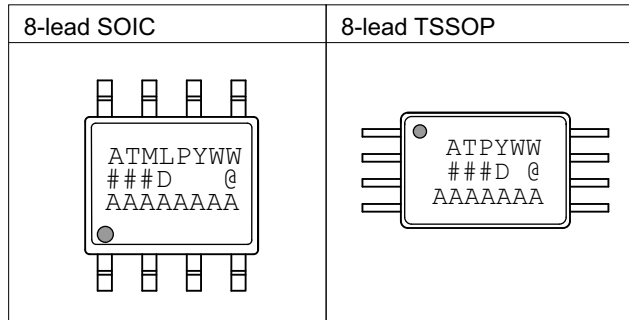


6.1 Power Recommendation

The device internal POR (Power-On Reset) threshold is just below the minimum device operating voltage. Power shall rise monotonically from 0.0Vdc to full V_{CC} in less than 1ms. Hold at full V_{CC} for at least 100 μs before the first operation. Power shall drop from full V_{CC} to 0.0Vdc in less than 1ms. Power dropping to a non-zero level and then slowly going to zero is *not* recommended. Power shall remain off (0.0Vdc) for 0.5s minimum. Please consult Atmel if your power conditions do not meet the above recommendations.

7. Part Markings

AT25128B and AT25256B: Package Marking Information



Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT25128B		Truncation Code ###: 5DB	
AT25256B		Truncation Code ###: 5EB	
Date Codes			Voltages
Y = Year	M = Month	WW = Work Week of Assembly	D: 2.5V min
2: 2012 6: 2016	A: January	02: Week 2	
3: 2013 7: 2017	B: February	04: Week 4	
4: 2014 8: 2018	
5: 2015 9: 2019	L: December	52: Week 52	
Country of Assembly		Lot Number	Grade/Lead Finish Material
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number	P: Automotive/NiPdAu
Trace Code			Atmel Truncation
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

4/5/12

Atmel	TITLE	DRAWING NO.	REV.
Package Mark Contact: DL-CSO-Assy_eng@atmel.com	25128-256BAM, AT25128B and AT25256B Automotive Package Marking Information	25128-256BAM	C

8. Ordering Code Information

Atmel Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT25128B-SSPD-T ⁽¹⁾	NiPdAu (Lead-free/Halogen-free)	8S1	2.5V to 5.5V	Automotive Temperature (-40°C to 125°C)
AT25128B-XPD-T ⁽¹⁾		8X		
AT25256B-SSPD-T ⁽¹⁾	NiPdAu (Lead-free/Halogen-free)	8S1	2.5V to 5.5V	Automotive Temperature (-40°C to 125°C)
AT25256B-XPD-T ⁽¹⁾		8X		

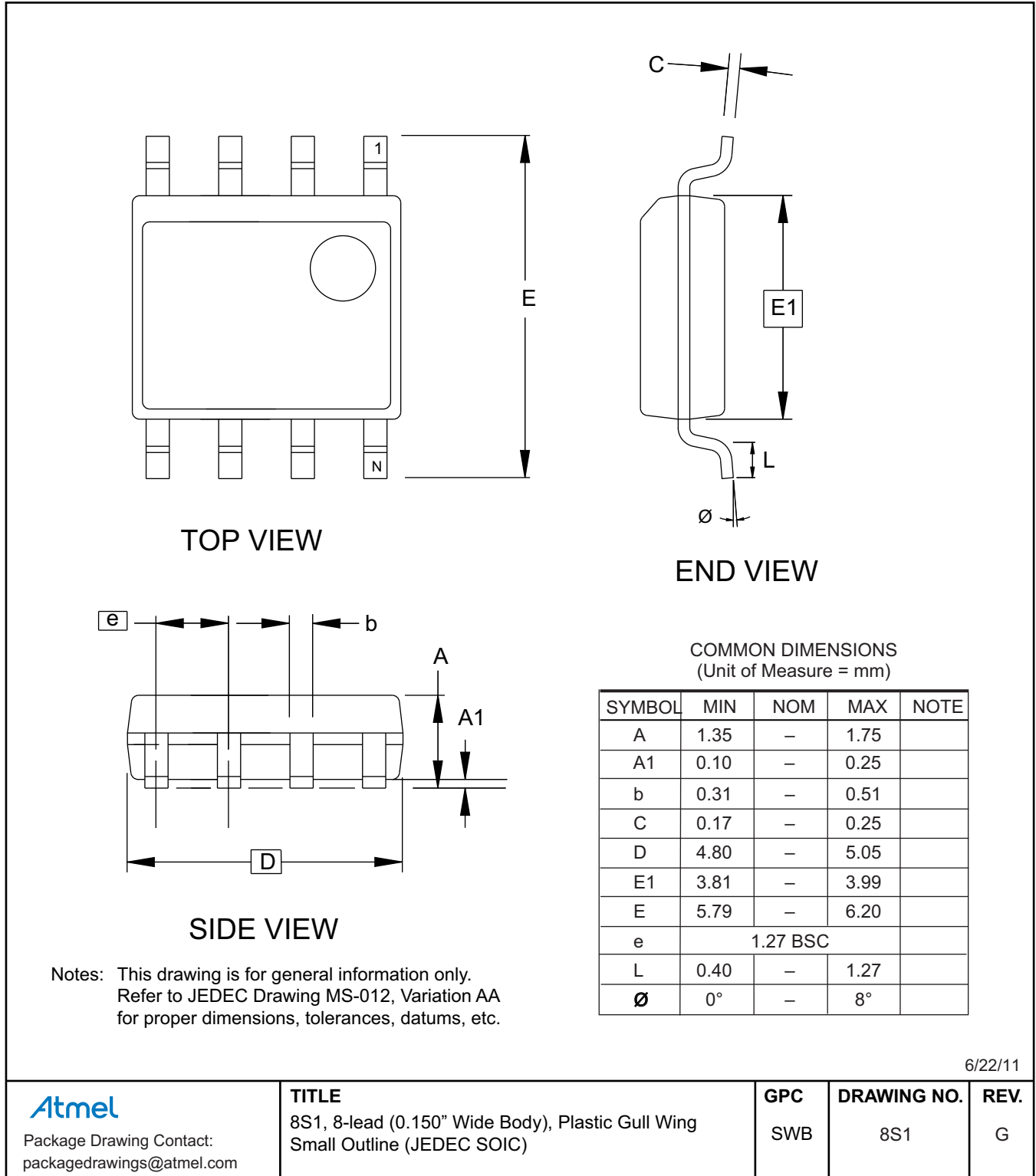
Note: 1. Tape and reel delivery:

- SOIC 4k/reel
- TSSOP 5k/reel

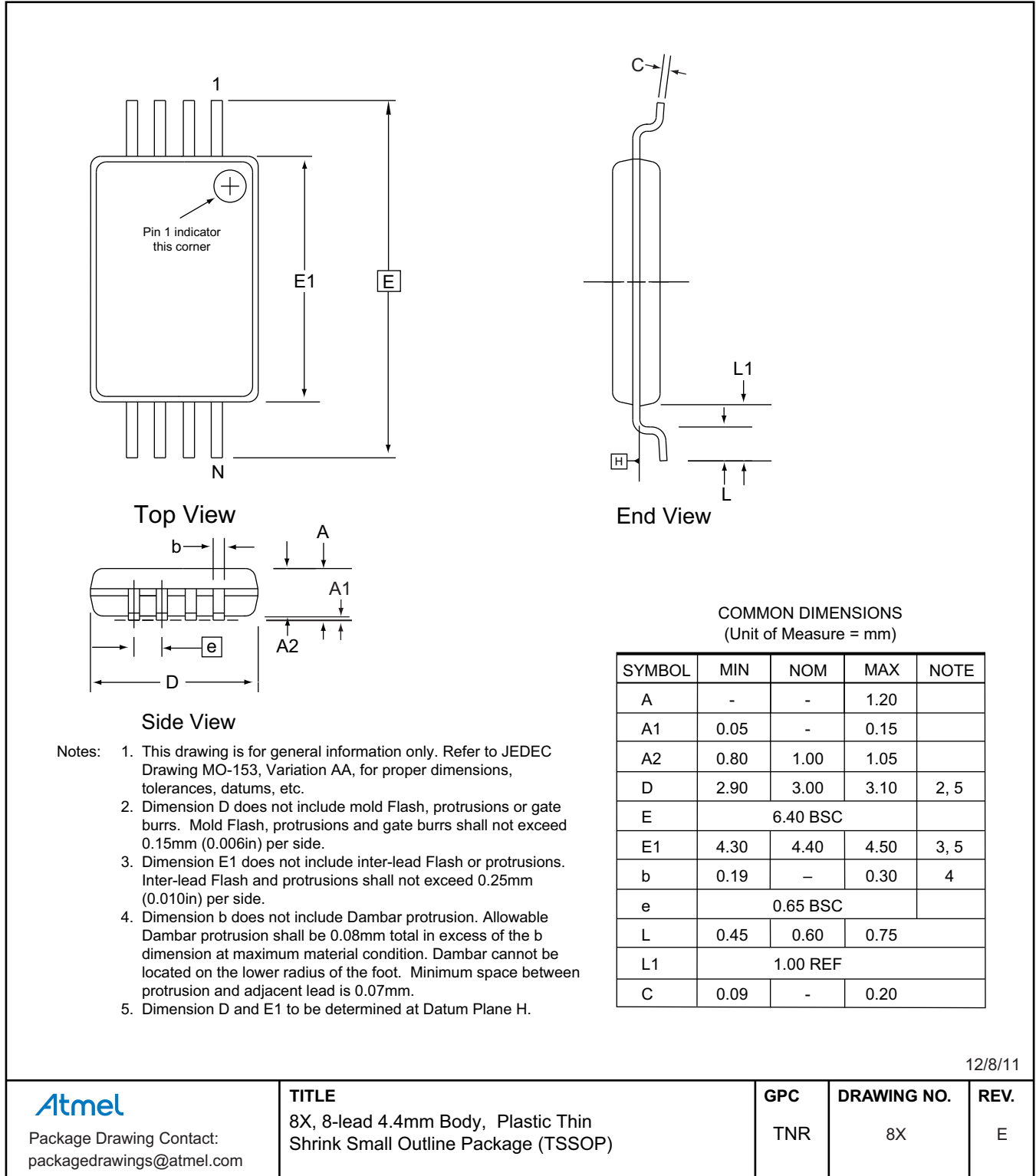
Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)

9. Packaging Information

9.1 8S1 — 8-lead JEDEC SOIC



9.2 8X — 8-lead TSSOP



10. Revision History

Doc. Rev.	Date	Comments
8810C	12/2012	Update ordering code tables. Update 8X package drawing.
8810B	08/2012	Remove preliminary status. Update Atmel logos and disclaimer/copy page.
8810A	04/2012	Initial document release.



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