Errata on SAM3S Engineering Sample Devices

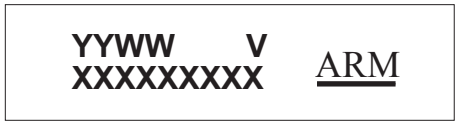
1. Scope

This document describes the known errata found on the SAM3S series engineering samples.

1.1 Marking

All devices are marked with the Atmel logo and the ordering code.

Additional marking is as follows:



where

- “YY”: manufactory year
- “WW”: manufactory week
- “V”: revision
- “XXXXXXXXX”: lot number

AT91SAM ARM-based FLASH MCU

SAM3S Series

Errata Sheet

11040B–ATARM–09-Feb-11

1.2 Errata: Device Identification “ES”

It applies to:

- SAM3S4C (with Marking ES) 0x28A00960
- SAM3S2C (with Marking ES) 0x28AA0760
- SAM3S1C (with Marking ES) 0x28A90560
- SAM3S4B (with Marking ES) 0x28900960
- SAM3S2B (with Marking ES) 0x289A0760
- SAM3S1B (with Marking ES) 0x28990560
- SAM3S4A (with Marking ES) 0x28800960
- SAM3S2A (with Marking ES) 0x288A0760
- SAM3S1A (with Marking ES) 0x28890560

1.2.1 SAM-BA Boot

1.2.1.1 SAM-BA Boot: Start-up Issue when Using No Clock on XIN

If no crystal (between XIN/XOUT) or no ceramic resonator (between XIN/XOUT) or no bypass mode (on XIN) is used, SAM-BA Boot may not start on some parts. As SAM-BA Boot is running by default when the Flash is erased, the parts cannot be accessed even by JTAG under those conditions.

Problem Fix/Workaround

Use an external crystal or ceramic resonator on XIN/XOUT, or use the Main oscillator in bypass mode (applying a clock on XIN).

1.2.2 Flash Memory

1.2.2.1 FLASH: Flash Reading in 64-bit mode

Higher power consumption than expected can be seen when reading Flash in 64-bit mode.

Problem Fix/Workaround

Use 128-bit mode instead.

1.2.2.2 FLASH: Flash issue running at frequency lower than 5 MHz

When the system clock (MCK) is lower than 5 MHz with 2 Wait States (WS) programmed in the EEFC_FMR, the Cortex® fetches erroneous instructions.

Problem Fix/Workaround

Do not use 2 WS when running at a frequency lower than 5 MHz.

1.2.2.3 FLASH: Flash Programming

When writing data into the Flash memory plane (either through the EEFC, using the IAP function or FFPI), the data may not be correctly written (i.e the data written is not the one expected).

Problem Fix/Workaround

Set the number of Wait States (WS) at 6 (FWS = 6) during the programming.

1.2.3 Power Supplies

1.2.3.1 Power Supplies: VDDIN greater than VDDIO

VDDIN voltage can not be greater than VDDIO+0.5V

Problem Fix/Workaround

Apply a voltage on VDDIN lower or equal than VDDIO+0.5V

A fix is planned for the next chip revision.

1.2.4 Backup Mode

1.2.4.1 Backup Mode: VDDIN current consumption in Backup mode

In Backup mode (when VDDCORE is not powered), the ADC current consumption measured on VDDIN can be around 1 mA instead of less than 0.1 µA.

Problem Fix/Workaround

Use Wait Mode instead.

A fix is planned for the next chip revision.

1.2.5 Analog Comparator Controller (ACC)

1.2.5.1 ACC: Selection of the external analog inputs

The analog input pins of the PIO used for the Analog Comparator are not automatically configured in analog mode by the ACC.

Problem Fix/Workaround

Select the inputs by enabling the corresponding ADC channel through ADC_CHER register.

A fix is planned for the next chip revision.

1.2.6 Analog-to-Digital Converter (ADC)

1.2.6.1 ADC: Saturation

When the ADC works in saturation (measurements below 0V or above ADVREF) the results may be erratic.

Problem Fix/Workaround

A fix is planned for the next chip revision.

1.2.6.2 ADC: ADVREF Voltage Greater than VDDIO

ADVREF voltage can not be greater than VDDIO+0.5V (diode between ADVREF and VDDIO).

Problem Fix/Workaround

Apply a voltage on ADVREF lower than VDDIO+0.5V.

1.2.6.3 ADC: Comparison Window, High Threshold Value

High threshold bits[27:16] of the ADC Compare Window Register (ADC_CWR) are not functionally read/write and return 0 **when** ADC_CWR register is **read**. However, the high threshold value is correctly registered and behaves accordingly.

Problem Fix/Workaround

Ignore the read value of ADC_CWR high threshold bits [27:16].

1.2.6.4 *ADC: End of Conversion (EOC) Flag*

Performing a software reset (SWRST bit in ADC_CR) does not reset the EOCx flags of the ADC Interrupt Status Register.

Problem Fix/Workaround

Reading the ADC_CDRx channels clears the corresponding EOCx flag.

1.2.6.5 *ADC: Trigger Launch Only One Conversion*

A start command initiates a conversion sequence of one channel, but not of all activated channels as expected.

Problem Fix/Workaround

Send as many start commands as the number of activated channels, or use the free run mode.

1.2.7 Cyclic Redundancy Check Calculation (CRCCU)

1.2.7.1 *CRCCU: Compare Function*

The Transfer Reference Register TR_CRC offset is not CRCCU_DSCR+0x10 but CRCCU_DSCR+0xE0.

Problem Fix/Workaround

Two Problem Fix/Workarounds are possible:

- Either do not use the compare function and process the comparison by software
- Or set the TR_CRC at the address CRCCU_DSCR+0xE0

1.2.8 Digital-to-Analog Converter (DAC)

1.2.8.1 *DAC: DNL value*

The DNL (Differential Non Linearity) of the DAC performs at -6/+1 LSB instead of +/- 2 LSB as defined in the datasheet.

Problem Fix/Workaround

A fix is planned for the next chip revision.

1.2.9 Serial Wire and JTAG Debug Port (SWJ-DP)

1.2.9.1 *SWJ-DP: Current Consumption on VDDIO when TDO/PB5 is at high level*

When TDO/PB5 is set externally or internally to high, an overconsumption on VDDIO can be seen.

Problem Fix/Workaround

Set TDO as output at low level (PIO mode using SWD instead of JTAG) without pull-up.

A fix is planned for the next chip revision.

1.3 Errata: Device Identification “ES3”

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Problem Fix/Workaround

Two Workarounds are possible:

- Either do not use the compare function and process the comparison by software
- Or set the TR_CRC at the address CRCCU_DSCR+0xE0

Revision History

Doc. Rev	Comments	Change Request Ref.
11040B	Missing errata added to Section 1.2 “Errata: Device Identification “ES””. Section 1.3 “Errata: Device Identification “ES3”” updated --> same contents as corresponding Errata section in SAM3S Datasheet, but with ‘Marking ES3’ instead of ‘Revision A Parts’.	7206 - 7623 7596
11040A	First issue	

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