Atmel AT24C128C and AT24C256C

I²C Automotive Temperature Serial EEPROM

128K (16,384 x 8), 256K (32,768 x 8)

DATASHEET

Features

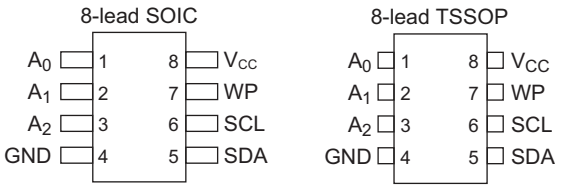
- Standard-voltage operation
  - V_{CC} = 2.5V to 5.5V
- Automotive temperature range –40°C to 125°C
- Internally organized 16,384 x 8 (128K), 32,768 x 8 (256K)
- 2-wire serial interface compatible with I²C
- Schmitt Trigger, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 400kHz compatibility
- Write Protect pin for hardware data protection
- 64 byte page write modes
- Partial page writes are allowed
- Self-timed write cycle (5ms max)
- High-reliability
  - Endurance: 1 million write cycles
  - Data retention: 100 years
- 8-lead JEDEC SOIC and 8-lead TSSOP packages

Description

The Atmel® AT24C128C/256C provides 131072/262144 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 16384/32768 words of eight bits each. The device is optimized for use in many automotive applications where low-power and low-voltage operation are essential. AT24C128C/256C is available in space-saving 8-lead JEDEC SOIC and 8-lead TSSOP packages and is accessed via a 2-wire serial interface. This device operates from 2.5V to 5.5V.

Figure 1. Pin Configurations

Pin Name	Function
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
A_0 - A_2	Address Inputs

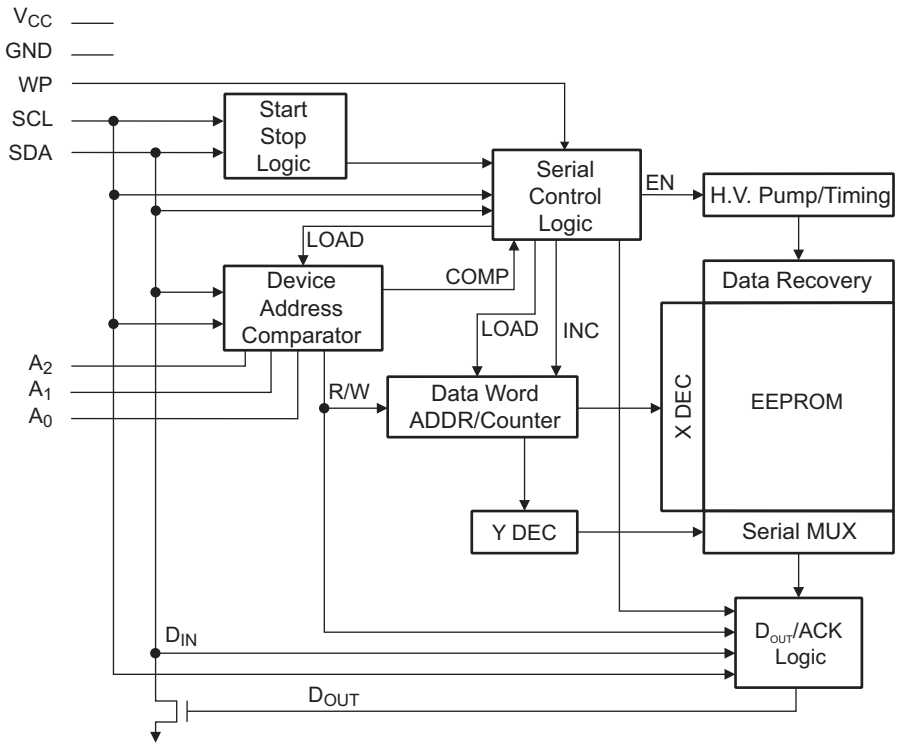


1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on any pin with respect to ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Block Diagram



3. Pin Description

Serial Clock (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device Addresses (A_2, A_1, A_0): The A_2, A_1, and A_0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other Atmel AT24C devices. When the pins are hardwired, as many as eight 128K/256K devices may be addressed on a single bus system (device addressing is discussed in detail in Section 6., Device Addressing). If the pins are left floating, the A_2, A_1, and A_0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF. If coupling is >3pF, Atmel recommends connecting the pin to GND.

Write Protect (WP): AT24C128C/256C has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

Table 3-1. Write Protect

WP Pin Status	Part of the Array Protected
	Atmel AT24C128C/256C
At V_{CC}	Full (128K/256K) Array
At GND	Normal Read/Write Operations

4. Memory Organization

AT24C128C/256C, 128K/256KSerial EEPROM: The 128K/256K is internally organized as 256/512 pages of 64 bytes each. Random word addressing requires a 14/15 bit data word address.

4.1 Pin Capacitance[1]

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

4.2 DC Characteristics

Applicable over recommended operating range from: T_A = -40°C to +125°C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		2.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	Read at 100kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	Write at 100kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB2}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		4.0	6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

4.3 AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +125°C, V_{CC} = +2.5V to +5.5V, CL = 1 TTL Gate and 100pF (unless otherwise noted).

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.6		µs
t_I	Noise Suppression Time(1)		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(2)	1.2		µs
$t_{HD.STA}$	Start Hold Time	0.6		µs
$t_{SU.STA}$	Start Set-up Time	0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		ns
t_R	Inputs Rise Time(2)		300	ns
t_F	Inputs Fall Time(2)		300	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		5	ms
Endurance(2)	5.0V, 25°C, Page Mode	1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested (T_A = 25°C).
2. This parameter is characterized.

5. Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 5-4 on page 7). Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 5-5 on page 7).

Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 5-5 on page 7).

Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Standby Mode: The AT24C128C/256C features a low-power standby mode which is enabled:

- Upon power-up.
- After the receipt of the stop bit and the completion of any internal operations.

Memory Reset: After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Clock up to nine cycles,
2. Look for SDA high in each cycle while SCL is high,
3. Create a start condition.

Figure 5-1. Memory Reset

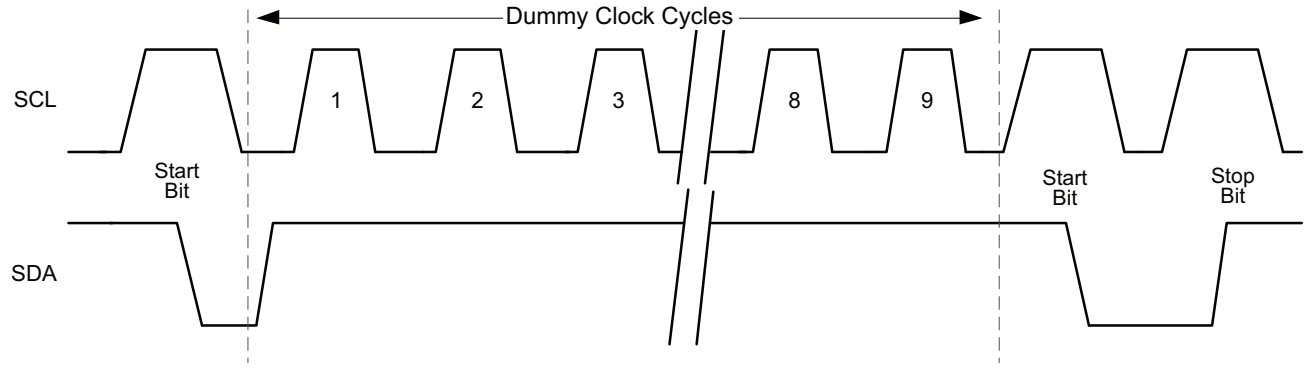


Figure 5-2. Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O

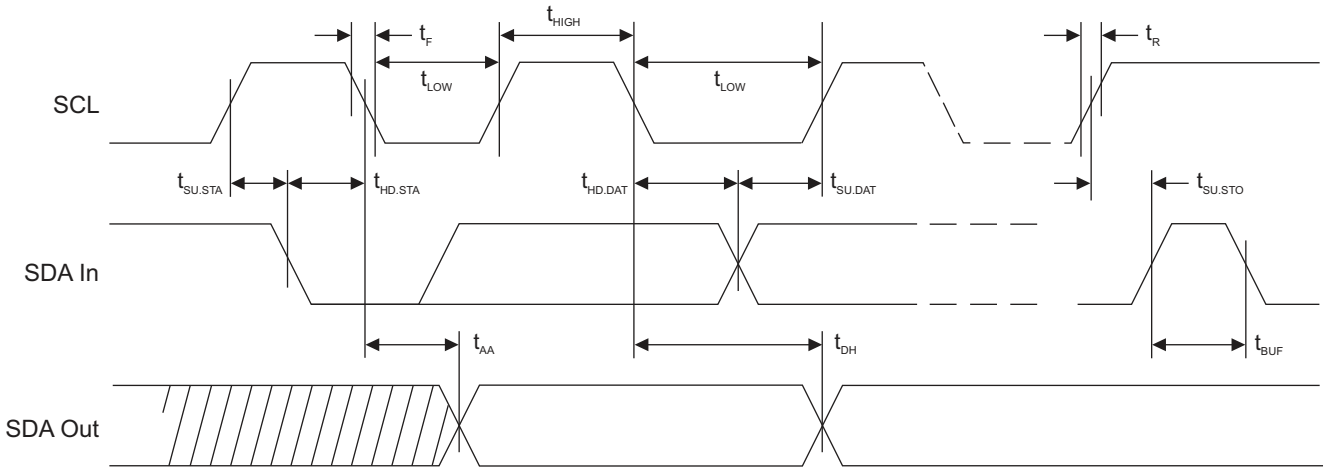
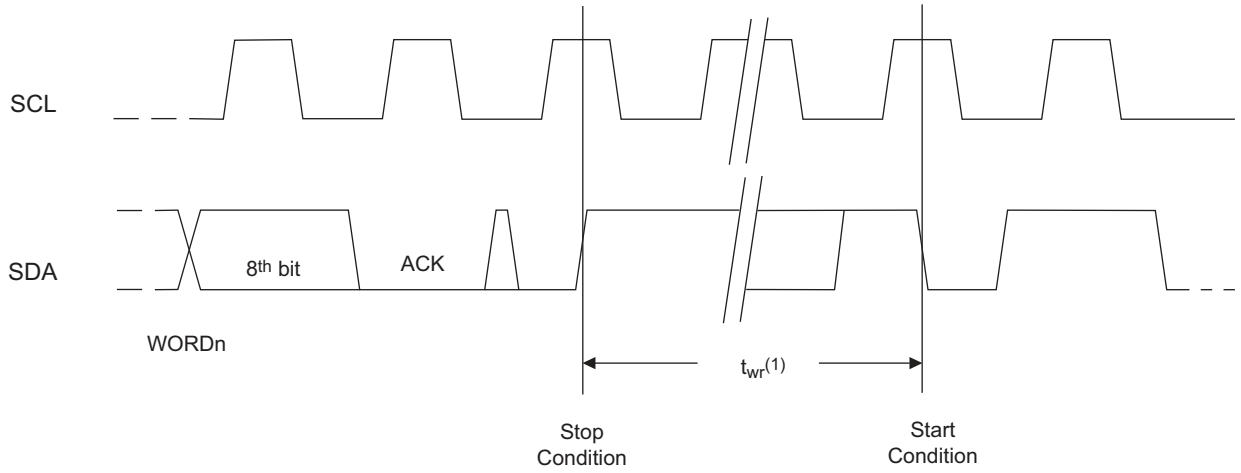


Figure 5-3. Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 5-4. Data Validity

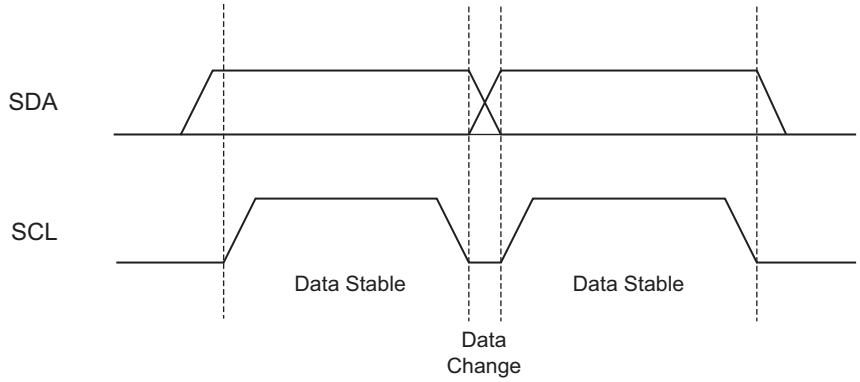


Figure 5-5. Start and Stop Definition

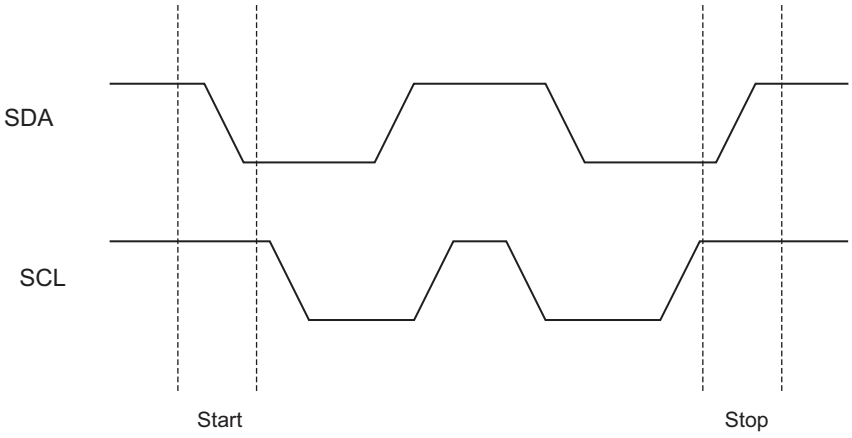
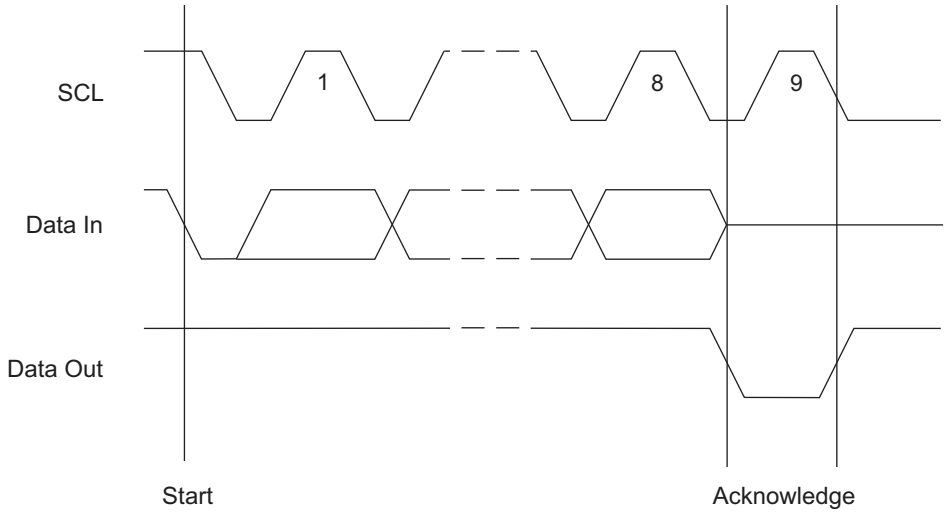


Figure 5-6. Output Acknowledge



6. Device Addressing

The 128K/256K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 8-1 on page 9).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 128K/256K uses the three device address bits, A2, A1, and A0, to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A_2, A_1, and A_0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a Write operation is initiated if this bit is low.

If the device address meets the requirements listed above, the device will acknowledge with a zero by pulling the SDA signal low. If the comparison is not made, the device will return to a standby state and the SDA signal will float high.

7. Write Operations

Byte Write: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8-2 on page 9).

Page Write: The 128K/256K EEPROM is capable of 64 byte page writes.

A Page Write is initiated the same as a Byte Write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to sixty-three more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the Page Write sequence with a stop condition (see Figure 8-3 on page 10).

The data word address lower six bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than thirty-one data words are transmitted to the EEPROM, the data word address will roll-over and previous data will be overwritten.

Acknowledge Polling: Once the internally timed Write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

8. Read Operations

Read operations are initiated the same way as Write operations with the exception that the Read/Write select bit in the device address word is set to one. There are three read operations: Current Address Read, Random Address Read, and Sequential Read.

Current Address Read: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during Read is from the last byte of the last memory page to the first byte of the first page. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following Stop condition (see Figure 8-4 on page 10).

Random Read: A Random Read requires a dummy Byte Write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 8-5 on page 10).

Sequential Read: Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not send an acknowledge (pull the SDA signal low), but does generate the stop condition. (see Figure 8-6 on page 10).

Figure 8-1. Device Address

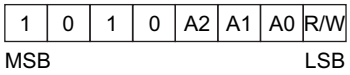
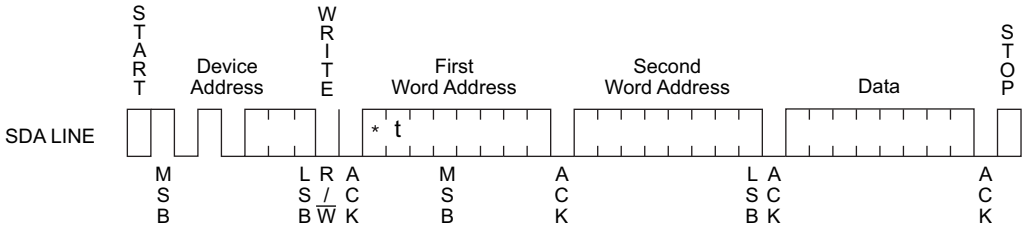
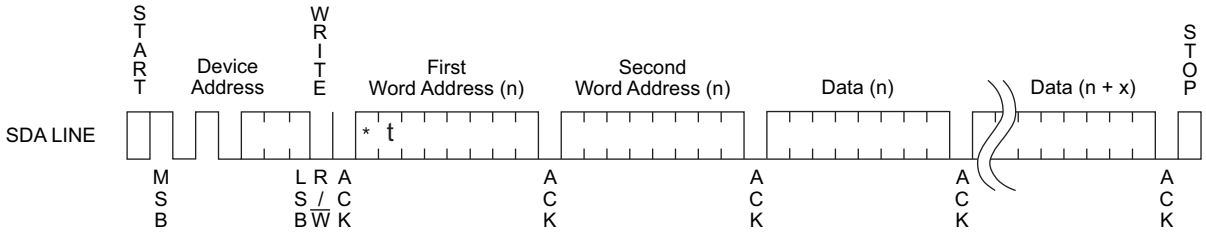


Figure 8-2. Byte Write



Notes: 1. * = Don't care bit
2. t = Don't care bit for AT24C128C

Figure 8-3. Page Write



Notes: 1. * = Don't care bit
2. t = Don't care bit for AT24C128C

Figure 8-4. Current Address Read

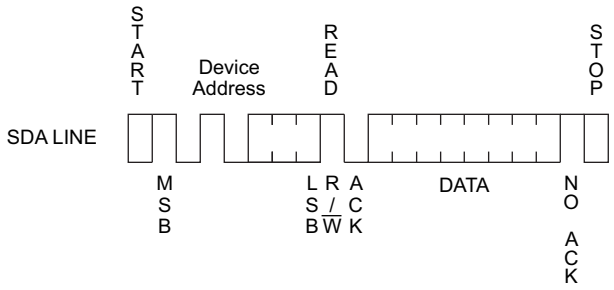
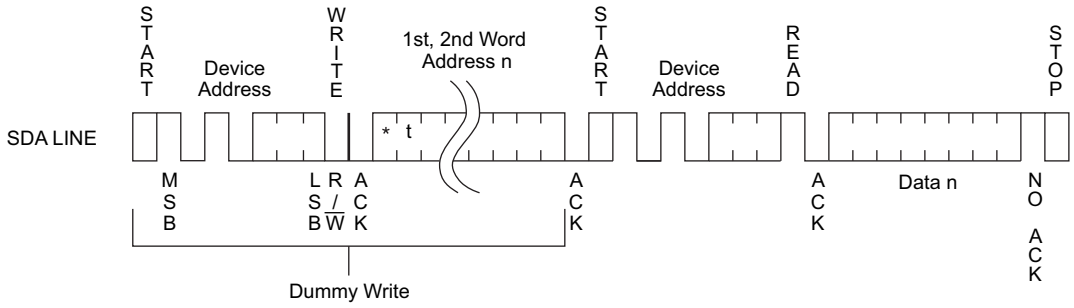
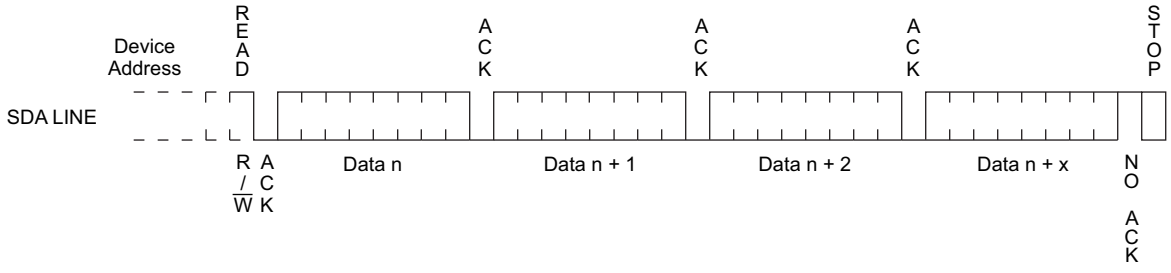


Figure 8-5. Random Read



Notes: 1. * = Don't care bit
2. t = Don't care bit for AT24C128C

Figure 8-6. Sequential Read

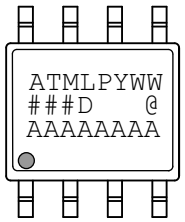


8.1 Power Recommendation

The device internal POR (Power-On Reset) threshold is just below the minimum operating voltage of the device. Power shall rise monotonically from 0.0Vdc to full V_{CC} in less than 1ms. Hold at full V_{CC} for at least 100µs before the first operation. Power shall drop from full V_{CC} to 0.0Vdc in less than 1ms. Power dropping to a non-zero level and then slowly going to zero is *not* recommended. Power shall remain off (0.0Vdc) for 0.5s minimum. Please consult Atmel if your power conditions do not meet the above recommendations.

9. Product Markings

AT24C128C and AT24C256C: Package Marking Information

8-lead SOIC	8-lead TSSOP
	

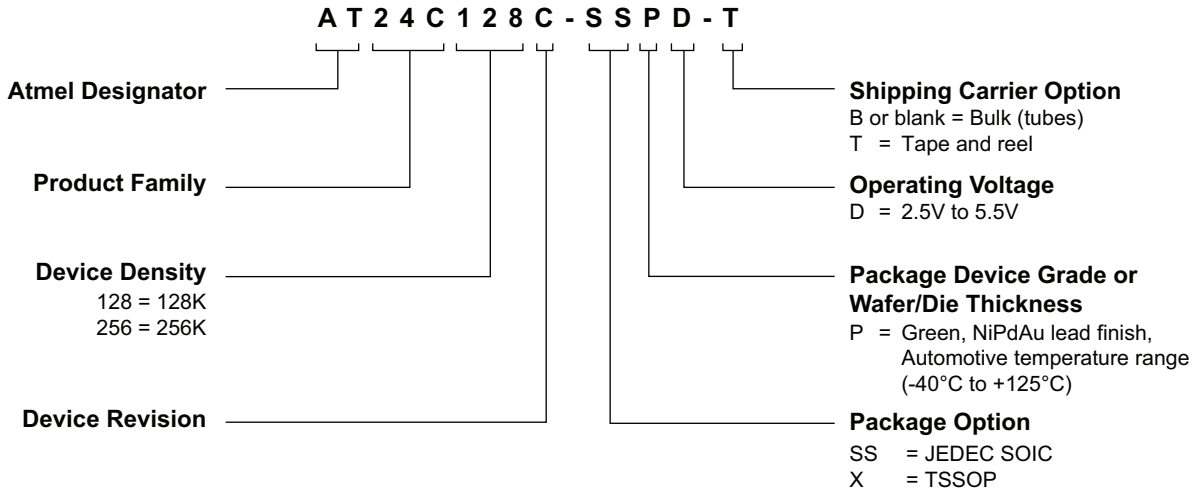
Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT24C128C		Truncation Code ###: 2DC	
AT24C256C		Truncation Code ###: 2EC	
Date Codes			**Voltages**
Y = Year		M = Month	WW = Work Week of Assembly	D: 2.5V min
2: 2012	6: 2016	A: January	02: Week 2	
3: 2013	7: 2017	B: February	04: Week 4	
4: 2014	8: 2018	...	...	
5: 2015	9: 2019	L: December	52: Week 52	
Country of Assembly		**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number		P: Automotive/NiPdAu
Trace Code				**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ				AT: Atmel ATM: Atmel ATML: Atmel

3/19/12

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	24C128-256CAM, AT24C128C and AT24C256C Automotive Package Marking Information	24C128-256CAM	B

10. Ordering Code Details



11. Ordering Code Information

11.1 Atmel AT24C128C Ordering Information

Atmel Ordering Code	Package	Voltage	Operation Range
AT24C128C-SSPD	8S1	2.5V to 5.5V	NiPdAu Lead-free/Halogen-free Automotive Temperature (–40°C to 125°C)
AT24C128C-SSPD-T(1)			
AT24C128C-XPD	8X		
AT24C128C-XPD-T(1)			

Note: 1. Tape and reel delivery:
- SOIC 4k/reel
- TSSOP 5k/reel

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 0.170" wide, Thin Shrink Small Outline (TSSOP)

11.2 Atmel AT24C256C Ordering Information

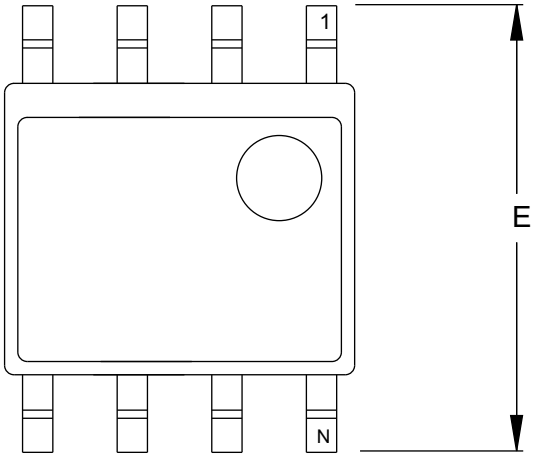
Atmel Ordering Code	Package		Operation Range
AT24C256C-SSPD	8S1	2.5V to 5.5V	NiPdAu Lead-free/Halogen-free Automotive Temperature (–40°C to 125°C)
AT24C256C-SSPD-T(1)			
AT24C256C-XPD	8X		
AT24C256C-XPD-T(1)			

Note: 1. Tape and reel delivery:
- SOIC 4k/reel
- TSSOP 5k/reel

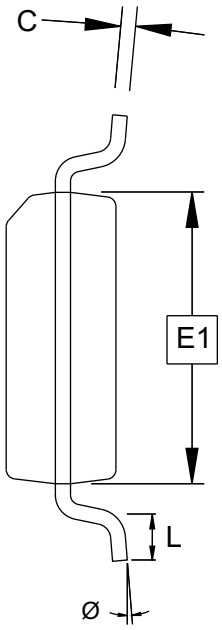
Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 0.170" wide, Thin Shrink Small Outline (TSSOP)

12. Packaging Information

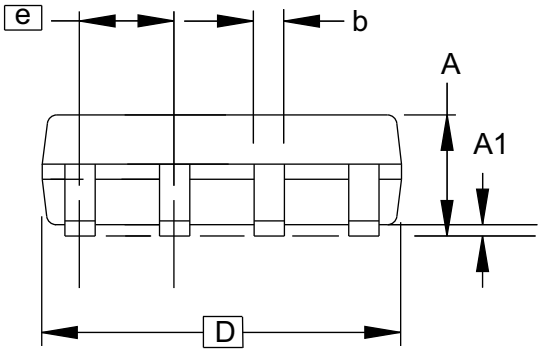
12.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

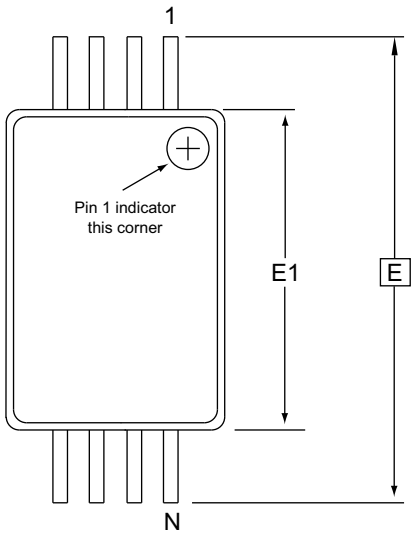
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

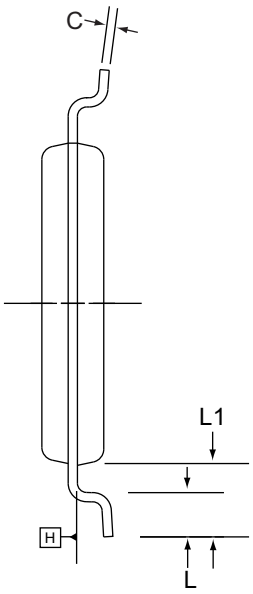
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	GPC SWB	DRAWING NO. 8S1	REV. G

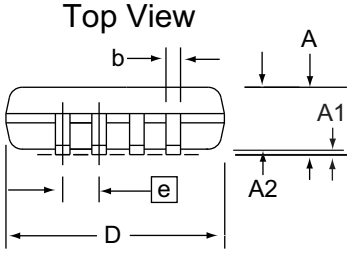
12.2 8X — 8-lead TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

12/8/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** E

13. Revision History

Doc. Rev.	Date	Comments
8818B	10/2012	Remove preliminary status. Update 8X — TSSOP package drawing. Update Atmel logos and disclaimer/copy page.
8818A	04/2012	Initial document release

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