

FQP13N50C / FQPF13N50C

N-Channel QFET® MOSFET

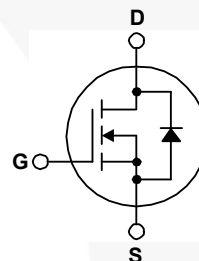
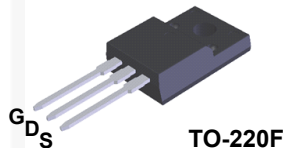
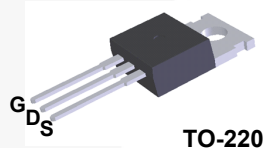
500 V, 13 A, 480 mΩ

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Features

- 13 A, 500 V, $R_{DS(on)} = 480 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 6.5 \text{ A}$
- Low Gate Charge (Typ. 43 nC)
- Low C_{rss} (Typ. 20 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQP13N50C	FQPF13N50C	Units
V_{DSS}	Drain-Source Voltage	500		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	13	13 *	A
		8	8 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	52	52 *	A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	860		mJ
I_{AR}	Avalanche Current (Note 1)	13		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	19.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	195	48	W
		1.56	0.39	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FQP13N50C	FQPF13N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.64	2.58	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP13N50C_F105	FQP13N50C	TO-220	Tube	N/A	N/A	50 units
FQPF13N50C_F105	FQPF13N50C	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics T_c = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	500	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 400 V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 6.5 A	--	0.39	0.48	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 6.5 A	--	15	--	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	1580	2055	pF
C _{oss}	Output Capacitance		--	180	235	pF
C _{rss}	Reverse Transfer Capacitance		--	20	25	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 13 A, R _G = 25 Ω (Note 4)	--	25	60	ns
t _r	Turn-On Rise Time		--	100	210	ns
t _{d(off)}	Turn-Off Delay Time		--	130	270	ns
t _f	Turn-Off Fall Time		--	100	210	ns
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 13 A, V _{GS} = 10 V (Note 4)	--	43	56	nC
Q _{gs}	Gate-Source Charge		--	7.5	--	nC
Q _{gd}	Gate-Drain Charge		--	18.5	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current	--	--	13	A	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	52	A	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 13 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 13 A,	--	410	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	--	4.5	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 6 mH, I_{AS} = 13 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 13 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Characteristics

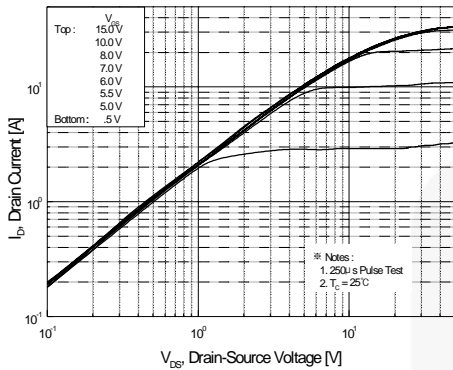


Figure 1. On-Region Characteristics

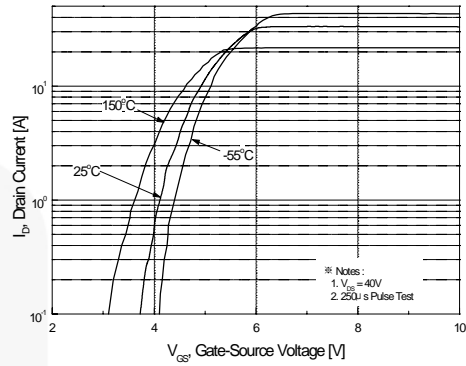


Figure 2. Transfer Characteristics

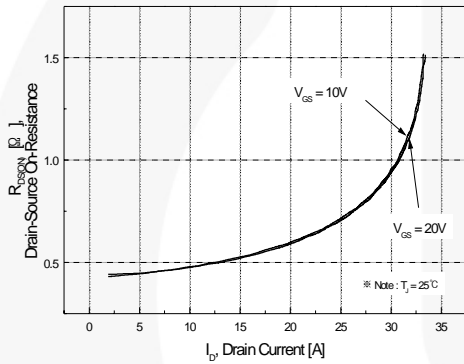


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

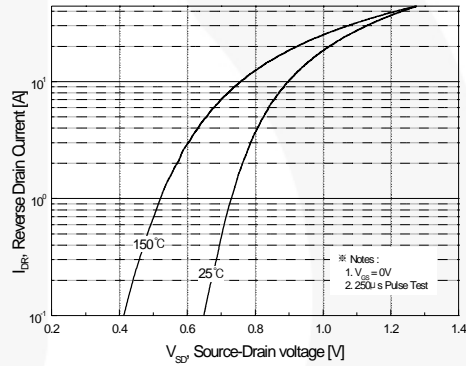


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

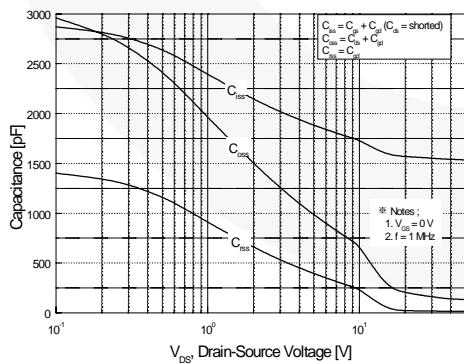


Figure 5. Capacitance Characteristics

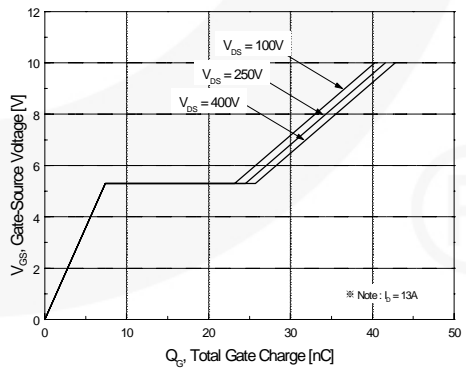


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

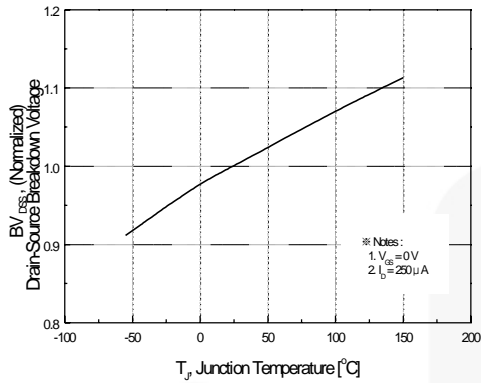


Figure 7. Breakdown Voltage Variation vs Temperature

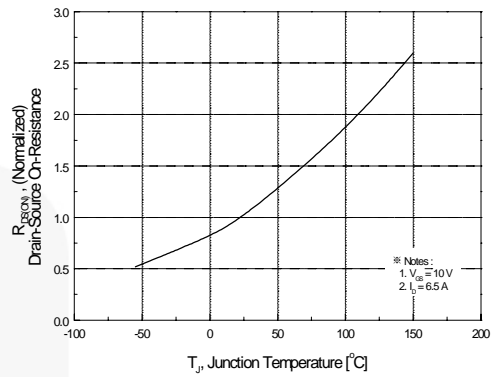


Figure 8. On-Resistance Variation vs Temperature

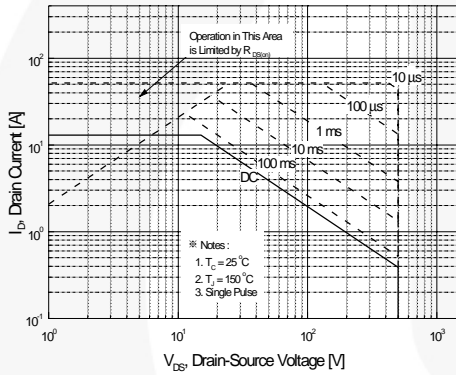


Figure 9-1. Maximum Safe Operating Area for FQP13N50C

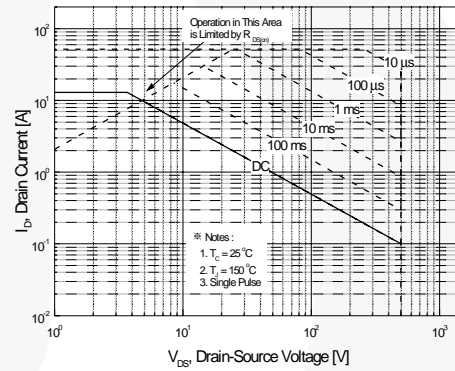


Figure 9-2. Maximum Safe Operating Area for FQPF13N50C

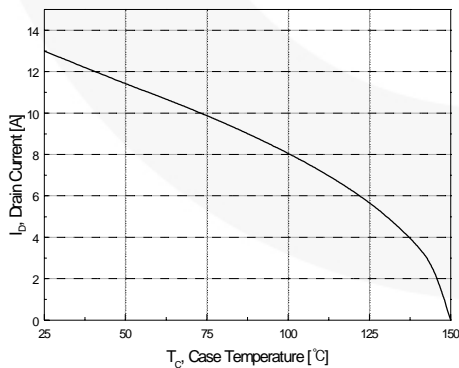


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (continued)

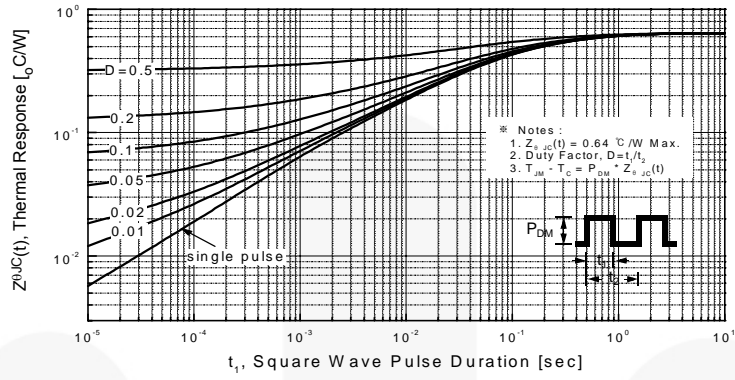


Figure 11-1. Transient Thermal Response Curve for FQP13N50C

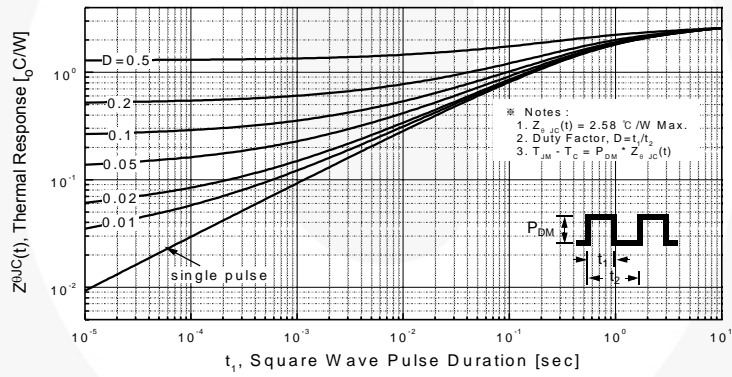


Figure 11-2. Transient Thermal Response Curve for FQPF13N50C

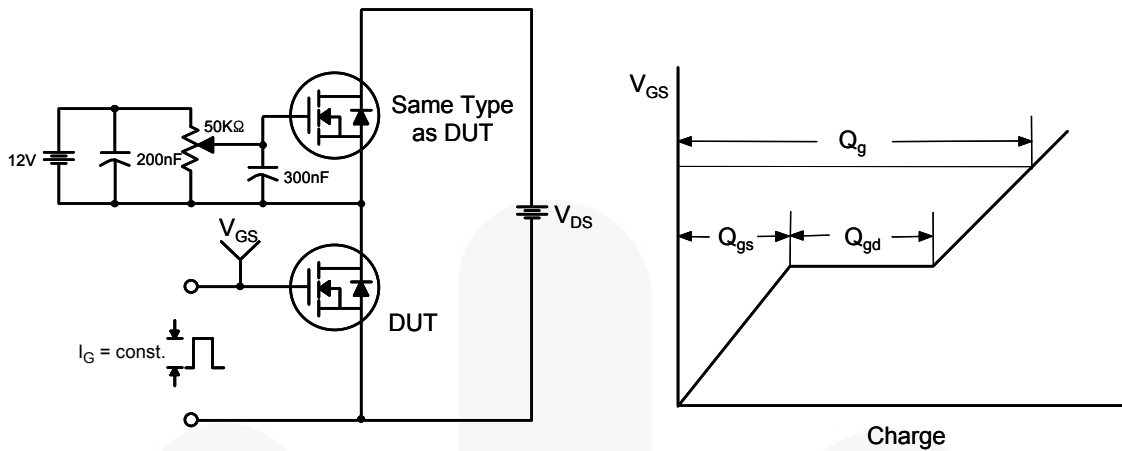


Figure 12. Gate Charge Test Circuit & Waveform

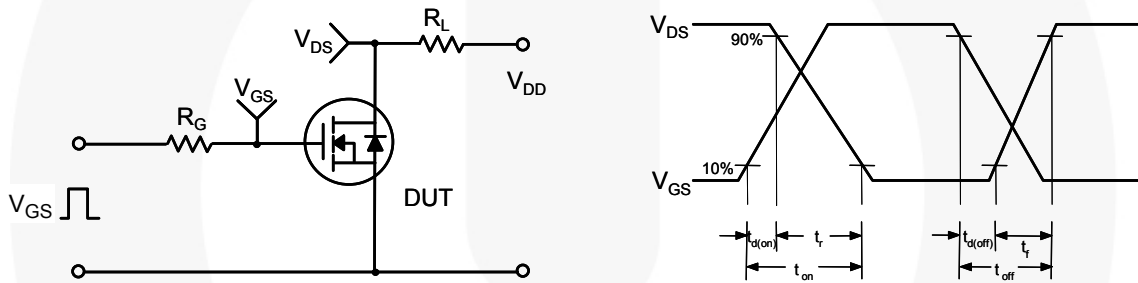


Figure 13. Resistive Switching Test Circuit & Waveforms

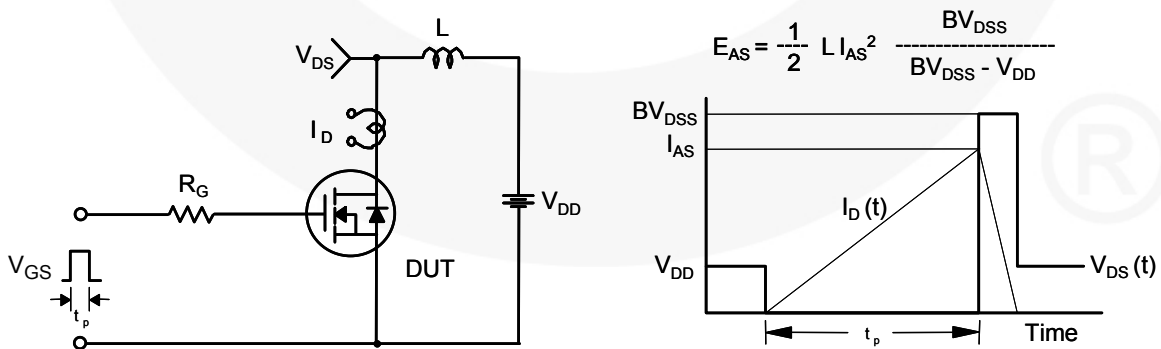


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

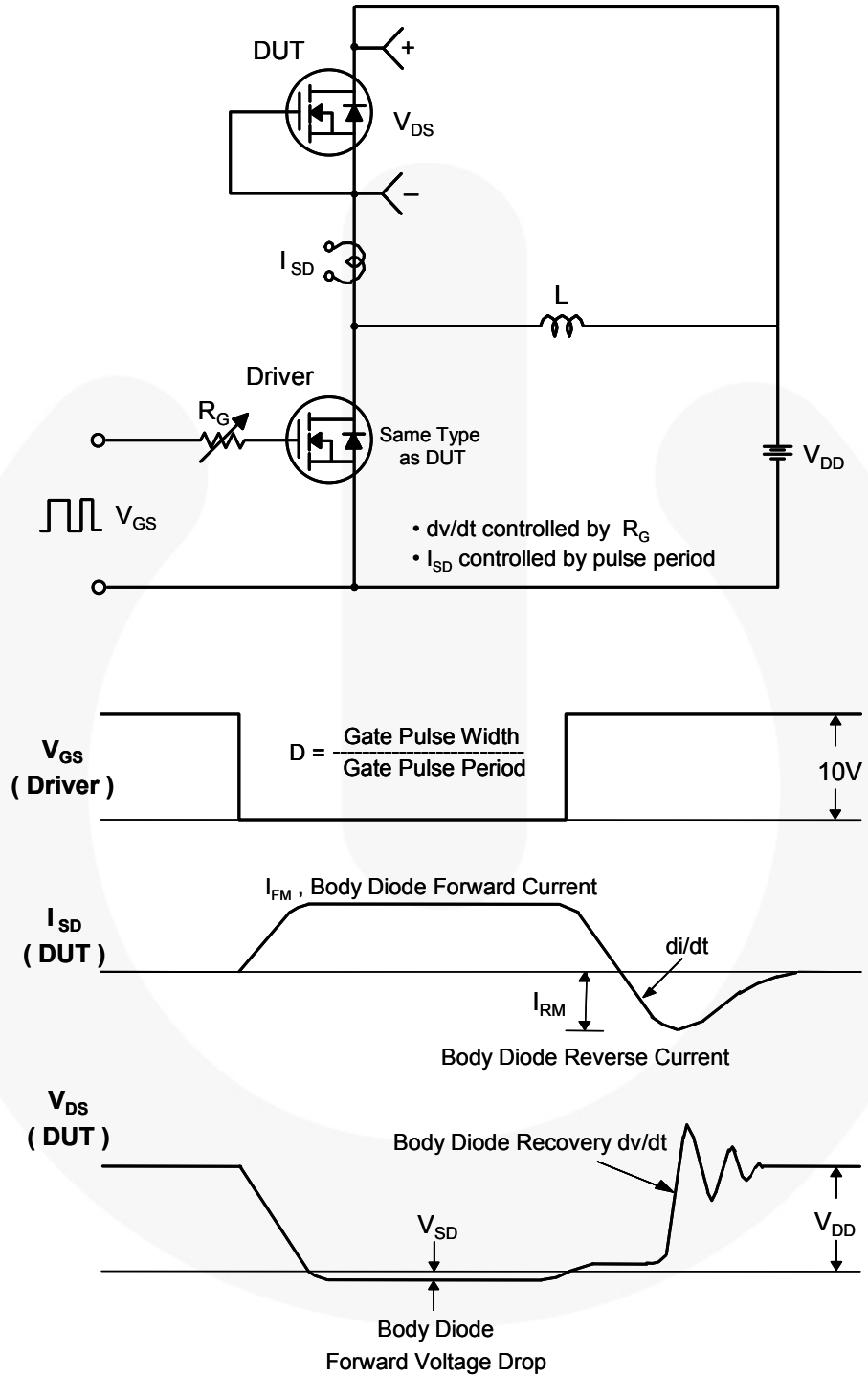


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

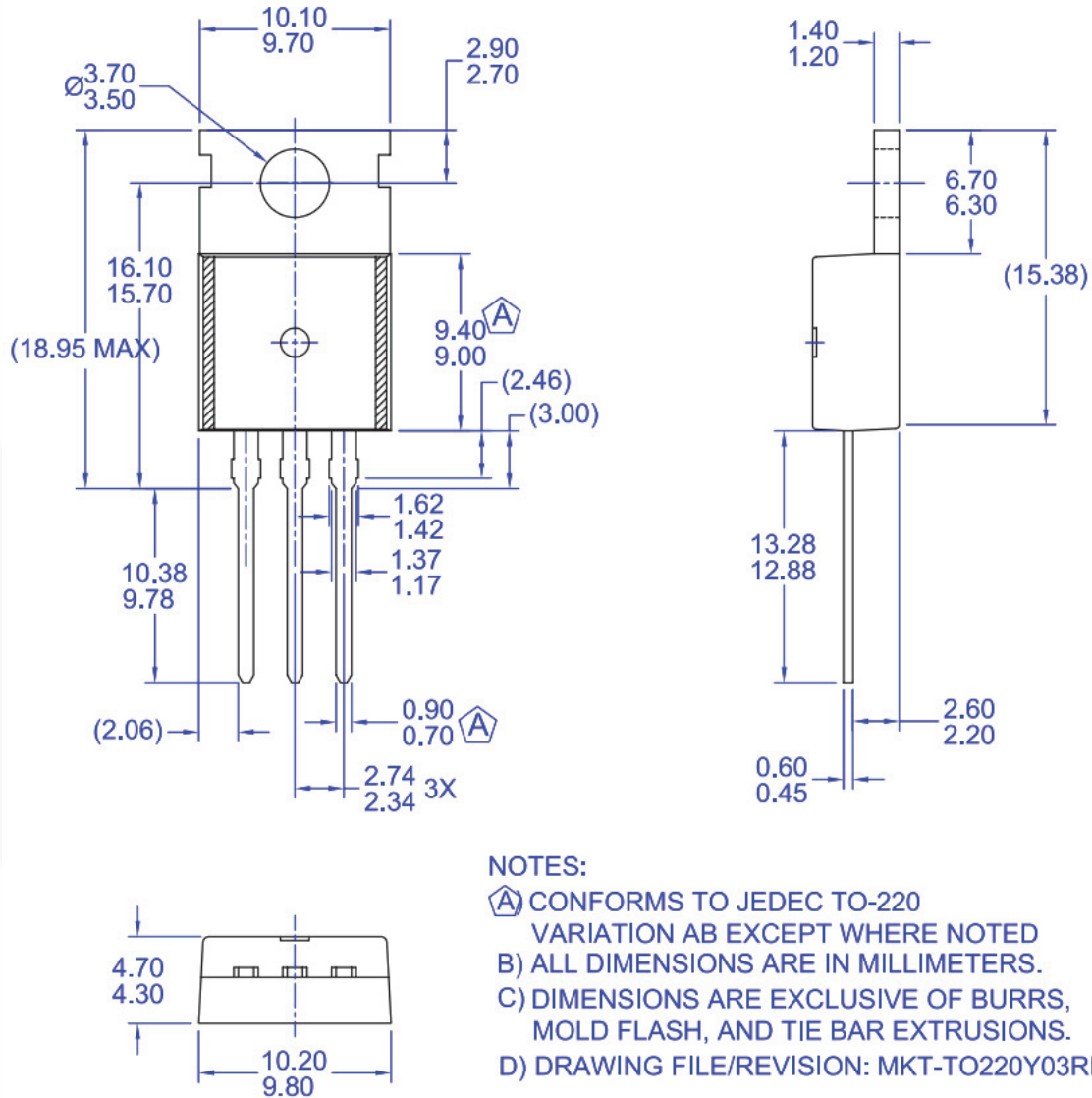


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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