Wide Operating Range, Valley Mode, No R_{SENSE}™ Synchronous Step-Down Controller

FEATURES

- **Wide V_{IN} Range: 2.2V to 22V**
- **Internal Boost Provides 6V Gate Drive For V_{IN} Down to 2.2V**
- **No Sensing Resistor Required**
- **Dual N-Channel MOSFET Synchronous Drive**
- Valley Current Mode Control
- Optimized for High Step-Down Ratio
- Power Good Output Voltage Monitor
- 0.8V Reference
- Three Pin-Selected Current Limit Levels
- Constant Switching Frequency: 300kHz
- Programmable Soft-Start
- Output Voltage Tracking
- Available in 16-Pin 5mm × 3mm DFN

APPLICATIONS

- Notebook and Palmtop Computers, PDA
- Portable Instruments
- Distributed Power Systems

DESCRIPTION

The LT®3740 is a synchronous step-down switching regulator controller that drives N-channel power MOSFET stages. The controller uses valley current mode architecture to achieve very low duty cycles with excellent transient response without requiring a sense resistor.

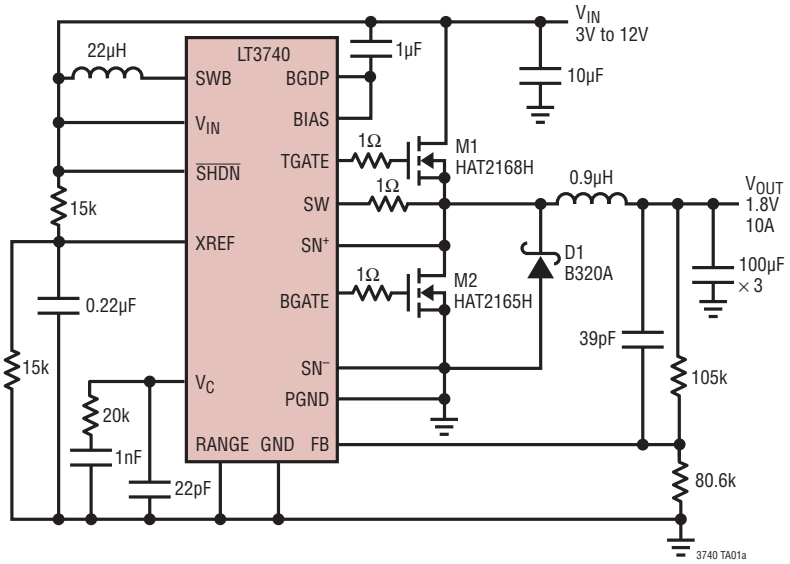
The LT3740 includes an internal step-up converter to provide a bias 7.8V higher than the input voltage for the drive. This enables the part to work from an input voltage as low as 2.2V.

The XREF pin is an external reference input that allows the user to override the internal 0.8V feedback reference with any lower value, allowing full control of the output voltage during operation, output voltage tracking or soft-start.

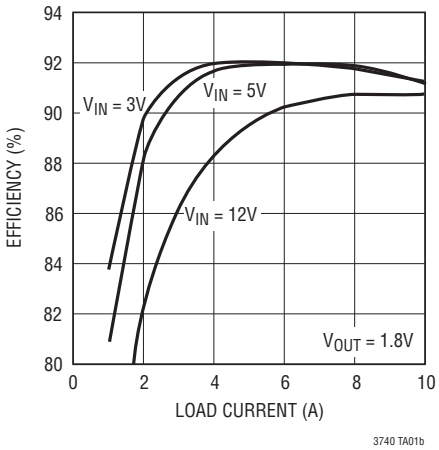
The LT3740 has three current limit levels that can be chosen by connecting the RANGE pin to ground, open, and input respectively.

TYPICAL APPLICATION

High Efficiency Step-Down Converter



Efficiency vs Load Current

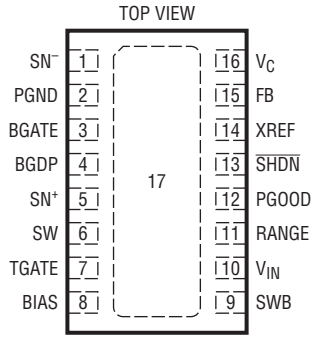


ABSOLUTE MAXIMUM RATINGS

(Note 1)

SN^-, BGATE, V_C, FB, XREF, PGOOD Voltages 10V
V_{IN}, $\overline{SHDN}$, SW, Range Voltages 22V
BIAS, TGATE, BGDP, SN^+ Voltages 32V
SWB Voltage 36V
Maximum Junction Temperature.....125°C
Operating Temperature Range (Note 2)....–40°C to 85°C
Storage Temperature Range.....–65°C to 125°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD IS GND (PIN 17), MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3740EDHC#PBF	LT3740EDHC#TRPBF	3740	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3740EDHC	LT3740EDHC#TR	3740	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 5V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operation Voltage		●	2.2			V
Maximum Operation Voltage		●			22	V
Input Supply Current	$\overline{SHDN}$ = 0V $\overline{SHDN}$ = 5V, BIAS = 14V, FB = 1.5V			0.6 2.5		µA mA
Feedback Reference Voltage	XREF=1V	●	794	800	808	mV
Feedback Voltage Line Regulation	V_{IN} = 2.5V to 22V			0.006		%
FB Pin Input Current	FB = 800mV			230		nA
Error Amplifier Transconductance	V_C = 1.2V			380		µS
Controller Switching Frequency		●	260	300	330	kHz
Minimum BGATE On Time (Note 3)				500	700	ns
Current Limit	RANGE = 0V RANGE = Open RANGE = V_{IN}		25 55 80	50 80 105	85 115 140	mV mV mV
Reverse Current Limit				35		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 5V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Voltage to Enable Device		●	1.1			V
$\overline{SHDN}$ Voltage to Disable Device		●			0.5	V
TGATE On Voltage				5.5		V
TGATE Off Voltage				0.2		V
BGATE On Voltage				5.5		V
BGATE Off Voltage				0.2		V
TGATE Rise Time	C_{LOAD} = 3300pF			30		ns
TGATE Fall Time	C_{LOAD} = 3300pF			30		ns
BGATE Rise Time	C_{LOAD} = 3300pF			50		ns
BGATE Fall Time	C_{LOAD} = 3300pF			50		ns
PGOOD Threshold		●	720	740	765	mV
PGOOD Low Voltage	I_{PGOOD} = 100µA	●			0.2	V
PGOOD Current Capacity			500			µA
Internal Boost Switching Frequency			0.8	1	1.2	MHz
Internal Boost Switch Current Limit			360	440	520	mA
(BIAS – V_{IN}) in Operation				7.8		V
(BIAS – V_{IN}) to Start Controller				7.2		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

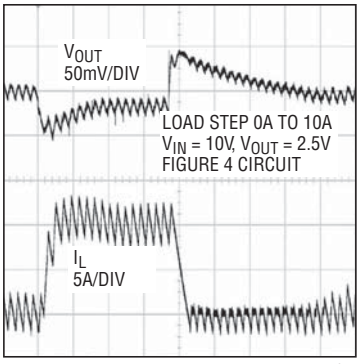
Note 2: The LT3740E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The minimum off time of the LT3740 application consists of the minimum BGATE on time, the delay from TGATE OFF to BGATE ON (80ns) and the delay from BGATE OFF to TGATE ON (80ns).

TYPICAL PERFORMANCE CHARACTERISTICS

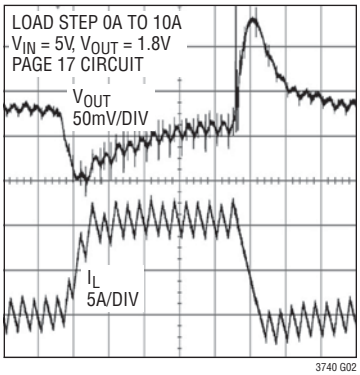
(T_A = 25°C, unless otherwise noted)

Transient Response



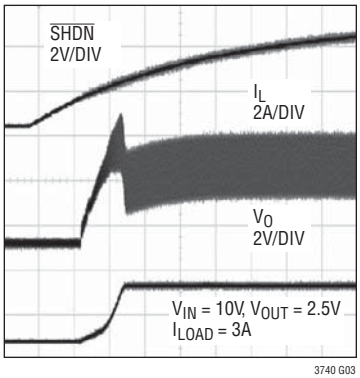
20µs/DIV

Transient Response



10µs/DIV

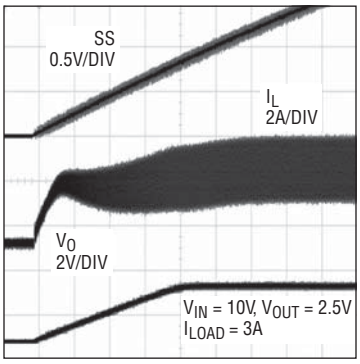
Shutdown Pin Start-Up



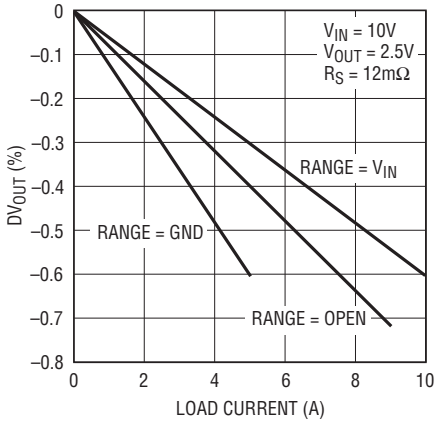
2ms/DIV

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

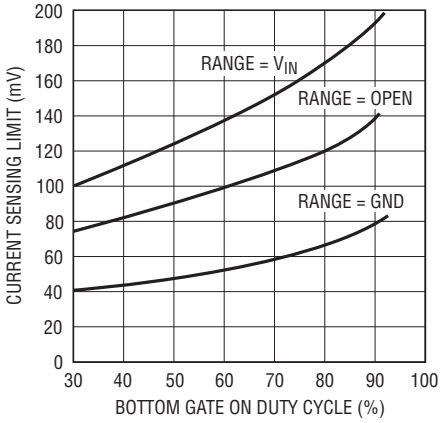
XREF Pin Start-Up



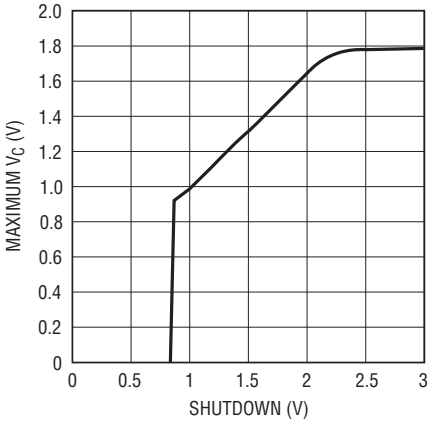
Load Regulation



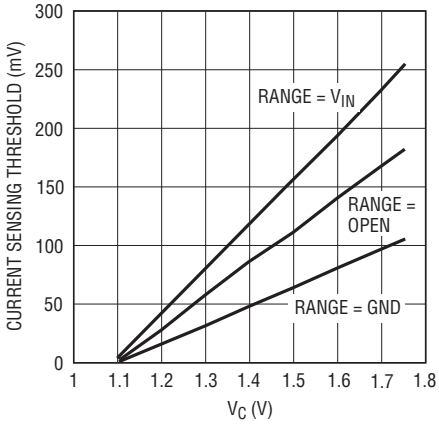
Current Limit vs Bottom Gate On-Time



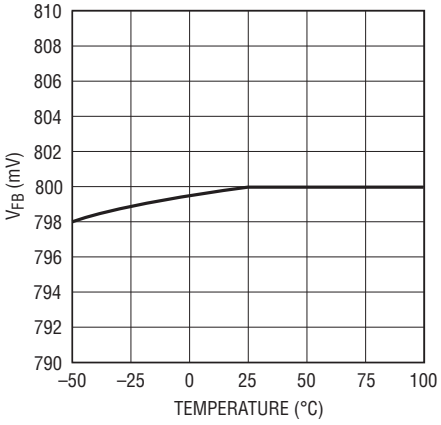
Shutdown vs Maximum V_C



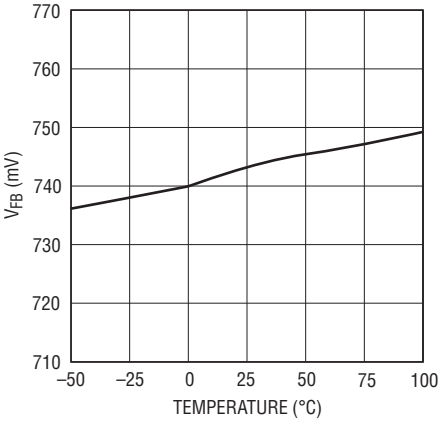
V_C vs Current Sensing Threshold



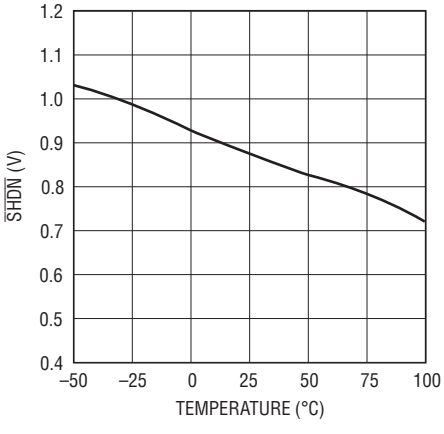
Feedback Reference Voltage vs Temperature



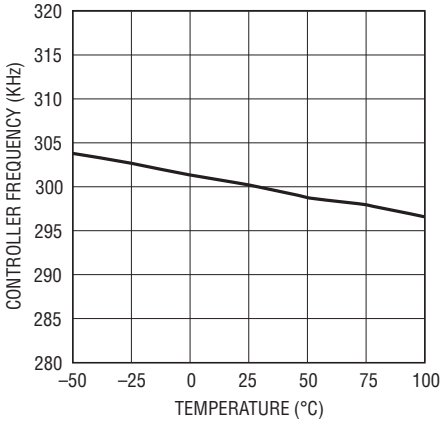
PGOOD Threshold vs Temperature



Shutdown Threshold vs Temperature

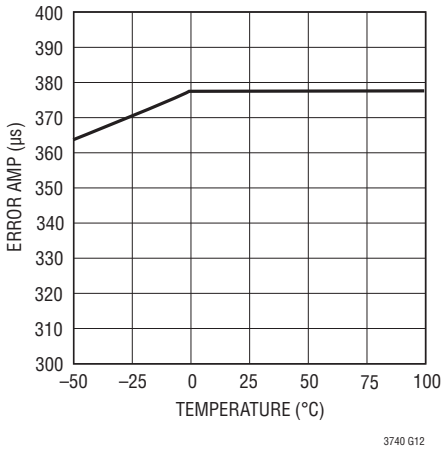


Switching Frequency vs Temperature

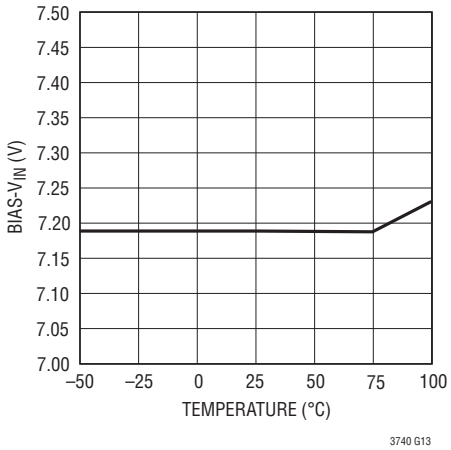


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

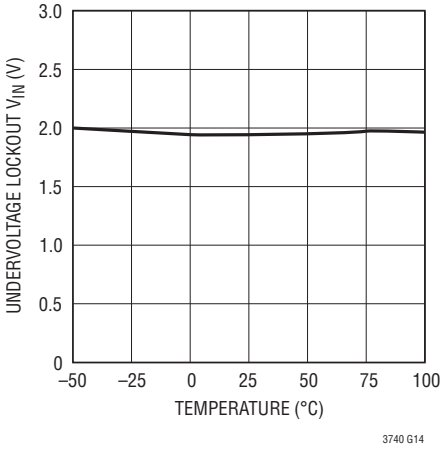
Error Amplifier Transconductance vs Temperature



BIAS-V_{IN} to Enable Controller vs Temperature



Undervoltage Lockout Threshold vs Temperature



PIN FUNCTIONS

SN^- (Pin 1): Negative Current Sensing Pin. Connect this pin to the source of the bottom MOSFET for No R_{SENSE} or to a current sense resistor.

PGND (Pin 2): Power Ground. Connect this pin closely to the source of the bottom N-channel MOSFET.

BGATE (Pin 3): Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET.

BGDP (Pin 4): Bottom Gate Drive Power Supply. Connect this pin to a voltage source higher than 7V (V_{IN} or BIAS).

SN^+ (Pin 5): Positive Current Sensing Pin. Connect this pin to the drain of the bottom MOSFET for No R_{SENSE} or to a current sense resistor.

SW (Pin 6): Switch Node. Connect this pin to the source of the top N-channel MOSFET and the drain of the bottom N-channel MOSFET.

TGATE (Pin 7): Top Gate Drive. Drives the gate of the top N-channel MOSFET to BIAS.

BIAS (Pin 8): Top Gate Drive Power Supply. Connect a capacitor between this pin and V_{IN}.

SWB (Pin 9): Switch Pin of the Internal Boost. Connect the boost inductor here.

V_{IN} (Pin 10): Input Supply Pin. Must be locally bypassed with a capacitor.

RANGE (Pin 11): Current Limit Range Select Pin. Ground this pin for 50mV current sense voltage limit. Leave this pin open for 80mV current sense voltage limit. Connect this pin to V_{IN} for current sense voltage limit of 105mV.

PGOOD (Pin 12): Power Good Output. Open collector logic output that is pulled low when the FB voltage lower than 720mV.

$\overline{SHDN}$ (Pin 13): Shutdown Pin. Connect to 2.5V or higher to enable device; 0.5V or less to disable device. Also, this pin functions as soft-start when a voltage ramp is applied.

XREF (Pin 14): External Reference Pin. This pin sets the FB voltage externally between 0V and 0.8V. It can be used to slave the output voltage during normal operation or the output start-up behavior to an external signal source. Tie this pin to 1V or higher to use the internal 0.8V reference.

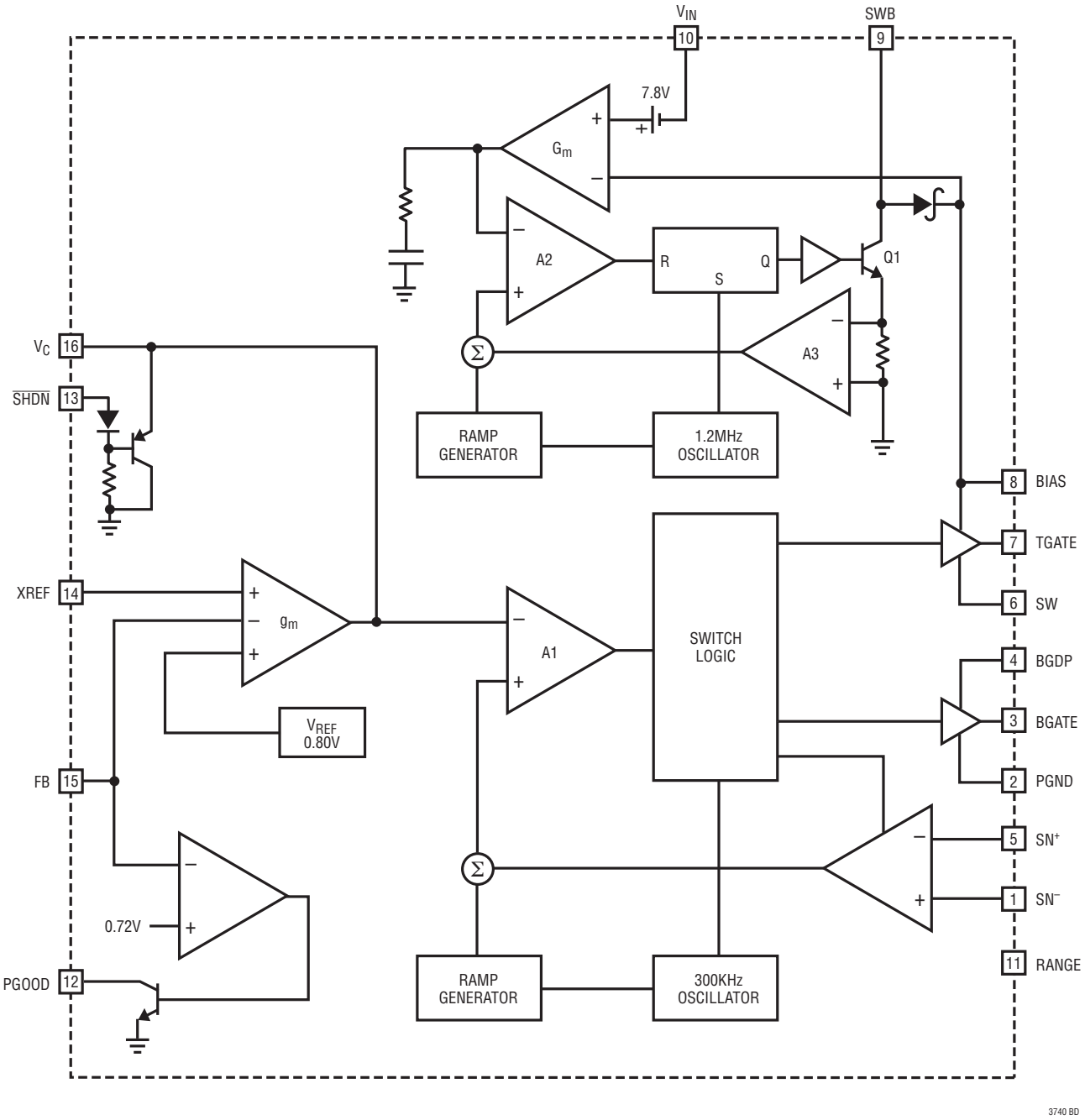
FB (Pin 15): Feedback Pin. Pin voltage is regulated to 0.8V if internal reference is used or to the XREF pin if voltage is between 0V and 0.8V. Connect the feedback resistor divider to this pin.

PIN FUNCTIONS

V_C (Pin 16): Error Amplifier Compensation Pin. Connect the external compensation RC to this pin. The current comparator threshold increases with the voltage of this pin.

Exposed Pad (Pin 17): Ground. Must be soldered to PCB ground.

BLOCK DIAGRAM



OPERATION

The LT3740 is a constant-frequency, valley current mode controller for DC/DC step-down converters. At the start of each oscillator cycle, the switch logic is set, which turns on the bottom MOSFET. After a 500ns blanking time, the bottom MOSFET current is sensed and added to a stabilizing ramp, and the resulting sum is fed into the PWM comparator A1. When this voltage goes below the voltage at V_C pin, the switch logic is reset, which turns off the bottom MOSFET, and turns on the top MOSFET. The top MOSFET remains on until the next oscillator cycle. The bottom MOSFET current can be determined by sensing the voltage between the drain and source of the MOSFET using the bottom MOSFET on-resistance, or by sensing the voltage drop across a resistor between the source of the bottom MOSFET and ground. The two current sensing pins are SN^+ and SN^-. The g_m error amplifier adjusts the voltage on the V_C pin by comparing the feedback signal V_{FB} with the reference, which is determined by the lower of the internal 0.8V reference and the voltage at the XREF pin. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered.

The LT3740 features an open collector PGOOD signal. When the voltage at FB pin is less than 720mV, the PGOOD output is pulled low by a NPN transistor. The 720mV threshold is independent of the voltage on XREF pin.

The small internal step-up converter provides a BIAS voltage about 7V higher than the input voltage V_{IN} for the drive of the top MOSFET. This enables the LT3740 to work from an input voltage as low as 2.2V. The controller starts operation when the BIAS pin is about 7V higher than V_{IN} pin. The voltage supply for the bottom MOSFET drive is provided through the BGDP pin. For V_{IN} lower than 7V, BGDP should be connected to BIAS to get enough drive bias. For V_{IN} higher than 7V, BGDP can be connected directly to V_{IN} to reduce power loss.

Grounding the $\overline{SHDN}$ pin turns both the internal step-up converter and the controller off. The $\overline{SHDN}$ pin can also be used to implement an optional soft-start function.

Start-Up and Shutdown

During normal operation, when the feedback voltage is above 720mV, the LT3740 operates in forced continuous mode. When the feedback voltage is below 720mV, either during the start-up or because an external reference is applied, a zero current detect comparator is enabled to monitor the on-state bottom MOSFET current. When the current reaches zero, both the top and bottom MOSFETs are turned off, resulting in discontinuous operation. During the time that both top and bottom MOSFETs are off, no current signal is fed into the LT3740. Only the stabilizing ramp is fed into the PWM comparator to decide the next turn on of the top MOSFET.

The LT3740 uses the $\overline{SHDN}$ pin to implement one of the two different startup schemes. As shown in the block diagram, the V_C pin is clamped to $\overline{SHDN}$ pin through a PNP transistor. If the $\overline{SHDN}$ pin is slowly ramped up, the V_C pin will track it up proportionally. As the V_C pin voltage is compared to the current signal at comparator A1, this will, in turn, slowly ramp up the switching current.

The tracking capability built into XREF can be used to implement another startup scheme. If less than 0.8V is applied to XREF, the LT3740 will use this voltage as the reference for regulation. Slowly ramping up the voltage at XREF forces the output to increase slowly, which limits the start-up current, as shown in Typical Performance Characteristics.

A sharp $\overline{SHDN}$ signal is recommended to shut down the LT3740. If $\overline{SHDN}$ slowly ramps down, the V_C signal will be dragged low for a considerable period of time before $\overline{SHDN}$ reaches its turn-off threshold. During this period of time, the output voltage could still be in regulation and the circuit operates in forced continuous mode. A low V_C voltage will result in large bottom MOSFET on-time, which may cause a reverse inductor current that pumps the energy from the output to the input. If there is another supply at the output or the output has a big capacitor, the input voltage could overshoot, and may cause overvoltage damage to certain devices.

APPLICATIONS INFORMATION

Current Sensing Range

Inductor current is determined by measuring the voltage across a sense resistance – either the on-resistance of the bottom MOSFET or an external sensing resistor. The maximum current sense threshold has three steps that are selected by the RANGE pin. The current sense threshold voltage without slope compensation is shown in Table 1. This is the value for high duty cycle operation.

Table 1. Current Sensing Thresholds

RANGE PIN	CURRENT SENSING THRESHOLD
Ground	50mV
Open	80mV
V_{IN}	105mV

Slope Compensation

The LT3740 has a compensation slope to stabilize the constant-frequency valley mode operation. The slope compensation signal increases with the bottom gate duty cycle, which results in a current sense threshold voltage change with duty cycle as shown in the figure in Typical Performance Characteristics. The three current limit levels correspond to three compensation slopes.

The compensation slope needs to overcome the difference between the up and down slope of the inductor current to avoid sub-harmonic oscillation. Maximum compensation slope is required for high input voltages, where the duty cycle is small. The compensation slope can only be selected by the RANGE pin. In the case of insufficient compensation slope, the inductor ripple current or the sensing resistance needs to be reduced.

Reverse Current Limit

Because the LT3740 operates in forced continuous mode when the feedback voltage is higher than 720mV, the inductor current can go negative on occasion, such as light load, shutting down with a slow $\overline{SHDN}$ signal, large load step-down transient response, or the output voltage being pulled up by some other power supply. The LT3740 has a reverse current comparator to limit the reverse current. During the on-time of the bottom MOSFET, when $(V_{SN}+)–(V_{SN}–)$ reaches 40mV, the comparator is triggered and turns off the bottom MOSFET.

When operated under light load, the inductor current goes negative every cycle. The design of the inductor current ripple and the sensing resistor need to ensure that the reverse current comparator is not triggered during normal operation.

Power MOSFET Selection

The LT3740 requires two external N-channel power MOSFETs, one for the top switch and one for the bottom switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, threshold voltage $V_{(GS)TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

When the bottom MOSFET is used as the current sense element, particular attention must be paid to the initial variation, the gate-source voltage effect and the temperature characteristics of its on-resistance. MOSFET on-resistance decreases as the gate-source voltage increases. The change of BGDP voltage could affect the bottom MOSFET gate voltage. Refer to the MOSFET datasheet for the MOSFET on-resistance corresponding to certain gate voltage.

MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)}$ at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)} = R_{SENSE}/\rho_T$$

APPLICATIONS INFORMATION

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C as shown in Figure 1. For a maximum junction temperature of 100°C, using a value ρ_T = 1.3 is reasonable.

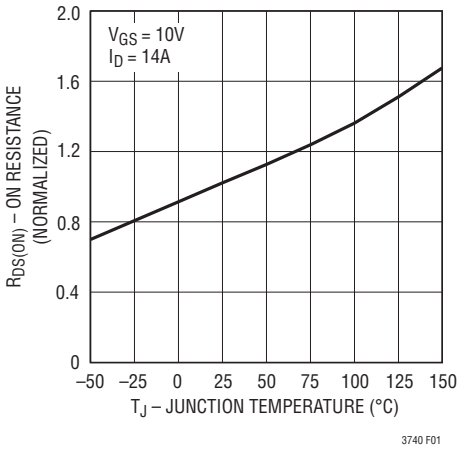


Figure 1. MOSFET $R_{DS(ON)}$ vs. Temperature

Gate Drives

The top gate drive power is provided by BIAS which is about 7.8V higher than V_{IN}. The top gate voltage can be as high as 7.8V and can droop to about 5.5V if the on-time is long enough. The bottom gate drive power is provided by the BGDP pin. BGDP needs to be connected to 7V or higher to get enough gate drive voltage for logic-level threshold MOSFETs. BGDP can be connected to V_{IN}, BIAS or an external voltage supply. For input voltages lower than 7V, BGDP should be connected to BIAS to be able to use logic-level threshold MOSFETs. For V_{IN} higher than 7V, BGDP can be connected to V_{IN} to reduce power loss in the bottom gate drive. For high BGDP voltages, the internal clamp circuit limits the bottom gate drive voltage to about 8V to prevent the gate from overvoltage damage.

For the case BGDP is connected to V_{IN}, if V_{IN} voltage ramp up slowly during startup, there will be a considerable period of time that BGDP is below 7V and the circuit is operating. The insufficient voltage on BGDP could cause malfunction of the circuit. One of the solution circuits is shown in Figure 2. The Zener diode and the small MOSFET limit the $\overline{SHDN}$ voltage to be about 6V below V_{IN}. This shuts down the LT3740 for V_{IN} lower than 7V. If V_{IN} can ramp up to 7V quick enough, this circuit is not necessary.

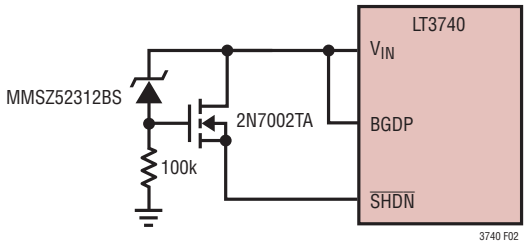


Figure 2. Circuit That Prevents Operation for V_{IN} < 7V

For V_{IN} higher than 14V, the high dv/dt at SW node and the strong drive of BGATE can generate extra noise and affect the operation. A resistor R_{BG} of 1Ω-2Ω between BGATE and the gate of the bottom MOSFET as shown in Figure 3 can effectively reduce the noise.

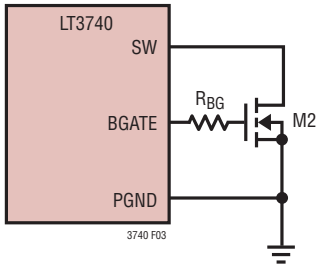


Figure 3. Noise Reduction for Bottom MOSFET

The LT3740 uses adaptive dead time control to prevent the top and bottom MOSFET shoot-through and minimize the dead time. When the internal top MOSFET on signal comes, the LT3740 delays the turn on of TGATE until BGATE is off. When the internal bottom MOSFET on signal comes, the LT3740 delays the turn on of BGATE until the SW node swings down to ground. In the case of small or negative inductor current that SW node cannot swing below ground after TGATE turns off, BGATE will turn on 200ns after TGATE is off.

APPLICATIONS INFORMATION

Choose MOSFET Sensing or Resistor Sensing

The LT3740 can use either the bottom MOSFET on-resistance or an external sensing resistor for current sensing. Simplicity and high efficiency are the benefits of using bottom MOSFET on-resistance. However, some MOSFETs have a wide on-resistance variation. As discussed previously, the gate-source voltage and the temperature also affect the MOSFET on-resistance. These factors affect the accuracy of the inductor current limit. The inductor saturation current will need enough margin to cover the current limit variation. In the cases where the input voltage supply has sufficient current limit, a wide current limit variation of the controller may be tolerated. As the load increases to reach the input supply current limit, the input voltage corrupts, and limits the total power in the circuit.

To reduce the current limit variation, a more accurate external sensing resistor can be used between the bottom MOSFET source and ground. Connect SN^+ and SN^- pins to the two terminals of the resistor.

Power Dissipation

The resulting power dissipation in the MOSFETs are:

$$P_{TOP} = D_{TOP} \bullet I_L^2 \bullet R_{DS(ON),TOP}$$

$$P_{BOT} = D_{BOT} \bullet I_L^2 \bullet R_{DS(ON),BOT}$$

If an external sensing resistor is used, the extra power dissipation in the sensing resistor is:

$$P_{RS} = D_{BOT} \bullet I_L^2 \bullet R_S$$

The power losses in the bottom MOSFET and external sensing resistor are greatest during an output short-circuit, where maximum inductor current and maximum bottom duty cycle occur.

Besides I^2R power loss, there are transition losses and gate drive losses. The transition losses that increase with the input voltage and inductor current are mainly in the top MOSFET. The losses can be estimated with a constant $k = 1.7A^{-1}$ as:

$$\text{Transition Loss} = k \bullet V_{IN}^2 \bullet I_L \bullet C_{RSS} \bullet F_S$$

The gate drive losses increase with the gate drive power supply voltage, gate voltage and gate capacitance as shown below:

$$P_{GD,TOP} = V_{BIAS} \bullet C_{GS,TOP} \bullet V_{GS,TOP} \bullet F_S$$

$$P_{GD,BOT} = V_{BGDP} \bullet C_{GS,BOT} \bullet V_{GS,BOT} \bullet F_S$$

Duty Cycle Limits

At the start of each oscillator cycle, the top MOSFET turns off and the bottom MOSFET turns on with a 500ns duty cycle on the top MOSFET. If the maximum duty cycle is reached, due to a dropping input voltage for example, the output voltage will droop out of regulation.

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. The highest efficiency is obtained with a small ripple current. However, achieving this requires a large inductor. There is a trade off between component size and efficiency.

A reasonable starting point is to choose a ripple current that is about 30% of $I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \bullet \left(\frac{V_{OUT}}{F_S \bullet \Delta I_{L(MAX)}}\right)$$

APPLICATIONS INFORMATION

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores; instead use ferrite, molypermalloy or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

Schottky Diode D1 Selection

The Schottky diode D1 shown in Figure 4 conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently. Another important benefit of the Schottky diode is that it reduces the SW node ringing at switching edges, which reduces the noise in the circuit and also makes the MOSFETs more reliable.

C_{IN} and C_{OUT} Selection

The input capacitance C_{IN} is required to filter the square wave current at the drain of the top MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

$$I_{RMS} \approx I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where:

$$I_{RMS} = \frac{1}{2} \bullet I_{OUT(MAX)}$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} < \Delta I_L \bullet \left(ESR + \frac{1}{8 \bullet F_S \bullet C_{OUT}} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications providing that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller. To dampen input voltage transients, add a small 5μF to 50μF aluminum electrolytic capacitor with an ESR in the range of 0.5Ω to 2Ω.

APPLICATIONS INFORMATION

Current Limit

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LT3740, the maximum sense voltage is selected by the RANGE pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SN(MAX)}}{R_S} + \frac{\Delta I_L}{2}$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The maximum sense voltage increases as duty cycle decreases. If MOSFET on-resistance is used for current sensing, it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of I_{LIMIT} which heats the MOSFET switches.

In the event of output short-circuit to ground, the LT3740 operates at maximum inductor current and minimum duty cycle. The actual inductor discharging voltage is the voltage drop on the parasitic resistors including bottom MOSFET on-resistance, inductor ESR, external sensing resistor if it is used and the actual short-circuit load resistance. Because of the big variation of these parasitic resistances, the top MOSFET on-time can vary considerably for the same input voltage. In the case of high input voltage and low parasitic resistance, pulse-skipping may happen.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LT3740 circuits:

1. DC I^2R losses. These arise from the on-resistances of the MOSFETs, external sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents. The average output current flows through the inductor, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)}$ = 0.01Ω and R_L = 0.005Ω, the loss will range from 15mW to 1.5W as the output current varies from 1A to 10A.
2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at high input voltages and can be estimated from:

   Transition Loss = $(1.7A^{-1}) \bullet V_{IN}^2 \bullet I_{OUT} \bullet C_{RSS} \bullet F_S$
3. Gate drive loss. The previous formula show the factors of this loss. For the top MOSFET, nothing can be done other than choosing a small C_{GS} MOSFET without sacrificing on-resistance. For the bottom MOSFET, the gate drive loss can be reduced by choose the right BGDP voltage supply.
4. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including C_{OUT} ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If a change is made and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

APPLICATIONS INFORMATION

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD}*(ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The V_C pin external components shown in Figure 2 will provide adequate compensation for most applications. For a detailed explanation of switching control loop theory see Application Note 76.

Step-Up Converter Inductor Selection

The step-up converter in the LT3740 provides a BIAS voltage about 7V higher than the input voltage V_{IN} for the top MOSFET drive and most of the internal controller circuitry. The step-up converter has a current limit of 400mA. An inductor ripple current from 100mA to 200mA is a reasonable design for the converter. For this consideration, a 22µH or 47µH inductor is recommended for most of the LT3740 applications. Small size and high efficiency are the major concerns. Inductors with low core losses and small DCR at 1MHz are good choices. Some inductors in this category with small size are listed in Table 2.

Table 2. Recommended Inductors for Step-Up Converter

PART NUMBER	DCR (Ω)	CURRENT RATING (MA)	MANUFACTURER
LQH3C220	0.71	250	Murata 814-237-1431 www.murata.com
ELT5KT-220	0.9	420	Panasonic 714-373-7334 www.panasonic.com
CDRH3D16-220 CR32-470	0.43 0.97	400 330	Sumida 847-956-0666 www.Sumida.com

The step-up converter inductor current is the greatest when the input voltage is the lowest. Larger Cgs of the MOSFETs results in large inductor current. Connecting the BGDP pin to the BIAS pin also greatly increases the inductor current. The saturation current of the inductor needs to cover the maximum input current.

The step-up inductor current decreases as the input voltage increases. For high input voltages, the step-up converter will begin skipping pulses. Although this will result in some low frequency ripple, the BIAS voltage remains regulated on an average basis, and the step-down controller operation is not affected.

For V_{IN} higher than 10V step-up inductor saturation current should be higher than 400mA. For V_{IN} lower than 10V, a lower current rating inductor could be used. The inductor RMS current should be higher than 250mA, and the inductance should not be less than 10µH at 400mA.

Step-Up Converter Capacitor Selection

The small size of ceramic capacitors makes them ideal for the output of the LT3740 step-up converter. X5R and X7R types are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 1µF capacitor is recommended for the output of the LT3740 step-up converter.

Table 3. Recommended Ceramic Capacitor Manufacturers

MANUFACTURER	PHONE	URL
Taiyo Yuden	408-573-4150	www.t-yuden.com
Murata	814-237-1431	www.murata.com
Kemet	408-986-0424	www.kemet.com

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 7V to 20V (15V nominal), V_{OUT} = 2.5V ±5%, $I_{OUT(MAX)}$ = 10A. First, choose the inductor for about 30% ripple current at nominal V_{IN}:

$$L = \frac{2.5V}{(300kHz) \bullet 0.3 \bullet 10A} \bullet \left(1 - \frac{2.5V}{15V}\right) = 2.3\mu H$$

APPLICATIONS INFORMATION

Selecting a standard value of 2.0µH results in a ripple current of:

$$\Delta I_L = \frac{2.5V}{(300kHz)\bullet(2\mu H)}\bullet\left(1-\frac{2.5V}{15V}\right)=3.47A$$

Set Range = V_{IN}. At minimum input voltage V_{IN} = 7V, the maximum current sensing voltage is 145mV. Use an external sensing resistor of 12mΩ. The inductor current valley will be clamped to 12A. The ripple current at V_{IN} = 7V is 2.68A, there is about 33% of margin for the 10A load current to cover the maximum current sensing voltage variation.

For the case of using MOSFET on-resistance for current sensing, choosing a Si4840 ($R_{DS(ON)}$ = 0.008Ω (NOM) 0.0095Ω (MAX) for V_{GS} = 7V, θ_{JA} = 40°C/W) yields a nominal sense voltage of:

$V_{SN(NOM)}$ = (10A)(1.3)(0.0095Ω) =123mV

To check if the current limit is acceptable, assume a junction temperature of about 55°C above a 70°C ambient with $\rho_{125°C}$ = 1.5:

$$I_{LIMIT} = \frac{145mV}{1.5\bullet 0.0095\Omega}+\frac{2.68A}{2}=11.5A$$

Double check the assumed T_J in the MOSFET at V_{IN} = 7V with maximum load current:

$P_{BOT} = D_{BOT} \bullet IL^2 \bullet R_{DS(ON),\ BOT}$

$$P_{BOT} = \left(1-\frac{2.5V}{7V}\right)\bullet(10A)^2\bullet 1.5\bullet 0.0095 = 0.92W$$

Double check the assumed T_J in the MOSFET:

T_J = 70°C + (0.92W)(40°C/W) = 107°C

The power dissipation in the bottom MOSFET increases with input voltage. For V_{IN} = 20V,

$$P_{BOT} = \left(1-\frac{2.5V}{20V}\right)\bullet(10A)^2\bullet 1.5\bullet 0.0095\Omega = 1.25W$$

Double check the assumed T_J in the MOSFET:

T_J = 70°C + (1.25W)(40°C/W) = 120°C

Choose a Si4840 (C_{RSS} = 200pF) for the top MOSFET and check its power dissipation at maximum load current with $\rho_{100°C}$ = 1.3:

$$P_{TOP} = \frac{2.5V}{20V}\bullet(10A)^2\bullet 1.3\bullet 0.0095\Omega + 17\bullet(20V)^2\bullet 10A\bullet 200pF\bullet 300kHz = 0.15W + 0.41W = 0.56W$$

T_J = 70°C + (0.56W)(40°C/W) = 92°C

This analysis shows that careful attention to heat sinking will be necessary in this circuit.

Check the reverse current comparator margin. The maximum ripple current happens at maximum input voltage:

$$\Delta I_{L(MAX)} = \frac{2.5V}{300kHz\bullet 2\mu H}\bullet\left(1-\frac{2.5V}{20V}\right)=3.65A$$

At no load, the maximum reverse current voltage is:

$$R_S \bullet \frac{\Delta I_{L(MAX)}}{2} = 12m\Omega \bullet \frac{3.65A}{2} = 22mV$$

APPLICATIONS INFORMATION

Which is adequately lower than the 35mV reverse current comparator threshold.

C_{IN} is chosen for an RMS current rating of about 5A at 85°C. The output capacitors are chosen for a low ESR of 0.005Ω to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$$\Delta V_{OUT(RIPPLE)} = \Delta I_L \bullet (ESR) = (3.47A)(0.005\Omega) = 17mV$$

However, a 0A to 10A load step will cause an output change of up to:

$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD} \bullet (ESR) = (10A)(0.005\Omega) = 50mV$$

An optional 100µF ceramic output capacitor is included to minimize the effect of ESL in the output ripple.

For the step-up converter, at V_{IN} = 7V, step-up inductor current is about 27mA. Choose a 22µH inductor and a 1µF output capacitor.

The complete circuit is shown in Figure 4.

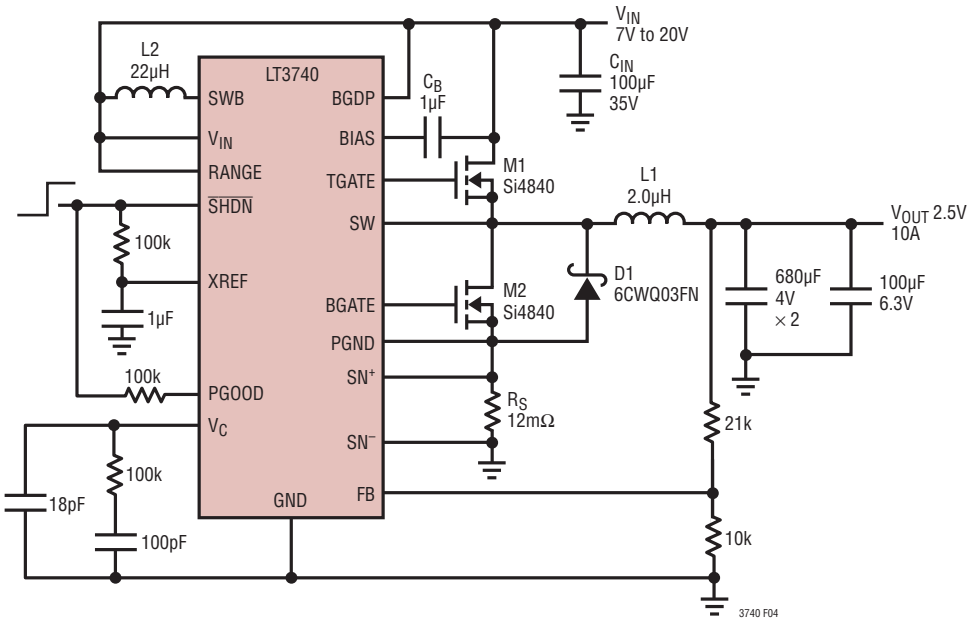


Figure 4. Design Example: 2.5V/10A Output

APPLICATIONS INFORMATION

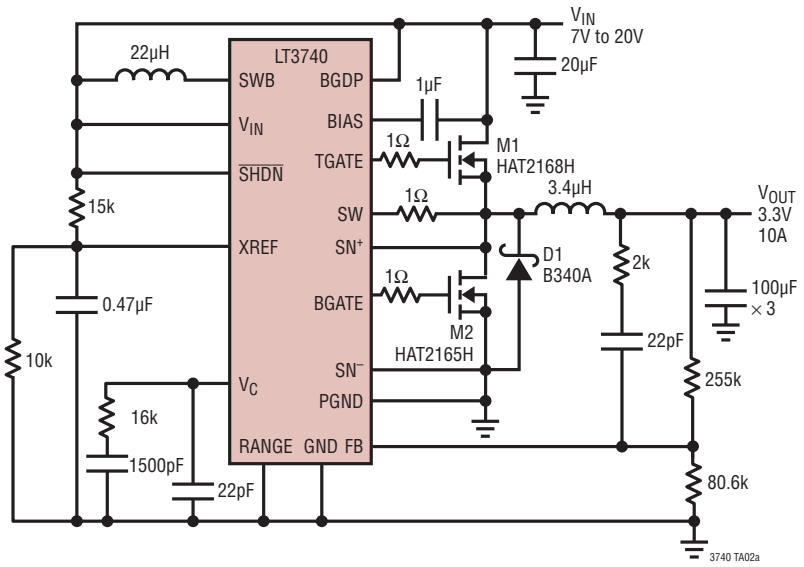
PC Board Layout Considerations

As with all switching regulators, careful attention must be paid to the PCB board layout and component placement.

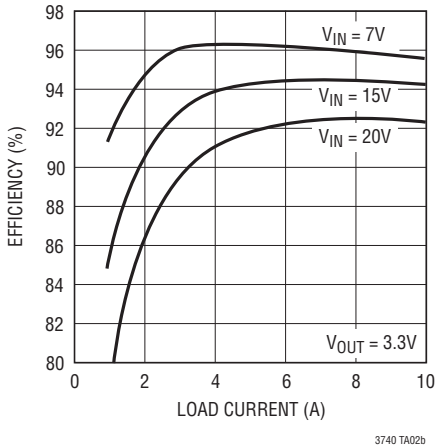
- Place the power components close together with short and wide interconnecting trances. The power components consist of the top and bottom MOSFETs, the inductor, C_{IN} and C_{OUT}. One way to approach this is to simply place them on the board first.
- Similar attention should be paid to the power components that make up the boost converter. They should also be placed close together with short and wide traces.
- Always use a ground plane under the switching regulator to minimize interplane coupling.
- Minimize the parasitic inductance in the loop of C_{IN}, MOSFETs and D1 which carries large switching current.
- Use compact plane for switch node (SW) to improve cooling of the MOSFETs and to keep EMI low.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low. Unused areas can be filled with copper and connect to any DC node (V_{IN}, V_{OUT}, GND)
- Place C_B close to BIAS pin and input capacitor.
- Keep the high dv/dt nodes (SW, TG, BG, SWB) away from sensitive small signal nodes.

TYPICAL APPLICATIONS

High Efficiency Step-Down Converter

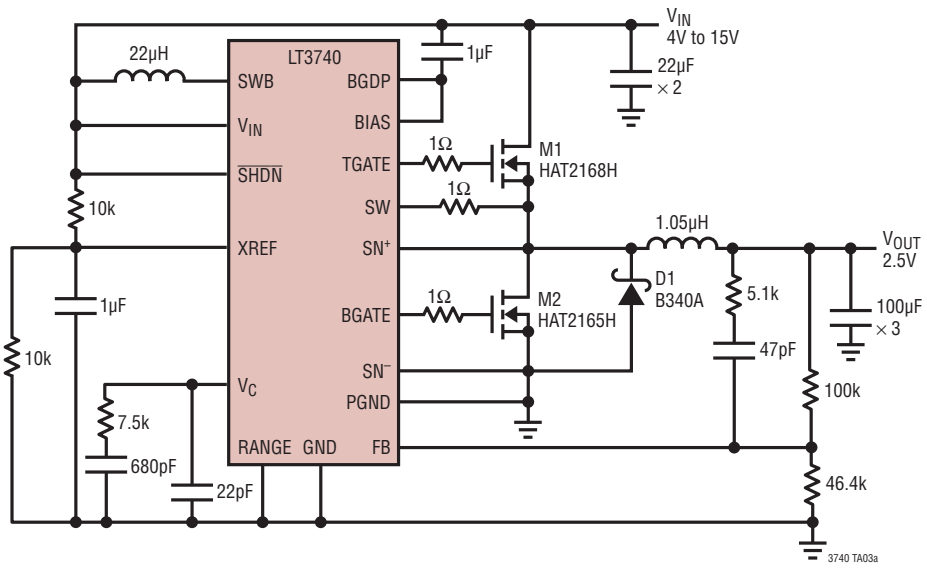


Efficiency vs Load Current

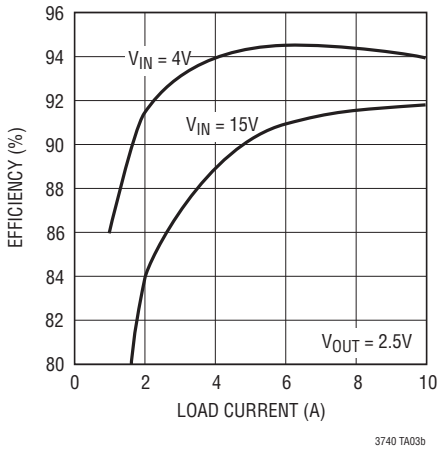


TYPICAL APPLICATIONS

2.5V/10A

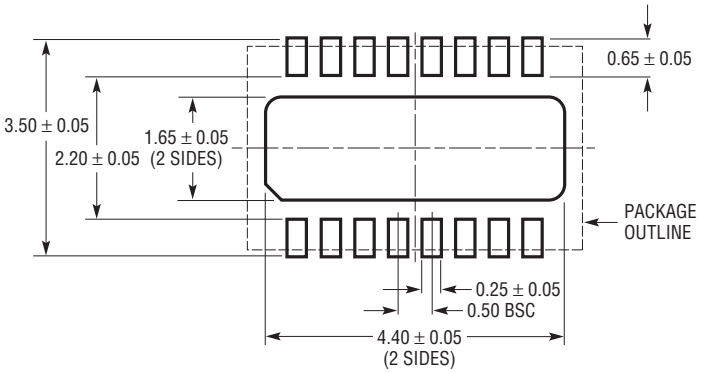


EFFICIENCY

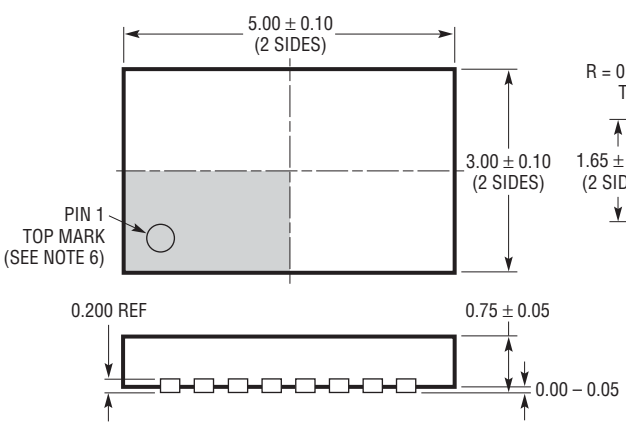


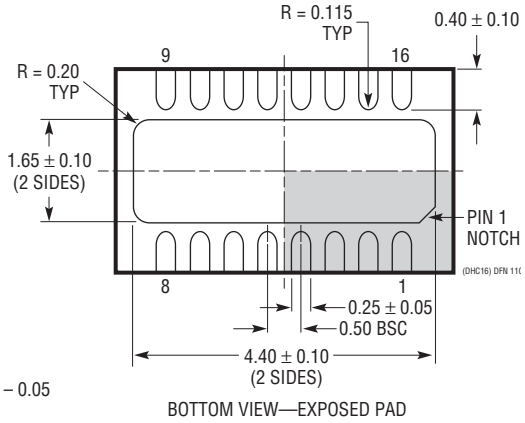
PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



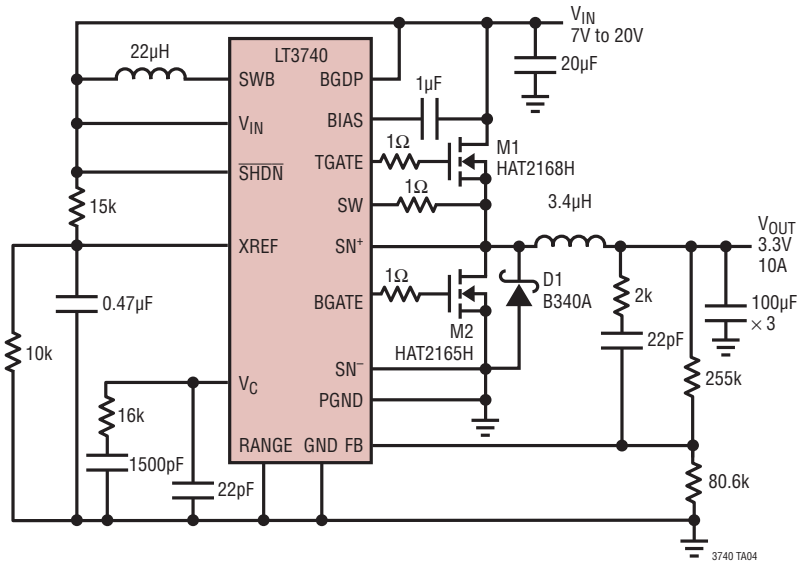


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

High Efficiency Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1778	No R_{SENSE}, Step-Down Synchronous DC/DC Controller	V_{IN}: 4V to 36V, Fast Transient Responds, Current Mode, $I_{OUT} \leq 20A$
LTC1876	2-Phase, Dual Synchronous Step-Down Switching Controller	Current Mode; 20A per Channel
LT3430/LT3431	Monolithic 3A, 200kHz/500kHz Step-Down Switching Regulator	V_{IN}: 5.5V to 60V, 0.1Ω Saturation Switch, 16-Lead SSOP Package
LTC3708	No R_{SENSE}, Dual, 2-Phase, Synchronous DC/DC Controller	V_{IN}: 4V to 36V, Current Mode, Up/Down Tracking, Synchronizable
LTC3728L	Dual, 2-Phase Synchronous Step-Down Controller	V_{IN}: 4V to 36V, 550kHz, PLL: 250kHz to 550kHz
LTC3778	Wide Operating Range, No R_{SENSE} Step-Down Controller	Single Channel, Separate V_{ON} Programming
LTC3824	High Voltage, Wide Input Range, Step-Down Controller With Low I_Q	V_{IN}: 4V to 60V, I_Q = 40µA, 100% Duty Cycle, 2A P-Channel Gate Drive, 10-Pin MSOP

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