

Ultralow Power Boost Converter with Output Disconnect

FEATURES

- **Ultralow Quiescent Current**
8.5 μ A in Active Mode
0 μ A in Shutdown Mode
- **Comparator Built into $\overline{\text{SHDN}}$ pin**
- **Low Noise Control Scheme**
- **Adjustable FB reference voltage**
- **Wide Input Range: 2.5V to 16V**
- **Wide Output Range : Up to 40V**
- **Integrated Power NPN Switch**
25mA Current Limit (LT8410)
8mA Current Limit (LT8410-1)
- **Integrated Schottky Diode**
- **Integrated Output Disconnect**
- **High Value (12.4M/0.4M) Feedback Resistors Integrated**
- **Built in Soft-Start (Optional Capacitor from V_{REF} to GND)**
- **Overvoltage Protection for CAP and V_{OUT} pins**
- **Tiny 8-Pin 2mm \times 2mm DFN package**

DESCRIPTION

The LT[®]8410/LT8410-1 are ultralow power boost converters with integrated power switch, Schottky diode and output disconnect circuitry. The parts control power delivery by varying both the peak inductor current and switch off-time. This control scheme results in low output voltage ripple as well as high efficiency over a wide load range. The quiescent current is a low 8.5 μ A, which is further reduced to 0 μ A in shutdown. The internal disconnect circuitry allows the output voltage to be blocked from the input during shutdown. High value (12.4M/0.4M) resistors are integrated on chip for output voltage detection, significantly reducing input referred quiescent current. The LT8410/-1 also features a comparator built into the $\overline{\text{SHDN}}$ pin, over voltage protection for the CAP and V_{OUT} pins, built in soft-start and comes in a tiny 8-pin 2mm \times 2mm DFN package.

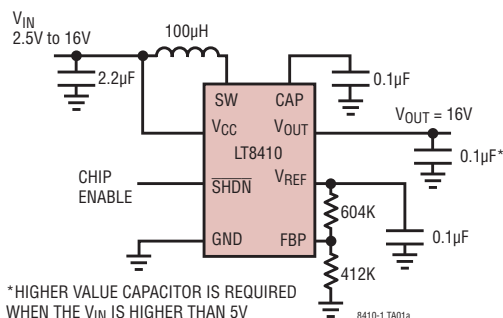
LT, LT, LTC and LTM are registered trademarks of Linear Technology Corporation. Hot Swap is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents including 5481178, 6580258, 6304066, 6127815, 6498466, 6611131.

APPLICATIONS

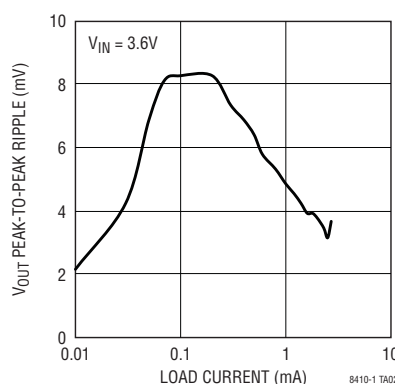
- Sensor Power
- RF MemS Relay Power
- General Purpose Bias

TYPICAL APPLICATION

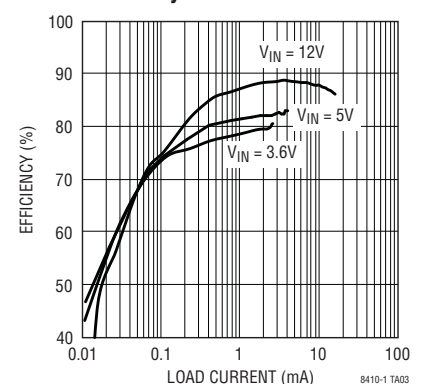
General Purpose Bias with Wide Input Voltage



Output Voltage Ripple vs Load Current



Efficiency vs Load Current



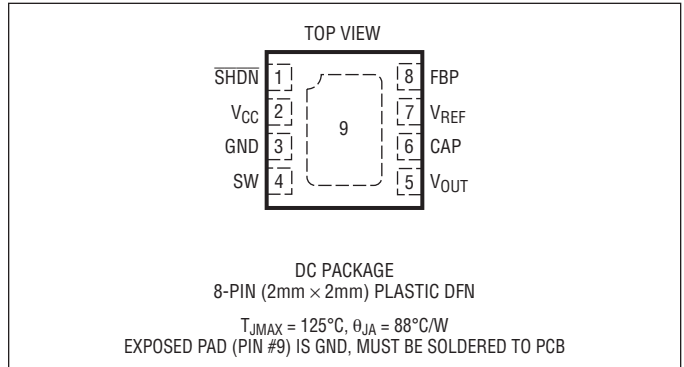
LT8410/LT8410-1

ABSOLUTE MAXIMUM RATINGS

(Note 1)

| | |
|---|----------------|
| V_{CC} Voltage | -0.3V to 16V |
| SW Voltage | -0.3V to 40V |
| CAP Voltage | -0.3V to 40V |
| V_{OUT} Voltage | -0.3V to 40V |
| \overline{SHDN} Voltage | -0.3V to 16V |
| V_{REF} Voltage..... | -0.3V to 2.5V |
| FBP Voltage | -0.3V to 2.5V |
| Maximum Junction Temperature | 125°C |
| Operating Temperature Range (Note 2) .. | -40°C to 125°C |
| Storage Temperature Range..... | -65°C to 150°C |

PIN CONFIGURATION



ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|------------------|-------------------|---------------|--------------------------------|-------------------|
| LT8410EDC#PBF | LT8410EDC#TRPBF | LDQR | 8-Lead (2mm × 2mm) Plastic DFN | -40°C to 125°C |
| LT8410IDC#PBF | LT8410IDC#TRPBF | LDQR | 8-Lead (2mm × 2mm) Plastic DFN | -40°C to 125°C |
| LT8410EDC-1#PBF | LT8410EDC-1#TRPBF | LFCC | 8-Lead (2mm × 2mm) Plastic DFN | -40°C to 125°C |
| LT8410IDC-1#PBF | LT8410IDC-1#TRPBF | LFCC | 8-Lead (2mm × 2mm) Plastic DFN | -40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_{IN} = 3.0\text{V}$, $V_{\overline{SHDN}} = V_{IN}$ unless otherwise noted. (Note 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|---|---------|------------|---------|---------------|----------|
| Minimum Operating Voltage | | | 2.2 | 2.5 | V | |
| Maximum Operating Voltage | | | | 16 | V | |
| Reference Voltage | | ● 1.220 | 1.235 | 1.255 | V | |
| V_{REF} Current Limit | (Note 3) | | 10 | | μA | |
| V_{REF} Discharge Time | | | 70 | | μS | |
| V_{REF} Line Regulation | | | 0.01 | | %/V | |
| Quiescent Current | Not Switching | ● | 8.5 | 12 | μA | |
| Quiescent Current in Shutdown | $V_{\overline{SHDN}} = 0\text{V}$ | ● | 0 | 1 | μA | |
| Quiescent Current from V_{OUT} and CAP | $V_{OUT} = 16\text{V}$ | | 3 | | μA | |
| Minimum Switch Off Time | After Start-Up (Note 4) During Start-Up (Note 4) | | 240 600 | | nS nS | |
| Switch Current Limit | LT8410 LT8410-1 | ● ● | 20 6 | 25 8 | 30 10 | mA mA |

84101f

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 3.0\text{V}$, $V_{SHDN} = V_{IN}$ unless otherwise noted. (Note 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|---|-----------|------------|----------|--------------------------------|
| Switch V_{CESAT} | LT8410, $I_{SW} = 10\text{mA}$ LT8410-1, $I_{SW} = 4\text{mA}$ | | 150 100 | | mV mV |
| Switch Leakage Current | $V_{SW} = 5\text{V}$ | | 0 | 1 | μA |
| Schottky Forward Voltage | $I_{DIODE} = 10\text{mA}$ | | 650 | 850 | mV |
| Schottky Reverse Leakage | $V_{CAP} - V_{SW} = 5$ $V_{CAP} - V_{SW} = 40$ | | 0 0 | 0.5 1 | μA μA |
| PMOS Disconnect Current Limit | LT8410 LT8410-1 | 14 2.5 | 19 4 | 25 5 | mA mA |
| PMOS Disconnect $V_{CAP} - V_{OUT}$ | $I_{OUT} = 1\text{mA}$ | | 50 | | mV |
| V_{OUT} Resistor Divider Ratio | | ● 31.6 | 31.85 | 32.2 | |
| FBP Pin Bias Current | $V_{FBP} = 0.5\text{V}$, Current Flows Out of Pin | ● | 1.3 | 30 | nA |
| SHDN Minimum Input Voltage High | SHDN Rising | ● 1.20 | 1.30 | 1.45 | V |
| SHDN Input Voltage High Hysteresis | | | 60 | | mV |
| SHDN Hysteresis Current | (Note 3) | 0.08 | 0.1 | 0.14 | μA |
| SHDN Input Voltage Low | | | | 0.3 | V |
| SHDN Pin Bias Current | $V_{SHDN} = 3\text{V}$ $V_{SHDN} = 16\text{V}$ | | 0 2 | 1 3 | μA μA |

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8410/LT8410-1 are guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over

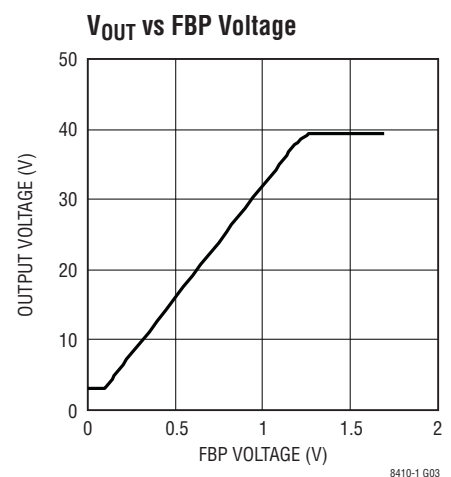
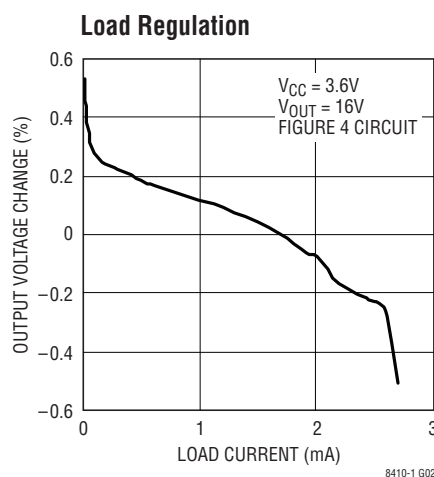
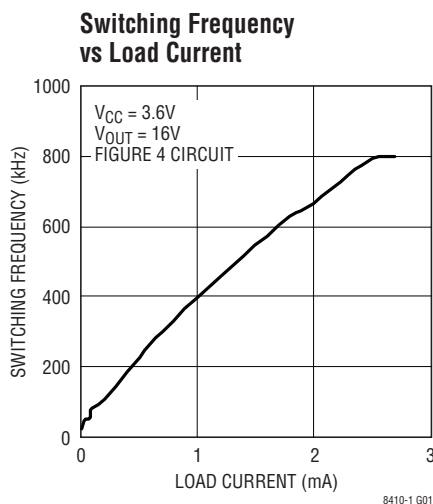
the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: See applications section for more information.

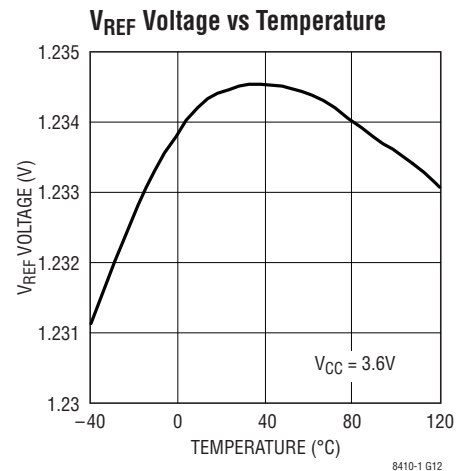
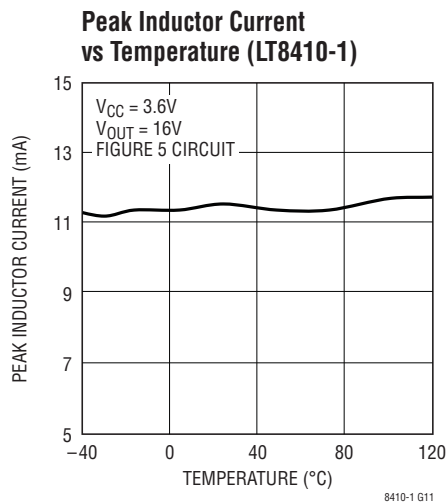
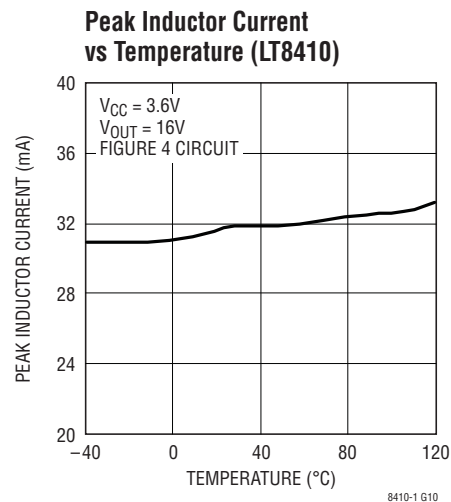
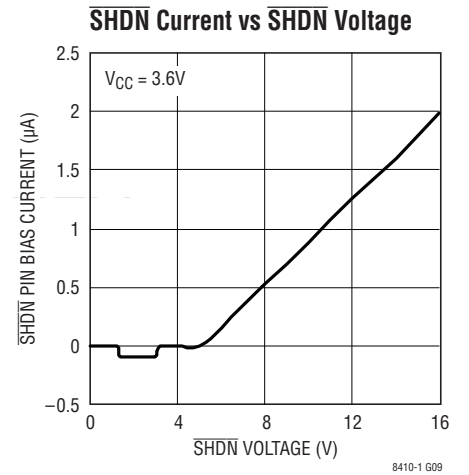
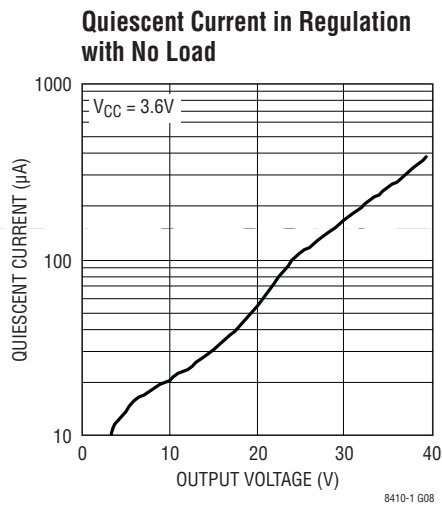
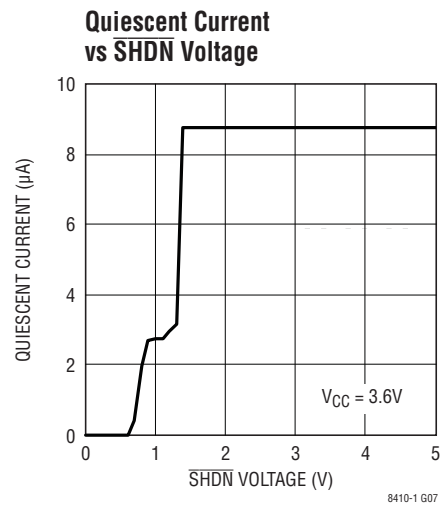
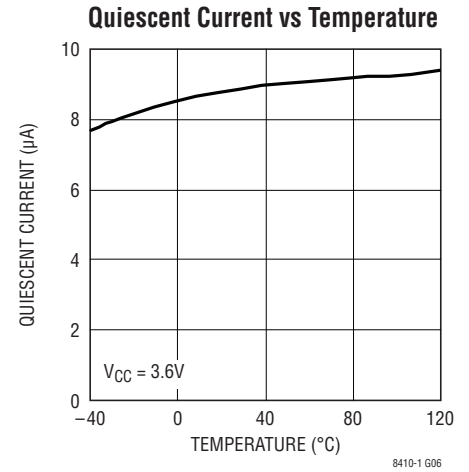
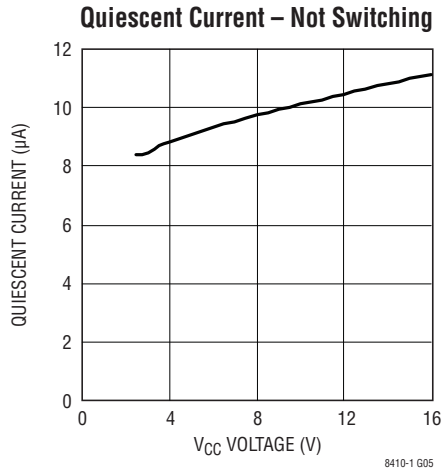
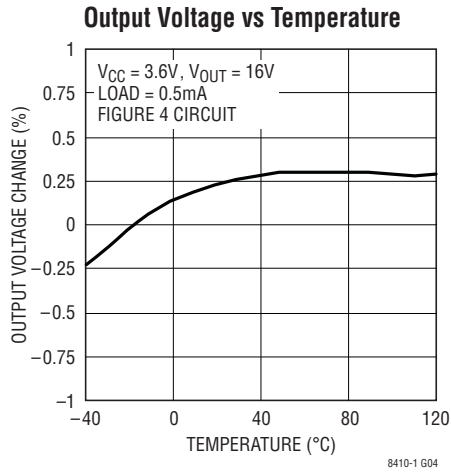
Note 4: Start-up mode occurs when V_{OUT} is less than $V_{FBP} \cdot 64/3$.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

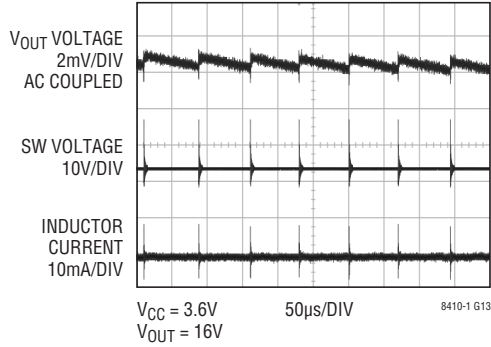


TYPICAL PERFORMANCE CHARACTERISTICS

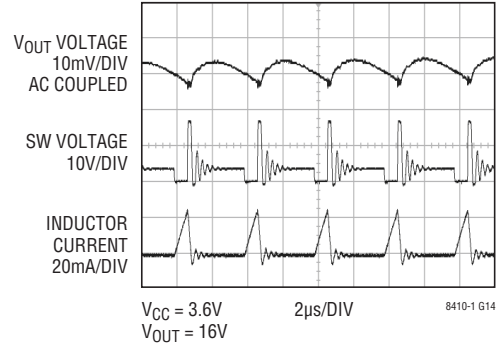


TYPICAL PERFORMANCE CHARACTERISTICS

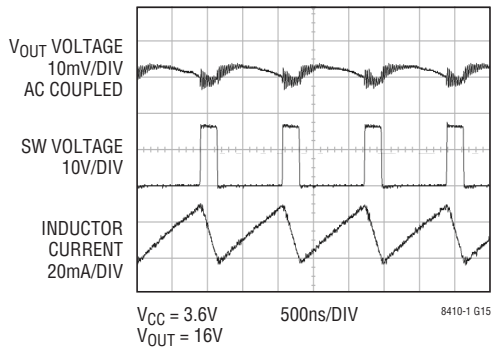
LT8410 Switching Waveform at No Load



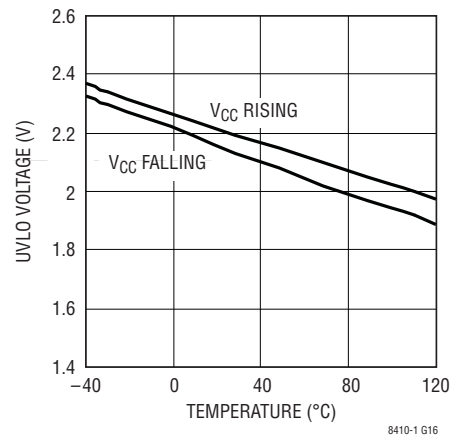
LT8410 Switching Waveform at 0.5mA Load



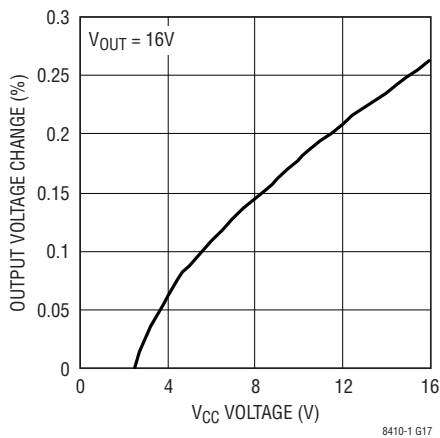
LT8410 Switching Waveform at 3mA Load



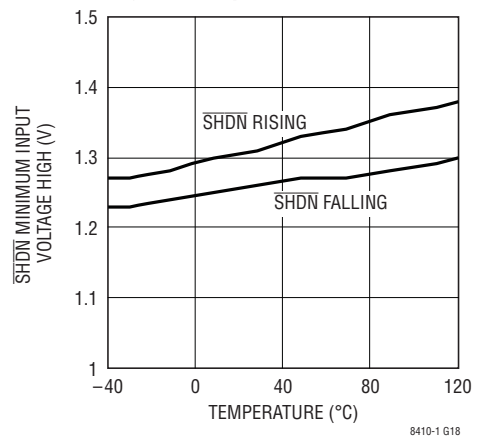
UVLO vs Temperature



Line Regulation

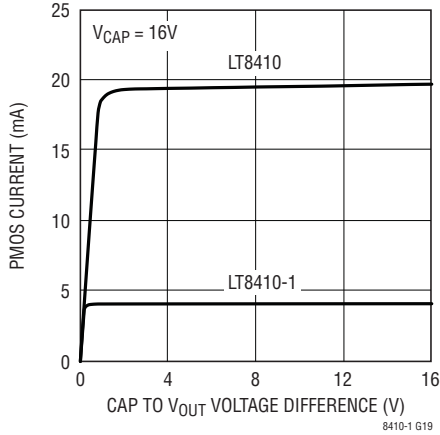


SHDN Minimum Input Voltage High vs Temperature

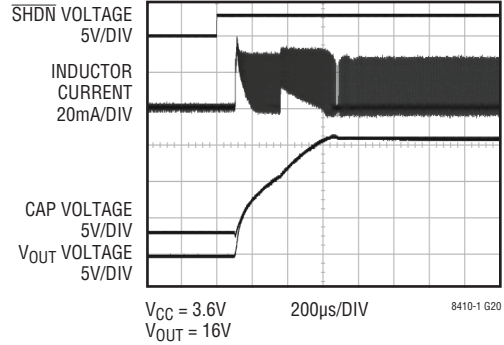


TYPICAL PERFORMANCE CHARACTERISTICS

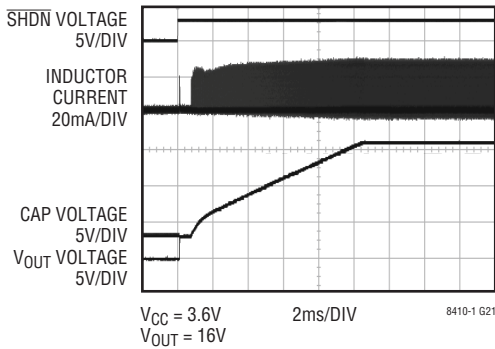
Output Disconnect PMOS Current vs CAP to V_{OUT} Voltage Difference



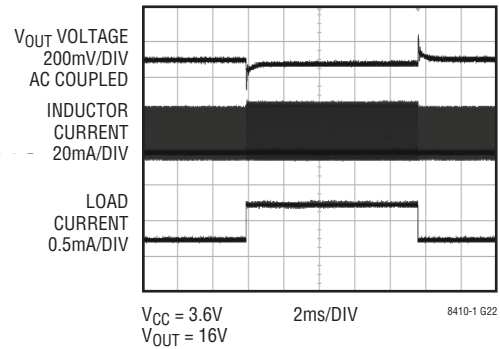
LT8410 Start-Up Waveforms Without Capacitor at V_{REF} Pin



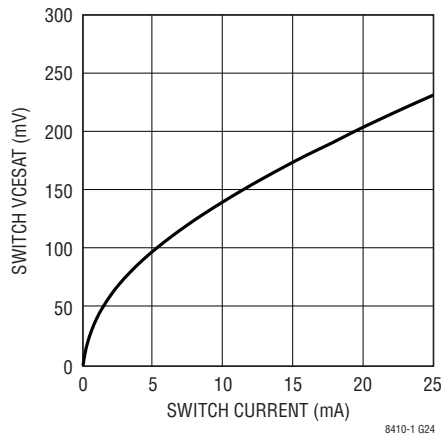
LT8410 Start-Up Waveforms With 0.1µF Capacitor at V_{REF} Pin



LT8410 Transient Response 0.5mA → 1.5mA → 0.5mA Load Pulse



SW Saturation Voltage vs Switch Current (LT8410)



PIN FUNCTIONS

SHDN (Pin 1): Shutdown Pin. This pin is used to enable/disable the chip. Drive below 0.3V to disable the chip. Drive above 1.4V to activate the chip. Do not float this pin.

V_{CC} (Pin 2): Input Supply Pin. Must be locally bypassed to GND. See typical applications section.

GND (Pin 3 and Pin 9): Ground. Tie directly to local ground plane. Pin 9 is floating but must be grounded for proper shielding.

SW (Pin 4): Switch Pin. This is the collector of the internal NPN power switch. Minimize the metal trace area connected to this pin to minimize EMI.

V_{OUT} (Pin 5): Drain of Output Disconnect PMOS. Place a bypass capacitor from this pin to GND.

CAP (Pin 6): This is the cathode of the internal Schottky Diode. Place a bypass capacitor from this pin to GND.

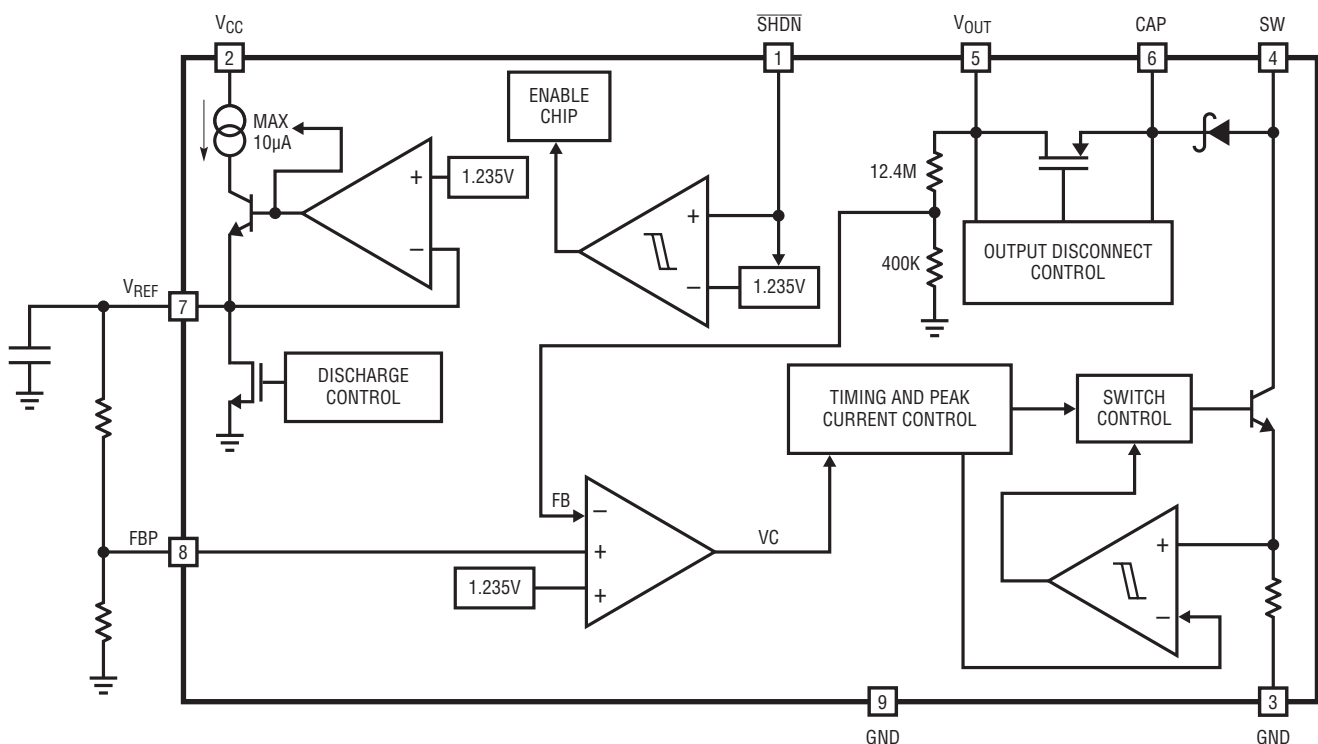
V_{REF} (Pin 7): Reference Pin. Soft-start can be achieved by placing a capacitor from this pin to GND. This cap will be discharged for 70μs (typical) at the beginning of start-up and then be charged to 1.235V with a 10μA current source.

FBP (Pin 8): Positive Feedback Pin. This pin is the error amplifier's positive input terminal. To achieve the desired output voltage, choose the FBP pin voltage (V_{FBP}) according to the following formula:

$$V_{FBP} = V_{OUT} / 31.85$$

For protection purposes, the output voltage can not exceed 40V even if V_{FBP} is driven higher than V_{REF}.

BLOCK DIAGRAM



OPERATION

The LT8410 series utilizes a variable peak current, variable off-time control scheme to provide high efficiency over a wide output current range.

The operation of the part can be better understood by referring to the Block Diagram. The part senses the output voltage by monitoring the internal FB node, and servoing the FB node voltage to be equal to the FBP pin voltage. The chip integrates an accurate high value resistor divider (12.4M/0.4M) from the V_{OUT} pin. The output voltage is set by the FBP pin voltage, which in turn is set by an external resistor divider from the V_{REF} pin. The FBP pin voltage can also be directly biased with an external reference, allowing full control of the output voltage during operation.

The Switch Control block senses the output of the amplifier and adjusts the switching frequency as well as other parameters to achieve regulation. During the start-up of

the circuit, special precautions are taken to ensure that the inductor current remains under control

The LT8410 series also has a PMOS output disconnect switch. The PMOS switch is turned on when the part is enabled via the $\overline{\text{SHDN}}$ pin. When the part is in shutdown, the PMOS switch turns off, allowing the V_{OUT} node to go to ground. This type of disconnect function is often required in power supplies.

The differences between the LT8410 and LT8410-1 are the SW current limit and the output disconnect PMOS current limit. For the LT8410, the SW current limit and PMOS current limit are approximately 25mA and 19mA respectively, while those of the LT8410-1 are approximately 8mA and 4mA respectively.

APPLICATIONS INFORMATION

Inductor Selection

Several inductors that work well with the LT8410 and LT8410-1 are listed in Table 1. The tables are not complete, and there are many other manufacturers and devices that can be used. Consult each manufacturer for more detailed information and for their entire selection of related parts, as many different sizes and shapes are available.

Inductors with a value of 47μH or higher are recommended for most LT8410 series designs. Inductors with low core losses and small DCR (copper wire resistance) are good choices for LT8410 series applications. For full output power, the inductor should have a saturation current rating higher than the peak inductor current. The peak inductor current can be calculated as:

$$I_{PK} = I_{LIMIT} + \frac{V_{IN} \cdot 150 \cdot 10^{-6}}{L} \text{ mA}$$

where the worst case I_{LIMIT} is 30mA and 10mA for LT8410 and LT8410-1 respectively. L is the inductance value in Henrys and V_{IN} is the input voltage to the boost circuit.

Table 1. Recommended Inductors for LT8410/-1

| PART | L (μH) | DCR (Ω) | SIZE (mm) | VENDOR |
|---------------|--------|---------|-----------------|-------------------|
| LQH2MCN680K02 | 68 | 6.6 | 2.0 × 1.6 × 0.9 | Murata |
| LQH32CN101K53 | 100 | 3.5 | 3.2 × 2.5 × 2.0 | www.murata.com |
| DO2010-683ML | 68 | 8.8 | 2.0 × 2.0 × 1.0 | Coilcraft |
| LPS3015-104ML | 100 | 3.4 | 3.0 × 3.0 × 1.4 | www.coilcraft.com |
| LPS3015-154ML | 150 | 6.1 | 3.0 × 3.0 × 1.4 | |
| LPS3314-154ML | 150 | 4.1 | 3.3 × 3.3 × 1.3 | |

Capacitor Selection

The small size and low ESR of ceramic capacitors make them suitable for most LT8410 applications. X5R and X7R types are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 2.2μF or higher input capacitor and a 0.1μF to 1μF output capacitor are sufficient for most applications. Always use a capacitor with a sufficient voltage rating. Many ceramic capacitors rated at 0.1μF to 1μF have greatly reduced capacitance when bias voltages are applied. Be sure to check actual capacitance at the desired output voltage. Generally a 0603

APPLICATIONS INFORMATION

or 0805 size capacitor will be adequate. A 0.1µF to 1µF capacitor placed on the CAP node is recommended to filter the inductor current while a 0.1µF to 1µF capacitor placed on the V_{OUT} node will give excellent transient response and stability. To make the V_{REF} pin less sensitive to noise, putting a capacitor on the V_{REF} pin is recommended, but not required. A 47nF to 220nF 0402 capacitor will be sufficient. Table 2 shows a list of several capacitor manufacturers. Consult the manufacturers for more detailed information and for their entire selection of related parts.

Table 2. Recommended Ceramic Capacitor Manufactures

| MANUFACTURER | PHONE | WEBSITE |
|--------------|----------------|-----------------|
| Taiyo Yuden | (408) 573-4150 | www.t-yuden.com |
| Murata | (814) 237-1431 | www.murata.com |
| AVX | (843) 448-9411 | www.avxcorp.com |
| Kemet | (408)986-0424 | www.kemet.com |
| TDK | (847) 803-6100 | www.tdk.com |

Setting Output Voltage

The output voltage is set by the FBP pin voltage, and V_{OUT} is equal to 31.85 • V_{FBP} when the output is regulated, shown in Figure 1. Since the V_{REF} pin provides a good reference (1.235V), the FBP voltage can be easily set by a resistor divider from the V_{REF} pin to ground. The series resistance of this resistor divider should be kept larger than 200KΩ to prevent loading down the V_{REF} pin. The FBP pin can also be biased directly by an external reference. For over voltage protection, the output voltage is limited to 40V. Therefore, if V_{FBP} is higher than 1.235V, the output voltage will stay at 40V.

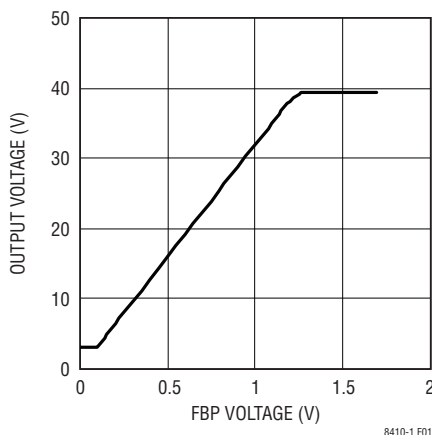


Figure 1. FBP to V_{OUT} Transfer Curve

Connecting the Load to the CAP Node

The efficiency of the converter can be improved by connecting the load to the CAP pin instead of the V_{OUT} pin.

The power loss in the PMOS disconnect circuit is then made negligible. No quiescent current will be consumed in the internal feedback resistor divider string during shutdown since the PMOS transistor will be open and the internal feedback resistor divider is connected at the V_{OUT} pin. The disadvantage of this method is that the CAP node cannot go to ground during shutdown, but will be limited to around a diode drop below V_{CC}. Loads connected to the part should only sink current. Never force external power supplies onto the CAP or V_{OUT} pins.

Maximum Output Load Current

The maximum output current of a particular LT8410 series circuit is a function of several circuit variables. The following method can be helpful in predicting the maximum load current for a given circuit:

Step 1. Calculate the peak inductor current:

$$I_{PK} = I_{LIMIT} + \frac{V_{IN} \cdot 150 \cdot 10^{-6}}{L} \text{ mA}$$

where I_{LIMIT} is 25mA and 8mA for LT8410 and LT8410-1 respectively. L is the inductance value in Henrys and V_{IN} is the input voltage to the boost circuit.

Step 2. Calculate the inductor ripple current:

$$I_{RIPPLE} = \frac{(V_{OUT} + 1 - V_{IN}) \cdot 200 \cdot 10^{-6}}{L} \text{ mA}$$

where V_{OUT} is the desired output voltage. If the inductor ripple current is less than the peak current, then the circuit will only operate in discontinuous conduction mode. The inductor value should be increased so that I_{RIPPLE} < I_{PK}. An application circuit can be designed to operate only in discontinuous mode, but the output current capability will be reduced.

Step 3. Calculate the average input current:

$$I_{IN(AVG)} = I_{PK} - \frac{I_{RIPPLE}}{2} \text{ mA}$$

APPLICATIONS INFORMATION

Step 4. Calculate the nominal output current:

$$I_{OUT(NOM)} = \frac{I_{IN(AVG)} \cdot V_{IN} \cdot 0.7}{V_{OUT}} \text{ mA}$$

Step 5. Derate output current:

$$I_{OUT} = I_{OUT(NOM)} \cdot 0.8$$

For low output voltages the output current capability will be increased. When using output disconnect (load current taken from V_{OUT}), these higher currents will cause the drop in the PMOS switch to be higher resulting in lower output current capability than predicted by the preceding equations.

Inrush Current

When V_{CC} is stepped from ground to the operating voltage while the output capacitor is discharged, a high level of inrush current may flow through the inductor and Schottky diode into the output capacitor. Conditions that increase inrush current include a larger more abrupt voltage step at V_{CC} , a larger output capacitor tied to the CAP pin and an inductor with a low saturation current. While the chip is designed to handle such events, the inrush current should not be allowed to exceed 0.3A. For circuits that use output capacitor values within the recommended range and have input voltages of less than 6V, inrush current remains low, posing no hazard to the device. In cases where there are large steps at V_{CC} (more than 6V) and/or a large capacitor is used at the CAP pin, inrush current should be measured to ensure safe operation.

Soft-Start

The LT8410 series contains a soft-start circuit to limit peak switch currents during start-up. High start-up current is inherent in switching regulators in general since the feedback loop is saturated due to V_{OUT} being far from its final value. The regulator tries to charge the output capacitor as quickly as possible, which results in large peak current.

When the FBP pin voltage is generated by a resistor divider from the V_{REF} pin, the start-up current can be limited by connecting an external capacitor (typically 47nF to 220nF) to the V_{REF} pin. When the part is brought out of shutdown,

this capacitor is first discharged for about 70 μ s (providing protection against pin glitches and slow ramping), then an internal 10 μ A current source pulls the V_{REF} pin slowly to 1.235V. Since the V_{OUT} voltage is set by the FBP pin voltage, the V_{OUT} voltage will also slowly increase to the regulated voltage, which results in lower peak inductor current. The voltage ramp rate on the pin can be set by the value of the V_{REF} pin capacitor.

Output Disconnect

The LT8410 series has an output disconnect PMOS that blocks the load from the input during shutdown. The maximum current through the PMOS is limited by circuitry inside the chip, helping the chip survive output shorts.

$\overline{\text{SHDN}}$ Pin Comparator and Hysteresis Current

An internal comparator compares the $\overline{\text{SHDN}}$ pin voltage with an internal voltage reference (1.3V) which gives a precise turn-on voltage level. The internal hysteresis of this turn-on voltage is about 60mV. When the chip is turned on, and the $\overline{\text{SHDN}}$ pin voltage is close to this turn-on voltage, 0.1 μ A current flows out of the $\overline{\text{SHDN}}$ pin. This current is called $\overline{\text{SHDN}}$ pin hysteresis current, and will go away when the chip is off. By connecting the external resistors as in Figure 2, a user-programmable enable voltage function can be realized.

The turn-on voltage for the configuration is:

$$1.30 \cdot (1 + R1/R2)$$

and the turn-off voltage is:

$$(1.24 - R3 \cdot 10^{-7}) \cdot (1 + R1/R2) - (R1 \cdot 10^{-7})$$

where R1, R2 and R3 are resistance value in Ω .

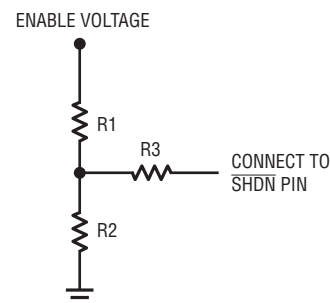
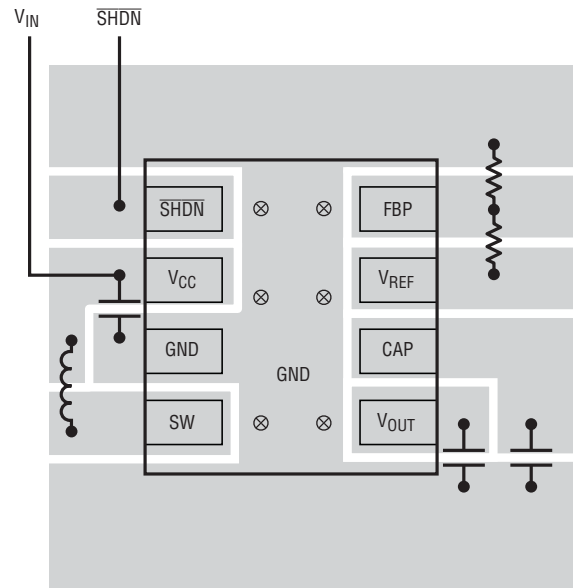


Figure 2. Programming Enable Voltage by Using External Resistors

APPLICATIONS INFORMATION

Board Layout Considerations

As with all switching regulators, careful attention must be paid to the PCB layout and component placement. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent electromagnetic interference (EMI) problems, proper layout of the high frequency switching path is essential. The voltage signal of the SW pin has sharp rising and falling edges. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. In addition, the FBP pin and V_{REF} pin are sensitive to noise. Minimize the length and area of all traces to these two pins is recommended. Recommended component placement is shown in Figure 3.



CAPACITOR GROUNDS MUST BE RETURNED DIRECTLY TO IC GROUND

Figure 3. Recommended Board Layout

TYPICAL APPLICATIONS

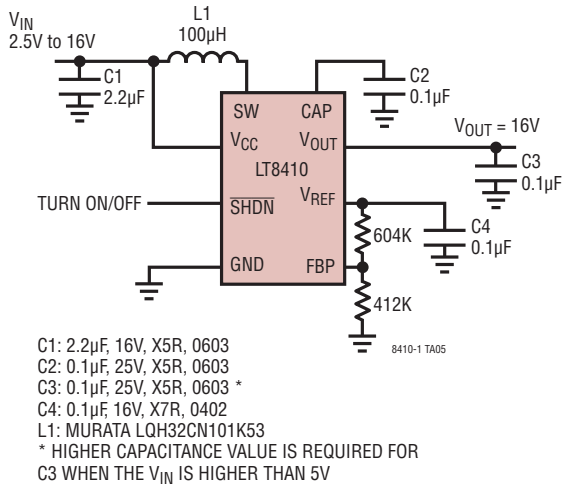
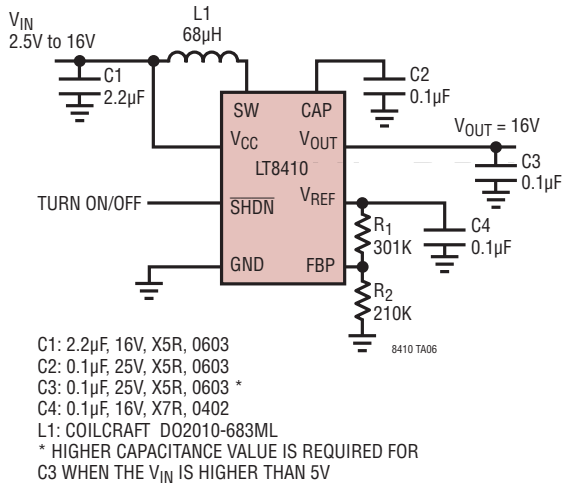
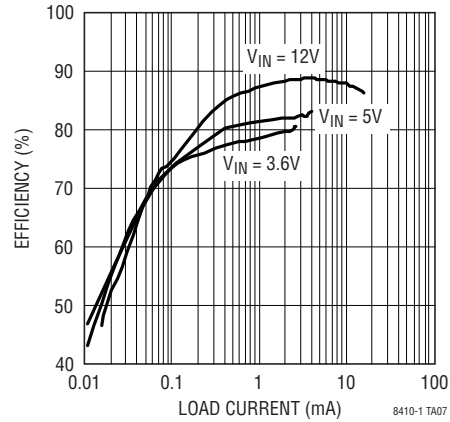


Figure 4. 16V Output Converter with Wide Input Voltage

16V Output Converter with 2mm x 2mm Inductor

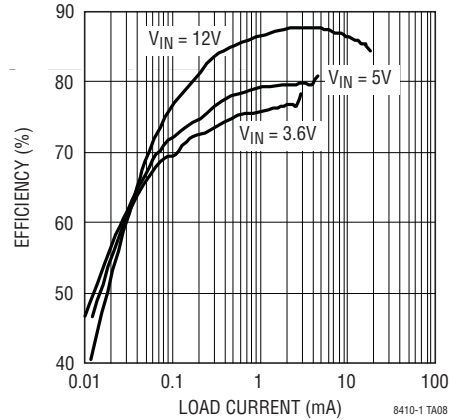


Efficiency vs Load Current



| V_{IN} (V) | I_{OUT} (mA) |
|--------------|----------------|
| 3.6 | 2.2 |
| 5 | 3.6 |
| 12 | 13 |

Efficiency vs Load Current

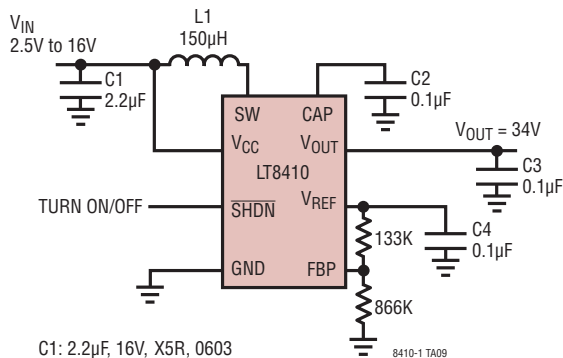


LT8410 Maximum Output Current vs Output Voltage

| V_{OUT} (V) | RESISTOR DIVIDER FROM V_{REF} $R1$ (k Ω) / $R2$ (k Ω) | MAXIMUM OUTPUT CURRENT (mA) | | | |
|---------------|--|-----------------------------|-----------------|-----------------|----------------|
| | | $V_{IN} = 2.8V$ | $V_{IN} = 3.6V$ | $V_{IN} = 5.0V$ | $V_{IN} = 12V$ |
| 40 | NA | 0.5 | 0.7 | 1.1 | 3.6 |
| 35 | 110/887 | 0.7 | 0.9 | 1.4 | 4.4 |
| 30 | 237/768 | 0.8 | 1.0 | 1.5 | 5.5 |
| 25 | 365/634 | 1.0 | 1.4 | 2.1 | 7.2 |
| 20 | 487/511 | 1.4 | 1.9 | 2.9 | 9.7 |
| 15 | 619/383 | 1.6 | 2.4 | 4.0 | 14 |
| 10 | 750/255 | 3.3 | 4.6 | 7.0 | NA |
| 5 | 866/127 | 8.0 | 11 | 17 | NA |

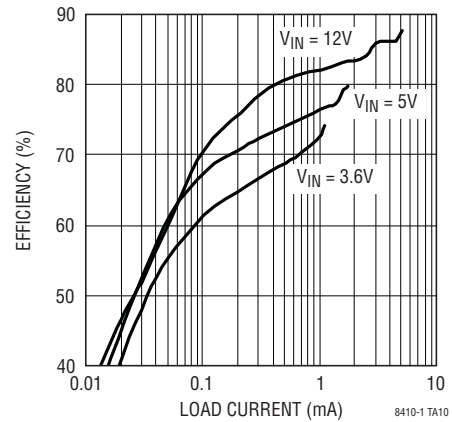
TYPICAL APPLICATIONS

34V Output Converter with Wide Input Voltage



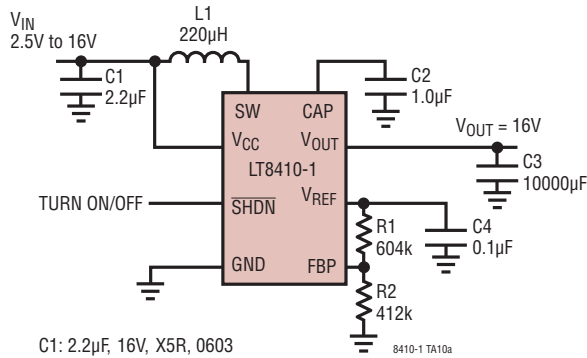
- C1: 2.2µF, 16V, X5R, 0603
 C2: 0.1µF, 100V, X5R, 0603
 C3: 0.1µF, 100V, X5R, 0603 *
 C4: 0.1µF, 16V, X7R, 0402
 L1: COILCRAFT LPS3314-154ML
 * HIGHER CAPACITANCE VALUE IS REQUIRED FOR
 C3 WHEN THE V_{IN} IS HIGHER THAN 8V

Efficiency vs Load Current



| V_{IN} (V) | I_{OUT} (mA) |
|--------------|----------------|
| 3.6 | 0.8 |
| 5 | 1.2 |
| 12 | 4.0 |

TYPICAL APPLICATIONS



C1: 2.2µF, 16V, X5R, 0603
 C2: 1.0µF, 25V, X5R, 0603 *
 C3: 10000µF, Electrolytic Capacitor
 C4: 0.1µF, 16V, X7R, 0402
 L1: COILCRAFT LPS3008-224ML
 * HIGHER CAPACITANCE VALUE IS REQUIRED FOR
 C2 WHEN THE V_{IN} IS HIGHER THAN 12V

Charging Waveforms

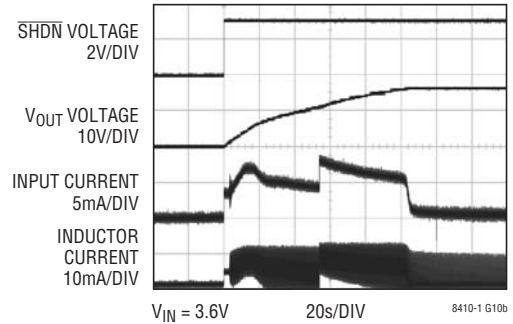


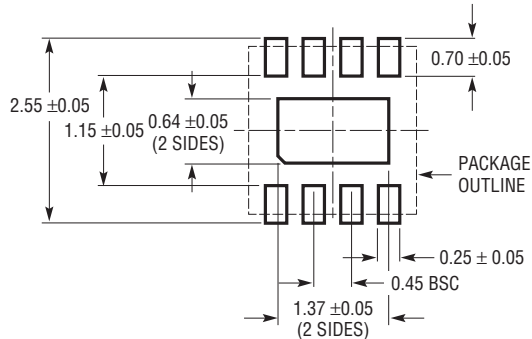
Figure 5. Capacitor Charger with the LT8410-1

LT8410-1 Maximum Output Current vs Output Voltage

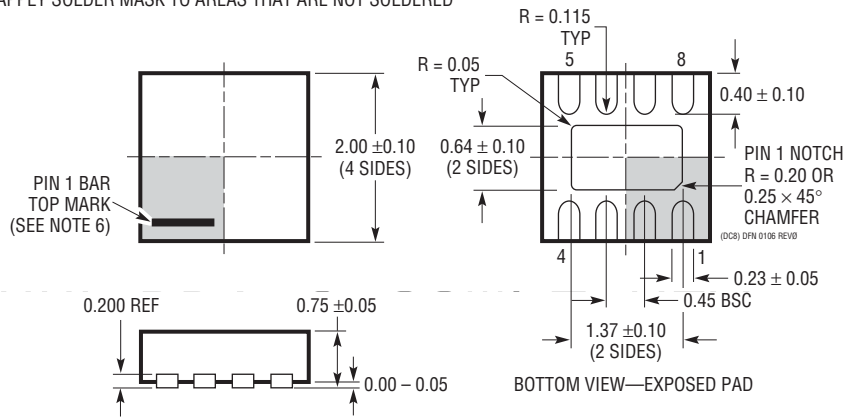
| V_{OUT} (V) | FEEDBACK RESISTOR DIVIDER R1 (k Ω) / R2 (k Ω) | MAXIMUM OUTPUT CURRENT (mA) | | | |
|---------------|---|-----------------------------|-----------------|-----------------|----------------|
| | | $V_{IN} = 2.8V$ | $V_{IN} = 3.6V$ | $V_{IN} = 5.0V$ | $V_{IN} = 12V$ |
| 40 | NA | 0.12 | 0.16 | 0.24 | 0.89 |
| 35 | 110/887 | 0.14 | 0.19 | 0.3 | 1.1 |
| 30 | 237/768 | 0.18 | 0.25 | 0.38 | 1.5 |
| 25 | 365/634 | 0.25 | 0.35 | 0.55 | 2 |
| 20 | 487/511 | 0.34 | 0.48 | 0.76 | 2.9 |
| 15 | 619/383 | 0.48 | 0.69 | 1.1 | 3.5 |
| 10 | 750/255 | 0.84 | 1.2 | 2.1 | NA |
| 5 | 866/127 | 2.3 | 3.3 | 3.5 | NA |

PACKAGE DESCRIPTION

DC Package
8-Lead Plastic DFN (2mm × 2mm)
 (Reference LTC DWG # 05-08-1719 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

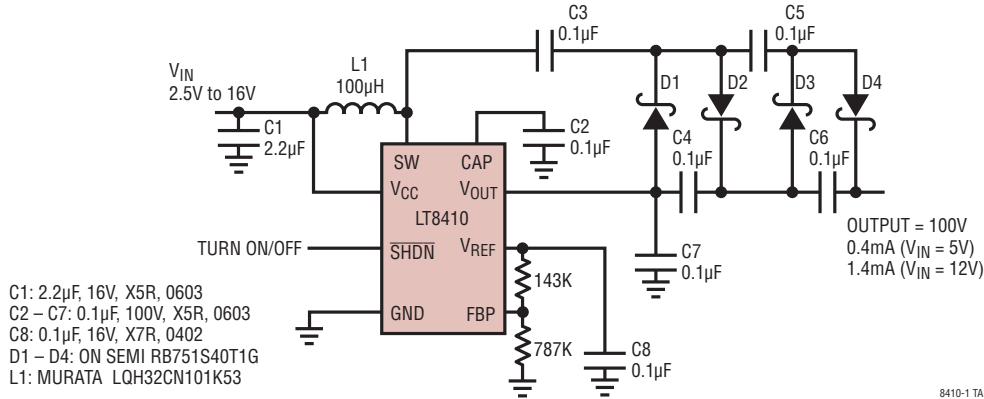


- NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
 2. DRAWING NOT TO SCALE
 3. ALL DIMENSIONS ARE IN MILLIMETERS
 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
 5. EXPOSED PAD SHALL BE SOLDER PLATED
 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

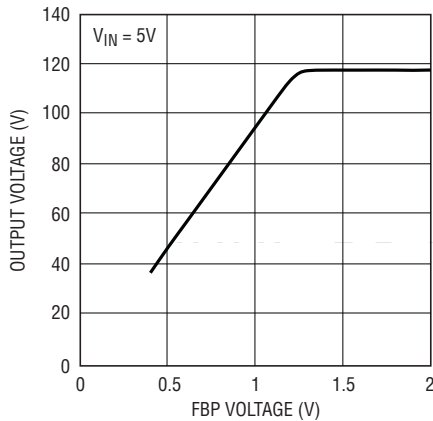
TYPICAL APPLICATION

High Voltage Power Supply Doesn't Need a Transformer

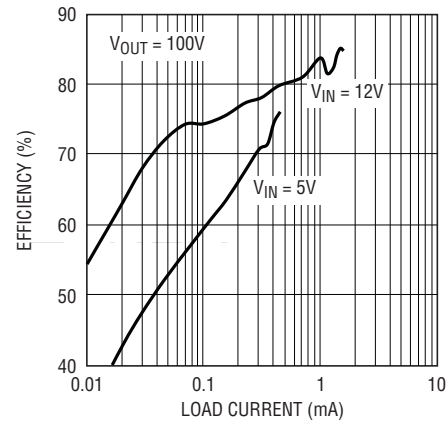
DANGER HIGH VOLTAGE! OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY



Output Voltage vs FBP Voltage



Efficiency vs Load Current



RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---------------------------------------|---|---|
| LT1946/LT1946A | 1.5A (I_{SW}), 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converters | V_{IN} : 2.45V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} < 1µA, 8-Lead MS Package |
| LT3464 | 85mA (I_{SW}), High Efficiency Step-Up DC/DC Converter with Integrated Schottky and PNP Disconnect | V_{IN} : 2.3V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 25µA, I_{SD} < 1µA, ThinSOT™ Package |
| LT3471 | Dual Output, Boost/Inverter, 1.3A (I_{SW}), High Efficiency Boost-Inverting DC/DC Converter | V_{IN} : 2.4V to 16V, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.5mA, I_{SD} < 1µA, DFN Package |
| LT3473/LT3473A | 1A (I_{SW}), 1.2MHz, High Efficiency Step-Up DC/DC Converter with Integrated Schottky Diode and Output Disconnect | V_{IN} : 2.2V to 16V, $V_{OUT(MAX)}$ = 36V, I_Q = 100µA, I_{SD} < 1µA, DFN Package |
| LT3494/LT3494A | 180mA/350mA (I_{SW}), High Efficiency, Low Noise Step-Up DC/DC Converter with Output Disconnect | V_{IN} : 2.1V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 65µA, I_{SD} < 1µA, DFN Package |
| LT3495/LT3495B/ LT3495-1/LT3495B-1 | 650mA/350mA (I_{SW}), High Efficiency, Low Noise Step-Up DC/DC Converter with Output Disconnect | V_{IN} : 2.3V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 60µA, I_{SD} < 1µA, DFN Package |