Wide Operating Range, No R_{SENSE}™ Step-Down DC/DC Controller with SMBus Programming

FEATURES

- **SMBus/I²C™ Programmable Output Voltage: 1.3V to 3.5V**
- **No Sense Resistor Required**
- **2% to 90% Duty Cycle at 200kHz**
- **$t_{ON(MIN)} \leq 100ns$**
- **True Current Mode Control**
- **Stable with Ceramic C_{OUT}**
- Power Good Output Voltage Monitor and 50µs Timer
- Wide V_{IN} Range: 4V to 36V (Abs Max)
- Precision Resistor Divider and Reference Provide ±1.35% Output Voltage Accuracy Over Temperature
- Adjustable Switching Frequency and Current Limit
- Forced Continuous Control Pin
- Programmable Soft-Start
- Output Overvoltage Protection
- Optional Short-Circuit Shutdown Timer
- Available in a 28-Lead SSOP Package

APPLICATIONS

- Power Supplies for DSPs, ASICs, FPGAs and CPUs
- Voltage Margining

DESCRIPTION

The LTC®1909-8 is a synchronous step-down switching regulator controller with a digitally programmable output voltage. The output voltage is selected from one of two 5-bit settings programmed into internal registers via a 2-wire SMBus/I²C interface. The interface features safeguards against invalid output voltages and allows the microprocessor to turn the regulator on and off. Valley current control delivers very low duty cycles without requiring a sense resistor. Operating frequency is selected by an external resistor and is compensated for variations in V_{IN} and V_{OUT}.

Discontinuous mode operation provides high efficiency operation at light loads. A forced continuous control pin reduces noise and RF interference and can assist secondary winding regulation by disabling discontinuous mode operation when the main output is lightly loaded.

Fault protection is provided by internal foldback current limiting, an output overvoltage comparator and optional short-circuit shutdown timer.

The LTC1909-8 is available in the 28-lead SSOP package.

TYPICAL APPLICATION

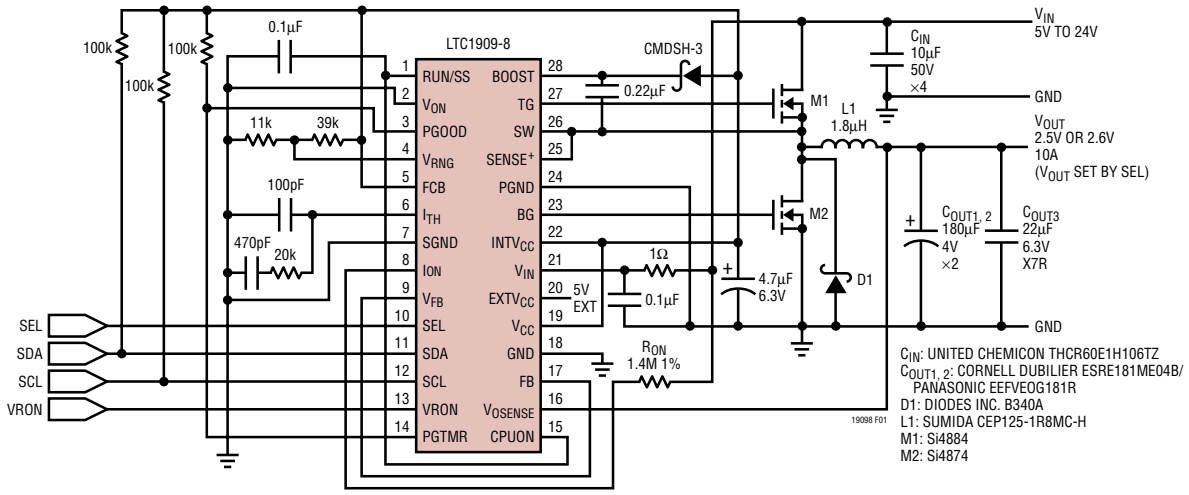


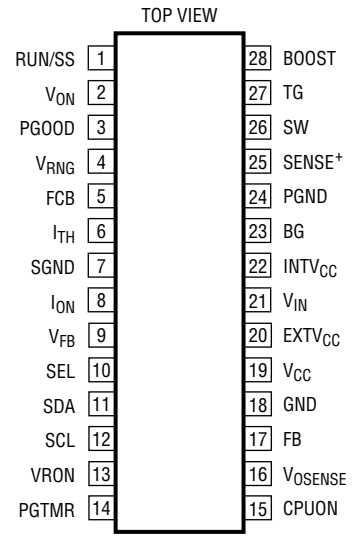
Figure 1. High Efficiency Step-Down Converter

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage
V_{IN}, I_{ON} .....–0.3V to 36V
Boosted Topside Driver Supply Voltage
BOOST ..... –0.3V to 42V
SW, SENSE+ Voltages ..... –5V to 36V
$EXTV_{CC}$, (BOOST – SW), RUN/SS, PGOOD, $INTV_{CC}$, SEL, SDA, SCL, VRON, PGTMR, V_{OSENSE}, FB, CPUON, V_{CC} Voltages ..... –0.3V to 7V
FCB, V_{ON}, V_{RNG} Voltages ..... –0.3V to ($INTV_{CC}$ + 0.3V)
I_{TH}, V_{FB} Voltages..... –0.3V to 2.7V
TG, BG, $INTV_{CC}$, $EXTV_{CC}$ Peak Currents..... 2A
TG, BG, $INTV_{CC}$, $EXTV_{CC}$ RMS Currents 50mA
Operating Ambient Temperature Range
LTC1909-8EG (Note 2) ..... –40°C to 85°C
Junction Temperature (Note 4)..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1909-8EG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

(Switching Regulator Controller) The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
I_Q	Input DC Supply Current Normal Shutdown Supply Current				 900 15	 2000 30	 µA µA
V_{FB}	Feedback Reference Voltage	I_{TH} = 1.2V (Note 3)	●	0.792	0.800	0.808	V
$\Delta V_{FB(LINEREG)}$	Feedback Voltage Line Regulation	V_{IN} = 4V to 30V, I_{TH} = 1.2V (Note 3)			0.002		%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	I_{TH} = 0.5V to 1.9V (Note 3)	●		–0.05	–0.3	%
I_{FB}	Feedback Input Current	V_{FB} = 0.8V			–5	±50	nA
$g_{m(EA)}$	Error Amplifier Transconductance	I_{TH} = 1.2V (Note 3)	●	1.4	1.7	2	mS
V_{FCB}	Forced Continuous Threshold		●	0.76	0.8	0.84	V
I_{FCB}	Forced Continuous Pin Current	V_{FCB} = 0.8V			–1	–2	µA
t_{ON}	On-Time	I_{ON} = 60µA, V_{ON} = 1.5V I_{ON} = 30µA, V_{ON} = 1.5V		212 425	250 500	288 575	ns ns
$t_{ON(MIN)}$	Minimum On-Time	I_{ON} = 180µA, V_{ON} = 0V			50	100	ns
$t_{OFF(MIN)}$	Minimum Off-Time	I_{ON} = 60µA, V_{ON} = 1.5V			250	400	ns
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold $V_{PGND} – V_{SENSE+}$	V_{RNG} = 1V, V_{FB} = 0.76V V_{RNG} = 0V, V_{FB} = 0.76V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.76V	 ● 	113 79 158	133 93 186	153 107 214	mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold $V_{PGND} – V_{SENSE+}$	V_{RNG} = 1V, V_{FB} = 0.84V V_{RNG} = 0V, V_{FB} = 0.84V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.84V			–67 –47 –93		mV mV mV
$\Delta V_{FB(OV)}$	Output Overvoltage Fault Threshold			5.5	7.5	9.5	%

ELECTRICAL CHARACTERISTICS

(Switching Regulator Controller) The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\Delta V_{FB(UV)}$	Output Undervoltage Fault Threshold			520	600	680	mV
$V_{RUN/SS(ON)}$	RUN Pin Start Threshold		●	0.8	1.5	2	V
$V_{RUN/SS(LE)}$	RUN Pin Latchoff Enable Threshold	RUN/SS Pin Rising			4	4.5	V
$V_{RUN/SS(LT)}$	RUN Pin Latchoff Threshold	RUN/SS Pin Falling			3.5	4.2	V
$I_{RUN/SS(C)}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 0V		–0.5	–1.2	–3	µA
$I_{RUN/SS(D)}$	Soft-Start Discharge Current	$V_{RUN/SS}$ = 4.5V, V_{FB} = 0V		0.8	1.8	3	µA
$V_{IN(UVLO)}$	Undervoltage Lockout	V_{IN} Falling	●		3.4	3.9	V
$V_{IN(UVLOR)}$	Undervoltage Lockout Release	V_{IN} Rising	●		3.5	4	V
TG R_{UP}	TG Driver Pull-Up On Resistance	TG High			2	3	Ω
TG R_{DOWN}	TG Driver Pull-Down On Resistance	TG Low			2	3	Ω
BG R_{UP}	BG Driver Pull-Up On Resistance	BG High			3	4	Ω
BG R_{DOWN}	BG Driver Pull-Down On Resistance	BG Low			1	2	Ω
TG t_r	TG Rise Time	C_{LOAD} = 3300pF, 20% to 80% of Swing			20		ns
TG t_f	TG Fall Time	C_{LOAD} = 3300pF, 20% to 80% of Swing			20		ns
BG t_r	BG Rise Time	C_{LOAD} = 3300pF, 20% to 80% of Swing			20		ns
BG t_f	BG Fall Time	C_{LOAD} = 3300pF, 20% to 80% of Swing			20		ns
Internal V_{CC} Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V, V_{EXTVCC} = 4V	●	4.7	5	5.3	V
$\Delta V_{LDO(LOADREG)}$	Internal V_{CC} Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 4V			–0.1	±2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 20mA, V_{EXTVCC} Rising	●	4.5	4.7		V
ΔV_{EXTVCC}	$EXTV_{CC}$ Switch Drop Voltage	I_{CC} = 20mA, V_{EXTVCC} = 5V			150	300	mV
$\Delta V_{EXTVCC(HYS)}$	$EXTV_{CC}$ Switchover Hysteresis				200		mV
PGOOD Output							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		5.5	7.5	9.5	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		–5.5	–7.5	–9.5	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning			1	2	%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.15	0.4	V

(SMBus VID Programmer) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 2.7V ≤ V_{CC} ≤ 5.5V (Note 5) unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Operating Supply Voltage Range			2.7		5.5	V
I_{CC}	Supply Current	CPUON, PGTMR Pins Are Open	●			350	µA
$R_{FB-SENSE}$	Resistance Between V_{OSENSE} and FB		●	14	20	26	kΩ
DE	Divider Error (Note 6)	V_{OSENSE} Programmed from 1.3V to 3.5V	●	–0.35		0.35	%
V_{IH}	SCL, SDA Input High Voltage		●	2.1			V
V_{IL}	SCL, SDA Input Low Voltage		●			0.8	V
V_{IH}	SEL, VRON Input High Voltage				1.3	2	V
V_{IL}	SEL, VRON Input Low Voltage		●	0.8	1.3		V
V_{HYST}	SEL, VRON Hysteresis				±50		mV
V_{OL}	SDA, CPUON PGTMR Output Low Voltage	I = 3mA	●			0.4	V
I_{IN}	SCL, SDA, SEL, VRON Input Current	SDA Not Acknowledging, 0 ≤ V_{PIN} ≤ 5.5V, V_{PIN} = 5.5V for VRON only	●			±10	µA

ELECTRICAL CHARACTERISTICS

(SMBus VID Programmer) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 2.7V ≤ V_{CC} ≤ 5.5V (Note 5) unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SK1}	SDA, PGTMR, CPUON Sink Current at V_{CC} = 2.7V	0 ≤ V_{PIN} ≤ 2.7V	●	5	19	60	mA
I_{SK2}	SDA, PGTMR, CPUON Sink Current at V_{CC} = 5.5V	0 ≤ V_{PIN} ≤ 5.5V	●	35	65	150	mA
I_{LKG}	PGTMR, CPUON Leakage Current	0 ≤ V_{PIN} ≤ 5.5V				±0.2	µA
I_{PU}	VRON Pull-Up Current	V_{PIN} = 0	●	–1	–2.5	–7	µA
Timing (Note 7)							
f_{SMB}	SMBus Operating Frequency		●	10		100	KHz
t_{BUF}	Bus Free Time Between Stop/Start		●	4.7			µs
$t_{HD:STA}$	Hold Time After (Repeated) Start		●	4			µs
$t_{SU:STA}$	Repeated Start Setup Time		●	4.7			µs
$t_{SU:STO}$	Stop Condition Setup Time		●	4			µs
$t_{HD:DAT}$	Data Hold Time		●	300			ns
$t_{SU:DAT}$	Data Setup Time		●	250			ns
t_{LOW}	Clock Low Period		●	4.7			µs
t_{HIGH}	Clock High Period		●	4			µs
t_f	SCL, SDA Fall Time	0.9V_{CC} to 0.65V	●			300	ns
t_r	SCL, SDA Rise Time	0.65V to 2.25V	●			1000	ns
t_{SSH}	SEL to V_{OSENSE} High (Note 8)	Toggle SEL to Switch from 01111B to 10000B, V_{FB} = 0.8V	●		500		ns
t_{SSL}	SEL to V_{OSENSE} Low (Note 8)	Toggle SEL to Switch from 10000B to 01111B, V_{FB} = 0.8V	●		500		ns
t_{SPL}	SEL Toggling to PGTMR Low	Toggle SEL to Select New Code C_L = 100pF, 10kΩ Pull-Up, S2 in Test Circuit	●		160	500	ns
t_{PH}	Stop Bit to CPUON High (Note 9)	C_L = 100pF, 10kΩ Pull-Up, S2 in Test Circuit	●			2	µs
t_{PL}	Stop Bit to CPUON Low (Note 9)	C_L = 0.1µF, 10kΩ Pull-Up, S1 in Test Circuit	●		20	50	µs
t_{PPL}	Stop Bit to PGTMR Low (Note 9)	C_L = 100pF, 10kΩ Pull-Up, S2 in Test Circuit	●			250	ns
t_{VH}	VRON High to CPUON High	C_L = 100pF, 10kΩ Pull-Up, S2 in Test Circuit	●			2	µs
t_{VL}	VRON Low to CPUON Low	C_L = 0.1µF, 10kΩ Pull-Up, S1 in Test Circuit	●			50	µs
t_{VPL}	VRON Low to PGTMR Low	C_L = 100pF, 10kΩ Pull-Up, S2 in Test Circuit	●		130	500	ns
t_{PGL}	PGTMR Low Duration	C_L = 100pF, 10kΩ Pull-Up, S2 in Test Circuit		30	50	70	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1909-8E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC1909-8 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

Note 4: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

LTC1909-8E: $T_J = T_A + (P_D \bullet 130°C/W)$

Note 5: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise noted.

Note 6: The divider error is tested in a feedback loop that adjusts FB to 0.8V for each 5-bit code.

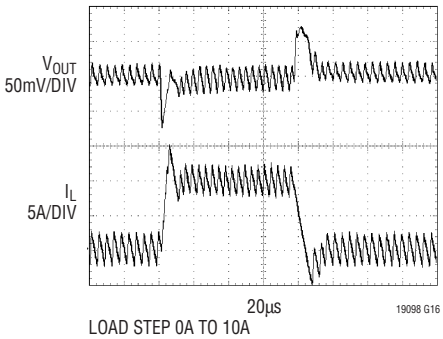
Note 7: These parameters are guaranteed by design and are not tested in production. SMBus timing is referenced to V_{IL} and V_{IH} levels.

Note 8: Dominated by the switching regulator. The delay due to the SMBus VID programmer is only 500ns typ.

Note 9: Measured from the rising edge of SDA during Data High acknowledgment.

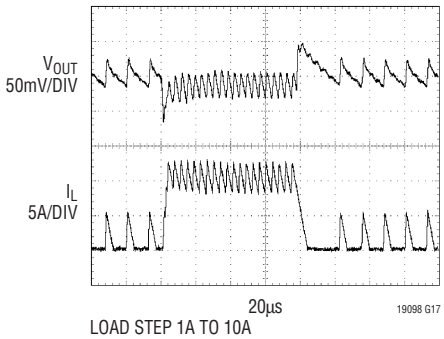
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response



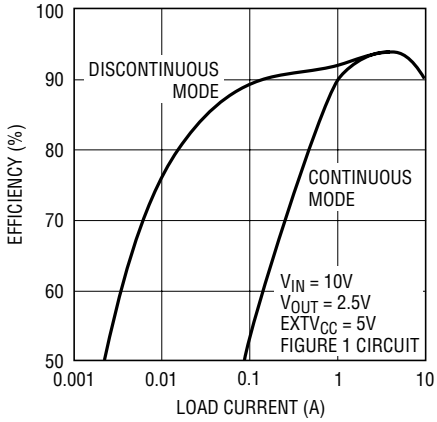
LOAD STEP 0A TO 10A
V_{IN} = 15V
V_{OUT} = 2.5V
FCB = 0V
FIGURE 1 CIRCUIT

Transient Response (Discontinuous Mode)

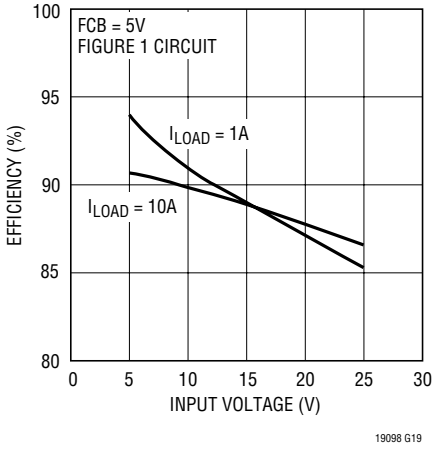


LOAD STEP 1A TO 10A
V_{IN} = 15V
V_{OUT} = 2.5V
FCB = $INTV_{CC}$
FIGURE 1 CIRCUIT

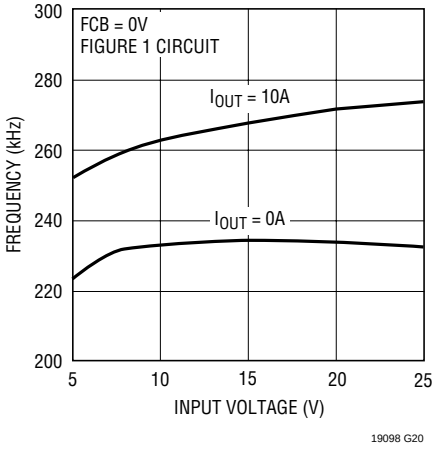
Efficiency vs Load Current



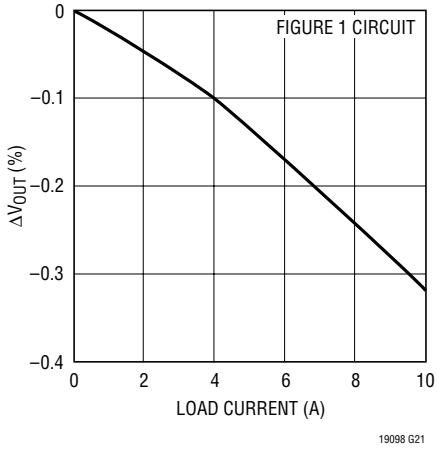
Efficiency vs Input Voltage



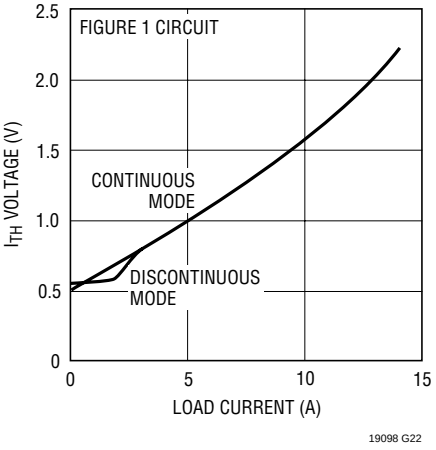
Frequency vs Input Voltage



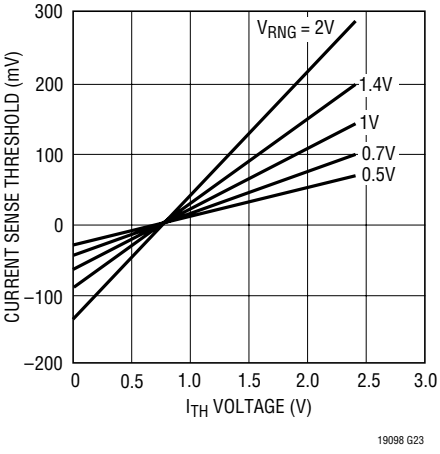
Load Regulation



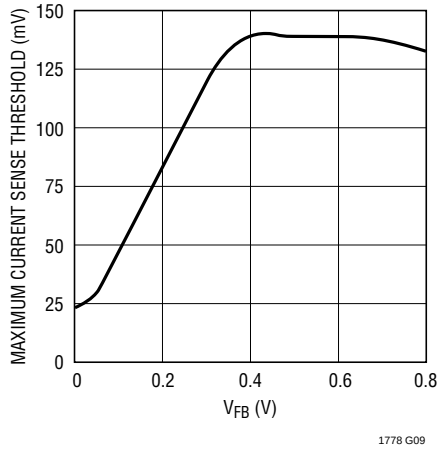
I_{TH} Voltage vs Load Current



Current Sense Threshold vs I_{TH} Voltage

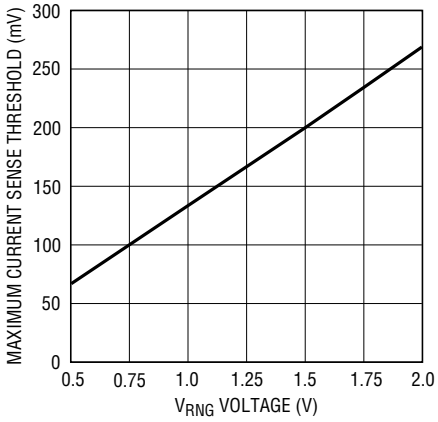


Current Limit Foldback

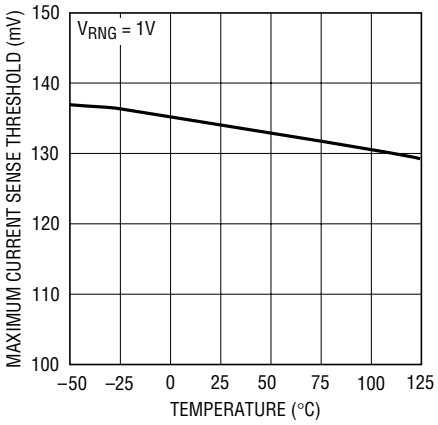


TYPICAL PERFORMANCE CHARACTERISTICS

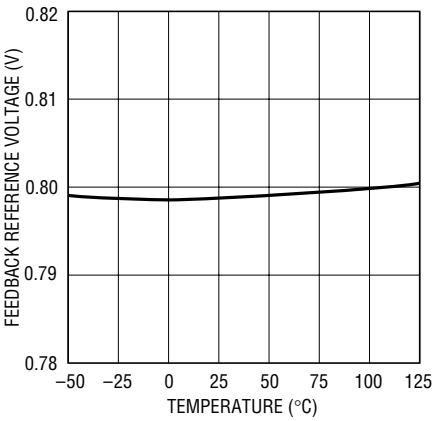
Maximum Current Sense Threshold vs V_{RNG} Voltage



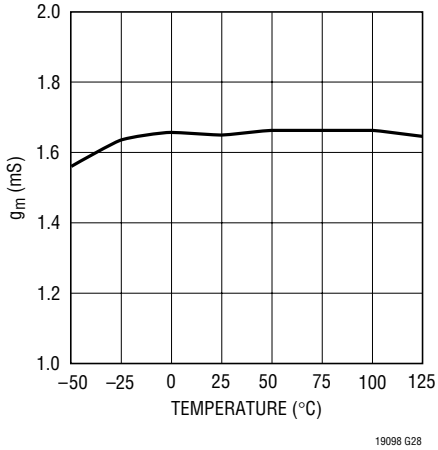
Maximum Current Sense Threshold vs Temperature



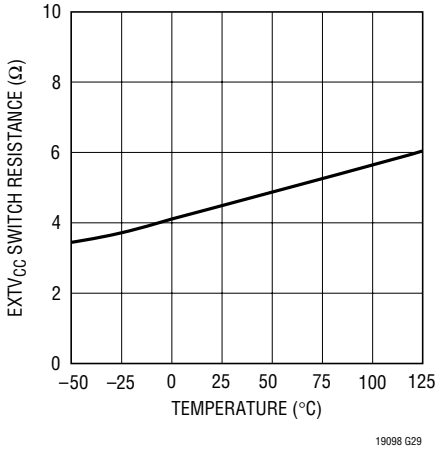
Feedback Reference Voltage vs Temperature



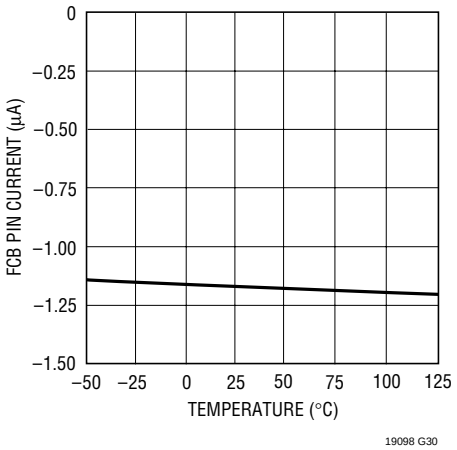
Error Amplifier g_m vs Temperature



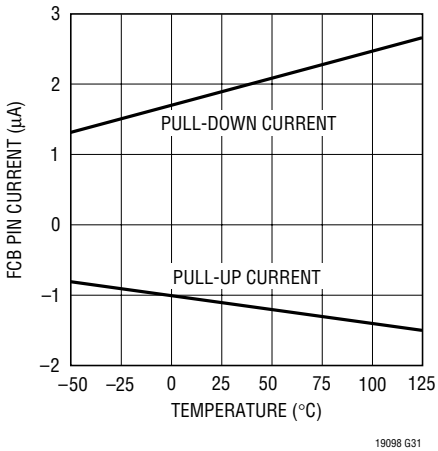
$EXTV_{CC}$ Switch Resistance vs Temperature



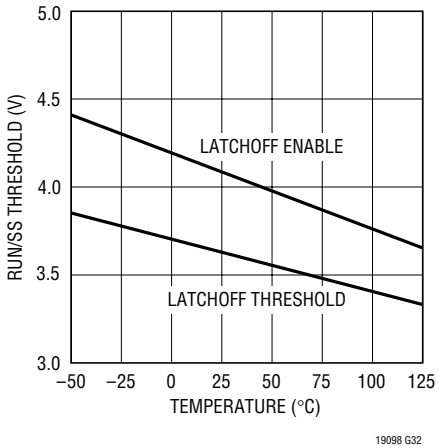
FCB Pin Current vs Temperature



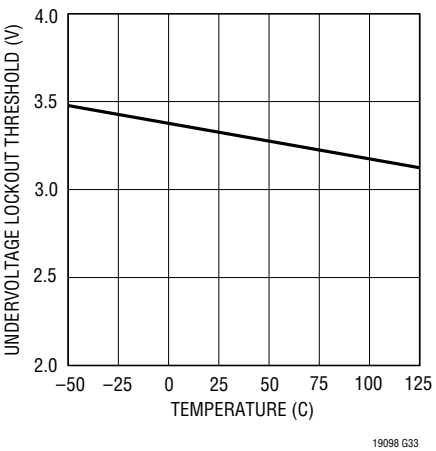
RUN/SS Pin Current vs Temperature



RUN/SS Latchoff Thresholds vs Temperature

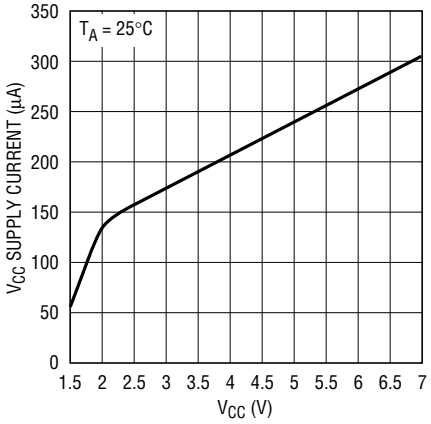


Undervoltage Lockout Threshold vs Temperature



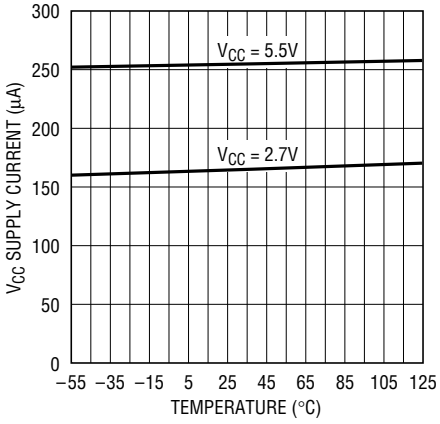
TYPICAL PERFORMANCE CHARACTERISTICS (SMBus VID Programmer)

V_{CC} Supply Current vs Supply Voltage



19098 G01

V_{CC} Supply Current vs Temperature



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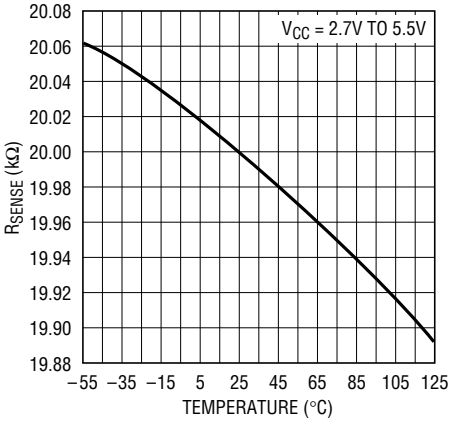
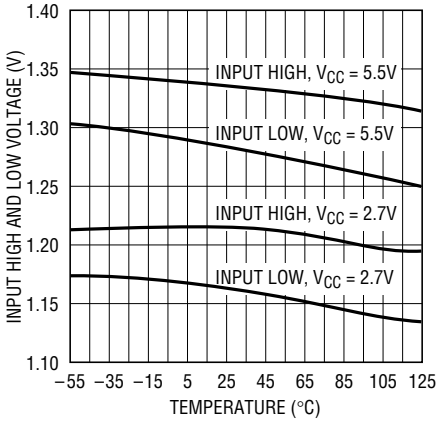
Resistance Between V_{OSENSE} and FB Pins vs Temperature



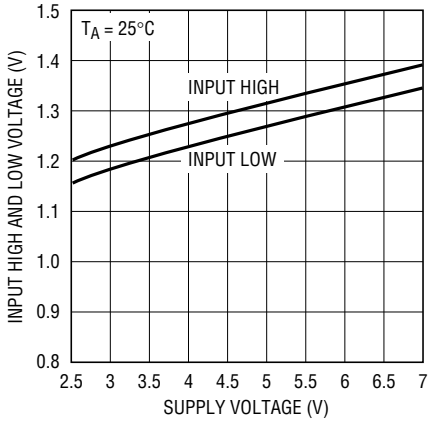
19098 G03

SCL, SDA, SEL and VRON Input High and Low Voltage vs Temperature



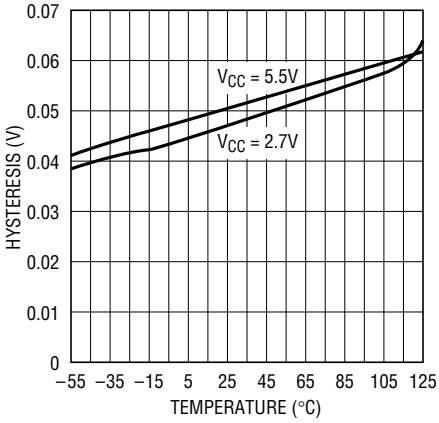
19098 G04

SCL, SDA, SEL and VRON Input High and Low Voltage vs Supply Voltage



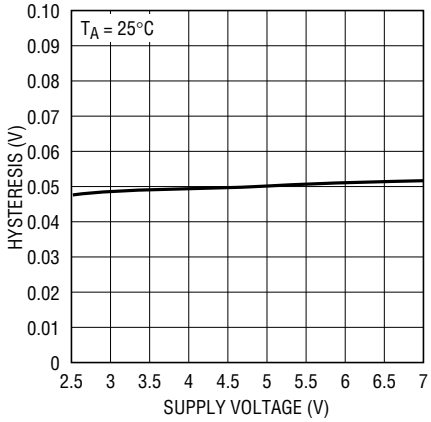
19098 G05

SCL, SDA, SEL and VRON Hysteresis vs Temperature



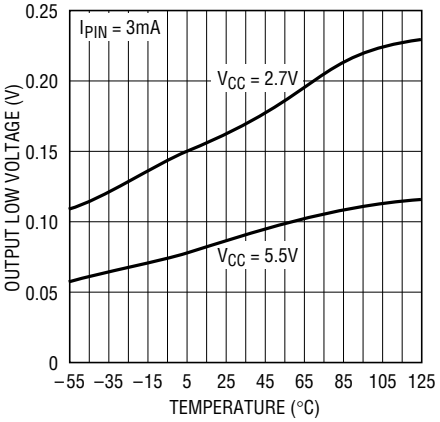
19098 G06

SCL, SDA, SEL and VRON Hysteresis vs Supply Voltage



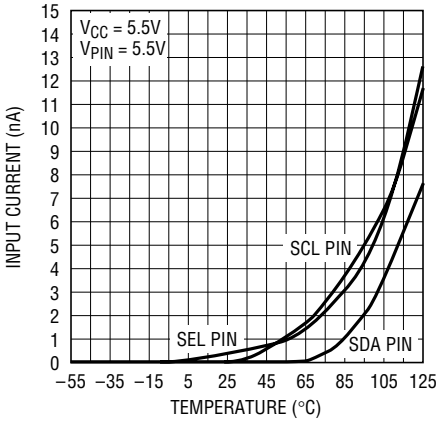
19098 G07

SDA, CPUON, PGTMR Output Low Voltage vs Temperature



19098 G08

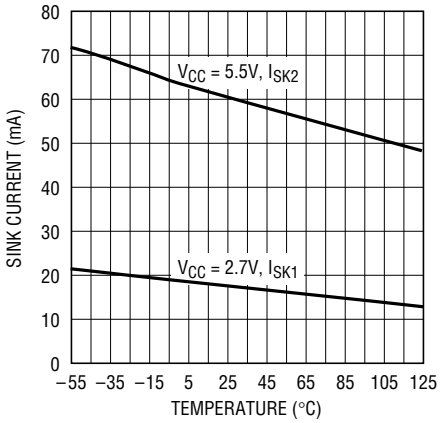
SCL, SDA, SEL Input Current vs Temperature



19098 G09

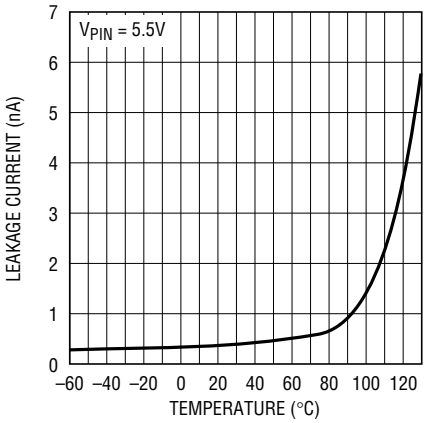
TYPICAL PERFORMANCE CHARACTERISTICS (SMBus VID Programmer)

SDA, PGTMR, CPUON Sink Current vs Temperature



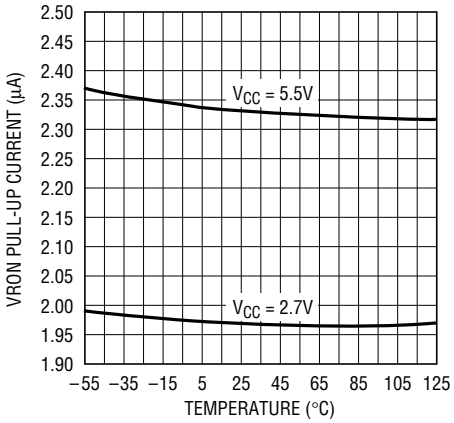
19098 G10

PGTMR, CPUON Leakage Current vs Temperature



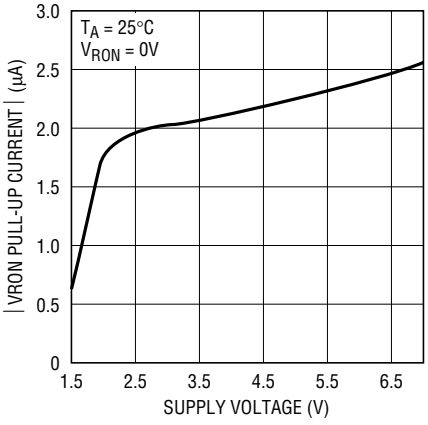
19098 G11

VRON Pull-Up Current vs Temperature



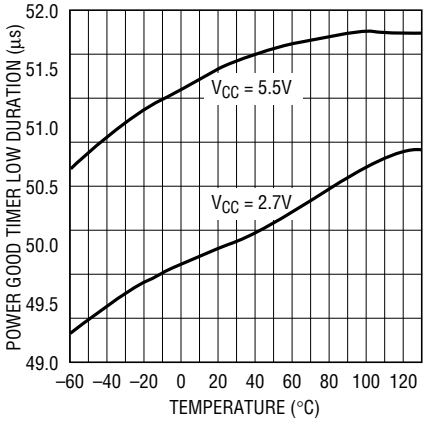
19098 G12

VRON Pull-Up Current vs Supply Voltage



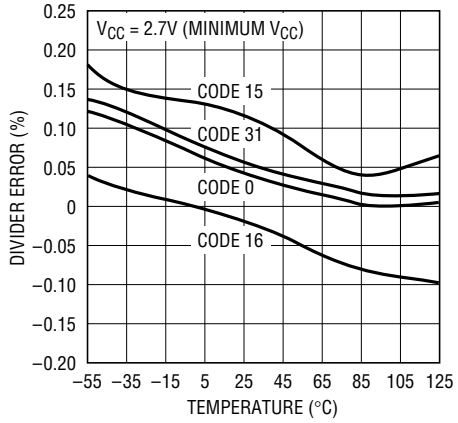
19098 G013

Power Good Timer Low Duration vs Temperature



19098 G14

Resistor Divider Error vs Temperature



19098 G15

PIN FUNCTIONS

RUN/SS (Pin 1): Run Control and Soft-Start Input. A capacitor to ground at this pin sets the ramp time to full output current (approximately 3s/µF) and the time delay for overcurrent latchoff (see Applications Information). Forcing this pin below 0.8V shuts down the device.

V_{ON} (Pin 2): On-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to V_{OUT}. The comparator input defaults to 0.7V when the pin is grounded and 2.4V when the pin is tied to $INTV_{CC}$.

PGOOD (Pin 3): Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

V_{RNG} (Pin 4): Sense Voltage Range Input. The voltage at this pin is ten times the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from $INTV_{CC}$. The nominal sense voltage defaults to 70mV when this pin is tied to ground, 140mV when tied to $INTV_{CC}$.

FCB (Pin 5): Forced Continuous Input. Tie this pin to ground to force continuous synchronous operation at low load, to $INTV_{CC}$ to enable discontinuous mode operation at low load or to a resistive divider from a secondary output when using a secondary winding.

I_{TH} (Pin 6): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.8V corresponding to zero sense voltage (zero current).

SGND (Pin 7): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

I_{ON} (Pin 8): On-Time Current Input. Tie a resistor from V_{IN} to this pin to set the one-shot timer current and thereby set the switching frequency.

V_{FB} (Pin 9): Error Amplifier Feedback Input. This pin connects to the error amplifier input to the center tap of the SMBus programmable divider at the FB pin (Pin 17).

SEL (Pin 10): Register Select Input. A TTL compatible logic input pin that is used to select 1 of 2 resistor divider settings. SEL selects the setting in Register 0 if pulled low and the setting in Register 1 if pulled high.

SDA (Pin 11): SMBus Data Input/Output. SDA is a high impedance input when address, command or data bits are shifted into the SMBus interface. It is an open-drain N-channel output when acknowledging or sending data back to the microprocessor during read back. It requires a pull-up resistor or current source to V_{CC}.

SCL (Pin 12): SMBus Clock Input. Data at the SDA pin is latched into the LTC1909-8 SMBus interface at the rising edge of the clock and is shifted out of the SDA pin at the falling edge of the clock. SCL is a high impedance input pin. It is driven by the open collector output of a microprocessor and requires a pull-up resistor or current source to V_{CC}.

VRON (Pin 13): Global Control Input. This TTL compatible input pin is pulled up internally by a 2.5µA current source. Pulling VRON low forces the open-drain output pins (CPUON and PGTMR) to pull to ground. If the LTC1909-8 is programmed to turn on a DC/DC converter, pulling VRON high three-states the CPUON pin and allows the switching regulator to soft-start if CPUON is tied to the RUN/SS pin.

PGTMR (Pin 14): Power Good Timer Output. This open-drain output is pulled low for 50µs each time the switching regulator is turned on or SEL is toggled to select a new code. PGTMR may be connected to the FCB pin to force the converter into continuous mode operation. This reduces the time needed for the converter output to settle to a lower output voltage under light load conditions if the SEL pin is toggled to select a lower output voltage.

CPUON (Pin 15): CPU DC/DC Converter Control. Open-drain output, usually connected to the RUN/SS pin. It pulls low to shut down the converter or becomes high impedance to allow the converter to soft-start.

V_{OSENSE} (Pin 16): Sense Input. Upper terminal of the SMBus programmable resistor divider that is connected directly to the regulated output voltage node.

PIN FUNCTIONS

FB (Pin 17): Feedback Input. Center tap of the SMBus programmable divider that is connected to Pin 9.

GND (Pin 18): SMBus Programmer Ground. Connect to regulator signal ground at Pin 7.

V_{CC} (Pin 19): Positive Supply of the SMBus VID Programmer. 2.7V ≤ V_{CC} ≤ 5.5V. May be connected to the $INTV_{CC}$ pin. Bypass this pin to ground with a 0.1µF ceramic capacitor if using an external supply.

$EXTV_{CC}$ (Pin 20): External V_{CC} Input. When $EXTV_{CC}$ exceeds 4.7V, an internal switch connects this pin to $INTV_{CC}$ and shuts down the internal regulator so that controller and gate drive power is drawn from $EXTV_{CC}$. Do not exceed 7V at this pin and ensure that $EXTV_{CC} < V_{IN}$.

V_{IN} (Pin 21): Main Input Supply. Decouple this pin to PGND with an RC filter (1Ω, 0.1µF).

$INTV_{CC}$ (Pin 22): Internal 5V Regulator Output. The driver and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7µF low ESR tantalum or other low ESR capacitor. The internal 5V regulator is shut down when $V_{RUN/SS}$ <1.5V.

BG (Pin 23): Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and $INTV_{CC}$.

PGND (Pin 24): Power Ground. Connect this pin closely to the source of the bottom N-channel MOSFET, the (–) terminal of C_{VCC} and the (–) terminal of C_{IN}.

$SENSE^+$ (Pin 25): Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the SW pin unless using a sense resistor (see Applications Information).

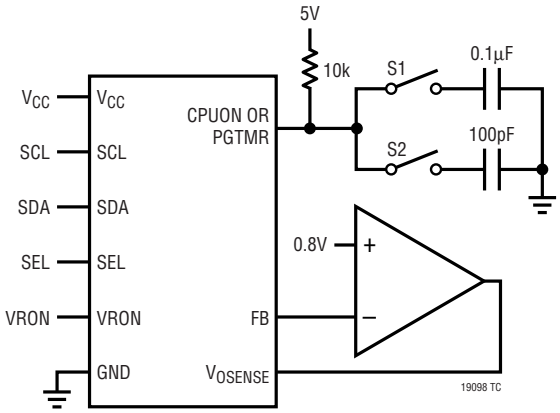
SW (Pin 26): Switch Node. The (–) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below ground up to V_{IN}.

TG (Pin 27): Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

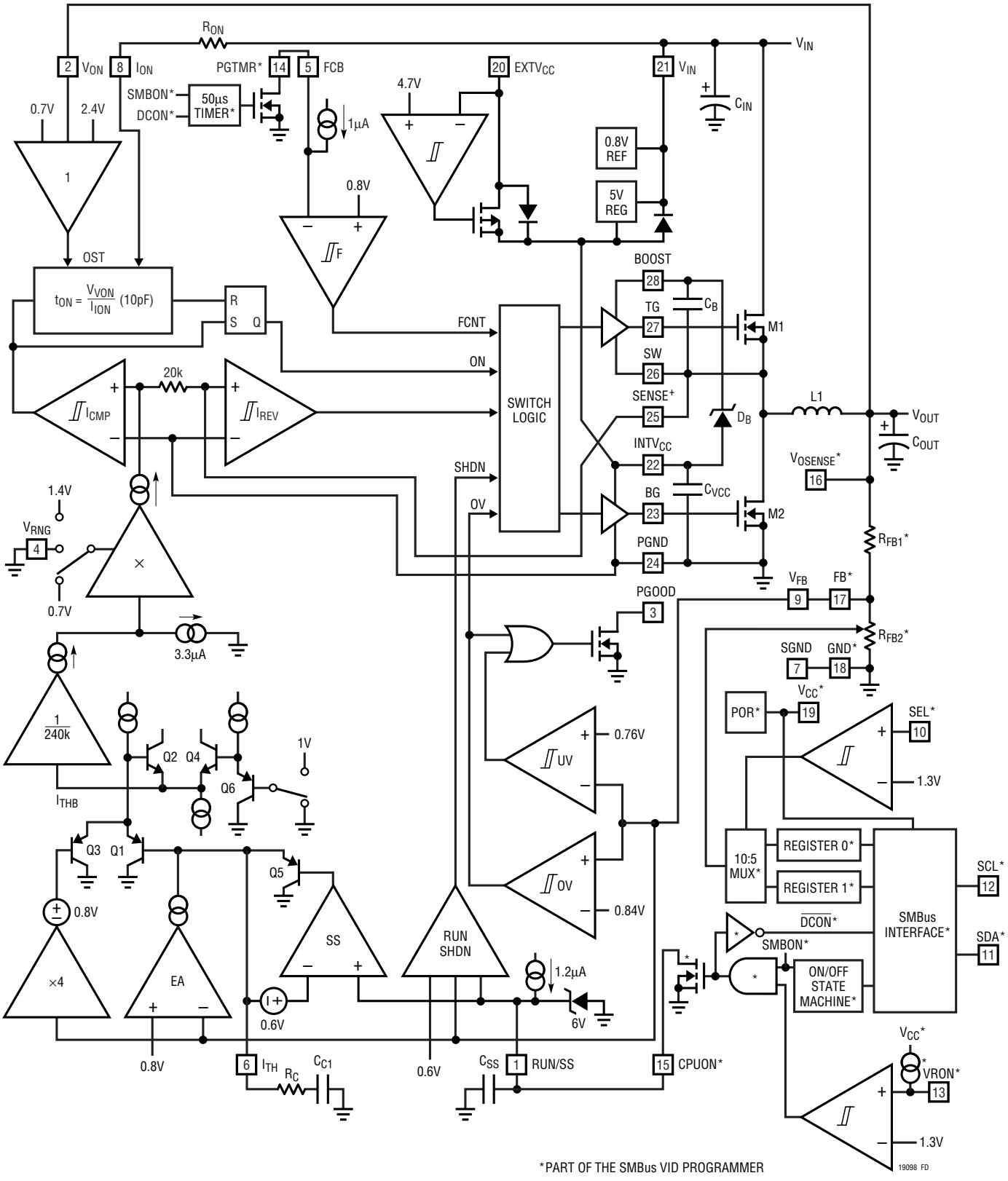
BOOST (Pin 28): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

TEST CIRCUIT

SMBus VID Programmer Test Circuit

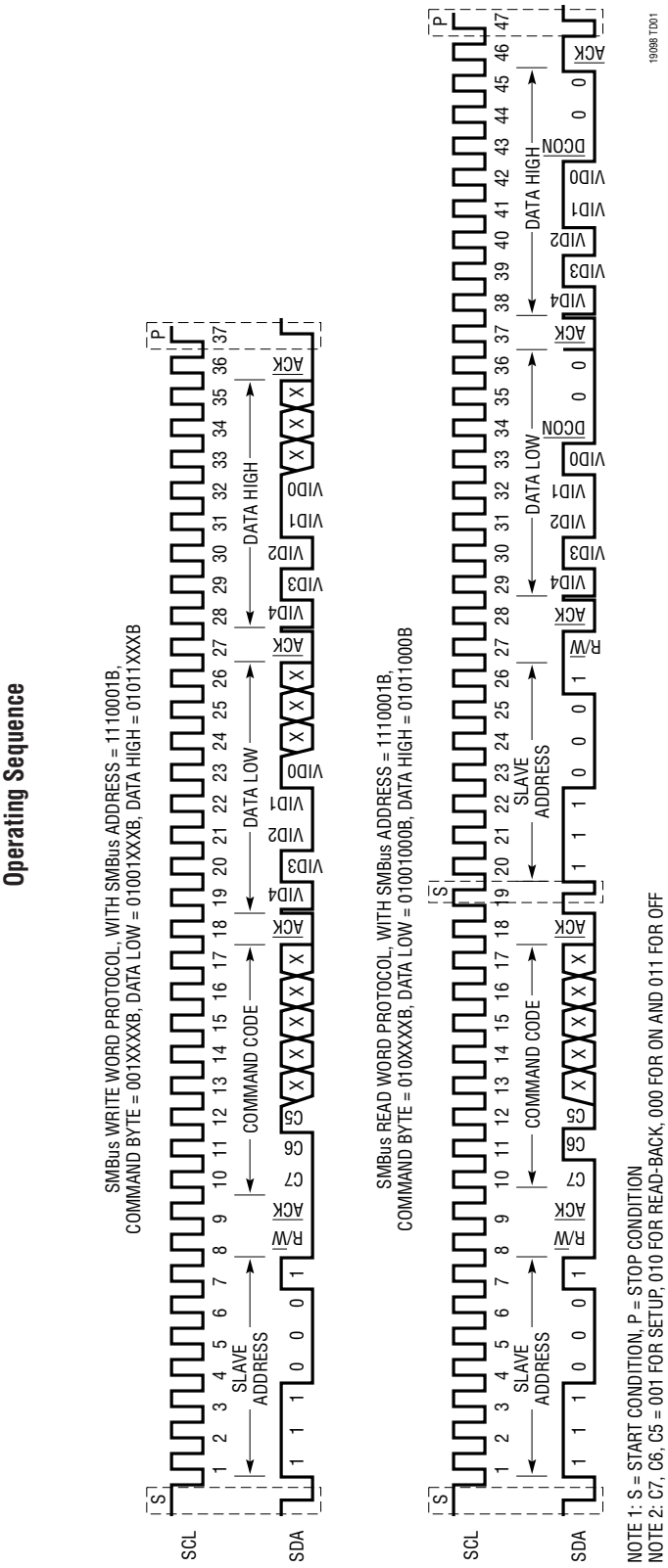


FUNCTIONAL DIAGRAM



TIMING DIAGRAMS

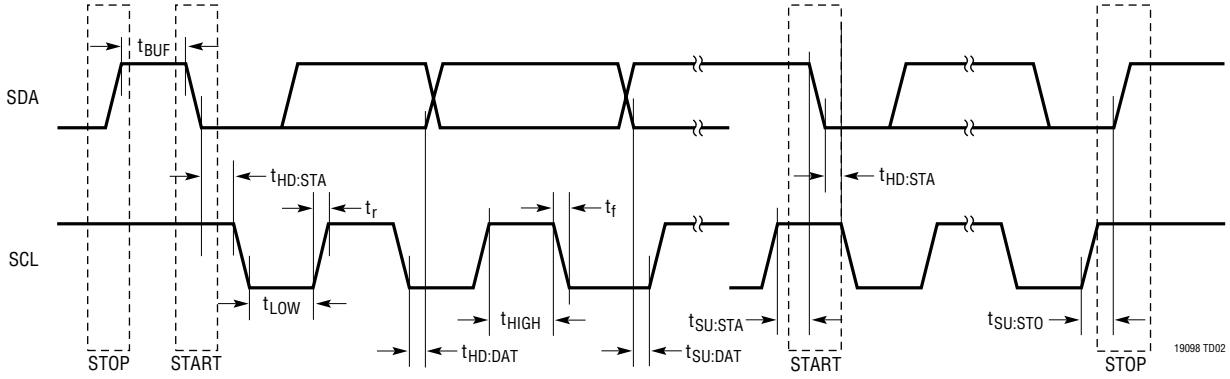
Operating Sequence



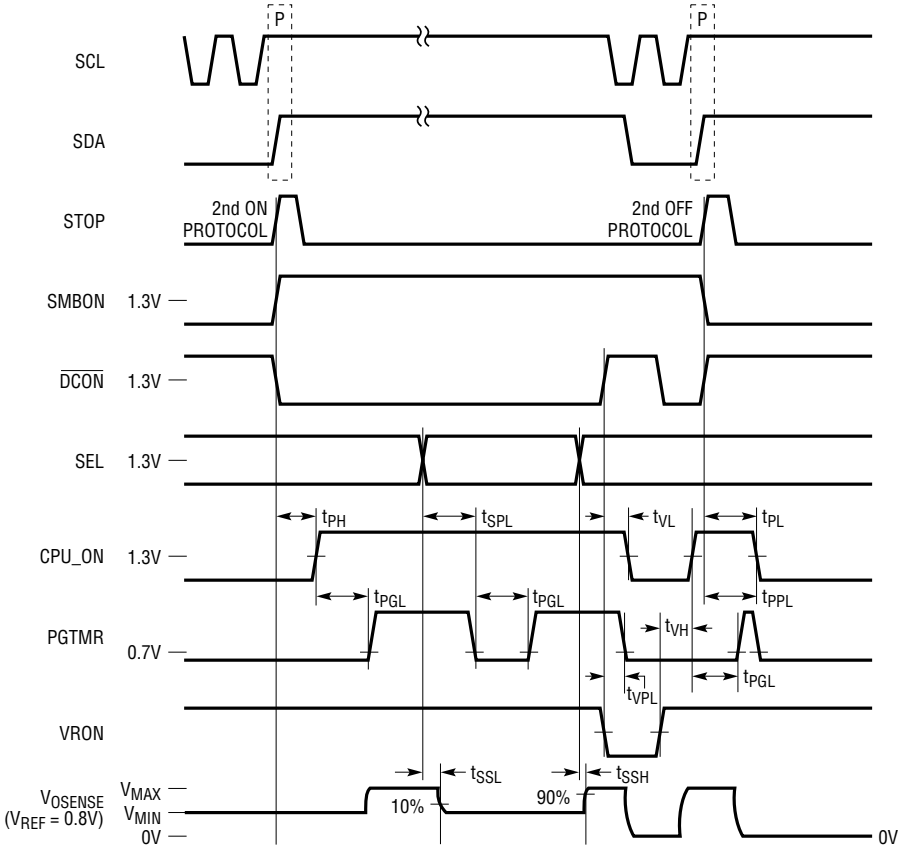
NOTE 1: S = START CONDITION, P = STOP CONDITION
NOTE 2: C7, C6, C5 = 001 FOR SETUP, 010 FOR READ-BACK, 000 FOR ON AND 011 FOR OFF

TIMING DIAGRAMS

Timing for SMBus Interface



VRON, SEL, CPUON and PGTMR Timing



NOTE: TIMING RELATIVE TO THE STOP BIT (P) IS MEASURED FROM THE RISING EDGE OF SDA
SEE TABLE 1 FOR V_{MIN} AND V_{MAX} SENSE VOLTAGES

19098 TD03

OPERATION (Refer to Functional Diagram)

The LTC1909-8 consists of two independent sections: a current mode controller for the DC/DC step-down converter and a SMBus VID voltage programmer. It simplifies the design of SMBus controlled power supplies.

Current Mode Controller

In normal operation, the top MOSFET of the current mode controller is turned on for a fixed interval determined by a one-shot timer OST. When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator I_{CMP} trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage between the PGND and SENSE$^+$ pins using either the bottom MOSFET on-resistance or a separate sense resistor. The voltage on the I_{TH} pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this voltage by comparing the feedback signal V_{FB} from the output voltage with an internal 0.8V reference. The feedback voltage is derived from the output voltage by a resistive divider in the SMBus VID programmer. If the load current increases, it causes a drop in the feedback voltage relative to the reference. The I_{TH} voltage then rises until the average inductor current again matches the load current.

At low load currents, the inductor current can drop to zero and become negative. This is detected by current reversal comparator I_{REV} which then shuts off M2, resulting in discontinuous operation. Both switches will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current level (0.8V) to initiate another cycle. Discontinuous mode operation is disabled by comparator F when the FCB pin is brought below 0.8V, forcing continuous synchronous operation.

The operating frequency is determined implicitly by the top MOSFET on-time and the duty cycle required to maintain regulation. The one-shot timer generates an on-time that is proportional to the ideal duty cycle, thus holding frequency approximately constant with changes in V_{IN}. The nominal frequency can be adjusted with an external resistor R_{ON}.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a ±7.5% window around the regulation point. Furthermore, in an overvoltage condition, M1 is turned off and M2 is turned on and held on until the overvoltage condition clears.

Foldback current limiting is provided if the output is shorted to ground. As V_{FB} drops, the buffered current threshold voltage I_{THB} is pulled down by clamp Q3 to a 1V level set by Q4 and Q6. This reduces the inductor valley current level to one sixth of its maximum value as V_{FB} approaches 0V.

Pulling the RUN/SS pin low forces the controller into its shutdown state, turning off both M1 and M2. Releasing the pin allows an internal 1.2µA current source to charge up an external soft-start capacitor C_{SS}. When this voltage reaches 1.5V, the controller turns on and begins switching, but with the I_{TH} voltage clamped at approximately 0.6V below the RUN/SS voltage. As C_{SS} continues to charge, the soft-start current limit is removed. Shorting the RUN/SS pin to the CPUON pin of the SMBus VID programmer puts the regulator under software control. The open-drain CPUON pin does not interfere with the soft-start cycle.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most of the internal controller circuitry is derived from the $INTV_{CC}$ pin. The top MOSFET driver is powered from a floating bootstrap capacitor C_B. This capacitor is recharged from $INTV_{CC}$ through an external Schottky diode D_B when the top MOSFET is turned off. When the $EXTV_{CC}$ pin is grounded and $V_{RUN/SS}$ >1.5V, an internal 5V low dropout regulator supplies the $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ rises above 4.7V, the internal regulator is turned off, and an internal switch connects $EXTV_{CC}$ to $INTV_{CC}$. This allows a high efficiency source connected to $EXTV_{CC}$, such as an external 5V supply or a secondary output from the converter, to provide the $INTV_{CC}$ power. Voltages up to 7V can be applied to $EXTV_{CC}$ for additional gate drive. If the input voltage is low and $INTV_{CC}$ drops below 3.5V, undervoltage lockout circuitry prevents the power switches from turning on.

SMBus VID Voltage Programmer

The SMBus interface is used to program the divider (to set the output voltage of the DC/DC converter) and to shut down the current mode controller or allow it to soft-start.

OPERATION (Refer to Functional Diagram)

It uses two pins, SCL and SDA to communicate with a master device through the Read Word and Write Word protocols. The V_{IL} and V_{IH} logic threshold voltages of the SDA and SCL pins are 0.8V and 2.1V respectively, which comply with Rev 1.1 version of the Intel System Management Bus Specifications. Both pins require a resistor or active pull-up (see the LTC1694 data sheet) to V_{CC}. Data is clocked out of the SDA pin at the falling edge and latched in at the rising edge of the SCL clock signal. The slave address of the interface for both Read and Write protocols is fixed at E2H.

There are three types of Write Word protocols: Setup, On and Off and one Read Word protocol called Read-Back. The Setup Write Word protocol is used to set up two internal 5-bit registers (Register 0 and Register 1) with alternate resistor divider DAC settings. The On and Off Write Word protocols do not modify register contents but are used to shutdown the converter or to allow it to soft-start. The Read Word protocol is used to verify the contents of the registers as well as to check whether the converter is operating or in shutdown from a status bit ($\overline{DCON}$). Table 3 in the Applications Information section shows the data bits that identify each protocol as Setup, On, Off or Read-Back.

Controller Control

The VID programmer provides the VRON and CPUON pins for the purpose of shutting down or allowing the converter to soft-start. CPUON is an open-drain, N-channel output pin that is normally tied to the RUN/SS pin of the controller along with its soft-start capacitor. If the N-channel is turned off, the pin enters a high impedance state and the capacitor is allowed to charge up and soft-start the converter. When shutting down the converter, the N-channel FET at the CPUON pin will typically discharge a 0.1µF soft-start capacitor from 3V to 0.35V in 21µs with V_{CC} = 2.7V. On power-up, the power-on reset (POR) circuit in the SMBus VID programmer turns on the N-channel to shut down the converter. The CPUON pin can also be controlled to clear overcurrent faults in the switching regulator (see Soft-Start and Latchoff with the RUN/SS Pin section).

The CPUON pin is under the control of an internal On/Off state machine that is accessed using the SMBus On/Off Write Word protocols and the VRON pin. The VRON pin has a trip point of 1.3V with ±50mV of hysteresis. It is TTL compatible and has a 2.5µA pull-up to V_{CC}. Pulling VRON low will force CPUON low immediately, regardless of the On/Off state machine. Pulling VRON high or allowing it to float high hands control to the On/Off state machine. Table 1 summarizes the function of the control pins. The SMBON control bit is explained in the next section.

Table 1. DC/DC Converter Control Pins

VRON	SMBON	$\overline{DCON}$	PGTMR	CPUON
0	X	1	0	0
1	0	1	0	0
1	↑	↓	0 for 50µs (Note 1)	Z (Note 2)
↑	1	↓	0 for 50µs (Note 1)	Z (Note 2)

Note 1: Also triggered by SEL pin toggling.

Note 2: Z = High Impedance

The LTC1909-8 provides safeguards against incorrect divider codes and the unintentional turn-on or turn-off of the DC/DC converter. Incorrect codes due to bus conflicts during Setup protocols can cause damage to circuits powered by the DC/DC converter. The safeguards built into the LTC1909-8 include Read-Back, repeated On and Off protocols, ignoring On protocols if the registers have not been set up (since power-up), locking out registers while the DC/DC converters are operating and latching in VID codes only in Setup protocols.

After power-up, the microprocessor must set up the registers before the LTC1909-8 recognizes On protocols. This requirement ensures that the correct DC/DC converter output is programmed before the converters are turned on. After setup, Read-Back allows the contents of Registers 0 and 1 to be verified in case the VID codes were corrupted by noise or bus conflicts.

In order to turn on the DC/DC converter, two On protocols must be sent to slave address E2H without any other (E2H) protocols in between. Protocols to other slave addresses are still allowed and are ignored. Similarly, two Off protocols must be sent to slave address E2H to turn the converters off. The On and Off protocols are monitored by an internal state machine. The output of the state machine, SMBON, is high after two On commands and low after two Off commands. Repeated On and Off protocols reduce the chances of bus conflicts and noise turning the converter

OPERATION (Refer to Functional Diagram)

on or off accidentally. In both On and Off protocols, the LTC1909-8 does not latch in the Data Low and Data High bytes. This protects the settings that have already been loaded into the registers and verified by read-back. Once the converter is turned on (both SMBON and VRON are high) the contents of Registers 0 and 1 are protected and can only be altered with Setup protocols if VRON is pulled low or two Off protocols are sent to the LTC1909-8 (to force SMBON low). During Read-Back, the microprocessor can check the On or Off state of the controller by testing the DCON status bit that follows each 5-bit code. This bit is low only when both SMBON and VRON are high.

Resistor Divider

The resistor divider settings comply with the Intel Desktop VRM8.4 VID Specifications. The divider consists of a fixed 20k (typical) resistor, R_{FB1}, connected between the V_{OSENSE} and $\overline{FB}$ pins and a variable resistor, R_{FB2}, from FB to GND. The FB pin is connected to the V_{FB} pin of the step-down controller to set the output voltage of the converter. Each resistor has a tolerance of ±30% but the divider ratio is accurate to ±0.35%. The error budget for the DC/DC converter output voltage must include the ±0.35% ratio tolerance and the ±1% tolerance in the 0.8V reference. The output of the DC/DC converter is given by:

$$V_{OUT} = V_{REF} \bullet (R_{FB2} + R_{FB1})/R_{FB2}$$

where V_{REF} = 0.8V is the internal reference voltage of the converter. Table 2 shows the 32 possible converter output voltages. The microprocessor controls the SEL pin to select the contents of one of the registers as the active divider setting. The SEL pin has a trip point of 1.3V with ±50mV of hysteresis and is TTL compatible. It controls an internal 10:5 digital multiplexer and selects the contents of register 0 when pulled low and register 1 when pulled high. When SEL is toggled, and the new converter output is lower or greater by 7.5%, the overvoltage and undervoltage comparators of the controller may trip causing the PGOOD pin of the controller to go low. This condition will recover automatically as the converter charges up the output or allows the output to drop to the new voltage setting.

Power Good Timer

The PGTMR or "Power Good Timer" pin is also an open-drain, N-channel output. It pulls low if the DC/DC converter is in shutdown or on power-up. When the converter is turned on, an internal timer keeps PGTMR low for 50µs (typical) which allows time for the converters to enter regulation. Toggling the SEL pin while the converter is turned on also causes the PGTMR pin to pull low for 50µs.

The PGTMR pin may be used to force continuous operation in the DC/DC converter. If the SEL pin is toggled to select a lower output voltage, if may take an unacceptably

Table 2. DC/DC Converter Output Voltage

VID4	VID3	VID2	VID1	VID0	OUTPUT VOLTAGE
0	0	0	0	0	2.05V
0	0	0	0	1	2.00V
0	0	0	1	0	1.95V
0	0	0	1	1	1.90V
0	0	1	0	0	1.85V
0	0	1	0	1	1.80V
0	0	1	1	0	1.75V
0	0	1	1	1	1.70V
0	1	0	0	0	1.65V
0	1	0	0	1	1.60V
0	1	0	1	0	1.55V
0	1	0	1	1	1.50V
0	1	1	0	0	1.45V
0	1	1	0	1	1.40V
0	1	1	1	0	1.35V
0	1	1	1	1	1.30V
1	0	0	0	0	3.50V
1	0	0	0	1	3.40V
1	0	0	1	0	3.30V
1	0	0	1	1	3.20V
1	0	1	0	0	3.10V
1	0	1	0	1	3.00V
1	0	1	1	0	2.90V
1	0	1	1	1	2.80V
1	1	0	0	0	2.70V
1	1	0	0	1	2.60V
1	1	0	1	0	2.50V
1	1	0	1	1	2.40V
1	1	1	0	0	2.30V
1	1	1	0	1	2.20V
1	1	1	1	0	2.10V
1	1	1	1	1	2.00V

OPERATION (Refer to Functional Diagram)

long time for the output of the DC/DC converter to decrease to the new voltage under light load conditions. To reduce this time needed, the PGTMR pin can be connected to the FCB (force continuous bar) pin of the converter. When the SEL pin is toggled to select a new code, the FCB pin is forced low for 50µs. This forces the DC/DC converter out of Burst Mode™ operation and into continuous mode. The PGTMR pin may be tied to the same pull-up resistor as the PGOOD pin.

SMBus Controller Supply

If the $EXTV_{CC}$ pin is tied to ground, the V_{CC} pin of the SMBus controller should be tied to an external 5V supply. It should not be tied to the $INTV_{CC}$ pin because the internal 5V regulator at the $INTV_{CC}$ pin is shut down while $V_{RUN/SS}$ is below 1.5V and the SMBus controller will not be powered up. If the $EXTV_{CC}$ pin is tied to an external 5V supply, the V_{CC} pin can be tied to the same supply or to the $INTV_{CC}$ pin since the $INTV_{CC}$ pin is connected to the $EXTV_{CC}$ pin by an internal switch when V_{EXTVCC} >4.7V. The $EXTV_{CC}$ and V_{CC} voltages should be kept below the absolute maximum rating of 7V.

Power-Up Reset

On power-up, the internal POR circuit generates a low reset pulse, which stays low until V_{CC} rises above approximately 2.2V. The reset pulse forces the SMBus interface into an idle state in which it listens for a start bit. At the same time the outputs of both Register 0 and Register 1 are set to 11111B. The $\overline{DCON}$ bit is pulled high so that the CPUON pin is pulled low to shut down the DC/DC converter. PGTMR is also pulled low as the converter is shut down and therefore not in regulation.

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APPLICATIONS INFORMATION

The basic LTC1909-8 application circuit is shown in Figure 1. External component selection is primarily determined by the maximum load current and begins with the selection of the sense resistance and power MOSFET switches. The LTC1909-8 uses either an external sense resistor or the on-resistance of the synchronous power MOSFET for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification.

Maximum Sense Voltage and V_{RNG} Pin

Inductor current is determined by measuring the voltage across a sense resistance that appears between the PGND and $SENSE^+$ pins. The maximum sense voltage is set by the voltage applied to the V_{RNG} pin and is equal to approximately (0.133) • V_{RNG}. The current mode control loop will not allow the inductor current valleys to exceed (0.133) • V_{RNG}/R_{SENSE}. In practice, one should allow some margin for variations in the LTC1909-8 and external component values and a good guide for selecting the sense resistance is:

$$R_{SENSE} = \frac{V_{RNG}}{10 \bullet I_{OUT(MAX)}}$$

An external resistive divider from $INTV_{CC}$ can be used to set the voltage of the V_{RNG} pin between 0.5V and 2V resulting in nominal sense voltages of 50mV to 200mV. Additionally, the V_{RNG} pin can be tied to SGND or $INTV_{CC}$ in which case the nominal sense voltage defaults to 70mV or 140mV, respectively. The maximum allowed sense voltage is about 1.33 times this nominal value.

Connecting the $SENSE^+$ Pin

The LTC1909-8 can be used with or without a sense resistor. When using a sense resistor, it is placed between the source of the bottom MOSFET M2 and ground. Connect the $SENSE^+$ pin to the source of the bottom MOSFET so that the resistor appears between the $SENSE^+$ and PGND pins. Using a sense resistor provides a well defined current limit, but adds cost and reduces efficiency. Alternatively, one can eliminate the sense resistor and use the bottom MOSFET as the current sense element by simply connecting the $SENSE^+$ pin to the switch node SW at the drain of the bottom MOSFET. This improves efficiency, but

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one must carefully choose the MOSFET on-resistance as discussed below.

Power MOSFET Selection

The LTC1909-8 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, threshold voltage $V_{(GS)TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

The gate drive voltage is set by the 5V $INTV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LTC1909-8 applications. If the input voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be considered.

When the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho_T}$$

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C as shown in Figure 2. For a maximum temperature of 100°C, using a value ρ_T = 1.3 is reasonable.

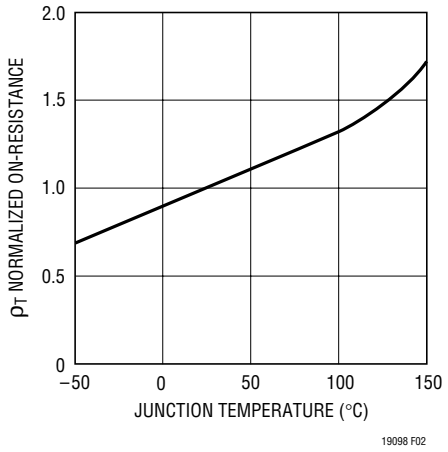

Figure 2. $R_{DS(ON)}$ vs. Temperature

The power dissipated by the top and bottom MOSFETs strongly depends upon their respective duty cycles and the load current. When the LTC1909-8 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$D_{TOP} = \frac{V_{OUT}}{V_{IN}}$$

$$D_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{TOP} = D_{TOP}\, I_{OUT(MAX)}^2\, \rho_{T(TOP)}\, R_{DS(ON)(MAX)} + k\, V_{IN}^2\, I_{OUT(MAX)}\, C_{RSS}\, f$$

$$P_{BOT} = D_{BOT}\, I_{OUT(MAX)}^2\, \rho_{T(BOT)}\, R_{DS(ON)(MAX)}$$

Both MOSFETs have I^2R losses and the top MOSFET includes an additional term for transition losses, which are largest at high input voltages. The constant $K = 1.7A^{-1}$ can be used to estimate the amount of transition loss. The bottom MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage.

Operating Frequency

The choice of operating frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance in order to maintain low output ripple voltage.

The operating frequency of LTC1909-8 applications is determined implicitly by the one-shot timer that controls the on-time t_{ON} of the top MOSFET switch. The on-time is set by the current into the I_{ON} pin according to:

$$t_{ON} = \frac{V_{VON}}{I_{ION}}(10pF)$$

Tying a resistor R_{ON} from V_{IN} to the I_{ON} pin yields an on-time inversely proportional to V_{IN}. For a step-down converter, this results in approximately constant frequency operation as the input supply varies:

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$$f = \frac{V_{OUT}}{V_{VON}\, R_{ON}(10pF)} \quad [Hz]$$

To hold frequency constant during output voltage changes, tie the V_{ON} pin to V_{OUT}. The V_{ON} pin has internal clamps that limit its input to the one-shot timer. If the pin is tied below 0.7V, the input to the one-shot is clamped at 0.7V. Similarly, if the pin is tied above 2.4V, the input is clamped at 2.4V.

Because the voltage at the I_{ON} pin is about 0.7V, the current into this pin is not exactly inversely proportional to V_{IN}, especially in applications with lower input voltages. To correct for this error, an additional resistor R_{ON2} connected from the I_{ON} pin to the 5V $INTV_{CC}$ supply will further stabilize the frequency.

$$R_{ON2} = \frac{5V}{0.7V} R_{ON}$$

Changes in the load current magnitude will also cause frequency shift. Parasitic resistance in the MOSFET switches and inductor reduce the effective voltage across the inductance, resulting in increased duty cycle as the load current increases. By lengthening the on-time slightly as current increases, constant frequency operation can be maintained. This is accomplished with a resistive divider from the I_{TH} pin to the V_{ON} pin and V_{OUT}. The values required will depend on the parasitic resistances in the specific application. A good starting point is to feed about 25% of the voltage change at the I_{TH} pin to the V_{ON} pin as shown in Figure 3a. Place capacitance on the V_{ON} pin to filter out the I_{TH} variations at the switching frequency. The resistor load on I_{TH} reduces the DC gain of the error amp and degrades load regulation, which can be avoided by using the PNP emitter follower of Figure 3b.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{fL}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f\,\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

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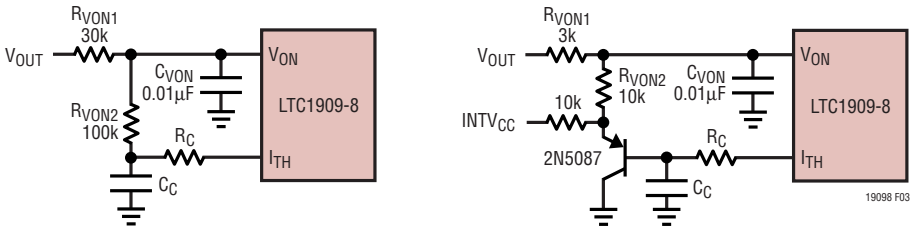

Figure 3. Correcting Frequency Shift with Load Current Changes

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Schottky Diode D1 Selection

The Schottky diode D1 shown in Figure 1 conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half to one fifth of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently. The diode can be omitted if the efficiency loss is tolerable.

C_{IN} and C_{OUT} Selection

The input capacitance C_{IN} is required to filter the square wave current at the drain of the top MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications providing that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller. To dampen input voltage transients, add a small 5µF to 50µF aluminum electrolytic capacitor with an ESR in the range of 0.5Ω to 2Ω. High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of their lead inductance.

Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from $INTV_{CC}$ when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately $V_{IN} + INTV_{CC}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications a 0.1µF to 0.47µF X5R or X7R dielectric capacitor is adequate.

Discontinuous Mode Operation and FCB Pin

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 0.8V threshold enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. The load current at which current reverses and discontinuous operation begins depends on the amplitude of the inductor ripple current and will vary with changes in V_{IN}. Tying the FCB pin below the

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0.8V threshold forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation.

In addition to providing a logic input to force continuous operation, the FCB pin provides a means to maintain a flyback winding output when the primary is operating in discontinuous mode. The secondary output V_{SEC} is normally set as shown in Figure 4 by the turns ratio N of the transformer. However, if the controller goes into discontinuous mode and halts switching due to a light primary load current, then V_{SEC} will droop. An external resistor divider from V_{SEC} to the FCB pin sets a minimum voltage $V_{SEC(MIN)}$ below which continuous operation is forced until V_{SEC} has risen above its minimum.

$$V_{SEC(MIN)} = 0.8V\left(1+\frac{R4}{R3}\right)$$

Fault Conditions: Current Limit and Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC1909-8, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SNS(MAX)}}{R_{DS(ON)}\,\rho T} + \frac{1}{2}\Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of I_{LIMIT} which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same amount below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

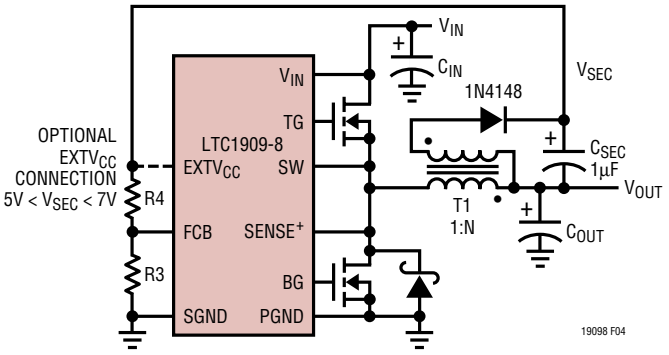

Figure 4. Secondary Output Loop and $EXTV_{CC}$ Connection

To further limit current in the event of a short circuit to ground, the LTC1909-8 includes foldback current limiting. If the output falls by more than 25%, then the maximum sense voltage is progressively lowered to about one sixth of its full value.

Minimum Off-time and Dropout Operation

The minimum off-time $t_{OFF(MIN)}$ is the smallest amount of time that the LTC1909-8 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 300ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT}\frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces the 5V supply that powers the drivers and internal circuitry within the LTC1909-8. The $INTV_{CC}$ pin can supply up to 50mA RMS and must be bypassed to ground with a minimum of 4.7µF tantalum or other low ESR capacitor. Good bypassing is necessary to supply the high transient

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currents required by the MOSFET gate drivers. Applications using large MOSFETs with a high input voltage and high frequency of operation may cause the LTC1909-8 to exceed its maximum junction temperature rating or RMS current rating. Most of the supply current drives the MOSFET gates unless an external $EXTV_{CC}$ source is used. In continuous mode operation, this current is $I_{GATECHG} = f(Q_{g(TOP)} + Q_{g(BOT)})$. The junction temperature can be estimated from the equations given in Note 2 of the Electrical Characteristics. For example, the LTC1909-8 is limited to less than 14mA from a 30V supply:

$$T_J = 70°C + (14mA)(30V)(130°C/W) = 125°C$$

For larger currents, consider using an external supply with the $EXTV_{CC}$ pin.

$EXTV_{CC}$ Connection

The $EXTV_{CC}$ pin can be used to provide MOSFET gate drive and control power from the output or another external source during normal operation. Whenever the $EXTV_{CC}$ pin is above 4.7V the internal 5V regulator is shut off and an internal 50mA P-channel switch connects the $EXTV_{CC}$ pin to $INTV_{CC}$. $INTV_{CC}$ power is supplied from $EXTV_{CC}$ until this pin drops below 4.5V. Do not apply more than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$. The following list summarizes the possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. $INTV_{CC}$ is always powered from the internal 5V regulator.

2. $EXTV_{CC}$ connected to an external supply. A high efficiency supply compatible with the MOSFET gate drive requirements (typically 5V) can improve overall efficiency.

3. $EXTV_{CC}$ connected to an output derived boost network. The low voltage output can be boosted using a charge pump or flyback winding to greater than 4.7V. The system will start-up using the internal linear regulator until the boosted output supply is available.

External Gate Drive Buffers

The LTC1909-8 drivers are adequate for driving up to about 30nC into MOSFET switches with RMS currents of 50mA. Applications with larger MOSFET switches or operating at frequencies requiring greater RMS currents will benefit from using external gate drive buffers such as the LTC1693. Alternately, the external buffer circuit shown in Figure 5 can be used. Note that the bipolar devices reduce the signal swing at the MOSFET gate and benefit from an increased $EXTV_{CC}$ voltage of about 6V.

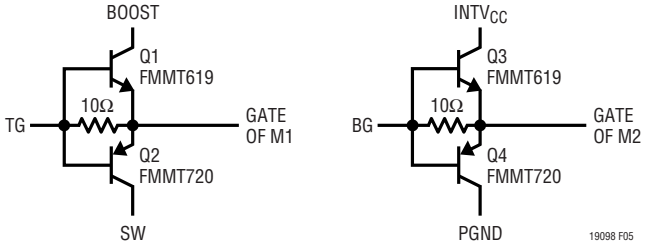

Figure 5. Optional External Gate Driver

Soft-Start and Latchoff with the RUN/SS Pin

The RUN/SS pin provides a means to shut down the LTC1909-8 as well as a timer for soft-start and overcurrent latchoff. Pulling the RUN/SS pin below 0.8V puts the LTC1909-8 into a low quiescent current shutdown ($I_Q < 30\mu A$). Releasing the pin allows an internal 1.2µA current source to charge up the external timing capacitor C_{SS}. If RUN/SS has been pulled all the way to ground, there is a delay before starting of about:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = \left(1.3s/\mu F\right) C_{SS}$$

When the voltage on RUN/SS reaches 1.5V, the LTC1909-8 begins operating with a clamp on I_{TH} of approximately 0.9V. As the RUN/SS voltage rises to 3V, the clamp on I_{TH} is raised until its full 2.4V range is available. This takes an additional 1.3s/µF, during which the load current is folded back until the output reaches 75% of its final value. The pin can be driven from logic (Figures 6a or 6b) or from the CPUON pin (Figures 6c and 6d). Diode D1 reduces the start delay while allowing C_{SS} to charge up slowly for the soft-start function.

After the controller has been started and given adequate time to charge up the output capacitor, C_{SS} is used as a short-circuit timer. After the RUN/SS pin charges above 4V, if the output voltage falls below 75% of its regulated value, then a short-circuit fault is assumed. A 1.8µA current then begins discharging C_{SS}. If the fault condition persists until the RUN/SS pin drops to 3.5V, then the

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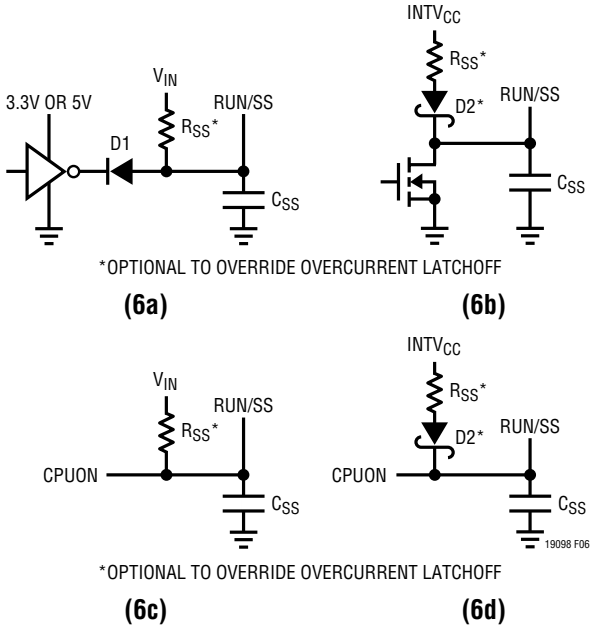

Figure 6. RUN/SS Pin Interfacing with Latchoff Defeated

controller turns off both power MOSFETs, shutting down the converter permanently. The RUN/SS pin must be actively pulled down to ground in order to restart operation. If the RUN/SS pin is tied to the CPUON pin, this is achieved by pulling the VRON pin low or by sending two Off protocols to the SMBus VID programmer to force the CPUON pin low.

The overcurrent protection timer requires that the soft-start timing capacitor C_{SS} be made large enough to guarantee that the output is in regulation by the time C_{SS} has reached the 4V threshold. In general, this will depend upon the size of the output capacitance, output voltage and load current characteristic. A minimum soft-start capacitor can be estimated from:

$$C_{SS} > C_{OUT}\ V_{OUT}\ R_{SENSE}\ (10^{-4}\ [F/V\ s])$$

Generally 0.1µF is more than sufficient.

Overcurrent latchoff operation is not always needed or desired. Load current is already limited during a short-circuit by the current foldback circuitry and latchoff operation can prove annoying during troubleshooting. The feature can be overridden by adding a pull-up current greater than 5µA to the RUN/SS pin. The additional current prevents the discharge of C_{SS} during a fault and also shortens the soft-start period. Using a resistor to V_{IN} as shown in Figure 6a or 6c is simple, but slightly increases shutdown current. Connecting a resistor to $INTV_{CC}$ as shown in Figure 6b and 6d eliminates the additional shutdown current, but requires a diode to isolate C_{SS}. Any pull-up network must be able to maintain RUN/SS above the 4.2V maximum latchoff threshold and overcome the 4µA maximum discharge current.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC1909-8 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)} = 0.01\Omega$ and $R_L = 0.005\Omega$, the loss will range from 15mW to 1.5W as the output current varies from 1A to 10A.

2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

$$\text{Transition Loss} \cong (1.7A^{-1})\ V_{IN}^2\ I_{OUT}\ C_{RSS}\ f$$

3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents. This loss can be reduced by supplying $INTV_{CC}$ current through the $EXTV_{CC}$ pin from a high efficiency source, such as an output derived boost network or alternate supply if available.

4. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and

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sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including C_{OUT} ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss. When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin external components shown in Figure 7 will provide adequate compensation for most applications. For a detailed explanation of switching control loop theory see Application Note 76.

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 7V to 24V (15V nominal), V_{OUT} = 1.5V ±100mV, $I_{OUT(MAX)}$ = 15A, f = 300kHz. First, calculate the timing resistor with $V_{ON} = V_{OUT}$:

$$R_{ON} = \frac{1}{(300kHz)(10pF)} = 330k$$

and choose the inductor for about 40% ripple current at the maximum V_{IN}:

$$L = \frac{1.5V}{(300kHz)(0.4)(15A)}\left(1-\frac{1.5V}{24V}\right) = 0.8\mu H$$

Selecting a standard value of 1µH results in a maximum ripple current of:

$$\Delta I_L = \frac{1.5V}{(300kHz)(1\mu H)}\left(1-\frac{1.5V}{24V}\right) = 4.7A$$

Next, choose the synchronous MOSFET switch. Because of the narrow duty cycle and large current, a single SO-8 MOSFET will have difficulty dissipating the power lost in the switch. Choosing two IRF7811A ($R_{DS(ON)}$ = 0.013Ω, C_{RSS} = 60pF, θ_{JA} = 40°C/W) yields a nominal sense voltage of:

$$V_{SNS(NOM)} = (15A)(0.5)(1.3)(0.012\Omega) = 117mV$$

Tying V_{RNG} to $INTV_{CC}$ will set the current sense voltage range for a nominal value of 140mV with current limit occurring at 186mV. To check if the current limit is acceptable, assume a junction temperature of about 100°C above a 50°C ambient with $\rho_{150°C}$ = 1.6:

$$I_{LIMIT} \geq \frac{186mV}{(0.5)(1.6)(0.012\Omega)} + \frac{1}{2}(4.7A) = 18A$$

and double check the assumed T_J in the MOSFET:

$$P_{BOT} = \frac{24V-1.5V}{24V}\left(\frac{21.7A}{2}\right)^2(1.6)(0.012\Omega) = 2.12W$$

T_J = 50°C + (2.12W)(50°C/W) = 156°C

Because the top MOSFET is on for such a short time, a single IRF7811A will be sufficient. Checking its power dissipation at current limit with $\rho_{90°C}$ = 1.3:

$$P_{BOT} = \frac{1.5V}{24V}(21.7A)^2(1.3)(0.012\Omega) + (1.7)(24V)^2(21.7A)(60pF)(300kHz)$$
$$= 0.46W + 0.38W = 0.84W$$

T_J = 50°C + (0.84W)(50°C/W) = 92°C

The junction temperatures will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking will be necessary in this circuit.

C_{IN} is chosen for an RMS current rating of about 6A at temperature. The output capacitors are chosen for a low ESR of 0.005Ω to minimize output voltage changes due to

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inductor ripple current and load steps. The ripple voltage will be only:

$$\Delta V_{OUT(RIPPLE)} = \Delta I_{L(MAX)} (ESR)$$
$$= (4.7A)\ (0.005\Omega) = 24mV$$

However, a 0A to 15A load step will cause an output change of up to:

$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD} (ESR) = (15A)\ (0.005\Omega) = 75mV$$

The complete circuit is shown in Figure 7.

Active Voltage Positioning

Active voltage positioning (also termed load "deregulation" or droop) describes a technique where the output voltage varies with load in a controlled manner. It is useful in applications where rapid load steps are the main cause of error in the output voltage. By positioning the output voltage above the regulation point at zero load, and below the regulation point at full load, one can use more of the error budget for the load step. This allows one to reduce the number of output capacitors by relaxing the ESR requirement.

In the design example, Figure 7, five 0.025Ω capacitors are required in parallel to keep the output voltage within tolerance. Using active voltage positioning, the same specification can be met with only three capacitors. In this case, the load step will cause an output voltage change of:

$$\Delta V_{OUT(STEP)} = (15A)\left(\frac{1}{3}\right)(0.025\Omega) = 125mV$$

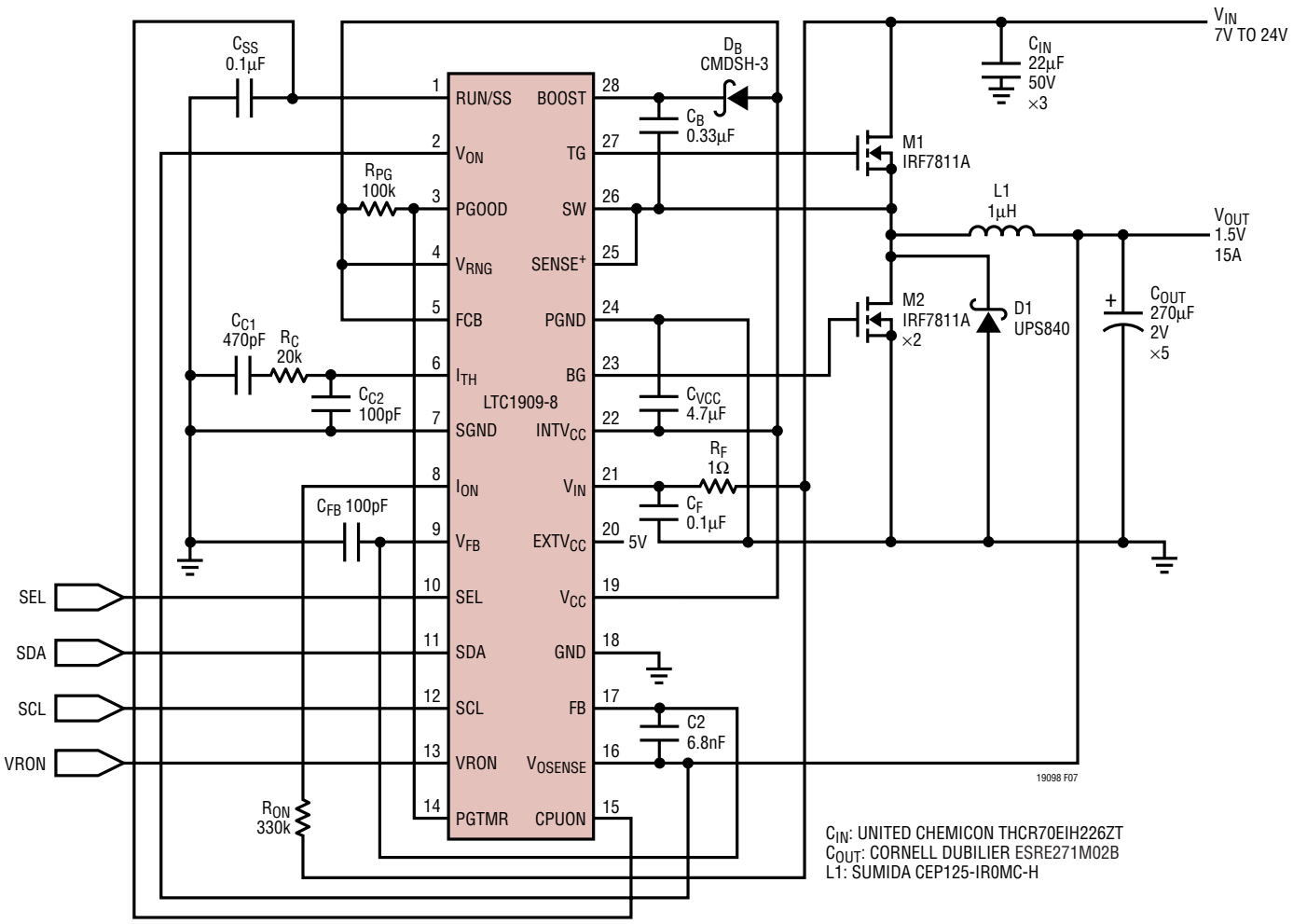

Figure 7. CPU Core Voltage Regulator 1.5V, 15A at 300kHz

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By positioning the output voltage 60mV above the regulation point at no load, it will only drop 65mV below the regulation point after the load step, well within the ±100mV tolerance. Implementing active voltage positioning requires setting a precise gain between the sensed current and the output voltage. Because of the variability of MOSFET on-resistance, it is prudent to use a sense resistor with active voltage positioning. In order to minimize power lost in this resistor, a low value is chosen of 0.003Ω. The nominal sense voltage will now be:

$$V_{SNS(NOM)} = (0.003\Omega)(15A) = 45mV$$

To maintain a reasonable current limit, the voltage on the V_{RNG} pin is reduced to its minimum value of 0.5V, corresponding to a 50mV nominal sense voltage.

Next, the gain of the LTC1909-8 error amplifier must be determined. The change in I_{TH} voltage for a corresponding change in the output current is:

$$\Delta I_{TH} = \left(\frac{12V}{V_{RNG}}\right) R_{SENSE}\, \Delta I_{OUT}$$
$$= (24)(0.003\Omega)(15A) = 1.08V$$

The corresponding change in the output voltage is determined by the gain of the error amplifier and feedback divider. The LTC1909-8 error amplifier has a transconductance g_m that is constant over both temperature and a wide ±40mV input range. Thus, by connecting a load resistance R_{VP} to the I_{TH} pin, the error amplifier gain can be precisely set for accurate active voltage positioning.

$$\Delta I_{TH} = g_m R_{VP} \left(\frac{0.8V}{V_{OUT}}\right) \Delta V_{OUT}$$

Solving for this resistance value:

$$R_{VP} = \frac{V_{OUT}\, \Delta I_{TH}}{(0.8V)\, g_m\, \Delta V_{OUT}}$$
$$= \frac{(1.5V)(1.08V)}{(0.8V)(1.7mS)(125mV)} = 9.53k$$

The gain setting resistance R_{VP} is implemented with two resistors, R_{VP1} connected from I_{TH} to ground and R_{VP2} connected from I_{TH} to $INTV_{CC}$. The parallel combination of these resistors must equal R_{VP} and their ratio determines nominal value of the I_{TH} pin voltage when the error amplifier input is zero. To center the load line around the regulation point, the I_{TH} pin voltage must be set to correspond to half the output current. The relation between I_{TH} voltage and the output current is:

$$I_{TH(NOM)} = \left(\frac{12V}{V_{RNG}}\right) R_{SENSE}\left(I_{OUT} - \frac{1}{2}\Delta I_L\right) + 0.8V$$
$$= \left(\frac{12V}{0.5V}\right)(0.003\Omega)\left(7.5A - \frac{1}{2}4.7A\right) + 0.8V$$
$$= 1.17V$$

Solving for the required values of the resistors:

$$R_{VP1} = \frac{5V}{5V - I_{TH(NOM)}} R_{VP} = \frac{5V}{5V - 1.17V} 9.53k$$
$$= 12.44k$$
$$R_{VP2} = \frac{5V}{I_{TH(NOM)}} R_{VP} = \frac{5V}{1.17V} 9.53k = 40.73k$$

The modified circuit is shown in Figure 8. Figures 9 and 10 show the transient response without and with active voltage positioning. Both circuits easily stay within ±100mV of the 1.5V output. However, the circuit with active voltage positioning accomplishes this with only three output capacitors rather than five. Refer to Design Solutions 10 for additional information about active voltage positioning.

SMBus Protocols

The Write Word and Read Word protocols (Figure 11) share three common features. First, the 7-bit slave address for both protocols is internally hardwired to 1110 001B = E2H. A single R/$\overline{W}$ bit follows the slave address. This bit is low for data transfer from the microprocessor to the LTC1909-8 and high for transfers in the opposite direction.

Second, the LTC1909-8 decodes only the three most significant bits of the 8-bit command code. Table 3 shows the four valid combinations. All other combinations are ignored.

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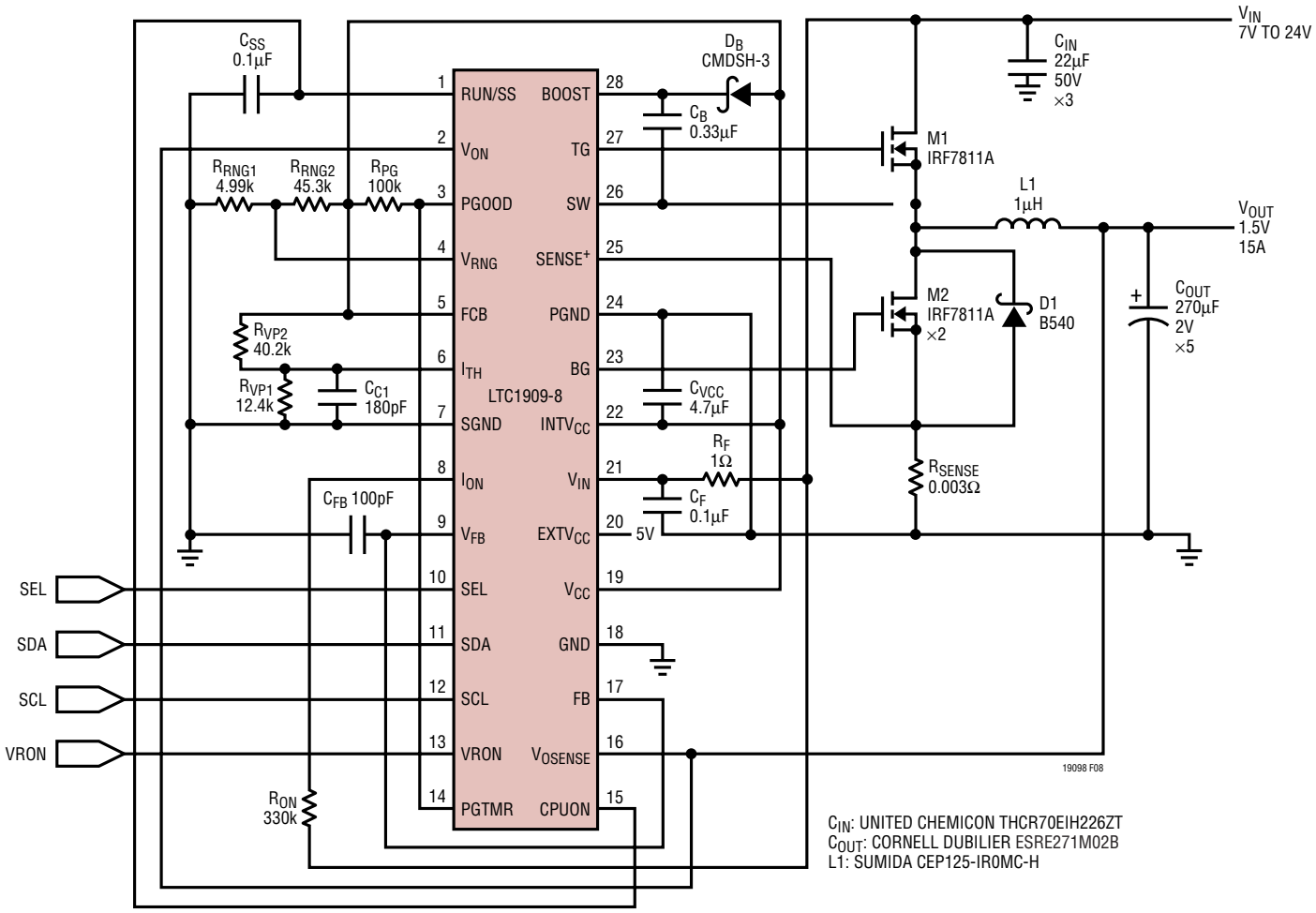

Figure 8. CPU Core Voltage Regulator with Active Voltage Positioning 1.5V/15A at 300kHz

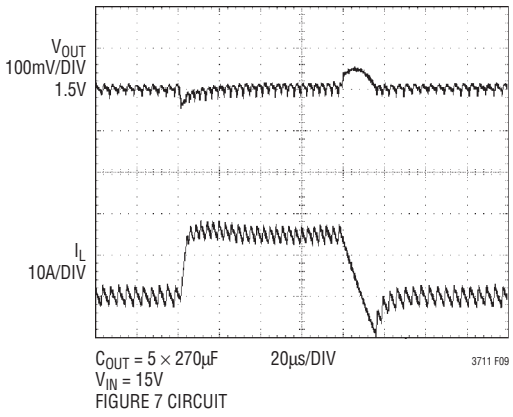

Figure 9. Normal Transient Response

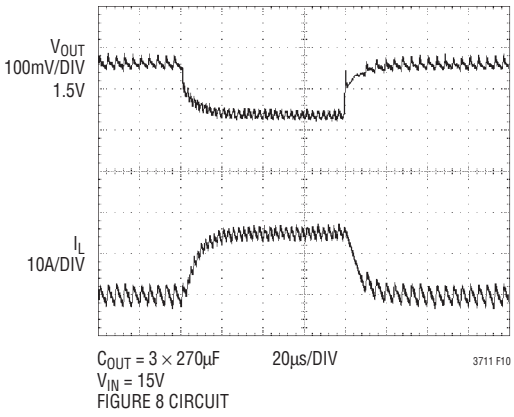

Figure 10. Transient Response with Active Voltage Positioning

APPLICATIONS INFORMATION

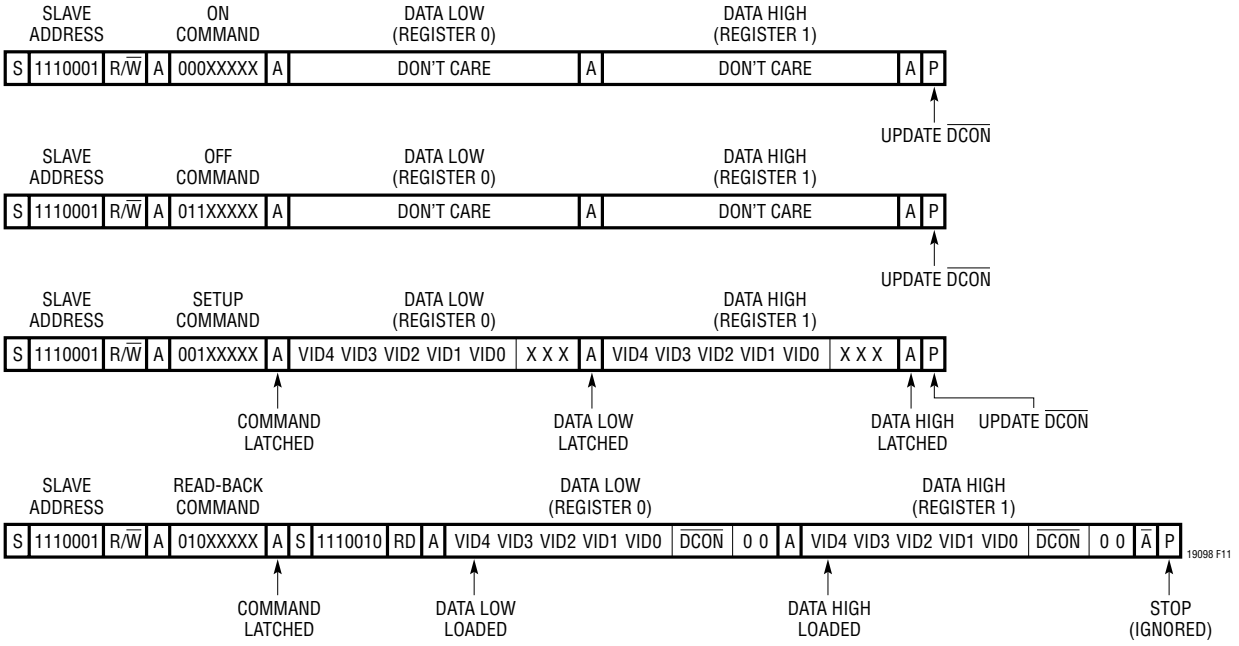

Figure 11. Write Word and Read Word Protocols

Third, the Data Low and Data High bytes correspond to Registers 0 and 1 respectively. In Write Word protocol with C7 = C6 = 0, C5 = 1, the five most significant bits (VID0-VID4) of these bytes specify a resistor divider setting.

Table 3. LTC1909-8 Command Bits

C7	C6	C5	COMMAND	PROTOCOL
0	0	0	On	Write Word
0	1	1	Off	Write Word
0	0	1	Setup	Write Word
0	1	0	Read-Back	Read Word

Write Word Protocol

Each Write Word protocol (Figure 11) begins with a start bit (S) and ends with a stop bit (P). As shown in the Timing Diagram the start and stop bits are defined as high-to-low and low-to-high SDA transitions respectively, while SCL is high. In between the start and stop bits, the microprocessor transmits four bytes to the LTC1909-8. These are the address byte, an 8-bit command code and two data bytes. The LTC1909-8 samples each bit at the rising edges of the SCL clock.

When the microprocessor issues a start bit, all the slave devices on the bus, including the LTC1909-8 clock in the address byte, which consists of a 7-bit slave address and the R/$\overline{W}$ bit (set to 0). If the slave address from the microprocessor does not match the internal hardwired address, the LTC1909-8 returns to an idle state and waits for the next start bit. If the slave address matches, the LTC1909-8 acknowledges by pulling the SDA line low for one clock cycle after the address byte. After detecting the acknowledgment bit (A), the microprocessor transmits the second byte or command code.

The command code identifies the type of Write Word protocol as Setup, On or Off (Table 3). The Setup protocol is used to load two resistor divider settings into Register 0 and 1. The On and Off protocols turn the converters on or off in conjunction with the VRON pin. Once all 8 bits of the command code are clocked in, the LTC1909-8 issues a second acknowledgment bit to the microprocessor. After detecting the acknowledgment bit, the microprocessor transmits two data bytes.

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Each data byte is acknowledged in turn for all three Write Word protocols but is only latched into Register 0 or 1 in Setup protocol. This prevents previously loaded settings from accidentally being changed. The first or Data Low byte is loaded into Register 0. The second or Data High byte is loaded into Register 1. After issuing the final acknowledgment bit, the SMBus interface returns to an idle state and waits for the next start bit.

Read Word Protocol

The Read Word protocol starts off like Write Word protocol but after the command code acknowledgment, the microprocessor issues a second start bit (called a repeated start). This is followed by the slave address but with the R/$\overline{W}$ bit set high to indicate that data direction is now from the LTC1909-8 to the microprocessor. The LTC1909-8 then acknowledges the slave address and clocks the contents of Register 0 (Data Low byte) to the microprocessor. The Data Low byte is acknowledged by the microprocessor. On detecting the acknowledgment bit, the LTC1909-8 clocks out the contents of Register 1 (Data High byte). As defined in the SMBus specifications, the microprocessor does not acknowledge the last data byte. The LTC1909-8 enters an idle state to wait for the next start bit after clocking out the Data High byte. The five most significant bits (VID0-VID4) of the Data Low and High bytes are the resistor divider settings previously loaded using the Setup protocol. The next bit below the VID0-VID4 bits is the status of the $\overline{DCON}$ signal. If this bit is low (high), the DC/DC converters are switched on (off). The two unused, least significant bits of the Data Low and Data High bytes are clocked out as zeros to eliminate the need to mask out these bits in software.

Operating Sequence

A typical control sequence for the LTC1909-8 is as follows:

- On power up, the $\overline{DCON}$ bit is preset to a high state by the power-on reset (POR) circuit. The CPUON pin is pulled low to shut down the DC/DC converter. PGTMR and PGOOD pull low to indicate that the converters are not in regulation.
- Pull VRON low as a precaution. Take SEL high or low to select the divider setting; e.g., one that suits the existing power source (battery or wall-pack) or intended CPU speed.
- Use the Setup protocol to load the appropriate divider settings in Registers 0 and 1 and enable the On/Off state machine.
- Use the Read-Back protocol to verify the contents of Registers 0 and 1.
- Repeat the setup and read-back if the codes are incorrect (due to bus conflicts).
- Send two On protocols in succession to clear the $\overline{DCON}$ bit.
- Use the Read-Back protocol to verify that the $\overline{DCON}$ is low. A high state will indicate that an On command code was corrupted by bus conflicts.
- Pull VRON high. Since $\overline{DCON}$ = 0, the CPUON pin enters a high impedance state, allowing the DC/DC converter to soft-start. PGTMR stays low for 50µs. PGOOD stays low until the regulator output rises above the –7.5% regulation limit.
- To shut down the supply, send two Off protocols to set the $\overline{DCON}$ bit high or pull VRON low if immediate shutdown is required.

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PC Board Layout Checklist

When laying out a PC board follow one of the two suggested approaches. The simple PC board layout requires a dedicated ground plane layer. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

- The ground layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, C_{OUT}, MOSFETs, D1 and inductor all in one compact area. It may help to have some components on the bottom side of the board.
- Place LTC1909-8 chip with Pins 20 to 28 facing the power components. Keep the components connected to Pins 16 to 18 close to LTC1909-8 (noise sensitive components).
- Use an immediate via to connect the components to ground plane including SGND, GND and PGND of LTC1909-8. Use several bigger vias for power components.
- Use compact plane for switch node (SW) to improve cooling of the MOSFETs and to keep EMI down.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Connect the V_{OSENSE}, FB and GND pins of the resistor divider directly to the output of the DC/DC converter, the V_{FB} pin and the SGND pin of the controller.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND or to any other DC rail in your system).

When laying out a printed circuit board, without a ground plane, use the following checklist to ensure proper operation of the controller. These items are also illustrated in Figure 12.

- Segregate the signal and power grounds. All small-signal components should return to the SGND pin at one point which is then tied to the PGND pin close to the source of M2. Tie the GND pin directly to SGND.
- Place M2 as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Connect the input capacitor(s) C_{IN} close to the power MOSFETs. This capacitor carries the MOSFET AC current.
- Keep the high dV/dT SW, BOOST and TG nodes away from sensitive small-signal nodes.
- Connect the $INTV_{CC}$ decoupling capacitor C_{VCC} closely to the $INTV_{CC}$ and PGND pins.
- Connect the top driver boost capacitor C_B closely to the BOOST and SW pins.
- Connect the V_{IN} pin decoupling capacitor C_F closely to the V_{IN} and PGND pins.

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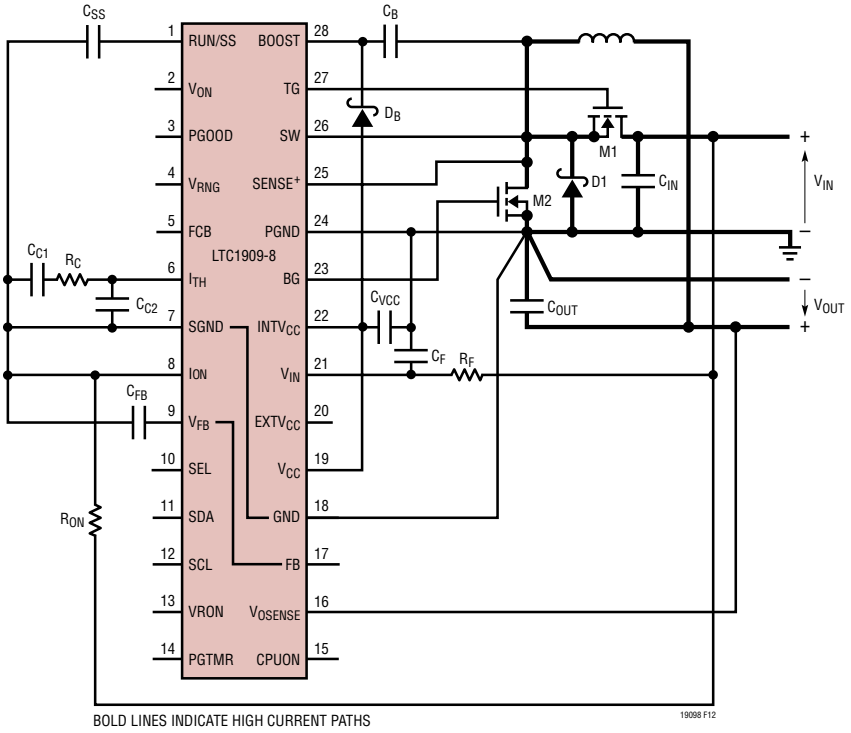
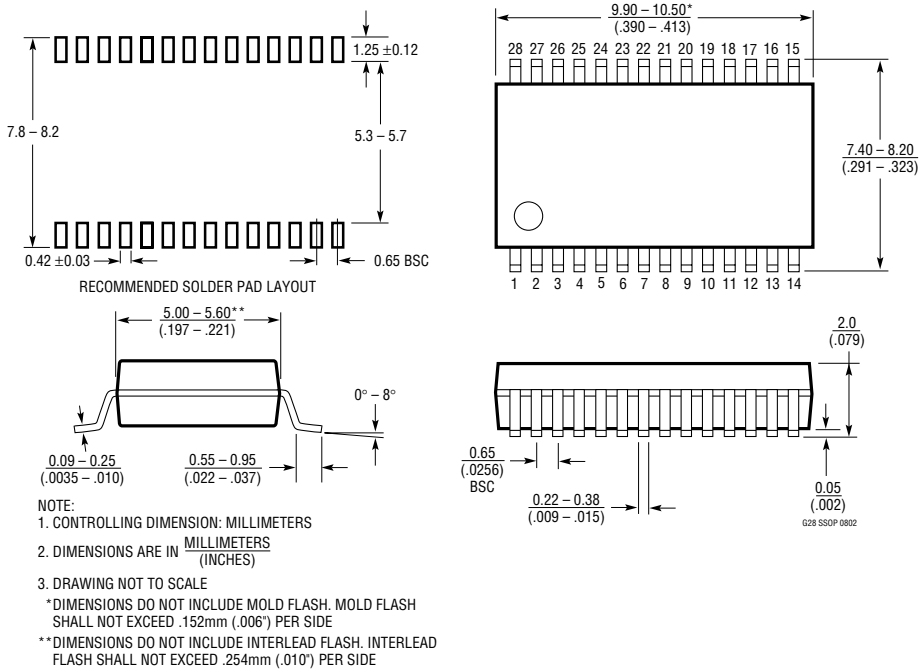


Figure 12. LTC1909-8 PCB Layout Diagram

PACKAGE DESCRIPTION

G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	Multiplexer with SMBus Interface	Single-Ended 8-Channel/Differential 4-Channel Analog MUX
LTC1622	550kHz Step-Down Controller	8-Pin MSOP, Synchronizable, Soft-Start; Current Mode
LTC1623	SMBus Dual High Side Switch Controller	Built-In Charge Pump Drives N-Channel MOSFETs, 8-Lead MSOP Package
LTC1625/LTC1775	No R_{SENSE} Current Mode Synchronous Step-Down Controller	97% Efficiency; No Sense Resistor; 16-Pin SSOP
LTC1628-SYNC	Dual, 2-Phase Synchronous Step-Down Controller	Synchronizable 150kHz to 300kHz
LTC1694/LTC1694-1	SMBus Accelerator	ThinSOT™, Active Pull-Up Improves Data Transmission and Reliability, Improves Low State Noise
LTC1699-80	SMBus VID Programmer Compliant with Intel 5-Bit Mobile Specifications	Precision ±0.35% Resistor Divider for Use with 0.8V Referenced Switching Regulators
LTC1699-81	SMBus VID Programmer Compliant with Intel Desktop VRM8.4 Specifications	Precision ±0.35% Resistor Divider for Use with 0.8V Referenced Switching Regulators
LTC1699-82	SMBus VID Programmer Compliant with Intel Desktop VRM9.0 Specifications	Precision ±0.35% Resistor Divider for Use with 0.8V Referenced Switching Regulators
LTC1709-7	High Efficiency, 2-Phase Synchronous Step-Down Controller	Up to 42A Output; $0.925V \le V_{OUT} \le 2V$
LTC1709-8	High Efficiency, 2-Phase Synchronous Step-Down Controller	Up to 42A Output; VRM 8.4, $1.3V \le V_{OUT} \le 3.5V$
LTC1710	SMBus Dual Monolithic High Side Switch	Two Integrated 0.4Ω/300mA N-Channel Switches
LTC1735	High Efficiency, Synchronous Step-Down Controller	Burst Mode Operation; 16-Pin Narrow SSOP; $3.5V \le V_{IN} \le 36V$
LTC1759	SMBus Interfaced Smart Battery Charger	Constant Current/Constant Voltage Battery Charger, Up to 8A Charge Current, High Efficiency Synchronous Charger
LTC1772	ThinSOT Step-Down Controller	Current Mode; 550kHz; Very Small Solution Size
LTC1778	No R_{SENSE} Synchronous Step-Down Controller	No Sense Resistor Required, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le (0.9)\ V_{IN}$, GN16
LT®1786F	SMBus Programmable CCFL Switching Regulator	Precision 100µA Full-Scale DAC, Grounded Lamp or Floating Lamp Configurations
LTC1876	2-Phase, Dual Synchronous Step-Down Controller with Step-Up Regulator	$3.5V \le V_{IN} \le 36V$, Power Good Output, 300kHz Operation
LTC3701	Dual, Step-Down Controller	Current Mode; 550kHz; Small 16-Pin SSOP, $V_{IN} < 9.8V$
LTC3711	5-Bit Adjustable, Wide Operating Range, No R_{SENSE} Step-Down Controller	GN24, Mobile VID, $0.925V \le V_{OUT} \le 2V$
LTC3714	Intel Compatible, Wide Operating Range, Step-Down Controller with Internal Op Amp	G28, $0.6V \le V_{OUT} \le 1.75V$, Programmable Output Offsets, 5-Bit VID

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