EMITSOP6EVB

EMITSOP6EVB Evaluation Board

Prepared by: Casey Stys
ON Semiconductor

ON Semiconductor®

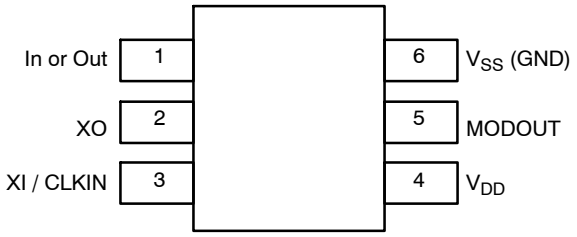
http://onsemi.com

Board Description

The EMI TSOP6 EVB universal Evaluation Board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the performance and operation of all twelve NB2XXXA EMI devices, and all of their possible configurations. This user's manual provides detailed information on board contents, layout and its use. It should be used in conjunction with the appropriate NB2XXXA datasheet: (www.onsemi.com). See Table 1.

Board Features

- Accommodates the Electrical Characterization of the NB2XXXA, Reduced EMI Series in the TSOP−6 Package
- Multiple Configurations − Refer to NB2XXXA Configurations Tables 1 and 2
- 26 Ω Series Termination Resistor Installed on MODOUT
- 15 pF Output Load Capacitor Installed on MODOUT
- Selectable Jumpers for SELECT Pin Logic Levels



Twelve EMI products share the same TSOP−6 (TSOT−23−6) package, but have minor pin configuration differences. See Table 2.

Figure 1. NB2XXXA TSOP−6 Pinout

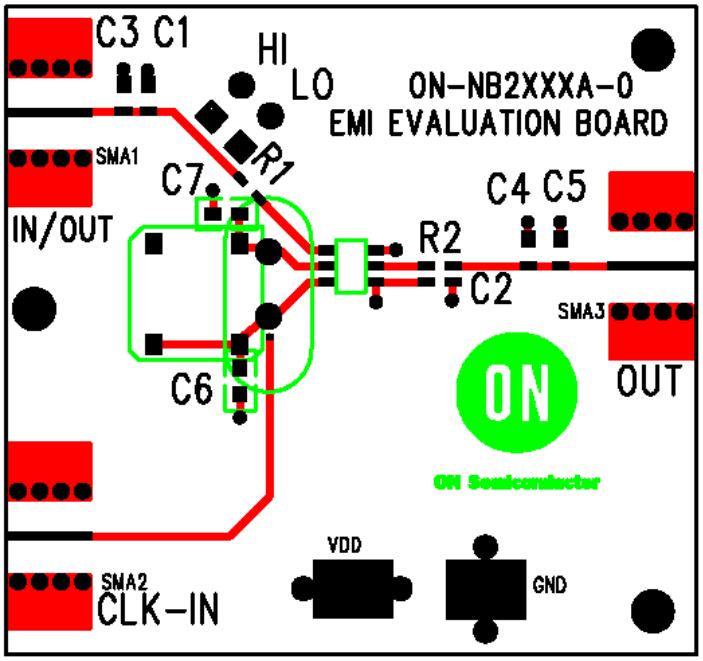


Figure 2. Evaluation Board

Table 1. NB2XXX PIN FUNCTION (see datasheet)

EMI Device	fin (MHz)	XTAL	CLKIN (External)	PD	SSON	Mod Eqn	Freq.	REFOUT
NB2579A	13 – 30	Y	Y	N	Y	$f_{in} \div 640$	±1%	N
NB2669A	6 – 13	N	Y	Y	N	$f_{in} \div 256$	±1%	N
NB2760A	6 – 13	Y	Y	Y	N	$f_{in} \div 256$	±0.75%	N
NB2762A	6 – 13	Y	Y	Y	N	$f_{in} \div 256$	−1.25%	N
NB2769A	6 – 13	Y	Y	Y	N	$f_{in} \div 256$	±1%	N
NB2779A	13 – 30	Y	Y	Y	N	$f_{in} \div 640$	±1%	N
NB2780A	30 – 50	Y	Y	Y	N	$f_{in} \div 1280$	±0.75%	N
NB2869A	6 – 13	Y	Y	N	N	$f_{in} \div 256$	±1%	Y
NB2870A	13 – 30	Y	Y	N	N	$f_{in} \div 640$	±0.75%	Y
NB2872A	15 – 30	Y	Y	N	N	$f_{in} \div 640$	−1.25%	Y
NB2879A	15 – 30	Y	Y	N	N	$f_{in} \div 640$	±1%	Y
NB2969A	6 – 13	Y	Y	N	N	$f_{in} \div 256$	±1%	Y, REFOUT ÷2

Table 2. NB2XXX PIN ASSIGNMENT (see datasheet)

EMI Device	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	See Table 4
NB2579A	I	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	R1 = 0 Ω
NB2669A	I	NC	CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	R1 = 0 Ω
NB2760A	I	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	R1 = 0 Ω
NB2762A	I	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	R1 = 0 Ω
NB2769A	I	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	R1 = 0 Ω
NB2779A	I	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	R1 = 0 Ω
NB2780A	I	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	R1 = 0 Ω
NB2869A	O	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	R1 = 26 Ω
NB2870A	O	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	C1
NB2872A	O	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	C1
NB2879A	O	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	C1
NB2969A	O	XO	XI / CLKIN	V_{DD}	MODOUT	V_{SS} (GND)	C1

LAB SETUP PROCEDURE

Lab Setup and Measurement Procedure

Equipment Used

- Agilent Signal Generator #81110A (or Crystal)
- Real−Time Oscilloscope, Frequency Counter or Spectrum Analyzer
- Agilent #6624A DC Power Supply
- Digital Voltmeter

Power Supply Connections

The NB2XXXA has a positive supply pin, V_{DD}, and a negative supply pin, GND.

Power supply "anvil" terminals are provided for V_{DD} and GND. Use of "minigrabber" banana plug cables work well for connections to the power supply.

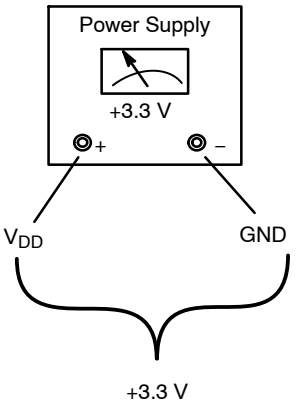


Figure 3. Power Supply Configuration

Table 3. POWER SUPPLY CONFIGURATIONS

Device Pin	Single Power Supply
V_{DD}	V_{DD} = +3.3 V
GND	GND = 0 V

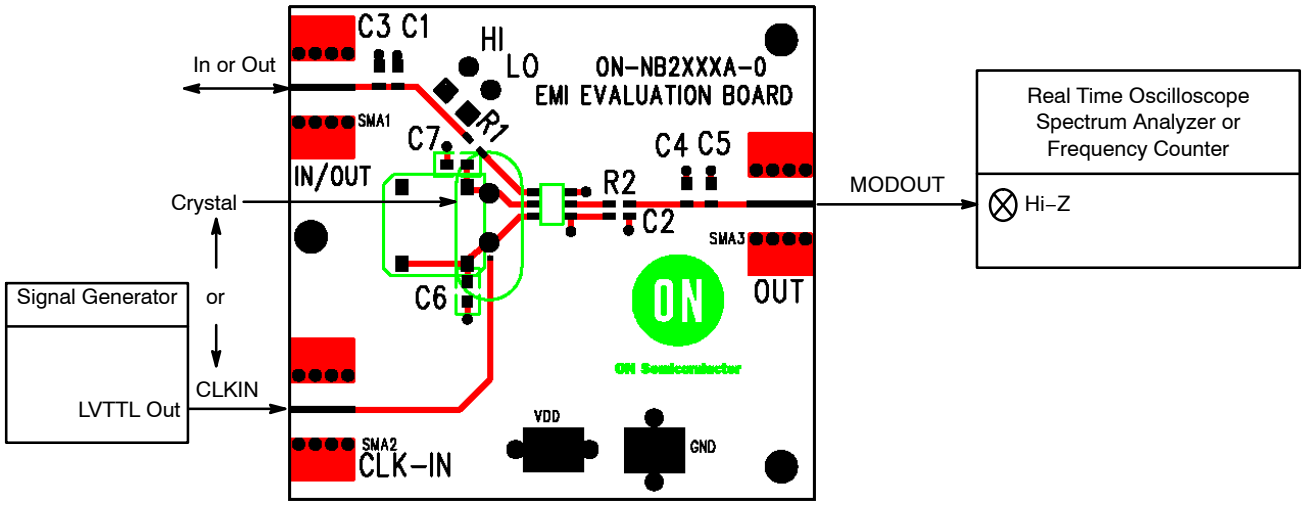


Figure 4. Input / Output Configuration

NB2XXXA

Lab Test Set−up Procedure

To monitor the MODOUT output on an oscilloscope, spectrum analyzer or frequency counter:

1. Connect a power supply to the evaluation board. (see Figure 3)
   Connect V_{DD} to +3.3 V
   Connect GND to 0 V
2. Connect an external clock reference to the CLKIN Pin 3 or install a crystal and appropriate (see CLKIN) crystal load capacitors to Pins 2 and 3.
3. Connect the MODOUT output to the measurement instrument.
4. For the MODOUT output, the NB2XXXA board provides a series 26 Ω source termination resistor and a load capacitor pad for each output; 15 pF is installed.

Board Layout

The evaluation board is constructed with FR4 material and 50 Ω trace impedance, designed to minimize noise and crosstalk.

Layer Stack

L1 Signal (top)
L2 Ground
L3 V_{DD} (positive power supply)
L4 Blank (bottom)

Pin 1 − IN / OUT Configuration

Pin 1 of the EMI TSOP6 EVB universal evaluation board can be configured to serve as an input or output, depending on device.

See Tables 1 and 2.

An SMA connector is provided to access Pin 1.
If Pin 1 is an input, a 0 Ω resistor may be used at R1.

Table 4. PIN 1 INPUT/OUTPUT

Device	Pin #1	R1	C1 (or C3)
See Table 2	Input	0 Ω	Open
See Table 2	Output	26 Ω	15 pF

If Pin 1 is an output, C1 can be used to install an output load capacitor, ie. a 15 pF capacitor. C1 and C3 can be used to parallel two output load capacitors. Also, a 26 Ω series termination resistor should be installed at R1.

When Pin 1 is an input, the select header pins, HI and LO, can manually control the Pin 1 logic level via the appropriate jumper/shunt. A connection from each header must then be made to the Pin 1 metal trace. When either HI or LO are jumpered, Pin 1 is forced to V_{DD} (logic High) or GND (logic Low).

MODOUT Output Series Resistor

An R2 resistor pad is provided to series terminate the MODOUT output and is installed with a 26 Ω resistor. This series resistor complements an internal 24 Ω resistor to match the 50 Ω trace impedance.

MODOUT Output Load Capacitor

An output load capacitor pad is provided to load the MODOUT output and is installed with a 15 pF capacitor. C4 and C5 can be used to parallel two output load capacitors for various combinations of capacitive loads, if needed.

CLKIN

An SMA connector is provided for CLKIN if an external clock source is used on Pin 3. **The metal trace at the crystal pad is intentionally open for crystal use, and must be shorted for a connection to Pin 3 for external clock use.** The unused component pad labeled C6 (used for the crystal load capacitor) may be used for a 50 Ω resistor to ground to terminate a signal generator.

NB2XXXA Output Loading

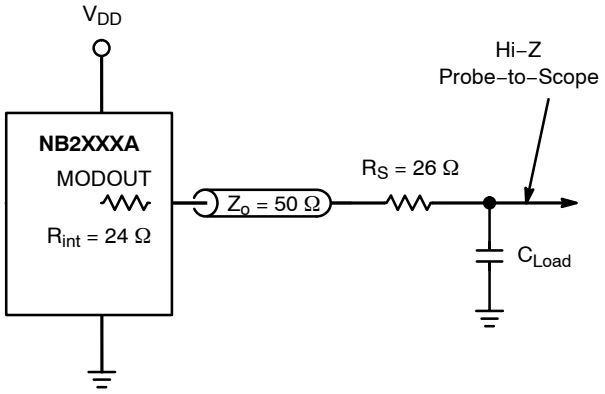


Figure 5. Output Loading for Test / Evaluation

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50 Ω trace (a commonly used trace impedance), place a 26 Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 24 Ω.

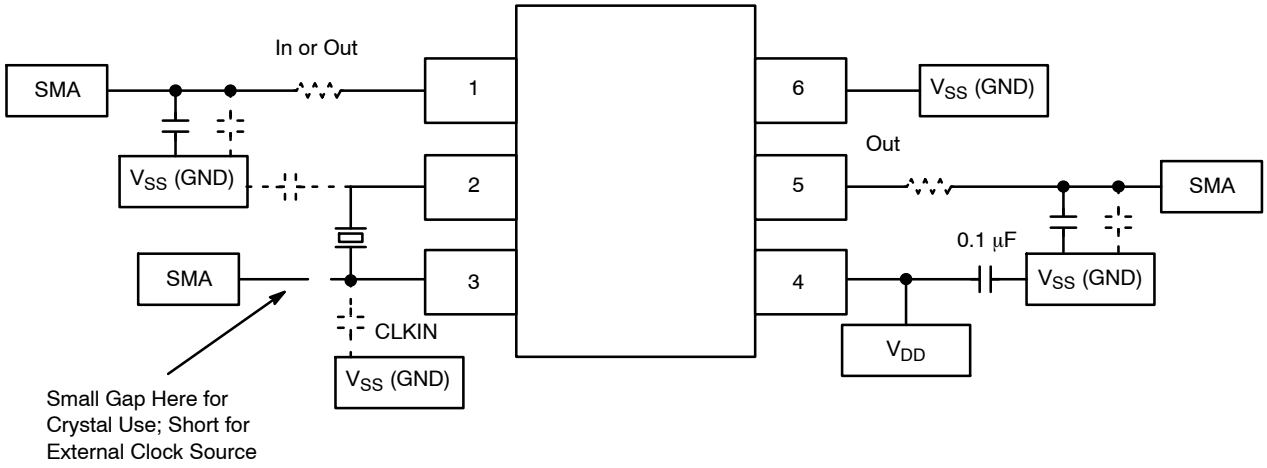


Figure 1. NB2XXXA Evaluation Board Schematic

Table 5. NB2XXXA EVALUATION BOARD BILL OF MATERIALS

	Component	Description	Qty
SMA 1 – 3	Connector	SMA Connector	1–3
C2	Capacitor	0.1 μF, 10%, KEMET, C0603C104K5RAC, Installed	1
C6 – C7	Capacitor (Crystal Load)	27 pF, Not Installed	2
C1, C3, C4, C5	Capacitor	15 μF, C5 Installed	1–4
	Jumper Header	100 mil, Berg	4
	Jumper		2
R1 – R2	Resistor	26 Ω or 0 Ω, R2 Installed with 26 Ω	2
C6	Resistor (optional)	50 Ω, 0.1%, 0.25 W	1
	Power Supply Connector	Anvil – Keystone #5016	2
U1	NB2XXXA	TSOP−6 device (Installed by User)	1
X1	Crystal (See Crystal Chart)	Fundamental Mode, Parallel Resonant, Ecliptek www.ecliptek.com	1
	Pin Recepticle	Through−Hole Crystal Connector	2
	Capacitor	V_{DD} to GND Bypass Capacitors 10 μF – 22 μF 0.01 μF – 0.1 μF	1 1

Table 6.

Crystal Frequency (MHz)	Ecliptek Part #	ESR (Ω MAX)
6.000	ECX−6074−6.000M	125
8.000	ECX−6075−8.000M	70
10.000	ECX−6078−10.000M	50
12.000	ECX−6081−12.000M	50
13.500	ECX−6082−13.500M	50
14.31818	ECX−6083−14.31818M	50
15.000	ECX−6084−15.000M	50
16.000	ECX−6087−16.000M	50
16.660	ECX−6090−16.660M	50
18.750	ECX−6125−18.750M	50
19.440	ECX−6091−19.440M	50
19.531	ECX−6126−19.531M	50
20.000	ECX−6094−20.000M	50
20.1416	ECX−6127−20.1416M	50
20.480	ECX−6099−20.480M	50
24.000	ECX−6102−24.000M	40
25.000	ECX−6105−25.000M	40
26.5625	ECX−6110−26.5625M	40
26.6000	ECX−6128−26.6000M	50
27.000	ECX−6115−27.000M	40
28.000	ECX−6118−28.000M	40
30.000	ECX−6119−30.000M	40
32.000	ECX−6120−32.000M	40

Table 7.

Crystal Parameter	Specification
Nominal Frequency	See Chart
Frequency Tolerance at 25°C/ Stability over OTR	±15 ppm / ±20 ppm
Operating Temperature Range	0°C to +70°C
Load Capacitance (C_L)	18 pF
Equivalent Series Resistance (Ω) (Maximum)	See Chart
Mode of Operation and Crystal Cut	AT−Cut Fundamental
Storage Temperature	−40°C to +85°C
Drive Level	100 μWatts Correlation 1 mW Maximum
Aging (at 25°C)	±3 ppm / 1st year, ±15 ppm / 10 year Maximum
Insulation Resistance	500 MΩ Minimum,100 V
Shunt Capacitance (pF (Maximum)	5 pF Maximum
Package	E2S (HC−49/UP SMD)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative