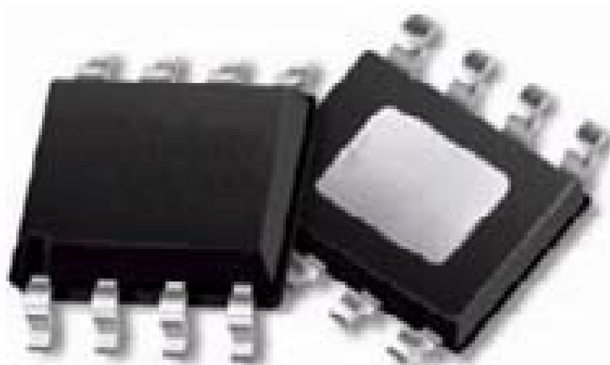
# Reliability Qualification Report

## CGA-6618 - SnPb Plated

## CGA-6618Z - Matte Sn, RoHS Compliant



| Initial Qualification | 08-2002 |
|---|---|
| RoHS Qualification | 02-2006 |

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*303 S. Technology Ct, Broomfield CO, 80021* *Phone: (800) SMI-MMIC* *http://www.sirenza.com*

*Document RQR-102330 Rev D*

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# CGA-6618/CGA-6618Z
# Reliability Qualification Report

## I. Qualification Overview

The CGA-6618/6618Z products have been subject to stresses such as high temperature operating life, extreme hot and cold environments (temperature cycling), and moisture sensitivity (MSL-1 and solder reflow testing), and has demonstrated reliable performance. This qualification reports summarizes the results and also includes reliability monitor data.

## II. Introduction

Sirenza Microdevice's CGA-6618/6618Z are high performance GaAs HBT MMIC Amplifiers. It is designed with the InGaP process technology for excellent reliability. A Darlington configuration is utilized for broadband performance. The heterojunction increases breakdown voltage and minimized leakage current between junctions. The amplifier contains two amplifier die for use in wideband Push-Pull CATV amplifiers requiring second order performance. The second and third order non-linearities are greatly improved in the push pull configuration.

## III. Fabrication Technology

The CGA-6618/6618Z amplifiers are manufactured using a InGaP/GaAs Heterojunction Bipolar Transistor (HBT) technology. The devices are fabricated using MOCVD epitaxy technology which produces consistent and reproducible performance from lot to lot. Through the use of InGaP emitters, a mature MMIC fabrication process and rigorous in-process monitoring, excellent reliability with MTTF of greater than 1 x 106 hrs at 150°C have been achieved.

## IV. Package Type

The CGA-6618/6618Z power amplifiers are packaged in a plastic encapsulated exposed pad EPAD-8 package that is assembled using a highly reproducible automated assembly process. The die is mounted using an industry standard thermally and electrically conductive silver epoxy. The paddle is exposed to provide a low thermal resistance heat conduction path when soldered directly to a PCB.

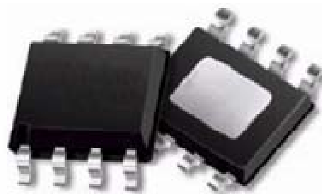

Figure 1 : EPAD-8 Encapsulated Plastic Package



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## V. Qualification Methodology

The Sirenza Microdevices qualification process consists of a series of tests designed to stress various potential failure mechanisms. This testing is performed to ensure that Sirenza Microdevices products are robust against potential failure modes that could arise from the various die and package failure mechanisms stressed. The qualification testing is based on JEDEC test methods common to the semiconductor industry. A FMEA approach is used to determine the test methods to be included in the qualification plan. The manufacturing test specifications are used as the PASS/FAIL criteria for initial and final DC/RF tests.

## VI. Operational Life Testing

Sirenza Microdevices defines operational life testing as a DC biased elevated temperature test performed at the maximum operational junction temperature limit. For the SHF, the maximum operational temperature limit is 150$^{o}$C. The purpose of the operational life test is to statistically show that the product operated at its maximum operational ratings will be reliable by operating devices up of 1000 hours. The results for this test are expressed in device hours that are calculated by multiplying the total number of devices passing the test by the number of hours tested.

## VII. Moisture Sensitivity Level - MSL Level 1 Device

The CGA-6618/6618Z have successfully completed 168 hours of moisture soak (85$^{o}$C/85%RH), followed by three passes through a convection reflow oven at 270$^{o}$C (Z versions), or at 235$^{o}$C (non-Z versions). The successful completion of this test classifies the parts as JESD 22-A113B Moisture Sensitivity Level 1 (MSL-1). MSL-1 indicates that no special dry pack requirements or time limits from opening of static bag to reflow exist. MSL-1 is highest level of moisture resistance that a device can be classified according to the above mentioned standard.



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## VIII. Electrostatic Discharge Classification

Sirenza Microdevices classifies Human Body Model (HBM) electrostatic discharge (ESD) according to the JESD22-A114 convention. All pin pair combinations were tested. Each pin pair is stressed at one static voltage level using 1 positive and 1 negative pulse polarity to determine the weakest pin pair combination. The weakest pin pair is tested with 3 devices below and above the failure voltage to classify the part. The Pass/Fail status of a part is determined by the manufacturing test specification. The ESD class quoted indicates that the device passed exposure to a certain voltage, but does not pass the next higher level. The following table indicates the JESD ESD sensitivity classification levels.

| Class | Passes | Fails |
|---|---|---|
| 0 | 0 V | <250 V |
| 1A | 250 V | 500 V |
| 1B | 500 V | 1000 V |
| 1C | 1000 V | 2000 V |
| 2 | 2000 V | 4000 V |

| Part | Class |
|---|---|
| CGA-6618/6618Z | 1A |

## IX. Operational Life Test Results

The results for CGA-6618/6618Z High Temperature Operating Life Test are as follows

| Test Duration | Junction Temperature | Quantity | Device Hours |
|---|---|---|---|
| **1000 hours** | **150˚C** | **79** | **79,000** |

Table 1: Summary of High Temperature Operational Life Test Cumulative Device Hours

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## X. Qualification Test Results

| Group | Test Name | Test Condition/<br>Standard | Sample Size | Results |
|---|---|---|---|---|
| A0 | Preconditioning | MSL1<br>Reflow @ 235ºC Peak<br>JESD22-A113C<br>(Non-Z version) | 250 | Pass |
| | | MSL1<br>Reflow @ 270ºC Peak<br>JESD22-A113C<br>(Z version) | 225 | Pass |
| A1 | Temperature Cycle | -65°C to +150°C<br>10 min dwell, 1 min transition<br>1000 cycles<br>JESD22-A104B<br>(Non-Z version) | 60 | Pass |
| | | -65°C to +150°C<br>10 min dwell, 1 min transition<br>1000 cycles<br>JESD22-A104B<br>(Z version) | 30 | Pass |
| A1a | Temperature Cycling | Air to Air, Soldered on PCB<br>-65ºC to 150ºC<br>10 min dwell, 1 min transition<br>1000 cycles<br>JESD22-A104B<br>(Non-Z version) | 15 | Pass |
| | | Air to Air, Soldered on PCB<br>-65ºC to 150ºC<br>10 min dwell, 1 min transition<br>1000 cycles<br>JESD22-A104B<br>(Z version) | 30 | Pass |



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## X. Qualification Test Results

| Group | Test Name | Test Condition/ Standard | Sample Size | Results |
|---|---|---|---|---|
| A2 | High Temperature Operating Life | Tj = 150°C<br>100 hours<br>JESD22-A108B<br>(Non-Z version)<br><br>Tj = 150°C<br>1000 hours<br>JESD22-A108B<br>(Z version) | 79<br><br>80 | Pass<br><br>Pass |
| B | HAST | Tamb=110°C, 85%RH<br>Biased, 264 hours<br>JESD22-A110B<br>(Non-Z version) | 15 | Pass |
| C | Autoclave | Tamb=121°C, 100%RH<br>Un-Biased, 96 hours<br>JESD22-A102C<br>(Non-Z version)<br><br>Tamb=121°C, 100%RH<br>Un-Biased, 96 hours<br>JESD22-A102C<br>(Z version) | 43<br><br>30 | Pass<br><br>Pass |
| | ESD HBM | JESD22-A114 | 33 | Class 1A |
| E | Power Temperature Cycle | -40°C to +85°C<br>Cycled bias (5' on/5'off)<br>500 cycles<br>JESD22-A109A<br>(Non-Z version)<br><br>-40°C to +85°C<br>Cycled bias (5' on/5'off)<br>1000 cycles<br>JESD22-A109A<br>(Z version) | 10<br><br>20 | Pass<br><br>Pass |

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## X. Qualification Test Results

| Group | Test Name | Test Condition/ Standard | Sample Size | Results |
|---|---|---|---|---|
| E | High Temperature Storage | Tamb=150°C<br>1000 hours<br>JESD22-A103B<br>(Z version) | 30 | Pass |
| | Low Temperature Storage | Tamb=-65°C<br>1000 hours<br>(Z version) | 30 | Pass |
| F | Tin Whisker | Tamb=60°C, 90%RH<br>2800 hours<br>NEMI<br>(Z version) | 10 | Pass |
| G | Solderability | Dip & Look<br>SnPb solder<br>Steam Age Condition C<br>Dip Condition A, 215°C<br>JESD22-B102C<br>(Non-Z version) | 45 | Pass |
| | | Dip & Look<br>SnPb solder<br>Steam Age Condition C<br>Dip Condition A, 215°C<br>JESD22-B102C<br>(Z version) | 15 | Pass |
| | | Dip & Look<br>Pb-free solder<br>Steam Age Condition C<br>Dip Condition B, 245°C<br>JESD22-B102C<br>(Z version) | 15 | Pass |



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## XI. Junction Temperature Determination

One key issue in performing qualification testing is to accurately determine the junction temperature of the device. Sirenza Microdevices uses a 3um spot size emissivity corrected infrared camera measurement to resolve the surface temperature of the device at the maximum operational power dissipation. The results are displayed below for the device running at operational current of Iq= 165mA, a device voltage of 4.7V, lead temperature of 85°C, and no RF applied.

**Junction Temperature Tj=108.6C**
Tlead = 85C, Id = 165mA, Vd = 4.7V

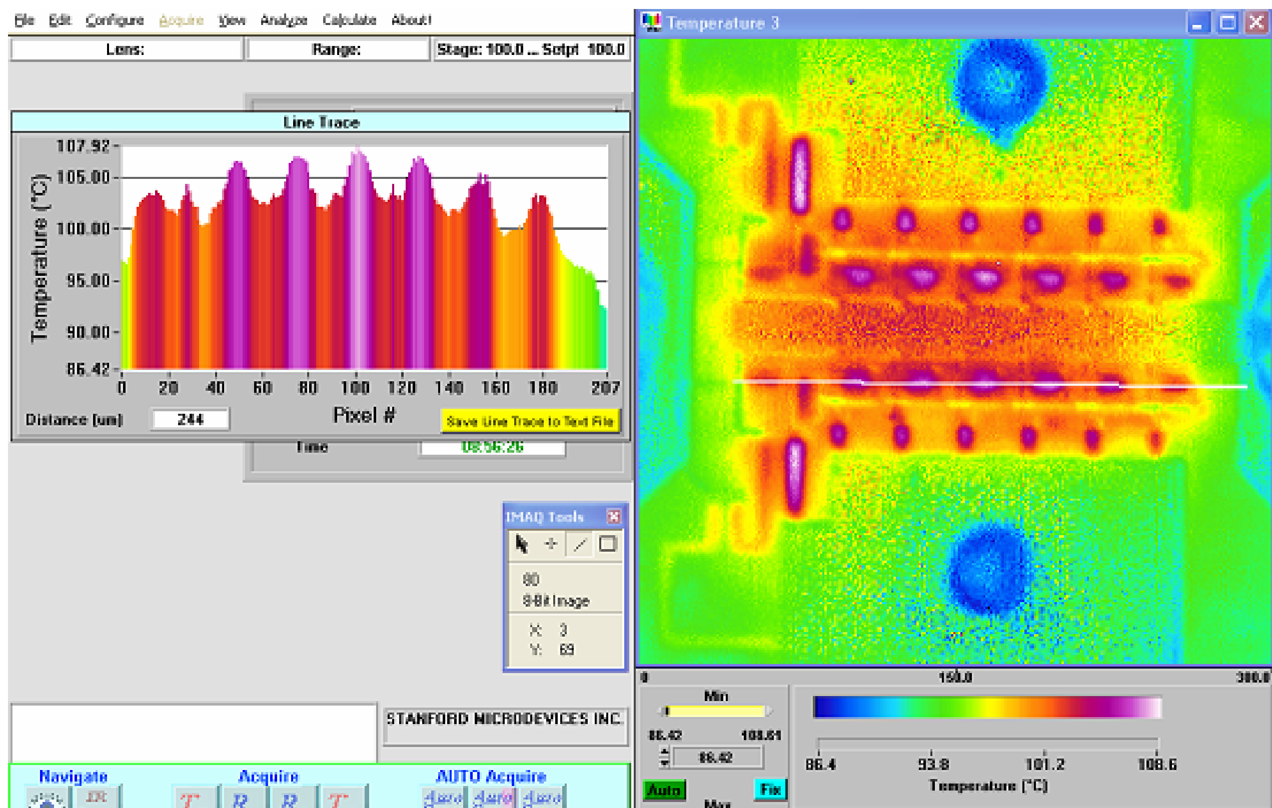


Figure 2: Infrared Thermal Image of CGA-6618, Vd =4.7V, Id =165 mA, Tlead = 85°C

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