

PM6670: complete DDR2/3 memory supply controller

Single step-down controller plus LDO



STMicroelectronics' PM6670 offers the most complete Double Data Rate (DDR) memory power supply solution designed to meet DDR2/3 JEDEC specifications.

The PM6670 belongs to a product family designed to support memory power management in notebook applications.

The advanced BCD technology not only supports high performance and ultra-low power consumption, but also allows the integration of high current ULDO.

This device integrates a buck controller, a 2Apk sink/source low dropout (LDO) regulator and an ultra-low noise buffered reference.

Available in a compact 4 x 4mm VFQFPN 24-pin package, the PM6670 is ideal for space-saving design requirements.

Key features

- Constant On-Time (C.O.T.) topology for very fast load transient response
- 1.8V (DDR2) or 1.5V (DDR3) fixed output voltages
- 0.9V to 2.6V adjustable output voltage
- No R_{SENSE} current sensing with low side MOSFET's $R_{DS(on)}$
- Soft start internally fixed at 3ms
- Selectable minimum frequency (33kHz) in pulse-skip mode
- Output voltage ripple compensation
- 2Apk LDO with foldback for V_{TT}
- High-Z V_{TT} output in S3
- $\pm 15mA$ low noise buffered reference
- Supports ceramic output capacitors
- Housed in space-saving VFQFPN 24L

Main applications

- DDR2/3 memory supply
- Notebook computers
- UMPC
- IDTV
- HDSTB/STB

The PM6670 integrates a pulse-width-modulation (PWM) buck controller, a 2Apk sink/source LDO regulator and a 15mA low noise buffered reference. The buck controller provides ultra high efficiency conversion (up to 92%), employing a lossless current sensing technique.

The PM6670 is based on a Constant On-Time (C.O.T.) architecture which allows the controller to convert with fast load transient over a wide input voltage range (4.5V- 28V). Both polymeric and ceramic output capacitors are supported. An embedded integrator control loop compensates the DC voltage error due to the output ripple

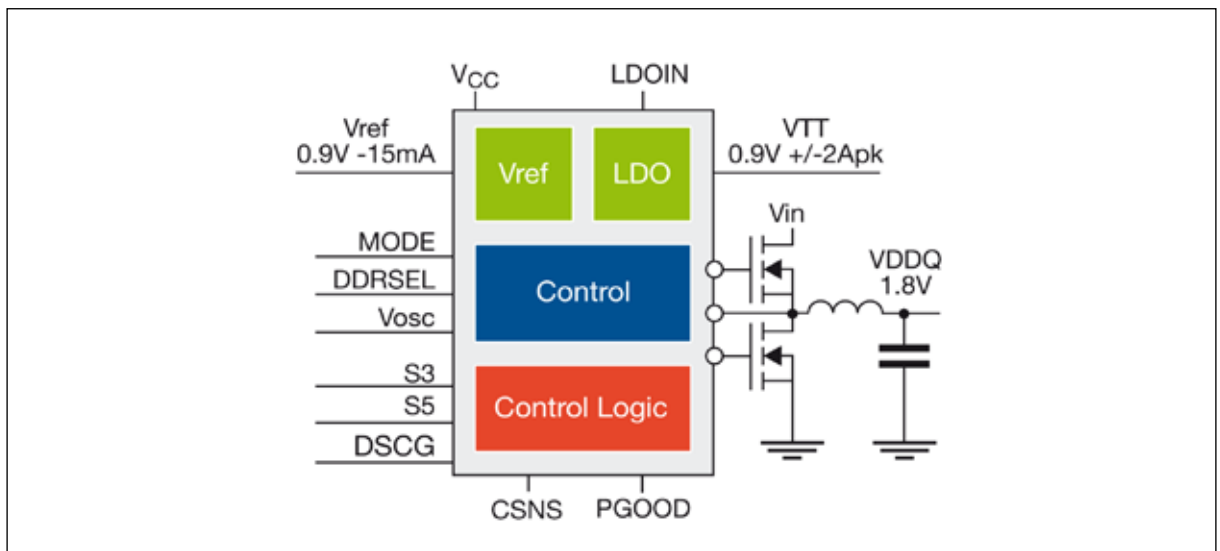
The DDR2/3 supply voltage VDDQ can be easily set to 1.8V (DDR2) or 1.5V (DDR3) without additional components. The output voltage can also be adjusted in the 0.9V to 2.6V range using an external resistance divider.

The output of the linear regulator (VTT) tracks the

reference voltage VTTREF of the memory within $\pm 35\text{mV}$, in accordance with JEDEC specifications, over the full spectrum of operating load conditions. The input of the LDO can be either VDDQ or a lower voltage rail in order to reduce the total power dissipation. The reference voltage (VTTREF) section provides a voltage equal to one half of VDDQ with an accuracy of $\pm 2\%$.

In light load conditions, a pulse-skip technique increases efficiency with minimum impact on the accuracy of the output regulation. During pulse-skip mode, a minimum switching frequency of 33kHz is available to prevent audio noise issues.

The device is fully compliant with system sleep states S3 (Suspend-To-RAM) and S4/S5 (Suspend-To-Disk), providing LDO high output impedance in STR and tracking discharge of all outputs in STD. S3 and S5 pins are compatible with chipset interface and define the system sleep state.



Main internal blocks of PM6670

DDR and GDDR memory power management

Part number	Number of outputs	Main applications	Regulated switching [V]	Regulated LDO [V]	LDO current [A]	IC supply voltage [V]	Output accuracy [%]	Switching frequency	Package
PM6670	3	DDR2/3	V _{ddq} : 1.5, 1.8 or adj	Fixed V _{ddq} /2	2 pk	5.5 to 28	± 1	200kHz to 1MHz	VFQFPN-24 4X4
PM6675	3	GDDR3/4	Adj from 0.6	Adj from 0.6	2 pk	5.5 to 28	± 1	200kHz to 1MHz	VFQFPN-24 4X4



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