PM0064
Programming manual

How to program the STM8T141 OTP options

Introduction

The STM8T141 integrated circuit family can be used in the default (unconfigured) state. However, for some applications, certain one-time-programmable (OTP) options must be set.

This document describes the hardware and software interfaces that are necessary to program the user selectable options on the STM8T141 family of integrated circuits.

Related documentation

- STM8T141 datasheet
- ST-TSLINK user manual (UM0795)

1 Glossary

This section gives a brief definition of acronyms and terms used in this document:

- **IC**: STM8T141 family integrated circuit
- **Option**: User programmable option
- **Option programming**: Programming of user programmable option
- **Option_0 thru option_7**: Refers to Option byte Opt0[0:7]
- **Option_8 thru option_15**: Refers to Option byte Opt1[0:7]
- **OUT**: Refers to the TOUT/POUT pin of the STM8T141

2 Hardware interface

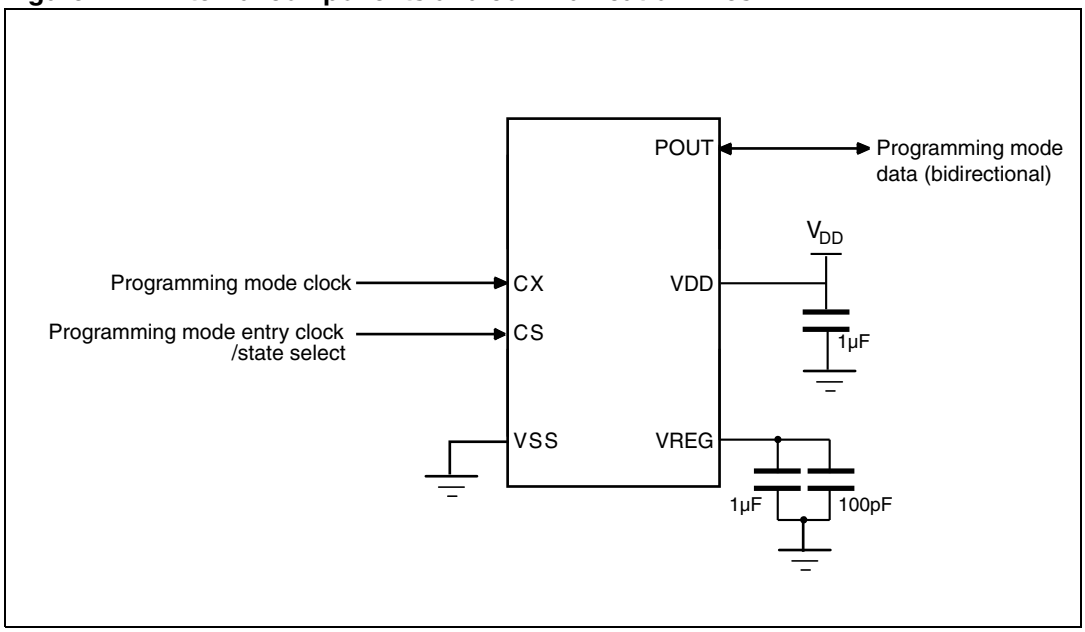
This section provides information on the hardware interface used to program the OTP options. For detailed information on other aspects of the device please refer to the STM8T141 datasheet.

2.1 External components

The STM8T141 has an internal voltage regulator that needs an external capacitor on the VREG pin to function correctly. For a cleaner external supply a 1µF capacitor and a ceramic 100 pF capacitor between VREG & VSS is also recommended. It is recommended to place a 1 µF capacitor between VDD and VSS.

Note: The VREG capacitors should be placed as close as possible to the VREG & VSS pins of the STM8T141*.*

Figure 1. External components and communication lines



2.2 Communication lines

The following lines are used for programming the device:

- CS: programming mode entry CLK and programming state SELECT
- CX: programming mode CLK
- POUT: programming mode DATA (bi-directional, i.e. input and output)

2.3 Voltage levels for communication

The following table gives the voltage specifications. It is recommended to use the typical values when designing a programming tool.

Table 1. Voltages for reading or programming

VDD pin	Min	Typ	Max	Units
Programming mode entry	2.9	5.0	5.5	V
Option byte programming	6.6	6.7	6.8	
Option byte reading	2.9	5.0	5.5	

Caution: All I/Os must have the same voltage level as VREG.

During option programming, the supply voltage of the STM8T141 is raised to 6.7 V. It is recommended to make sure that the I/Os of the programmer can operate at 6.7 V.

- CS: Same voltage level as VREG
- CX: Same voltage level as VREG
- OUT: Same voltage level as VDD

The CS and CX pins have ESD protection diodes connected to VREG, therefore voltage levels higher than VREG should not be used on CS and CX.

A level shifter that follows the VREG voltage of the STM8T141 should be used to communicate with the STM8T141 at the correct voltages,

The only time that a voltage higher than VREG may be used on CS and CX is during option programming when VREG is tied to VDD.

Note: 1 For in-circuit programming: make sure that no external components will influence the voltage swing of the CS, CX and OUT pins.

2 For in-circuit programming: an external voltage regulator on the product may clip the VDD voltage at its regulation voltage and prevent VDD from reaching the required option programming voltage of 6.7 V. Large capacitors on VDD or VREG can increase the time needed for the programmer to reach 6.7 V - sometimes the option programming instruction might be given before the required voltage has been reached. Adjust all timing delays accordingly.

3 The user documentation of the programming tool must contain the maximum load current permitted to drive the application without disturbing the programming signals.

3 Programming sequence

Figure 4 describes how to program the STM8T141 device and then verify that your programming was successful. Each state transition depends on the CS value and the clock pulses applied to CX.

3.1 Programming mode entry

Programming mode entry (State_1) is the point from where you navigate to other programming mode states. Each sequence in the following chapters uses the programming mode entry sequence described in *Table 2*.

Refer to *Figure 2* and *Figure 3* for special sequences on CS (step 6) and CX (step 10).

Table 2. Programming mode entry (State_1)

Step	Action	Explanation
1.	Make OUT input	Make the OUT pin an input.
2.	IC power ON	VDD = 5V
3.	CX = LOW	Start state of CX.
4.	CS = High	Start state of CS.
5.	Wait > 4ms	Wait for VREG to stabilize. Increase time if necessary to allow for a larger capacitor on VREG.
6.	CS – 9 transitions (starting with a falling transition)	See *Figure 2*. The timing on CS is important. This timing is taken from the center frequency. If the frequency is changed, or is not according to specification, the timing must be scaled accordingly.
7.	Wait 100us	Wait for CS capacitor to discharge.
8.	CX = HIGH	CX is normally HIGH. Clocking is done with negative pulses.
9.	Wait 100us	Wait for CS capacitor to charge.
10.	CX - 9 double clock	18 negative pulses on CX to get into programming mode (State_0). All CX clocks consist of two consecutive negative going pulses. See *Figure 3*.
11.	CS = HIGH	CS = 1 required for transition from State_0 to State_1.
12.	CX - 1 double clock	Clock IC into State_1.

Figure 2. Programming mode entry pulses on CS: all 4 pulses

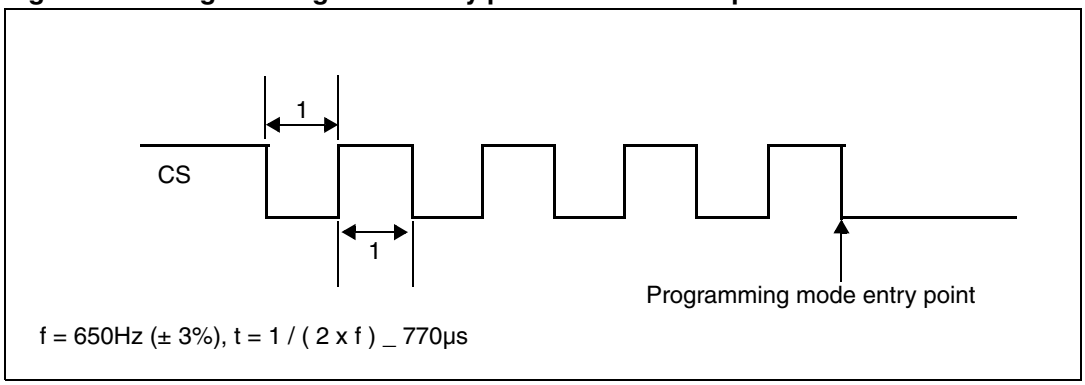
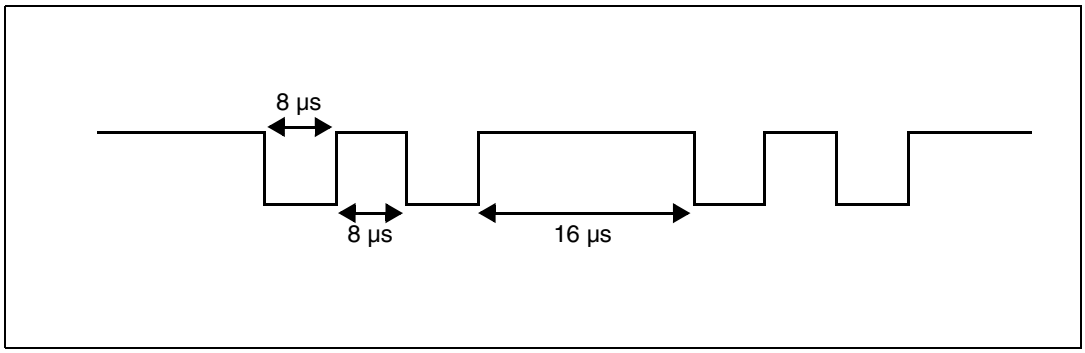


Figure 3. Programming mode clock on CX: double clock + time delay between double clocks



3.2 Option read

1. Programming mode entry (State_1): Follow steps to enter programming mode as in *Table 2*.
2. Option read (State_20) reads the options. See *Table 3: Option read (State_20)*. Option bit interpretation: 0 = option not programmed; 1 = option programmed.

Note: Whenever the state of CS is changed, allow enough time for the transition to occur depending on the CS capacitor connected to the circuit.

Table 3. Option read (State_20)

Step	Action	Explanation
1.	CS = LOW	CS should be LOW to move through states 3, 7, 11, 15 into State_19.
2.	CX - 5 double clock	Clock IC until it is in State_19.
3.	CS = HIGH	CS = 1 required for transition from State_19 to State_20.
4.	CX - 1 double clock	Clock IC into State_20.
5.	CX - 1 double clock	The IC places option_0 value on OUT pin.
6.	Read option on OUT	Option value is now available on OUT pin.

Table 3. Option read (State_20)

Step	Action	Explanation
7.	Repeat steps 5 and 6 for all 16 options.	Each option's value is clocked out - one after another. (As long as CS remains HIGH, the IC will stay in State_20)
8.	IC power OFF	VDD = 0V

3.3 Option programming

1. Programming mode entry (State_1): Follow steps to enter programming mode as in *Table 2*.
2. Option register write (State_2) writes the value of the options that must be programmed into the Option register. See *Table 4: Option programming (State_2)*.
3. Option programming (State_4) is the first stage to program the options that were programmed into the Option register. See *Table 5: Option programming (State_4)*.
4. Option programming (State_6) is the second stage of programming the options. See *Table 6: Option programming (State_6)*.

Note: The reserved Option bits must not be altered (one way to ensure they are not altered is to set them to 0 regardless of their value).
Refer to the STM8T141 datasheet for the position of the reserved Option bits.

Table 4. Option programming (State_2)

Step	Action	Explanation
1.	CS = HIGH	CS = 1 required for transition from State_1 to State_2.
2.	CX - 1 double clock	Clock IC into State_2.
3.	Make OUT an output	In State_2 OUT is an IC input, data can be written to it by the programmer.
4.	OUT = LOW	Place a 0 on OUT.
5.	CX - 1 double clock	Clock in the 0 on OUT to prepare the register.
6.	OUT = option bit value	Place the value for option_0 on OUT.
7.	CX - 1 double clock	Clock in option value.
8.	Repeat Steps 6 and 7 for all options except option_15.	Clock in all the options until option_14 is clocked in, leaving only option_15 not yet clocked into the register.
9.	CS = LOW	The final option is written to the register while moving into State_3.
10.	OUT = option_15	Place the final option on OUT.
11.	CX - 1 double clock	Clock in option_15; this automatically clocks the IC into State_3.
12.	Tri-state OUT pin	Any controller attached to the IC's OUT must be tri-stated.

Table 5. Option programming (State_4)

Step	Action	Explanation
1.	CS = HIGH	CS = 1 required for transition from State_3 to State_4.
2.	CX - 1 double clock	Clock IC into State_4.
3.	VDD = 6.7 V	Increase power for IC up to 6.7 V (+/- 0.1V).
4.	Wait 1 ms.	Wait for voltage to stabilize at 6.7 V (+/- 0.1V).
5.	CX - 1 double clock	Signal for IC to program options.
6.	CX = LOW	CX = 0 to prevent false signal when VREG is raised later on.

Table 5. Option programming (State_4) (continued)

Step	Action	Explanation
7.	CS = LOW	CS = 0 to prevent false signal when VREG is raised later on.
8.	VREG = VDD	Connect VREG to VDD (6.7 V).
9.	Wait 200 ms.	Allow time for option programming process.
10.	VREG release	Disconnect VREG from VDD.
11.	Wait 20 ms.	Allow time for VREG capacitor to discharge.

Note: The 'Low' level of Steps 6 and 7 during programming are not absolutely mandatory. They could be 'High' if it is easier for the electronic command; provided they have the correct level for the next state transition.

Table 6. Option programming (State_6)

Step	Action	Explanation
1.	CX - 1 double clock	Clock the IC into State_6.
2.	CS = HIGH	CS = 1 required to remain in State_6.
3.	CX - 1 double clock	Signal for IC to program options.
4.	CX = LOW	CX = 0 to prevent false signal when VREG is raised later on.
5.	CS = LOW	CS = 0 to prevent false signal when VREG is raised later on.
6.	VREG = VDD	Connect VREG to VDD (6.7 V).
7.	Wait 200ms	Allow time for option programming process.
8.	VREG release VDD = 5.0 V	Disconnect VREG from VDD and decrease VDD voltage back to 5 V.
9.	Wait 20 ms	Allow time for VREG capacitor to discharge.
10.	CX - 1 double clock	Clock the IC into State_7.

3.4 Option verify (directly after option programming)

The STM8T141 has been successfully programmed if both the following reads return the correct option values.

1. Option read (State_20) reads the options that were programmed. See *Table 7: Option verify (State_20)*.
2. Option read (State_22) reads the options at a different level - as a double check. See *Table 8: Option verify (State_22)*.

Table 7. Option verify (State_20)

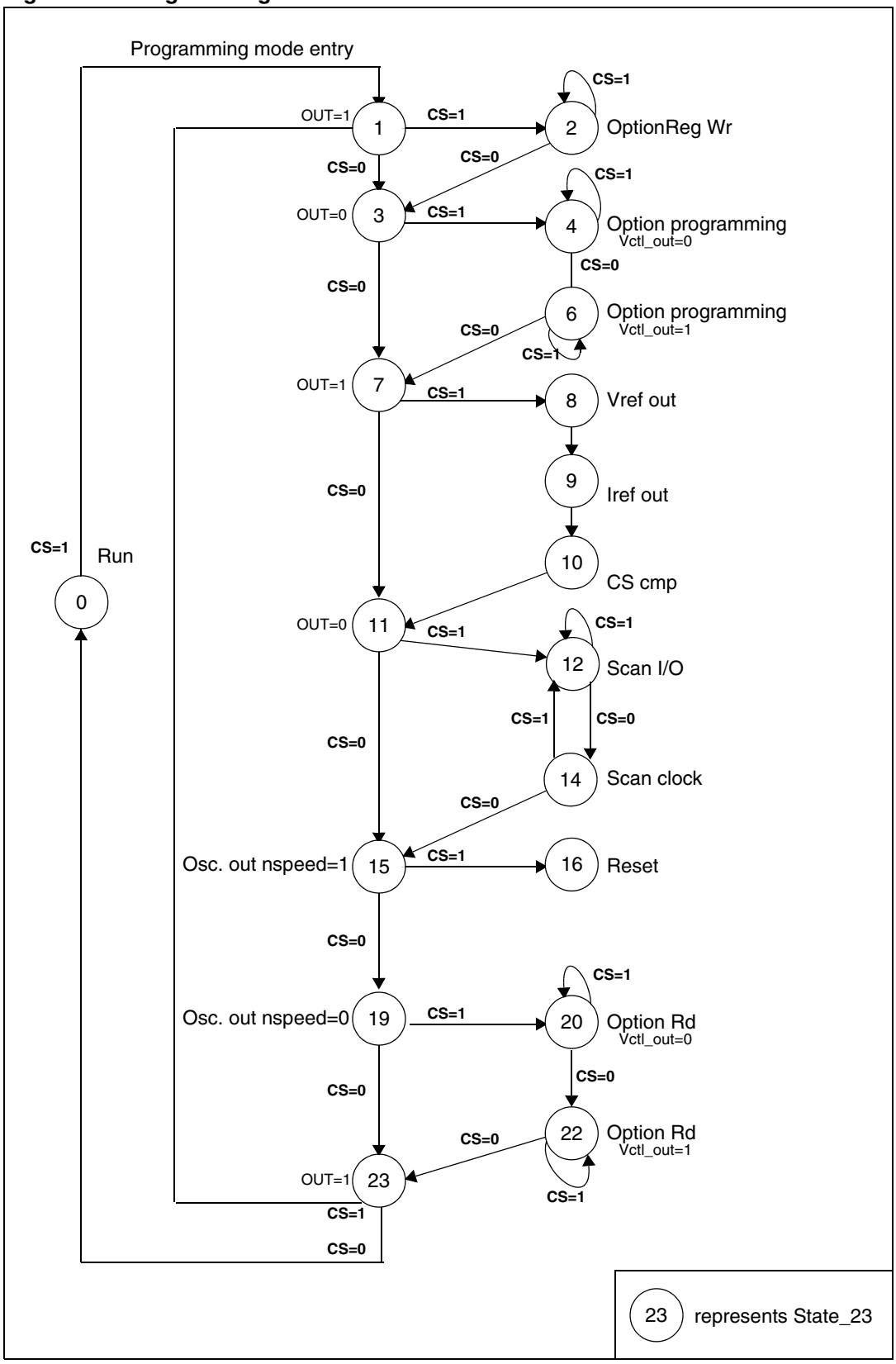
Step	Action	Explanation
1.	CX - 3 double clock	Clock IC until it is in State_19 (with CS still low).
2.	CS = HIGH	CS = 1 required for transition from State_19 to State_20.
3.	CX - 1 double clock	Clock IC into State_20.
4.	CX - 1 double clock	The IC place option_0 value on OUT.
5.	Read option on OUT	Option value is now available on OUT pin.
6.	Repeat Steps 4 and 5 for all 16 options.	Each option's value is clocked out - one after another.

Note: The 'Low' level of Steps 4 and 5 during programming are not absolutely mandatory. They could be 'High' if it is easier for the electronic command; provided they have the correct level for the next state transition.

Table 8. Option verify (State_22)

Step	Action	Explanation
1.	CS = LOW	CS = 0 required for transition from State_20 to State_22.
2.	CX - 1 double clock	Clock IC into State_22.
3.	CS = HIGH	CS = 1 required to remain in State_22 while reading options.
4.	CX - 1 double clock	The IC place option_0 value on OUT.
5.	Read option on OUT	Option value is now available on OUT pin.
6.	Repeat Steps 4 and 5 for all options.	Each option's value is clocked out - one after another.
7.	IC power OFF	VDD = 0 V

Figure 4. Programming mode finite state machine



4 Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Oct-2009	1	Initial release.
23-Nov-2009	2	Changed VDD tolerance.
16-May-2011	3	Added note after *Table 5: Option programming (State_4) on page 8* and *Table 7: Option verify (State_20) on page 10*.