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WHAT DESIGNERS SHOULD KNOW ABOUT DATA CONVERTER DRIFT

Understanding the Components of Worst-Case Degradation Can Help in Avoiding Overspecification

Exactly how inaccurate will a change in temperature make an analog-to-digital or digital-to-analog converter? As designers are well aware, a 12-bit device may provide a much lower accuracy at its operating-temperature extremes, perhaps only to 9 or even 8 bits. But for lack of more precise knowledge, many play it safe (and expensive) and overspecify.

Yet it is fairly simple to determine a converter's absolute worst-case degradation from its various drift specifications. Considering these specifications separately and examining their bases will help to unravel the labyrinth of converter drift and show how to go about calculating the actual worst-case drift error for most devices.

Accuracy drift for a D/A converter or a successive-approximation A/D converter has three primary components: its gain, offset, and nonlinearity temperature coefficients. Instead of calling out the gain and offset drifts separately, some manufacturers specify a full-scale drift, which takes both into account. Another important specification in many applications is differential nonlinearity, which reflects the equality (or rather, the inequality) of the analog steps between adjacent digital codes. But, since this parameter is really describing only the distribution of the linearity error, its temperature coefficient does not contribute to the converter's worst-case accuracy drift.

EXAMINING THE COMPONENTS OF DRIFT

The transfer function of a D/A converter will illustrate how the different kinds of drift degrade accuracy.

In a bipolar D/A converter, which produces both positive and negative analog voltages, offset drift changes all the output voltages by an equal amount, moving the entire transfer function up or down from the ideal in parallel to it (Figure 1a). The drift of the converter's voltage reference is the main cause of this error—which may also be called the minus-full-scale drift, since it occurs even when all the input bits are logic 0 or off. In a unipolar unit, the offset drift is usually much smaller, being due mostly to drift in the offset voltage of the output operational amplifier and secondarily to leakage in the current switches.

Unlike offset drift, gain drift rotates the transfer function (Figure 1b). In a bipolar unit it does so around minus full scale (all bits off), and in a unipolar unit it does so around zero (again all bits off). The gain drift affects each output voltage by the same percentage (not the same amount), tipping the transfer function at an angle to the ideal. In general, about 70% of this drift is caused by the drift of the converter's voltage reference.

Obviously, then, reference drift is a major contributor to total inaccuracy due to gain and offset drift. A positive temperature coefficient for the reference causes the transfer function to rotate about zero, as shown in Figure 1c for a bipolar converter. Since the gain and bipolar offset drifts due to the reference will always be opposite in direction, the worst-case accuracy drift may be less than half the sum of the individual drift specifications. In a unipolar converter, the gain and offset drifts may well add together, but the unipolar offset drift is usually insignificant compared to the magnitude of the gain drift, so it is not so important a factor.

Full-scale drift describes the change in the output voltage when all bits are on. For a unipolar converter, it is simply the sum of the offset and gain drifts. In contrast, for a bipolar converter, the full-scale drift is the sum of half the reference drift, the gain drift exclusive of the reference, and the offset drift exclusive of the reference.

POOR TRACKING CAUSES LINEARITY DRIFT

Finally, linearity drift reflects the shift in the analog output voltage from the straight line drawn between the output value when all the bits are off (minus full scale) and the output value when all the bits are on (plus full scale). This error is caused by the varying temperature coefficients of the ratio resistances of the converter's current-weighting (scaling) resistor, as well as the ratio drifts of the base-emitter voltages and betas of its transistor current switches.

Since the change in linearity with temperature depends on how closely various parameters track each other, and not on absolute parameters values, it is fairly easy to control with present-day hybrid and monolithic technologies. As a result, linearity drift is usually much smaller than either the gain or offset drift. Moreover, it is generally guaranteed to be within some maximum limit over the converter's full operating temperature range.

Another specification that is important in some applications is bipolar zero drift, which reflects the change in the output voltage of a bipolar converter at midscale, when only the most significant bit is on and all other bits are off. This drift error at zero is not affected by reference drift at all, but is caused mainly by poor tracking in the converter's scaling resistors and current switches. Therefore, it appears as a

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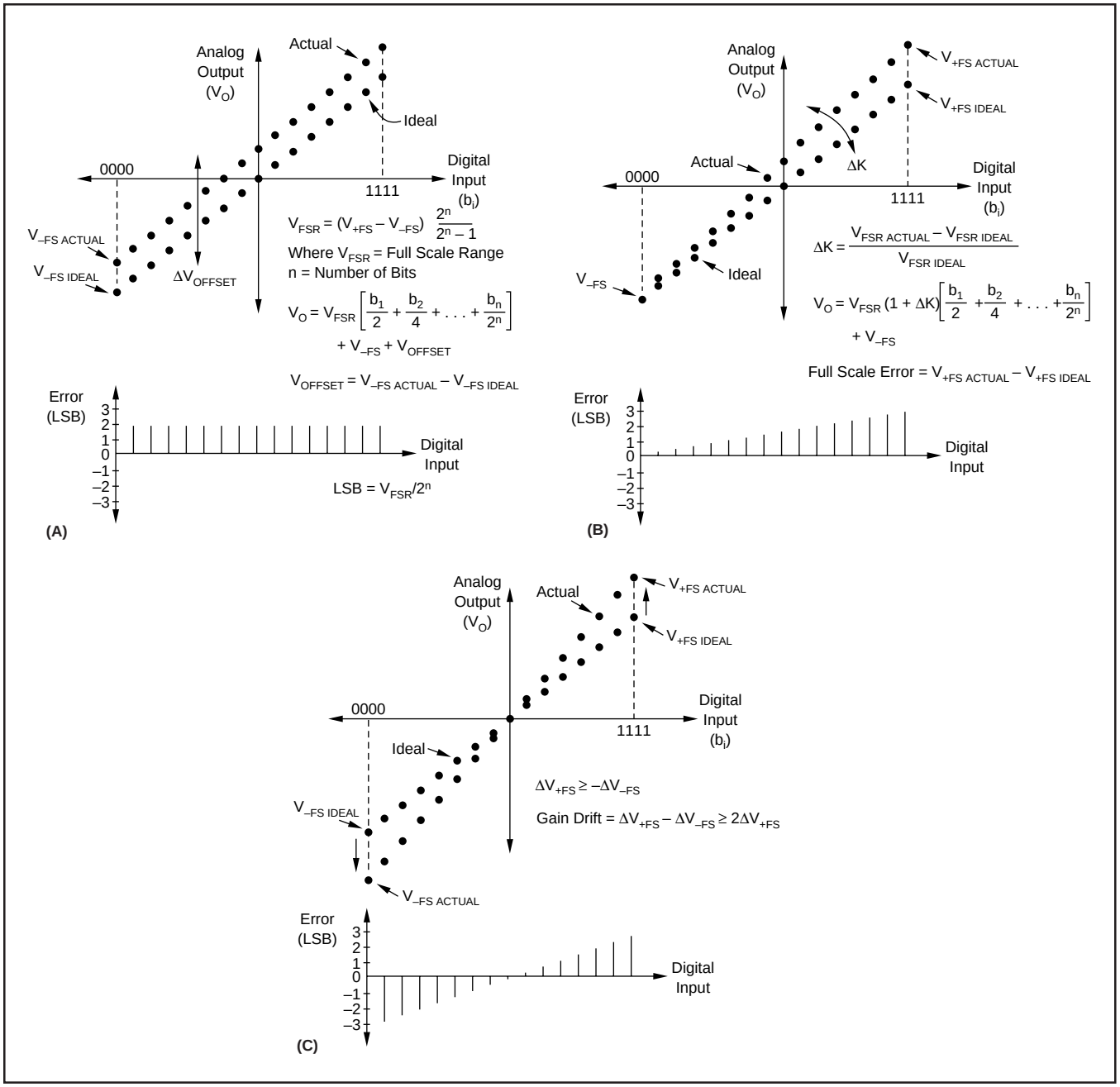

FIGURE 1. Effects of Drift. For a bipolar D/A converter, offset drift (a) moves the unit's transfer function up or down, whereas gain drift (b) rotates is about digital zero. Both of these errors are chiefly due to reference drift (c), which causes a rotation about analog zero.

random variation about zero, and it has a worst-case magnitude equal to the offset drift exclusive of the reference plus half the gain drift exclusive of the reference.

To understand more fully how these drift errors are generated, consider the simplified schematic (Figure 2) of a typical 12-bit bipolar D/A converter. Circuit operation is fairly simple. The reference current flows through reference transistor Q_C, producing a voltage drop across resistor R_C. Since the base of Q_C is connected to the bases of all the other transistor current switches, the same potential is also generated across resistors R_1 through R_{12}. The multiple emitters of the transistors cause current density to be the same for each of these binarily weighted current sources, thereby providing good matching and tracking of the transistors' V_{BE} and β.

TRACKING ERRORS TEND TO CANCEL

Now suppose that, because of temperature or aging, the value of every resistor on network RN_1 increases by 1%. Since the reference current remains constant, the voltage across these resistors also increases by 1%, so the output current and the output voltage are unchanged. If, instead, the value of all the resistors on network RN_2 increase by 1%, the

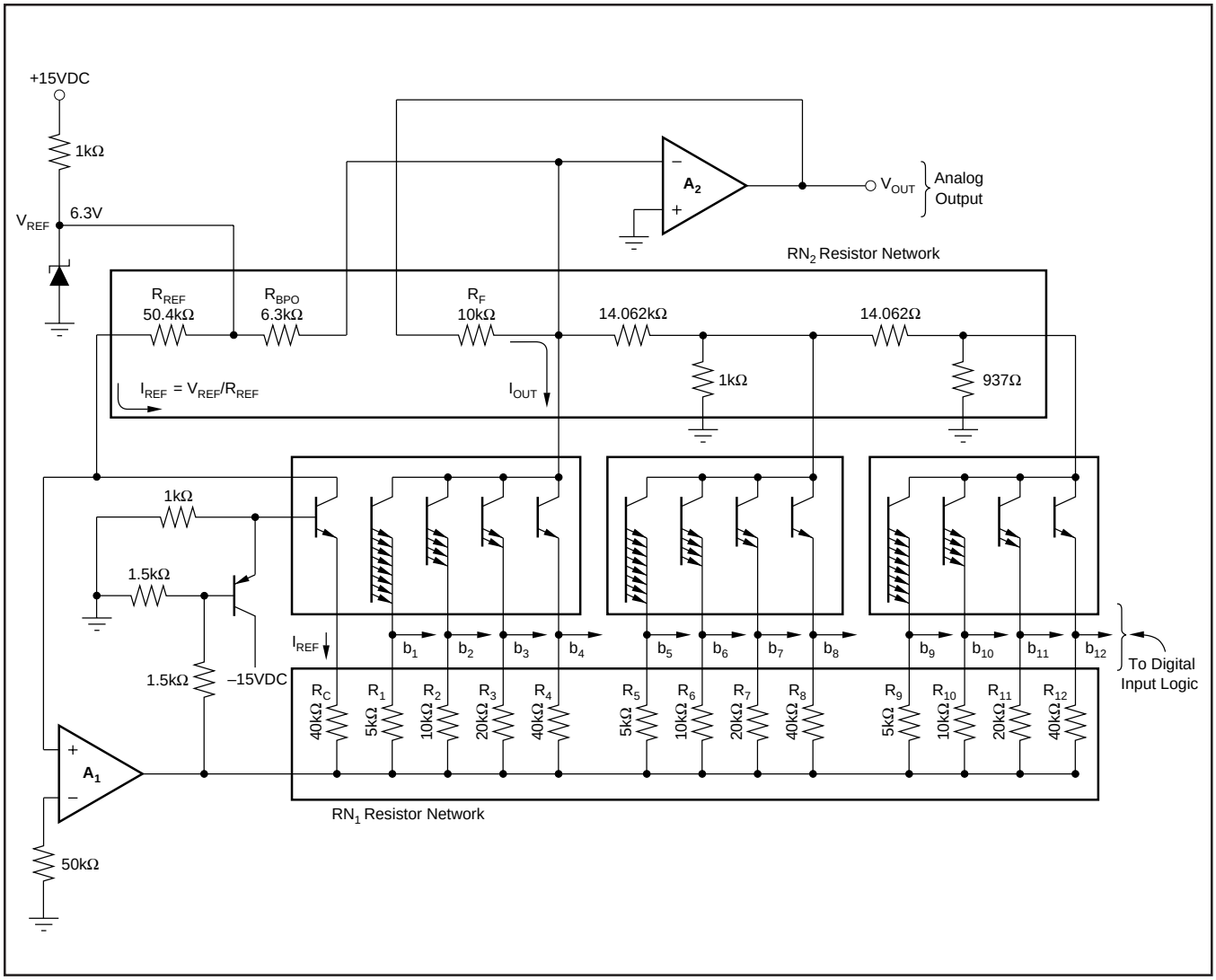

FIGURE 2. Typical D/A Circuit. In general, the circuit design for a D/A converter largely compensates for tracking errors in the resistor networks and transistor current switches. By far the dominant error source is the drift of the zener diode that makes up the reference.

reference current decreases by 1%, reducing the voltage across R_C by 1% and causing the output current to drop by 1%. However, since the value of the feedback resistor, R_F is now 1% higher, the output voltage, which is equal to $I_{OUT}R_F$, does not change.

The converter compensates for variations in the transistor V_{BE} and β in the same manner. Although the individual resistors on RN_1 and RN_2 may have temperature coefficients as high as ±50 parts per million per degree Celsius, the tracking of these resistors, and therefore their contribution to drift in linearity and gains, is typically as little as 1 to 2 ppm/°C. In fact, the only error sources for which the circuit does not compensate are the drifts in offset voltage and offset current of amplifiers, A_1 and A_2, as well as the drift of the zener reference diode. By far, the dominant error source is the drift of this zener, while the offsets of A_1 contribute to the gain drift exclusive of the reference, and the offsets of A_2 contribute to offset drift exclusive of the reference.

THE EFFECT OF REFERENCE DRIFT

To evaluate the effect of variations in the reference voltage on the overall accuracy of the converter requires determining the variation in output voltage for a change in ambient temperature. A good first-order approximation is to assume that all other drift errors — those due to tracking errors and random variations — are zero.

Writing the node equation for the summing junction at the inverting input of amplifier A_2 yields:

$$\frac{V_{OUT}}{R_F} + \frac{V_{REF}}{R_{BPO}} - \frac{V_{REF}}{R_{REF}} K\left[\frac{b_1}{2} + \frac{b_2}{4} + \ldots + \frac{b_n}{2^n}\right] = 0$$

where K is a gain constant, and b_1 through b_n represent the digital bits, which are either 1 or 0, depending on whether a bit is on or off. This equation may be used to determine the output voltage for any digital input.

At minus full scale, with $B_1 = b_2 ... = b_n = 0$, the output voltage becomes:

$$V_{OUT} = V_{-FS} = -\left[\frac{R_F}{R_{BPO}}\right]V_{REF}$$

At bipolar zero ($b_1 = 1$, $b_2 = b_3 = ... = b_n = 0$), the output voltage for an ideal converter is equal to zero:

$$V_{OUT} = V_{BPZ} = 0 = \left[\frac{R_F}{2R_{REF}}K - \frac{R_F}{R_{BPO}}\right]V_{REF}$$

At plus full scale, with $b_1 = b_2 = ... = b_n = 1$, the output voltage becomes:

$$V_{OUT} = V_{+FS} = \left[\frac{R_F}{R_{REF}}K - \frac{R_F}{R_{BPO}}\right]V_{REF}$$

Solving the equation for V_{BPZ} for gain constant K yields:

$$K = \frac{R_F}{R_{BPO}}\frac{2R_{REF}}{R_F} = \frac{2R_{REF}}{R_{BPO}}$$

Substituting this expression for K in the appropriate equations, the variation in output voltage for a change in reference caused by temperature may be computed. At minus full scale, this drift is:

$$\frac{\Delta V_{-FS}}{\Delta T} = -\frac{R_F}{R_{BPO}}\frac{\Delta V_{REF}}{\Delta T}$$

where ΔT is the change in ambient temperature. As mentioned previously, drift error at midscale is caused by tracking errors, not by variations in the reference, so:

$$\frac{\Delta V_{BPZ}}{\Delta T} = 0$$

At plus full scale, the change in the output becomes:

$$\frac{\Delta V_{+FS}}{\Delta T} = \frac{R_F}{R_{BPO}}\quad\frac{\Delta V_{REF}}{\Delta T}$$

Therefore, the drift in the output voltage due to reference variations at minus full scale (or the bipolar offset drift) will be equal in magnitude but opposite in direction to that at plus full scale. Each of these drift errors amounts to half the reference drift. The gain drift due to reference variations may be written as:

$$\left(\Delta V_{+FS} - \Delta V_{-FS}\right) / \Delta T$$

which is equal to the reference drift. It should be noted that the gain and reference drifts are specified in ppm/°C, while the full-scale and offset drifts are in ppm of full-scale range (FSR) per °C.

COMPUTING THE WORST-CASE ERROR

These results may now be used to find the worst-case total accuracy drift error for the typical converter of Figure 2. Suppose the maximum temperature coefficient of the device's internal reference is ±20ppm/°C, resulting in a gain drift of ±20ppm/°C, a plus-full-scale drift of ±10ppm of FSR/°C, and a bipolar offset drift of ±10 ppm of FSR/°C. The maximum gain drift exclusive of the reference is ±10ppm/°C, and the offset drift exclusive of the reference is ±5ppm of FSR/°C.

The worst-case error occurs at plus full scale. To compute it, the errors due to the reference as well as those exclusive of the reference that are due to random variations must be taken into account. Therefore, the only contributors to the worst-case full-scale accuracy drift are the plus-full-scale drift due to the reference, and the random errors of the offset drift and the gain drift exclusive of the reference. Summing these together yields a worst-case full-scale accuracy drift of ±25ppm of FSR/°C or ± 0.0025% of FSR/°C.

The converter is a 12-bit device having a linearity error of ±1/2 least significant bit, or ±0.01%. Also, for its operating temperature range of 0°C to 70°C, the maximum excursion from room temperature (25°C) will be 45°C. Assuming that gain and offset errors are adjusted to zero at room temperature, the total accuracy error may be computed as the sum of the linearity error and the full-scale accuracy error:

worst-case total accuracy error = (linearity error)
+ (full-scale accuracy error)
= (±0.01%) + (±0.0025%/°C) (45°C)
= ±0.12%

which is about 9-bit accuracy. The accuracy for many 12-bit D/A converters will typically be twice as good as this with most devices providing 10-bit accuracy.

All of the drift relationships and causes examined in this article also apply to a successive-approximation A/D converter, which uses a D/A converter as one if its circuit blocks, as shown in Figure 3. In the equations, simply substitute V_{IN} for V_{OUT} and R_{IN} for R_F. Also, in the A/D converter, comparator drift, rather than op amp drift, contributes to the device's unipolar offset drift.

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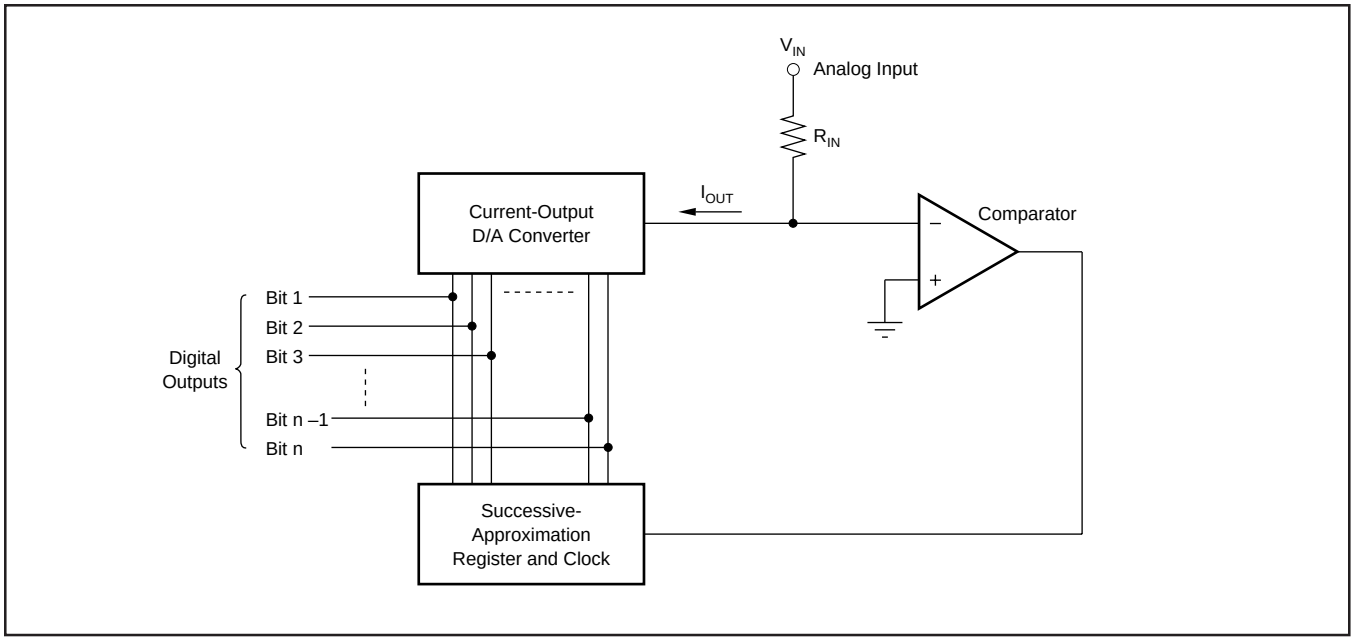

FIGURE 3. A/D Converter. All of the relationships that apply to the drift errors in a D/A converter also hold for a successive approximation A/D converter, since this component includes a current-output D/A converter as one of its circuit blocks, as shown here.

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