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APPLICATION BULLETIN
Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX (602) 889-1510 • Immediate Product Info: (800) 548-6132

PRINCIPLES OF DATA ACQUISITION AND CONVERSION

Data acquisition and conversion systems are used to acquire analog signals from one or more sources and convert these signals into digital form for analysis or transmission by end devices such as digital computers, recorders, or communications networks. The analog signal inputs to data acquisition systems are most often generated from sensors and transducers which convert real-world parameters such as pressure, temperature, stress or strain, flow, etc., into equivalent electrical signals. The electrically equivalent signals are then converted by the data acquisition system and are then utilized by the end devices in digital form. The ability of the electronic system to preserve signal accuracy and integrity is the main measure of the quality of the system.

The basic components required for the acquisition and conversion of analog signals into equivalent digital form are the following:

1. Analog Multiplexer and Signal Conditioning
2. Sample/Hold Amplifier
3. Analog-to-Digital Converter
4. Timing or Sequence Logic

Typically, today's data acquisition systems contain all the elements needed for data acquisition and conversion, except perhaps, for input filtering and signal conditioning prior to analog multiplexing. The analog signals are time multiplexed by the analog multiplier; the multiplexer output signal is then usually applied to a very-linear fast-settling differential amplifier and/or to a fast-settling low aperture sample/hold. The sample/hold is programmed to acquire and hold each multiplexed data sample which is converted into digital form by an A/D converter. The converted sample is then presented at the output of the A/D converter in parallel and serial digital form for further processing by the end devices.

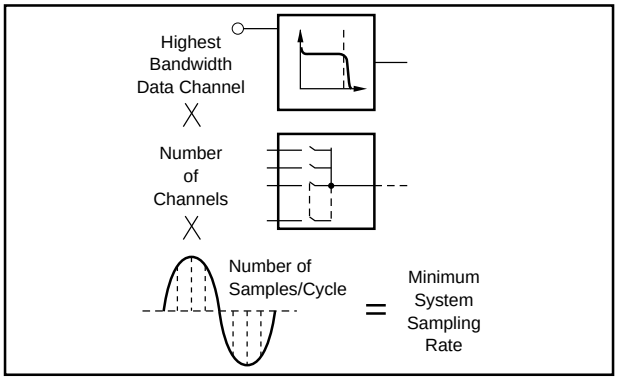

FIGURE 1. Determining Minimum System Sampling Rate.

SYSTEM SAMPLING RATE —

Error Considerations

The application and ultimate use of the converted data determines the required sampling and conversion rate of the data acquisition and conversion system. System sampling rate is determined, as shown in Figure 1, by the highest bandwidth channel, the number of data channels and the number of samples per cycle.

Aliasing Error

From the Nyquist sampling theorem, a minimum of two samples per cycle of the data bandwidth is required in an ideal sampled data system to reproduce sampled data with no loss of information. Thus, the first consideration for determining system sampling rate is aliasing error, i.e., errors due to information being lost by not taking a sufficient number of samples per cycle of signal frequency.

Figure 2 illustrates aliasing error caused from an insufficient number of samples per cycle of data bandwidth.

How Many Samples per Cycle?

The answer to this question depends on the allowable average error tolerance, the method of reconstruction (if any), and the end use of the data. Regardless of the end use, the actual error of the discrete data samples will be equal to the throughput error of the data acquisition and conversion system plus any digital errors contributed by a digital computer or other digital end device.

For incremental devices such as stepping motors and switches, the average error of sampled digital data is not as important

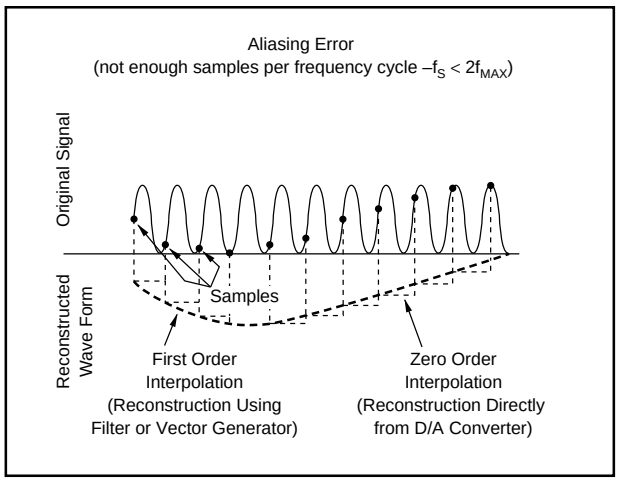

FIGURE 2. Aliasing Error vs Sampling Rate.

Printed in U.S.A. May, 1994

as it is for end devices that require continuous control signals. To illustrate average sampling error in sampled data systems, consider the case where the minimum of 2 samples per cycle of sinusoidal data are taken, and the data is reconstructed directly from an unfiltered D/A converter (zero-order reconstruction). The average error between the reconstructed data and the original signal is one-half the difference in area for one-half cycle divided by π, or 32% for zero order data, and 14% for first order reconstruction. However, the instantaneous accuracy at each sample point is equal to the accuracy of the acquisition and conversion system, and in many applications, this may be sufficient for driving band-limited end devices. The average accuracy of sampled data can be improved by (1) increasing the number of samples per cycle; (2) presample filtering prior to multiplexing, or (3) filtering the D/A converter output.

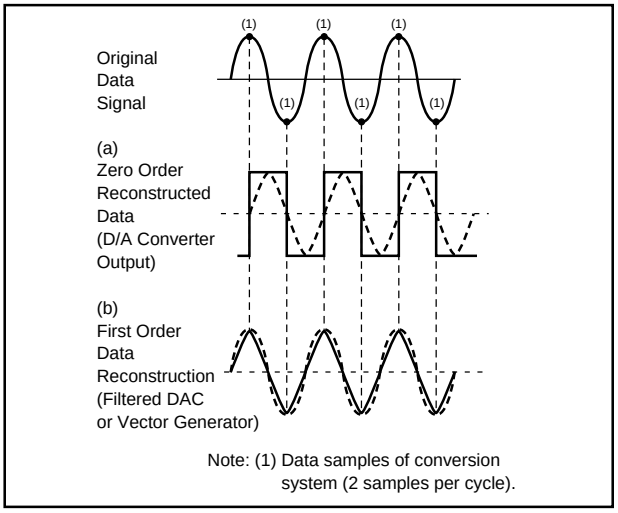

FIGURE 3. Reconstruction of Sampled Data Where $f_S = 2f_{MAX}$.

The improvement in average accuracy of sampled data is dramatic with only a slight increase in the number of samples per cycle as shown in Figure 4. The theoretical limit is the throughput accuracy of the acquisition and conversion system for continuous sampling.

For zero order reconstruction of data, it can be seen from Figure 4 that more than 10 samples per cycle of data bandwidth are required to reconstruct sampled data to average accuracies of 90% or better. A commonly used range is 7 to 10 samples per cycle.

Aperture Error

Aperture error is defined as the amplitude and time errors of the sampled data points due to the uncertainty of the dynamic data changes during sampling. In data acquisition and conversion systems, aperture error can be reduced or made insignificant either by the use of a sample/hold or with a very fast A/D converter.

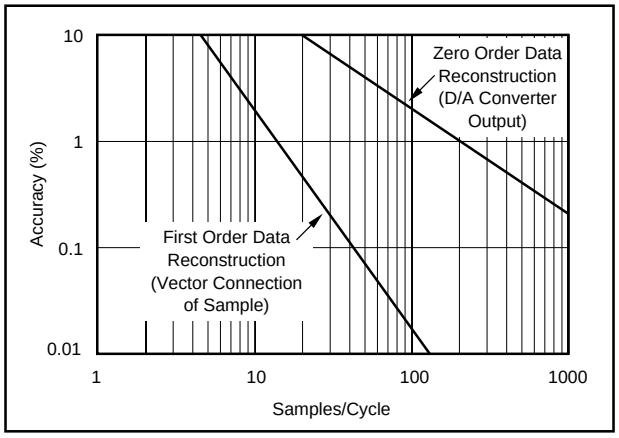

FIGURE 4. Reconstruction Accuracy vs Number of Samples Per Cycle.

For sinusoidal data, maximum aperture error occurs at the zero crossing where the greatest dv/dt occurs, and is expressed mathematically as:

$$\text{Aperture Error} = d\left(\frac{A \sin 2\pi ft}{dt}\right) \times t_A \times 100\%$$

$$= 2\pi f t_A \times 100\% \text{ max}$$

where f = maximum data frequency

t_A = aperture time of system (This can be the conversion time of the A/D converter with no sample/hold, or the aperture time of a sample/hold if one is in front of an A/D converter).

This expression is shown graphically in Figure 5 for frequencies of 1Hz to 10kHz with ±1/2LSB error highlighted for 8-, 10- and 12-bit resolution A/D converters. The need for a sample/hold becomes readily apparent when data frequencies of 10Hz or higher are sampled, because the A/D converter conversion speed must be 2µs or faster for aperture errors less than ±l/2LSB for l2-bit resolution, and high speed A/D converters are complicated and expensive when compared to slower A/D converters with a low aperture sample/hold.

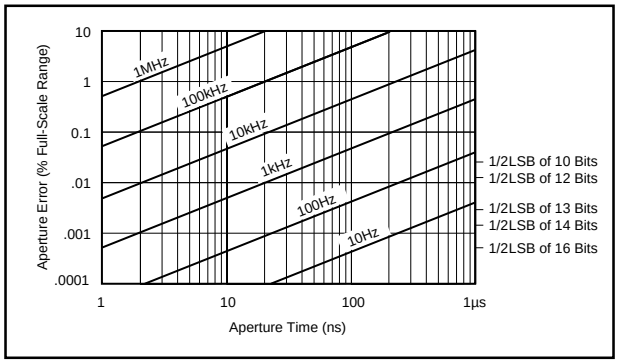

FIGURE 5. Aperture Error vs Aperture Time for Data Frequencies from 10Hz to 1MHz.

A sample/ hold with an aperture time of 50ns to 60ns produces negligible aperture error for data frequencies up to 100Hz for 10- and 12-bit resolution A/ D converters, and is less than ±1/2LSB for 8-bit resolution for data frequencies near 5kHz. Use Figure 5 to determine your system aperture error for each data channel versus the desired resolution

A FEW A/D CONVERTER POINTS

A brief discussion of A/D converter terminology will help the reader understand system resolution and accuracy a little better.

Accuracy

All analog values are presumed to exist at the input to the A/D converter. The A/D converter quantizes or encodes specific values of the analog input into equivalent digital codes as an output. These digital codes have an inherent uncertainty or *quantization error* of ±1/2LSB. That is, the quantized digital code represents an analog voltage that can be anywhere within ±1/2LSB from the mid-point between adjacent digital codes. An A/D converter can never be more accurate than the inherant ±1/2LSB quantizing error. Analog errors such as gain, offset, and linearity errors also affect A/D converter accuracy. Usually, gain and offset errors can be trimmed to zero, but *linearity error* is unadjustable because it is caused by the fixed-value ladder resistor network and network switch matching. Most quality A/D converters have less than ±1/2LSB linearity error. Another major error consideration is *differential linearity error*. The size of steps between adjacent transition points in an *ideal* A/D converter is one LSB. Differential linearity error is the difference between adjacent transition points in an actual A/D converter and an ideal one LSB step. This error must be less than one LSB in order to guarantee that there are no missing codes. An A/D converter with ±1/2LSB linearity error does not necessarily imply that there are no missing codes.

Selecting the Resolution

The number of bits in the A/D converter determines the resolution of the system. System resolution is determined by the channel(s) having the widest dynamic range and/or the channel(s) that require measurement of the smallest data increment. For example, assume a channel that measures pressure has a dynamic range of 4000psi that must be measured to the nearest pound. This will require an A/D converter with a minimum resolution of 4000 digital codes. A 12-bit A/D converter will provide a resolution of 2^{12} or 4096 codes—adequate for this requirement. The actual resolution of this channel will be 4000/4096 or 0.976 psi.

The A/D converter can resolve this measurement to within ±0.488 psi (±1/2LSB).

Resolution

The number of bits in an A/D converter determines the resolution of the data acquisition system. A/D converter resolution is defined as:

$$\text{Resolution} = \text{One LSB} = \frac{V_{FSR}}{2^n}, \text{ for binary A/D converters}$$

$$= \frac{V_{FSR}}{10^D}, \text{ for decimal A/D converters}$$

LSB = Least Significant Bit

V_{FSR} = Full Scale Input Voltage Range

where n = number of bits

D = numbers of decimal digits

The number of bits defines the number of digital codes and is 2^n discrete digital codes for A/D converters.

For this discussion, we will use binary successive-approximation A/D converters. Table I shows resolutions and LSB values for typical A/D converters.

A/D Converter Resolution (Binary Code)		Value of 1LSB		Value of 1/2LSB	
Number of Bits (n)	Number Of Increments (2^n)	0 to +10V Range (mV)	+10V Range (mV)	0 to +10V Range (mV)	+10V Range (mV)
16	65536	0.152	0.305	0.076	0.152
12	4096	2.44	4.88	1.22	2.44
11	2048	4.88	9.77	2.44	4.88
10	1024	9.77	19.5	4.88	9.77
9	512	19.5	39.1	9.77	19.5
8	256	39.1	78.2	19.5	39.1

TABLE I. Relationship of A/D Converter LSB Values and Resolutions for Binary Codes.

INCREASING SYSTEM THROUGHPUT RATE

The throughput rate of the system is determined by the settling times required in the analog multiplexer and input amplifier, sample/hold acquisition time and A/D converter settling and conversion time.

Two programming modes that are commonly used in data acquisition systems are normal serial programming (Figure 6a) and overlap mode programming (Figure 6b). The range of typical system throughput rates for these types of modes are shown in Table II for the Burr-Brown SDM857KG modular data acquisition systems.

A wide range of throughput speeds can be achieved by “short cycling” the A/D converter to lower resolutions and by overlap programming the data acquisition system.

The multiplexer and amplifier settling time is eliminated by selecting the next sample (channel n + 1) while the held sample (channel n) is being converted. This requires a sample/hold with very low feed-through error.

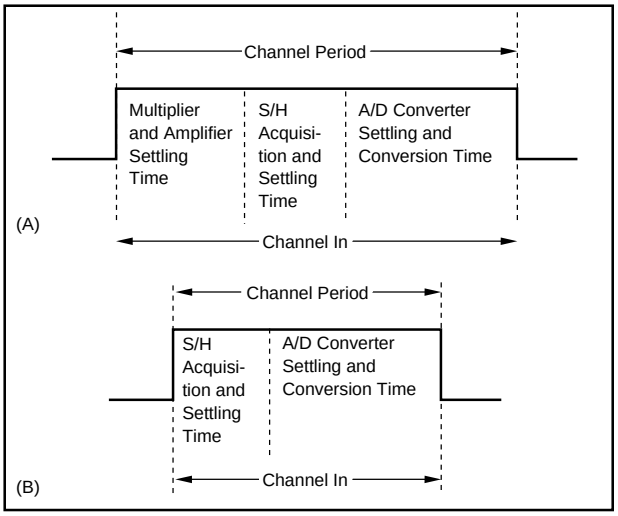

FIGURE 6a. System Throughput Rate-Signal Programming and, 6b, System Throughput Rate-Overlap Mode.

Resolution	NORMAL PROGRAMMING		OVERLAP MODE	
	Max System Throughput Rate	RSS Accuracy	Max System Throughput Rate	RSS Accuracy
12 Bits	18kHz	0.025%	27kHz	0.025%
10 Bits	19.5kHz	0.08%	30kHz	0.08%
8 Bits	21.1kHz	0.30%	34.1kHz	0.30%

TABLE II. System Throughput Rates and RSS Accuracy for Normal and Overlap Mode Programming for Burr-Brown Model SDM857KG Modular Data Acquisition System.

SYSTEM THROUGHPUT ACCURACY

The most common method used to describe data acquisition and conversion system accuracy is to compute the root-sum squared (RSS) errors of the system components. The RSS error is a statistical value which is equivalent to the standard deviation (1σ), and represents the square root of the sum of the squares of the peak errors of each system component, including ADC quantization error:

$$\varepsilon_{RSS} = \sqrt{\varepsilon_{MUX}^2 + \varepsilon_{AMP}^2 + \varepsilon_{SH}^2 + \varepsilon_{ADC}^2}$$

where ε_{MUX} = analog multiplexer error
ε_{AMP} = input amplifier error
ε_{SH} = sample/hold error
ε_{ADC} = A/D converter error

The source irnpedance, data bandwidth, A/D converter resolution and system throughput rate affect these error calculations. To simplify, errors can be calculated by assuming the following:

1. Aperture error is negligible - i.e., less than 1/10LSB.
2. Source impedance is less than 1000Ω.
3. Signal range is ±10 volts.
4. Throughput rate is equal to or less than the maximum shown in Table III.

Error Source	RESOLUTIONS		
	8 Bits	10 Bits	12 Bits
MUX Error	0.0025%	0.0025%	0.0025%
AMP Error	0.01%	0.01%	0.01%
S/H Error	0.01%	0.01%	0.01%
ADC Errors Analog Quantizing	 0.2% 0.2%	 0.05% 0.05%	 0.012% 0.012%
RSS Error	0.283%	0.072%	0.022%

TABLE III. System Error Contribution and RSS Error vs Resolution for Burr-Brown Model857KG Modular Data Acquisition System.

DIGITAL CODES

One final consideration in data acquisition and conversion systems is the digital coding of the data at the output of the A/D converter. Data is usually encoded in either binary or binary-coded-decimal (BCD) form.

Binary encoded data formats are most commonly employed for digital computer-oriented applications where the processing is normally performed in binary notation. BCD data encoding is usually required in applications where the data is fed to decimal end devices such as digital readouts and printers. The majority of applications require binary encoding.

The most commonly used binary codes in A/D converters are:

1. *Unipolar Straight Binary (USB)*—used for unipolar analog signal ranges, i.e., 0 to ±5V, 0 to ±10V, etc.
2. *Bipolar Offset Binary (BOB)*—used for bipolar analog signal ranges, i.e., ±5V, ±10V, etc.
3. *Bipolar Two's Complement (BTC)*—used for bipolar analog signal ranges in many digital computer applications.

Two BCD codes, unipolar BCD and sign-magnitude BCD (SMD) are used in A/D converters. The definition of these codes is shown in Table IV and V.

DEFINITION	OUTPUT DIGITAL CODE	USB CODE	BOB(2) CODE
	MSB LSB		
+Full Scale	111....11ϕ(1)	$+V_{FSR}$ –1/2LSB	$\frac{+V_{FSR}}{2}$ –1/2LSB
Mid Scale	100....00ϕ	$+V_{FSR}/2$	Zero
–Full Scale	000....00ϕ	+1/2LSB	$\frac{-V_{FSR}}{2}$ +1/2LSB
One Least Significant Bit		$\frac{V_{FSR}}{2^n}$	$\frac{\pm V_{FSR}}{2^n}$
NOTES: (1) ϕ is the transition value of the LSB. (2) BTC Code–invert the MSB (sign bit) of the digital code—ranges same as BOB codes.			

TABLE IV. Definition of Binary Codes.

DEFINITION	OUTPUT DIGITAL CODE (3 DIGITS)	DECIMAL VALUE	
		BCD CODE	SMD CODE
Sign	MSD[1] LSD		
+ Full Scale	1 1001 1001 1001	999	+999
Zero	1 0000 0000 0000	000	+000
–Full Scale	0 1001 1001 1001	N/A	–999
One Least Significant Bit		$\frac{V_{FSR}^{(2)}}{10^n}$	$\frac{\pm V_{FSR}^{(2)}}{10^n}$

NOTES: (1) MSD = Most Significat Digit. (2) n represents number of digits—4 bits per digit.

TABLE V. Definition of Decimal Codes.

SUMMARY

The criteria that determine the key parameters and performance requirements of a data acquisition and conversion system are:

1. Number of analog input channels;
2. Amplitude of data source signals;
3. Bandwidth of data;
4. Desired resolution of data; and,
5. End use of converted data.

Although this discussion did not treat all system criteria from a rigorous mathematical point of view, it does not identify and attempt to shed insight on the most important considerations from a practical viewpoint.

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