Virtex-5 FPGA Serial ATA Generation 2 Protocol Standard

Characterization Test Report

RPT087 (v1.0) November 13, 2007

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/13/07	1.0	Initial Xilinx release.

Virtex-5 FPGA Serial ATA Generation 2 Protocol Standard

Introduction

Virtex™-5 FPGA system connectivity technology delivers low-power solutions for building high-speed, high-bandwidth connections between devices, boards, and boxes. The GTP transceiver design and SelectIO™ parallel I/O technologies enable flexible bridging between existing parallel standards and emerging serial standards. The features of the GTP transceivers in Virtex-5 FPGAs include:

- Current Mode Logic (CML) drivers/buffers with configurable termination, voltage swing, and coupling
- Programmable transmit pre-emphasis and receive equalization for optimal signal integrity
- Line rates from 500 Mb/s to 3.75 Gb/s with optional 5X oversampling to reduce the low end to 100 Mb/s
- Optional built-in physical coding sublayer (PCS) features, such as 8B/10B encoding/decoding, comma alignment, channel bonding, and clock correction
- Fixed latency modes for minimized, deterministic datapath latency
- Out-of-band (OOB) signaling support, specifically designed to address the requirements of PCI Express® technology and Serial ATA protocols
- Built-in pseudorandom bitstream (PRBS) generation/checking logic for easier bit error rate (BER) checking
- A configuration wizard provided in the CORE Generator™ software and an internal bit error rate tester (IBERT) integrated into the ChipScope™ Pro analyzer tool for easy implementation of GTP transceiver interfaces

This characterization report compares the GTP transceiver electrical performance against the Serial ATA specification, revision 2.6 across process, voltage, and temperature conditions. GTP transmitter and receiver electrical characteristics were measured using lab bench setups. The methods used to characterize the transceiver are based on the standard specifications and also follow the best-practice methods for some parameters.

Background

Serial ATA (SATA) is a high-speed serial link replacement for the parallel ATA (PATA) physical storage interface. The serial link employed is a high-speed differential link that utilizes Gigabit technology and 8B/10B encoding. The advantages of the SATA interface over the PATA interface include greater speed, simpler upgradeable storage devices, and easier configuration.

This report contains the XC5VLXT device high-speed serial (GTP) transceiver characterization results for the SATA Generation 2 interface, which supports interface rates at 3 Gb/s. All measurement methods and reported parameters were conducted according to the specifications published by the Serial ATA workgroup. [Ref 1]

SATA is a layered architecture with four layers: application, transport, link, and physical. In addition, multiple usage models are defined based on the link speed and connection type as shown in Table 2, "Usage Model Descriptions" of the SATA specification, revision 2.6. This characterization report focuses only on the GTP transceiver electrical characteristics under the 3 Gb/s short backplane to device (Gen2m) usage model. Gen2m requirements are more stringent than the internal host to device cable (Gen2i) usage model with the same parameters. Thus, the results can also apply to Gen2i with extra margin. This report presents the GTP transceiver characteristics as a SATA 3 Gb/s physical layer transmitter and receiver. It does not consider the interconnect (cables and backplane) or overall system performance.

Lab Board Setup

A Xilinx ML523 evaluation board [Ref 2] with an Oztek socket hosting the FF1136 package was used to test the Virtex-5 devices. The devices chosen for characterization covered the process corner materials. Two devices were used from each process corner: slow, typical, and fast. Test samples were subjected to different extreme operating conditions including temperature and voltage variations. Table 1 and Table 2 summarize the test supply voltages and test temperatures, respectively.

Table 1: **Test Supply Voltages**

Voltage Conditions	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTRX (V)	MGTAVTTTX (V)	V_{CCO} (V)	V_{CCAUX} (V)	V_{CCINT} (V)
V_{MIN}	0.95	1.14	1.14	1.14	2.38	2.38	0.95
V_{NOM}	1.0	1.20	1.20	1.20	2.5	2.5	1.0
V_{MAX}	1.05	1.26	1.26	1.26	2.63	2.63	1.05

Table 2: **Test Temperatures**

Condition	Temperature (°C)
T_{MAX}	100
T_{ROOM}	25
T_{MIN}	–40

All tests were performed on the GTP0 transceiver at location 122 (GTP_DUAL_X0Y0). Reference clock inputs were driven from location 122 (MGTREFCLK_122). A 150 MHz reference clock frequency generated from an HP 81130A pulse data generator was provided to the GTP transceiver through two SMA cables and two DC blocks. The receiver equalizer and transmitter amplitude booster were both switched off. Spread spectrum clocking (SSC) was also disabled during the transmitter and receiver tests. Refer to "Spread Spectrum Clocking," page 26 for more details. For a complete listing of all the equipment used in this characterization, refer to "Appendix B: Test Equipment," page 32.

The four test categories were receiver tolerance testing, transmitted signal requirements, OOB transmit and receive testing, and spread spectrum clocking. The transmitter and receiver were tested individually for compliance testing. The transmitter consists of the

driver, printed circuit board, and mated connector pair. The receiver consists of the receiver IC, printed circuit board, and mated connector pair.

SATA Connector Fixture

All SATA Gen2m parameters require the use of mated SATA connectors as part of the interconnect. A pair of SMA-SATA connector fixtures from Crescent Heart Software were employed to fulfill this requirement. Figure 1 and Figure 2 show the SATA near-end and far-end test fixtures, respectively. The SATA connector ends were connected to form the specified mated connector during all tests.

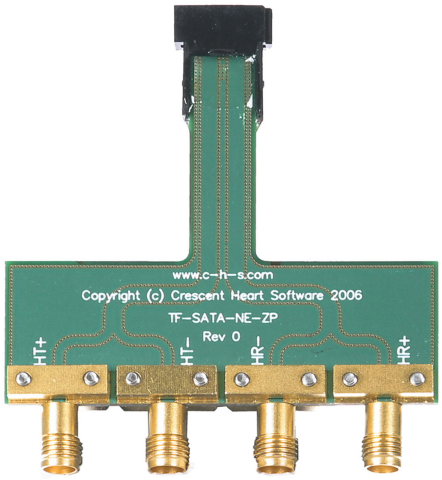

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Figure 1: **Near-End SATA Test Fixture**

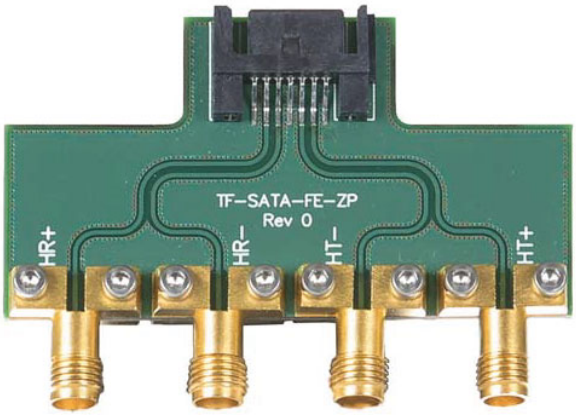

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Figure 2: **Far-End SATA Test Fixture**

Figure 3 shows the complete lab equipment setup for this characterization.

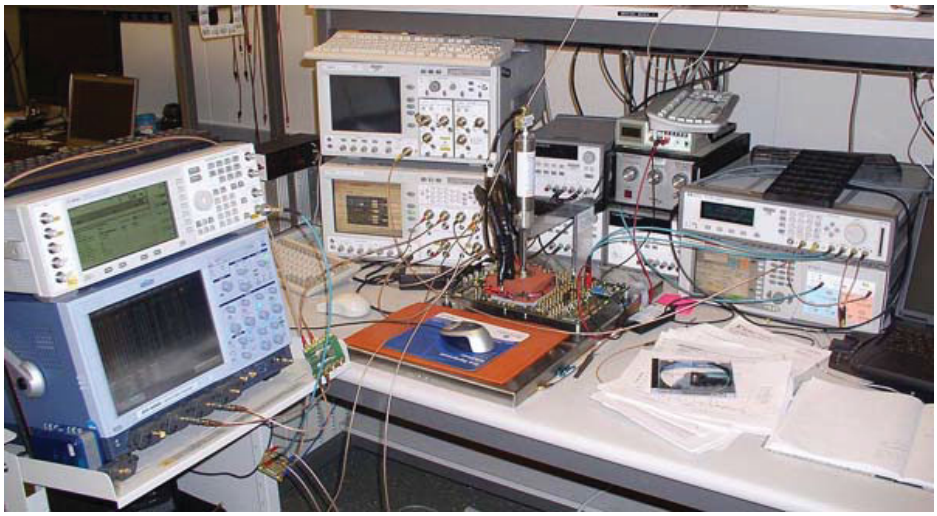

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Figure 3: **Lab Equipment Setup**

Summary of Results

Table 3 summarizes the SATA Gen2m transmitter parameters in the SATA specification and the test results of the GTP transceiver.

Table 3: **Summary of SATA 3 Gb/s Transmitter Test Results**

Parameters	Limit	Value	GTP TX Value	Units	Compliant	Comments
T_{UI} (unit interval)	Min	333.2167	333.3254	ps	Y	Spread spectrum clocking disabled
	Max	335.1167	333.3421		Y	
F_{tol} (TX frequency long-term stability)	Min	–350	–1	ppm	Y	Spread spectrum clocking disabled
	Max	350	1		Y	
V_{diffTX} (TX differential output voltage)	Min	400	435	mVpp	Y	Compliant in Gen2m model. See "TX Differential Output Voltage," page 15
	Max	700	> 700		–	
$t_{20\text{-}80TX}$ (TX rise/fall time)	Min	67 (0.20)	84 (0.25)	ps (UI)	Y	
	Max	136 (0.41)	133 (0.4)		Y	
t_{skewTX} (TX differential skew)	–	20	13	ps	Y	FPGA skew only. See "TX Differential Skew," page 18
$V_{cm, acTX}$ (AC common mode voltage)	Max	50	32	mVp-p	Y	
$D_{vdiffOOB}$ (OOB differential delta)	Max	25	15	mV	Y	
$D_{vdiffOOB}$ (OOB common mode delta)	Max	50	27	mV	Y	

Table 3: **Summary of SATA 3 Gb/s Transmitter Test Results *(Continued)***

Parameters	Limit	Value	GTP TX Value	Units	Compliant	Comments
R/F_{bal} (TX rise/fall imbalance)	Max	20	20	%	Y	
Amp_{bal} (TX amplitude imbalance)	Max	10	32	%	–	See "TX Amplitude Imbalance," page 20
TJ at Connector, Clk-Data, $f_{BAUD}/500$	Max	0.37 (123.3)	0.29 (96.63)	UI (ps)	Y	Total jitter (TJ) and deterministic jitter (DJ) at $f_{BAUD}/10$ are obsolete as stated in the SATA specification errata [Ref 3]
DJ at Connector, Clk-Data, $f_{BAUD}/500$	Max	0.19 (63.3)	0.14 (45.6)	UI (ps)	Y	

Table 4 summarizes the lab-source signal requirements for receiver tolerance listed in the SATA specification. It also shows the measured parameters of the actual lab signal used during the characterization. The GTP receiver passed the 10^{-12} BER with a 95% confidence level. The signal exceeds the limit in some parameters. Therefore, the GTP receiver performed better than the SATA receiver tolerance requirements.

Table 4: **Summary of SATA 3 Gb/s Receiver Tolerance Test Results**

Parameters	Limit	Value	GTP RX Value	Units	Compliant	Comments
V_{diffRX} (RX differential input voltage)	Min	240	240	mVppd	Y	Voltage includes interconnect.
	Max	750	1000		Y	Maximum input voltage exceeds specification.
$t_{20\text{-}80RX}$ (RX rise/fall time)	Min	67	–	ps	–	Minimum rise and fall times not covered.
	Max	136	188		Y	Test value exceeds the specification.
UI_{VminRX} (RX minimum voltage measurement interval)	–	0.5	0.5	UI	Y	
t_{skewRX} (RX differential skew)	Max	50	50	ps	Y	
$V_{cm,acRX}$ (RX AC common mode voltage)	Max	100	101	mVp-p	Y	Test value exceeds the specification.
$f_{cm,acRX}$ (RX AC common mode frequency)	Min	2	2	MHz	Y	Frequency sweeps from minimum to maximum over 20 steps. Each step lasts for 2 seconds.
	Max	200	200		Y	

Table 4: **Summary of SATA 3 Gb/s Receiver Tolerance Test Results *(Continued)***

Parameters	Limit	Value	GTP RX Value	Units	Compliant	Comments
TJ at Connector, Clk-Data, $f_{BAUD}/500$	Max	0.60	0.63	UI	Y	TJ and DJ at $f_{BAUD}/10$ are obsolete as stated in the SATA specification errata
DJ at Connector, Clk-Data, $f_{BAUD}/500$	Max	0.42	0.43	UI	Y	

Table 5 summarizes the SATA Gen2m OOB parameters shown in the SATA specification and the test results of the GTP transceiver.

Table 5: **Summary of the SATA 3 Gb/s OOB Results**

Parameters	Limit	Value	GTP Transceiver Value	Units	Compliant	Comments
V_{thresh} (OOB signal detection threshold)	Min	75	134	mVppd	Y	OOB detect threshold attribute set to 111.
	Nom	125	–		–	
	Max	200	186		Y	
COMINIT/ COMRESET and COMWAKE (transmit burst length)		106	106.3–108.0	ns	Y	Minimum and maximum values are shown.
COMINIT/ COMRESET (transmit gap length)		320	319.5–321.3	ns	Y	Minimum and maximum values are shown.
COMWAKE (transmit gap length)		106.7	106.3–108.0	ns	Y	Minimum and maximum values are shown.
COMWAKE (gap detection windows)	May detect	$35 \le T < 175$	$80 \le T \le 140$	ns	Y	Default values shown. GTP transceiver OOB detector windows were programmable.
	Shall detect	$101.3 \le T \le 112$			Y	
	Shall not detect	$T < 35$ or $T \ge 175$			Y	
COMINIT/ COMRESET (gap detection windows)	May detect	$175 \le T < 525$	$240 \le T \le 440$	ns	Y	Default values shown. GTP transceiver OOB detector windows were programmable.
	Shall detect	$304 \le T \le 336$			Y	
	Shall not detect	$T < 175$ or $T \ge 525$			Y	

Table 6 and Table 7 show the return loss versus frequency for the receiver in differential and common modes, respectively. Table 8 and Table 9 show similar data for the transmitter.

Table 6: **RX Differential Return Loss vs. Frequency**

Parameter	Limit	Value	GTP RX Value	Units	Compliant	Comments
$RL_{DD11,RX}$	150 MHz – 300 MHz	18	17	dB	–	See "Return Loss," page 28 for the distribution
	300 MHz – 600 MHz	14	14		Y	
	600 MHz – 1.2 GHz	10	10		Y	
	1.2 GHz – 2.4 GHz	8	8		Y	
	2.4 GHz – 3.0 GHz	3	8		Y	

Notes:

1. RX differential mode return loss. All values minimum.

Table 7: **RX Common Mode Return Loss vs. Frequency**

Parameter	Limit	Value	GTP RX Value	Units	Compliant	Comments
$RL_{CC11,RX}$	150 MHz – 300 MHz	5	12	dB	Y	See "Return Loss," page 28 for the distribution
	300 MHz – 600 MHz	5	11		Y	
	600 MHz – 1.2 GHz	2	9		Y	
	1.2 GHz – 2.4 GHz	1	7		Y	
	2.4 GHz – 3.0 GHz	1	7		Y	

Notes:

1. RX common mode return loss. All values minimum.

Table 8: **TX Differential Return Loss vs. Frequency**

Parameter	Limit	Value	GTP TX Value	Units	Compliant	Comments
$RL_{DD11,TX}$	150 MHz – 300 MHz	14	17	dB	Y	See "Return Loss," page 28 for the distribution
	300 MHz – 600 MHz	8	14		Y	
	600 MHz – 1.2 GHz	6	12		Y	
	1.2 GHz – 2.4 GHz	6	9		Y	
	2.4 GHz – 3.0 GHz	3	7		Y	

Notes:

1. TX differential mode return loss. All values minimum.

Table 9: **TX Common Mode Return Loss vs. Frequency**

Parameter	Limit	Value	GTP TX Value	Units	Compliant	Comments
$RL_{CC11,TX}$	150 MHz – 300 MHz	5	13	dB	Y	See "Return Loss," page 28 for the distribution
	300 MHz – 600 MHz	5	13		Y	
	600 MHz – 1.2 GHz	2	12		Y	
	1.2 GHz – 2.4 GHz	1	8		Y	
	2.4 GHz – 3.0 GHz	1	8		Y	

Notes:

1. TX common mode return loss. All values minimum.

Receiver Electrical Tests

AC Common Mode Noise Injection Board

The SATA specification requires the receiver to tolerate a sinusoidal common mode interfering signal during receiver tolerance tests. A special AC common mode noise injection board was made by Xilinx to avoid introducing signal distortion (Figure 4). For more information, refer to "AC Common Mode Noise Injection," page 12.

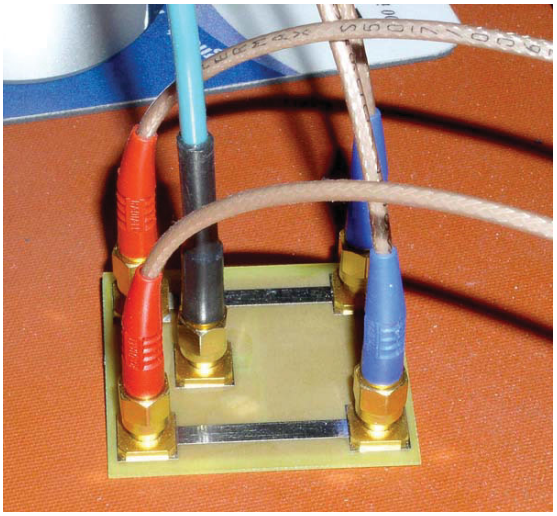

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Figure 4: **AC Common Mode Noise Injection Board**

Receiver Tolerance Test Setup

The receiver tolerance test setup is shown in Figure 5. It is based on the setup shown in the SATA specification. The Agilent BitAlyzer outputs, Data and DataB, were directly connected to the AC common mode injection board. The sinusoidal signal used to create the common mode came from an Agilent E4438C ESG vector signal generator. The AC common mode board was then connected to the test fixture CHS-TF-SATA-NE-ZP board by two short SMA cables. The CHS-TF-SATA-NE-ZP test fixture was mated with the CHS-TF-SATA-FE-ZP test fixture on the SATA connector side. The SMA side of the CHS-TF-

SATA-FE-ZP test fixture was connected to a 15-inch Xilinx quad serial loop to create the deterministic jitter.

The GTP-122 RX0 inputs (P and N) of the Virtex-5 FPGA on the ML523 board were connected to the Xilinx quad serial loop through two short SMA cables and two DC blocks. This pair of SMA cables was slightly different in length to create the differential skew needed for the tolerance tests.

The transmitter GTP-122 TX0-P output of the Virtex-5 FPGA was routed back to the DataIn of the Agilent BitAlyzer for BER testing. The GTP-122 TX0-N output was routed to a LeCroy SDA11000 serial data analyzer to be monitored.

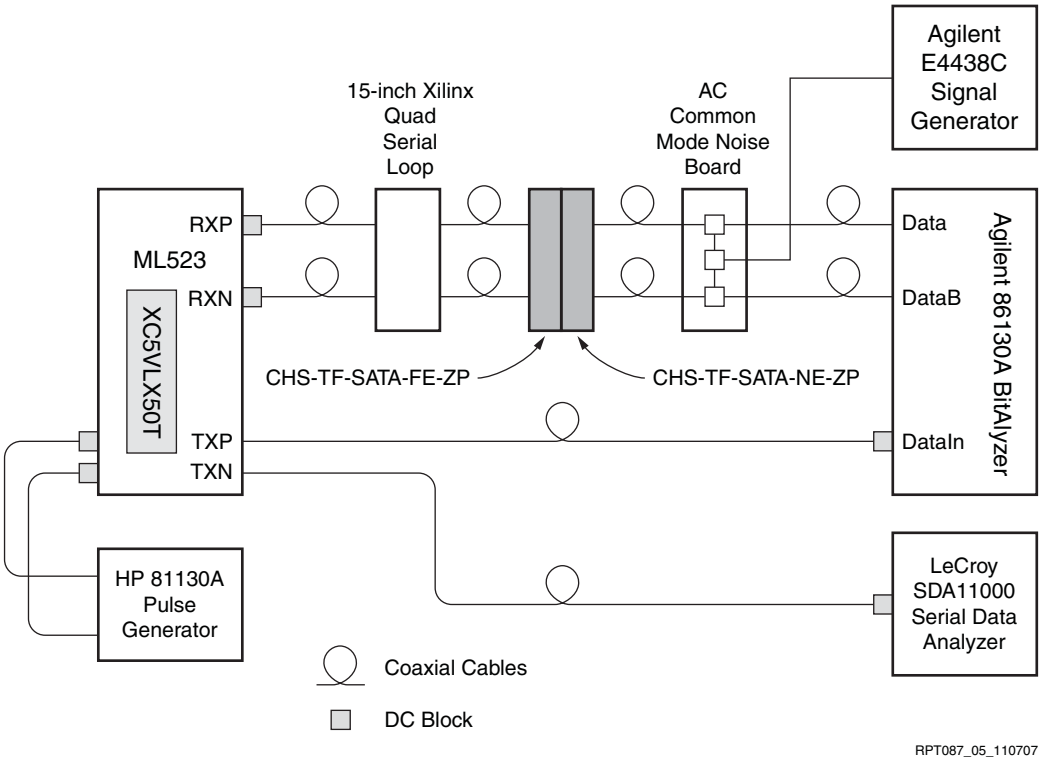

Figure 5: **Receiver Tolerance Test Setup**

Detailed Receiver Results

The signal applied to the GTP receiver is called the laboratory-sourced signal. Its source signal was generated by the Agilent BitAlyzer. The signal's rise and fall times, amplitude, differential skew, common mode, and jitter were adjusted by the BitAlyzer, cables, external source, and passive backplane to meet or exceed the receiver parameters listed in the SATA specification. The minimum rise and fall times were not tested due to limitations of the test equipment.

Receiver Tolerance Tests

During the receiver tolerance tests, the device under test was configured with the Xilinx bit-error rate tester (XBERT) design. The Agilent BitAlyzer created a long version of the composite (COMP) pattern to the GTP receiver. The received pattern was then transmitted unaltered back to the BitAlyzer through the GTP transmitter for BER calculation.

Bit Error Rate

The SATA specification states that the frame error rate (FER) is 8.2 x 10^{-8} with a 95% confidence level. However, FER is the measure of system performance including the physical layer, link layer, and transport layer. The goal of this evaluation was to measure the physical layer electrical compliance only. The FER was calculated based on a target BER of 10^{-12}. Therefore, a BER of 10^{-12} with a 95% confidence level was used as the benchmark instead.

Receiver Tolerance Confidence Level

The SATA specification recommends that the test run time be longer than the time needed to achieve a 95% confidence level. The test time t can be calculated using a Gaussian error distribution according to Equation 1:

$$t = -\frac{\ln(1-c)}{b \times r} \qquad \text{Equation 1}$$

where:

c = the degree of confidence level
b = upper bound of BER
r = bit rate

For the purpose of this evaluation, c = 95%, $b = 10^{-12}$, and r = 3.0 Gb/s. Substituting these values in Equation 1, the test time was 999 seconds (approximately 16.6 minutes). The actual run time during receiver testing was at least 17 minutes. Therefore, the confidence level was at least 95%.

AC Common Mode Noise Injection

The SATA specification requires the receiver to operate within the given parameters when subject to a sinusoidal mode interfering signal with a peak-to-peak voltage of 100 mV and a sweep across the frequency range from 2 to 200 MHz. The sweep rate period should be no smaller than 33.33 µs.

This requirement was achieved by using the Xilinx AC common mode noise injection board. This board was designed to minimize impedance mismatch. Figure 6 shows the schematic of the board.

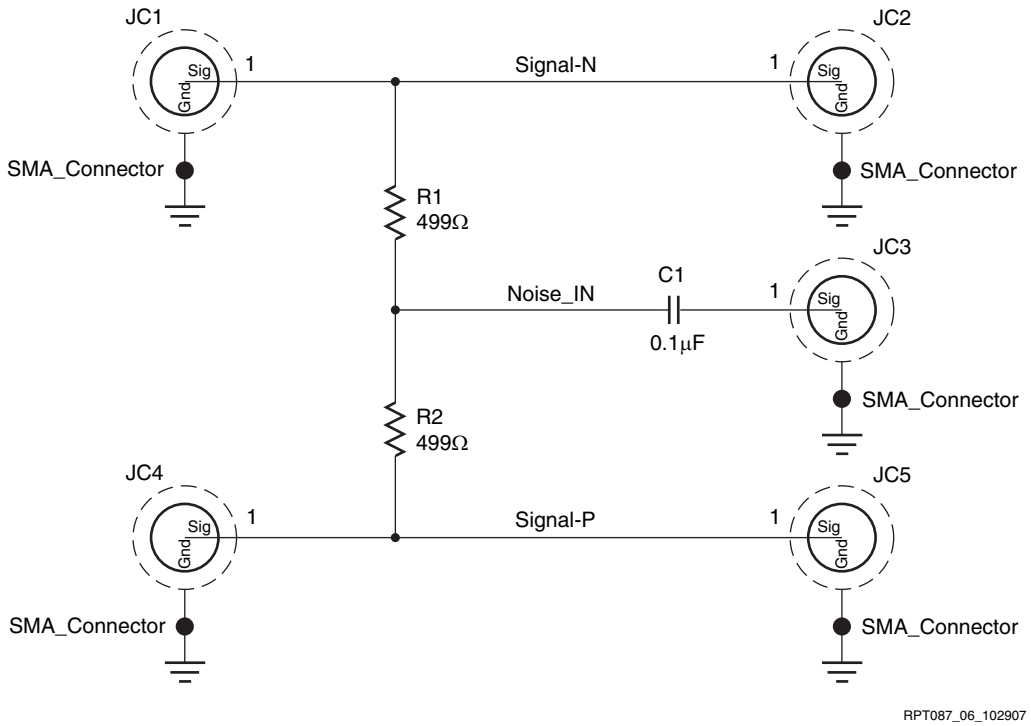

Figure 6: **AC Common Mode Noise Injection Board Schematic**

The Agilent E4438C ESG vector signal generator inserted sinusoidal signals in the lab-sourced signal creating the AC common mode effect. The signal generator was set up to sweep from 2 to 200 MHz in 20 steps and then reverse direction. Each step lasted exactly 2 seconds.

Receiver Jitter Tolerance

In this measurement, both jitter components of deterministic jitter and random jitter (RJ) were added to the input datapath. Based on channel calibration, the DJ and RJ components were corrected to introduce 0.60 UI of total jitter. The 0.42 UI DJ component was generated by passing the test pattern through 15 inches of Xilinx standard FR4 trace board. TJ and DJ at $f_{BAUD}/10$ are obsolete as stated in the SATA specification errata.

Transmitter Electrical Tests

Transmitter Test Setup

The transmitter amplitude and jitter test setup is shown in Figure 7. It is based on the SATA specification. The transmitter outputs of the GTP0 transceiver at location 122 were connected to the CHS-TF-SATA-NE-ZP test fixture through a pair of SMA cables. The CHS-TF-SATA-NE-ZP test fixture was mated with the CHS-TF-SATA-FE-ZP test fixture on the SATA connector side. The SMA connectors of the CHS-TF-SATA-FE-ZP test fixture were connected to the inputs of the LeCroy SDA 11000 through a pair of SMA cables and DC blocks.

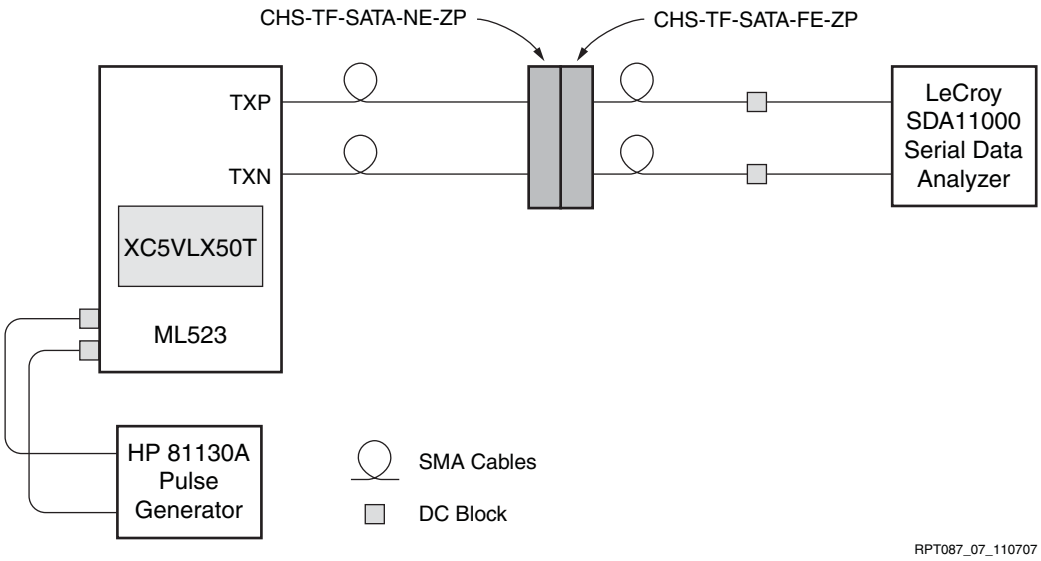

Figure 7: **Transmitter Test Setup**

Transmitted Signal Tests

During the transmitted signal tests, the LeCroy SDA-SATA test software ran a series of scripts within the SDA oscilloscope to complete the measurements. Several test designs were used to create the required patterns for different tests. For example, the high-frequency test pattern (HFTP), mid-frequency test pattern (MFTP), and lone bit pattern (LBP) were generated from the FPGA configurable logic to the GTP transmitter during the amplitude, rise and fall times, and period tests. The composite pattern was also created from configurable logic during the transmitter jitter tests. Short versions of all test patterns were used, as described in the SATA specification.

Detailed Transmitter Results

Unit Interval

The minimum and maximum unit interval parameters (T_{UI}) were the measures of the data period. Figure 8 and Table 10 show the minimum transmitter unit interval distribution. Figure 9 and Table 11 show the maximum transmitter unit interval distribution. Both Figure 8 and Figure 9 include the long-term frequency stability. The nominal value was not measured because it is architecture-specific.

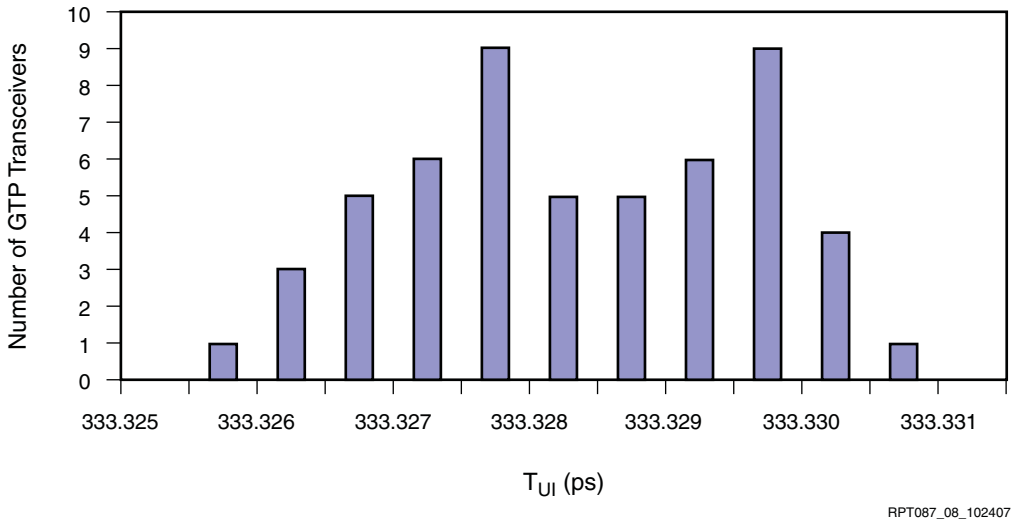

Figure 8: **Minimum TX Unit Interval (T_{UI}) Distribution**

Table 10: **Minimum TX Unit Interval Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
333.325	333.328	333.330	333.328	0.001	ps

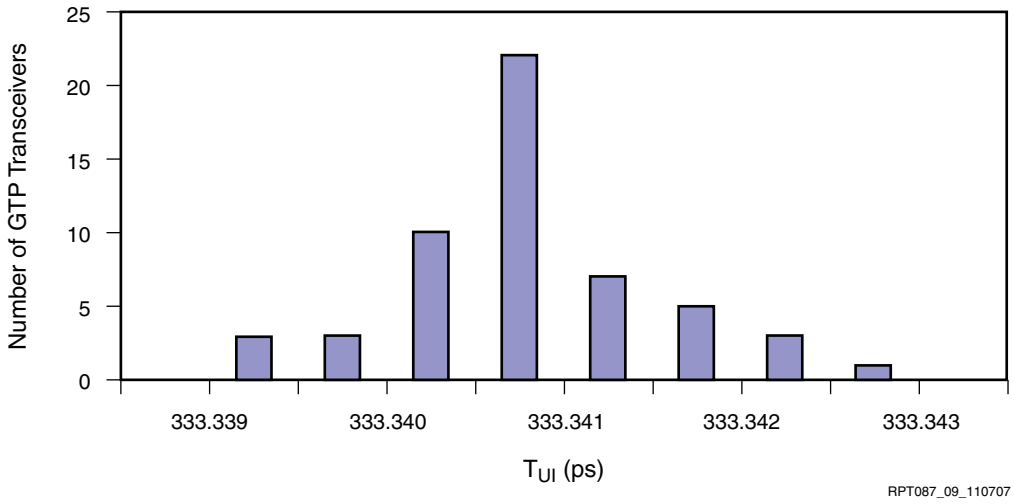

Figure 9: **Maximum TX Unit Interval (T_{UI}) Distribution**

Table 11: **Maximum TX Unit Interval Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
333.339	333.340	333.342	333.340	0.001	ps

TX Differential Output Voltage

The transmitter pre-driver and main driver settings were chosen to guarantee that the minimum differential swing requirement could be met. These settings are shown in Table 28, page 31. Figure 10 and Table 12 show the minimum TX differential swing distribution.

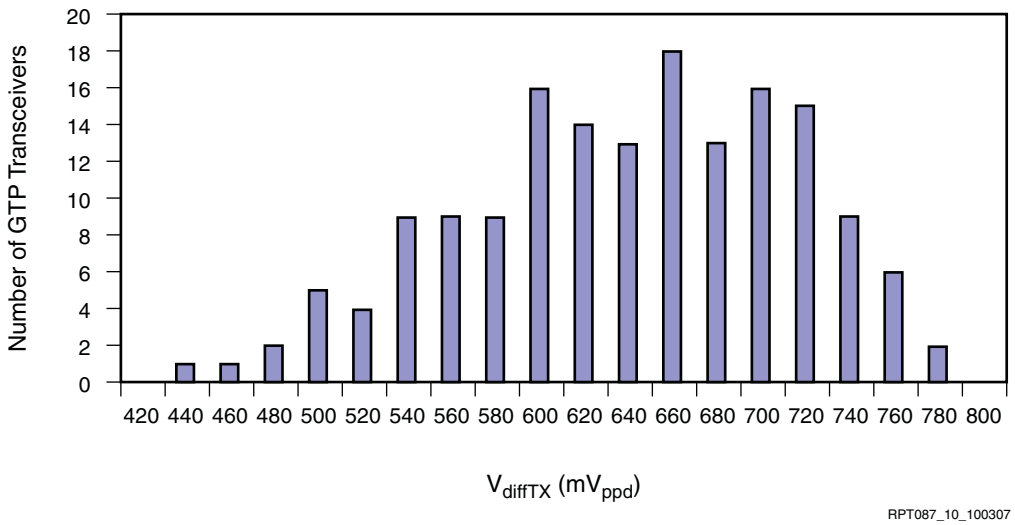

Figure 10: **Minimum TX Differential Output (V_{diffTX}) Distribution**

Table 12: **Minimum TX Differential Output Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
435	630	764	636	73.6	mVppd

The TX differential output swing exceeded the maximum requirement during tests with MFTP. The maximum transmitter output voltage parameter is not the absolute maximum voltage limit. Instead, the tests measure the percentage of samples exceeding the maximum TX differential output voltage as stated in the SATA specification. The two determining percentage parameters are *pu* and *pl*. Both have to be less than 0.05 (5%) to pass. Figure 11 shows the distribution of *pu* and *pl* parameters, and Table 13 summarizes this distribution.

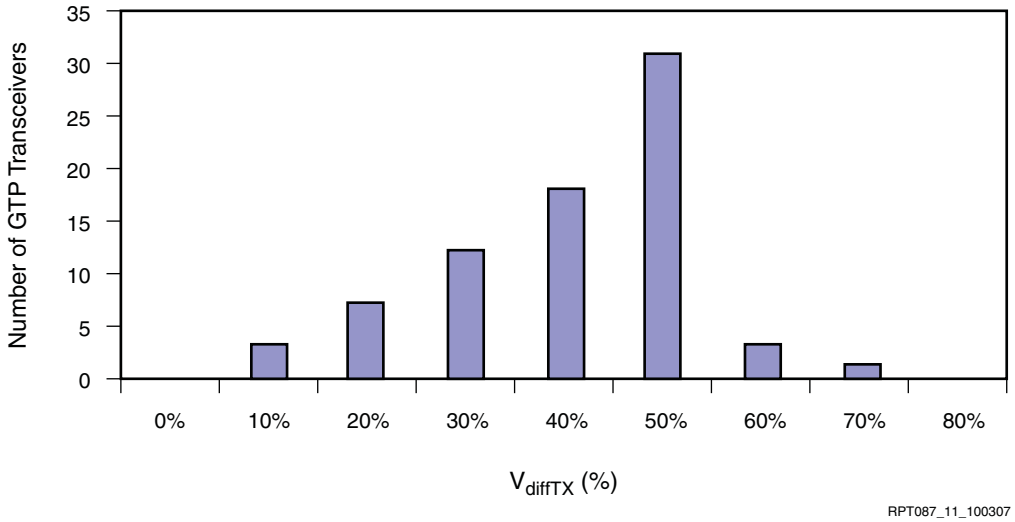

Figure 11: **Maximum TX Differential Output (V_{diffTX}) Distribution**

Table 13: **Maximum TX Differential Output Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
7	36	78	39	13	%

The signaling at the host controller connector is allowed to exceed the Gen2m transmit maximum provided that the Gen2i receiver maximum is not exceeded at the device connector. For Gen2i usage model (cables), the designer should verify that the TX output level does not exceed the absolute maximum input limit of the receiver.

The designer is advised to use the transmitter pre-driver and main driver settings listed in Table 28, page 31 to guarantee that the minimum voltage level is met. It is possible to reduce the TX differential output swing by lowering the transmitter pre-driver and main driver levels from those shown in Table 28 to meet the maximum requirement. However, the designer should verify that the new setting still meets the minimum requirement.

Rise and Fall Times

Figure 12 and Table 14 show the 20–80% rise time distribution, while Figure 13 and Table 15 summarize the 20–80% fall time distribution.

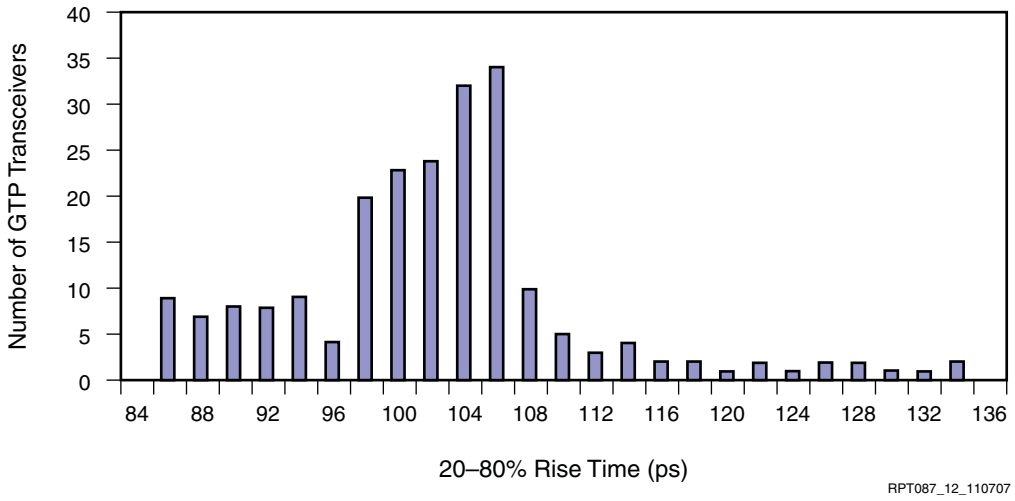

Figure 12: **20–80% Rise Time Distribution**

Table 14: **20–80% Rise Time Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
84	102	133	102	9.1	ps

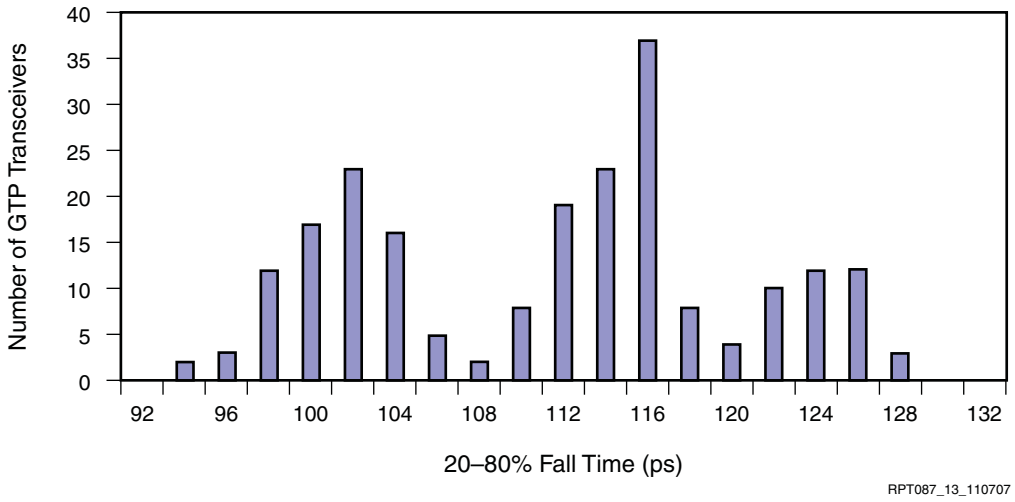

Figure 13: **20–80% Fall Time Distribution**

Table 15: **20–80% Fall Time Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
93	110	128	112	8.9	ps

TX Differential Skew

TX differential skew or intra-pair skew is a measure of the symmetry of the transmitter silicon. Extra care was taken when measuring TX differential skew because the measurement values were typically just a few picoseconds. For example, the skew in the SMA cables was determined and removed from the measurements. The socket, board traces, and connectors contributed some amount of skew as well. The absolute delays and, eventually, the skew of these elements were measured by time-domain reflectometer (TDR) and eliminated. The TX differential skew shown in Table 3, page 6 and Figure 14 therefore reflects only the values observed at the FPGA package balls. TX differential skew is a system parameter, and the test result is provided for reference. Designers are encouraged to validate the final skew in their systems to meet the SATA specification. Figure 14 shows the TX differential skew distribution. This data was measured from four GTP transceivers (100, 101, 102, and 103) across all corners. Table 16 summarizes the TX differential skew distribution.

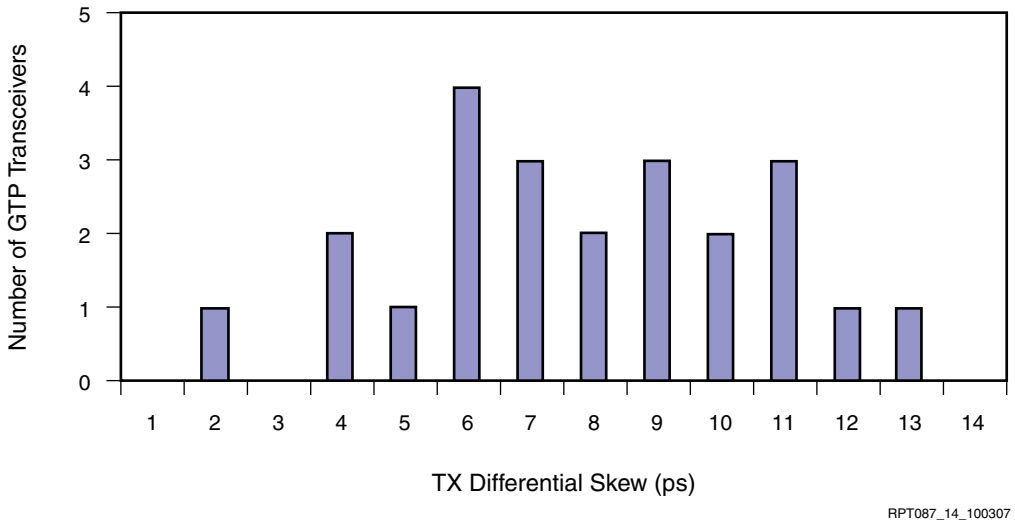

Figure 14: **TX Differential Skew Distribution**

Table 16: **TX Differential Skew Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
2	7	13	8	2.8	ps

OOB Common Mode/Differential Delta

TX OOB differential delta and OOB common mode delta measure the difference in the common mode between OOB burst and idle. Figure 15 and Table 17 show the OOB common mode delta. Figure 16 and Table 18 show the OOB differential delta.

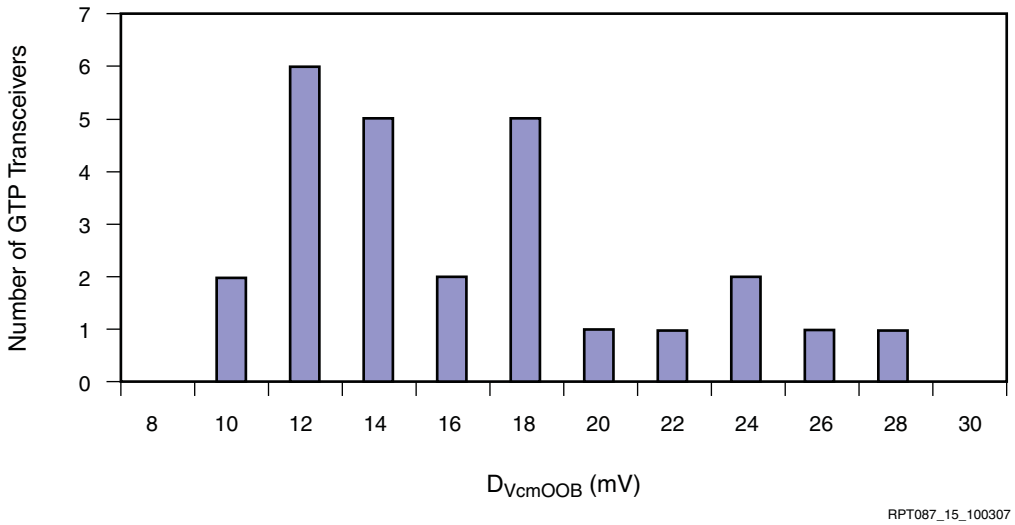

Figure 15: **OOB Common Mode Delta (D_{VcmOOB}) Distribution**

Table 17: **OOB Common Mode Delta Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
9	15	27	14	4.8	mV

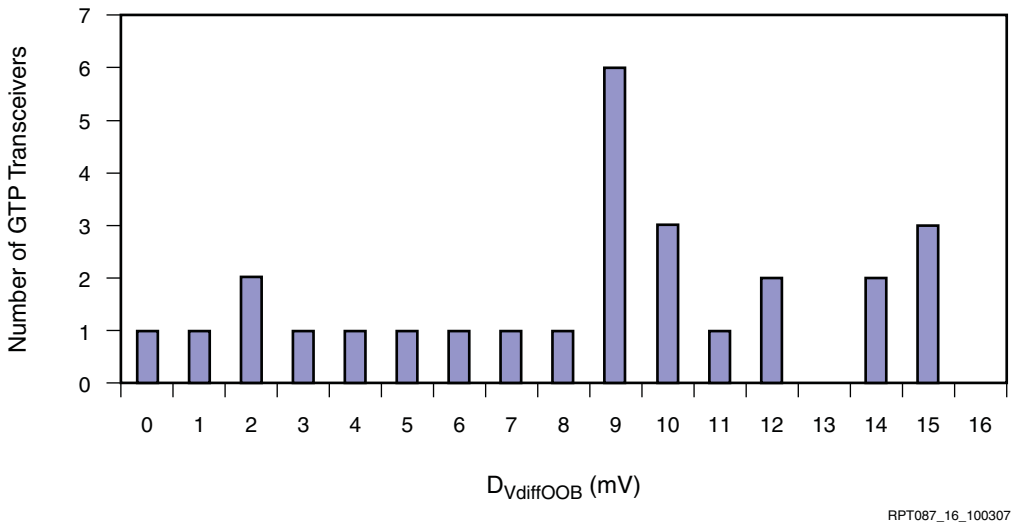

Figure 16: **OOB Differential Delta ($D_{VdiffOOB}$) Distribution**

Table 18: **OOB Differential Delta Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
1	8	15	9	4.1	mV

TX Amplitude Imbalance

TX amplitude imbalance measures the match in the single-ended amplitude of TX+ and TX–. The GTP transmitter did not meet the requirement for amplitude imbalance during tests using the HFTP. However, it passed the imbalance tests using the MFTP. The SATA link quality is not significantly impaired because the transmitter can still meet the jitter and rise and fall time requirement. The imbalance can affect the electromagnetic interference (EMI) more due to excess common mode fluctuations. Figure 17 and Table 19 show the TX amplitude imbalance distribution using the HFTP.

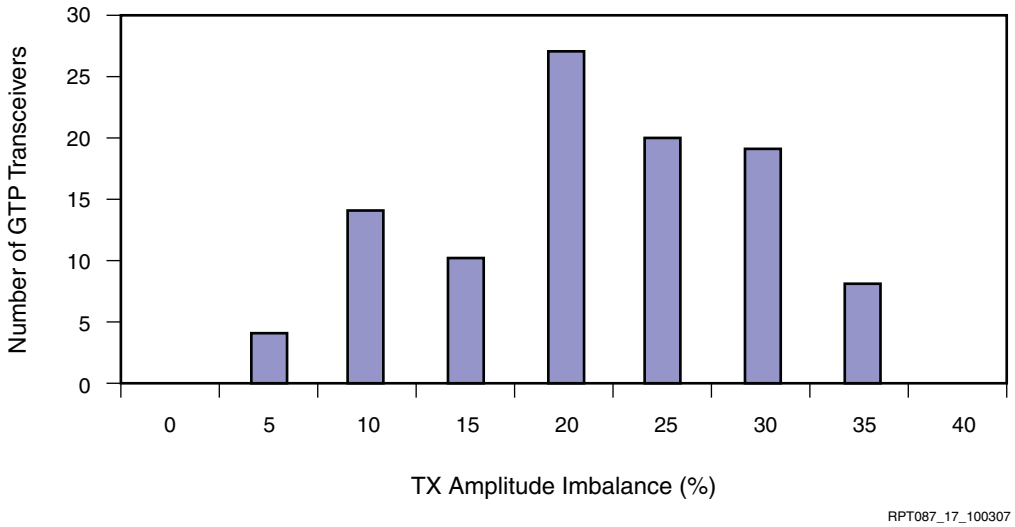

Figure 17: **TX Amplitude Imbalance Distribution**

Table 19: **TX Amplitude Imbalance (HFTP) Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
0	20	35	20	8	%

TX Jitter

The SATA specification contains two sets of TX jitter parameters, $f_{Baud}/10$ and $f_{Baud}/500$. However, TJ and DJ at $f_{Baud}/10$ are both obsolete as stated in the SATA revision 2.6 errata. Therefore, only TJ and DJ at $f_{Baud}/500$ were measured. Figure 18 and Table 20 show the TJ distribution. Figure 19 and Table 21 show the DJ distribution.

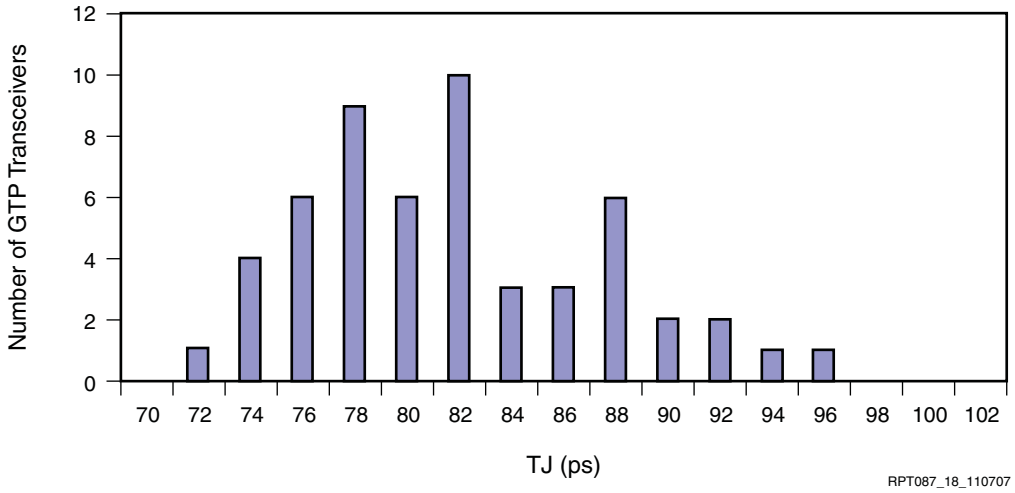

Figure 18: **Total Jitter Distribution**

Table 20: **Total Jitter Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
71.3	80.7	96.6	80.2	5.6	ps

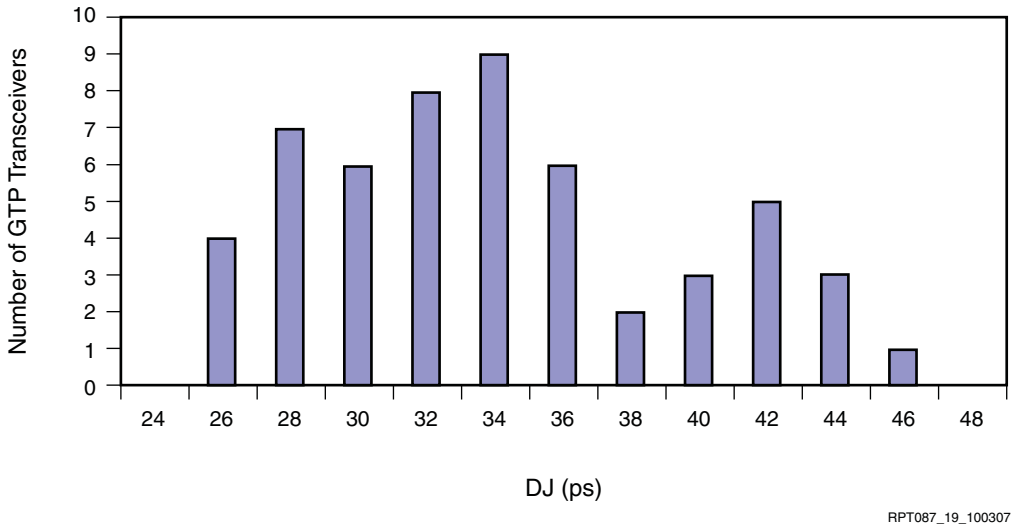

Figure 19: **Deterministic Jitter Distribution**

Table 21: **Deterministic Jitter Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
24.3	33.2	45.6	32.2	5.43	ps

Out-of-Band Signaling

RX OOB Detection

OOB signaling is crucial in SATA operation. It is used to initialize the SATA link and perform power management. OOB signaling can be achieved by transmission of a burst followed by idle periods (at common-mode levels). OOB signals are observed by detecting the temporal spacing between adjacent bursts of activity on the differential pair. The SATA specification requires that V_{diffRX} signals less than 75 mVppd not be detected as activity, and signal levels greater than 200 mVppd be detected as activity.

The GTP transceiver has a built-in OOB detector with eight programmable threshold levels. The OOBDETECT_THRESHOLD attribute sets the detect threshold level. The OOB detector has been thoroughly characterized in the RX OOB signal detect section of the Virtex-5 GTP transceiver characterization report. [Ref 4] The report shows that the optimal setting of OOBDETECT_THRESHOLD to meet the SATA OOB specification was `111` (OOB7). Because the data in that report was collected at 2.5 Gb/s, the OOB detect threshold test has been repeated at 3 Gb/s in this report to ensure good correlation with the general characterization data.

The OOB detector threshold level of the GTP transceiver was measured as follows. The Agilent BitAlyzer generated PRBS2^{31}-1 patterns at 3 Gb/s to the GTP receiver through the test fixture. The RXELECIDLE port was monitored throughout the test. The amplitude of the signal was initially above 200 mVppd. It was reduced stepwise until RXELECIDLE changed, indicating that the threshold detector had been tripped. The trip voltage was then measured on the oscilloscope. The test covered all voltages, temperatures, and process corners. Figure 20 and Table 22 show the OOB detector threshold distribution. The results match closely with the data from the Virtex-5 GTP transceiver characterization report at the same location on the GTP transceiver.

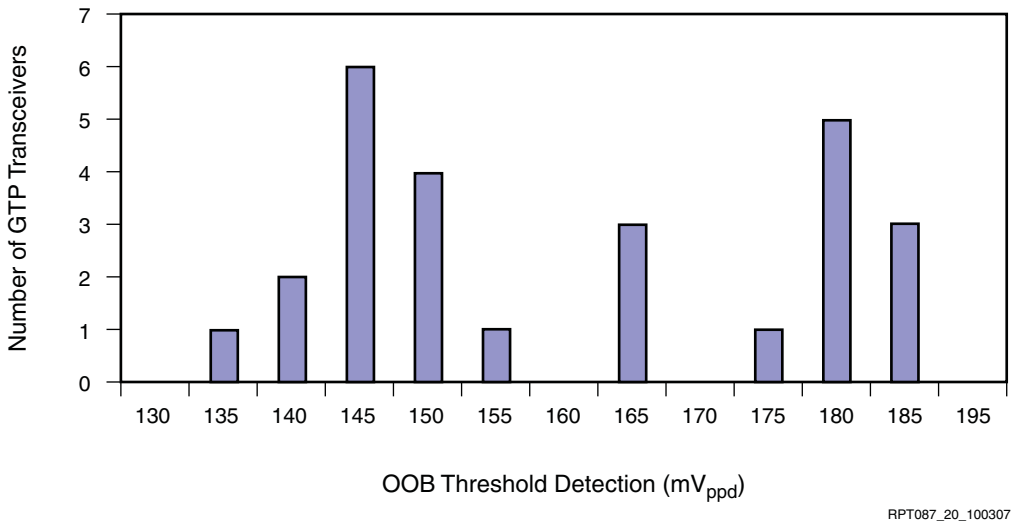

Figure 20: **OOB Threshold Detection Distribution**

Table 22: **OOB Threshold Detection Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
134	157	185	149	18	mVppd

TX OOB Signals

Figure 21 and Figure 22 show the oscilloscope screen shots of the COMRESET and COMWAKE OOB signals, respectively, generated by the GTP transmitter.

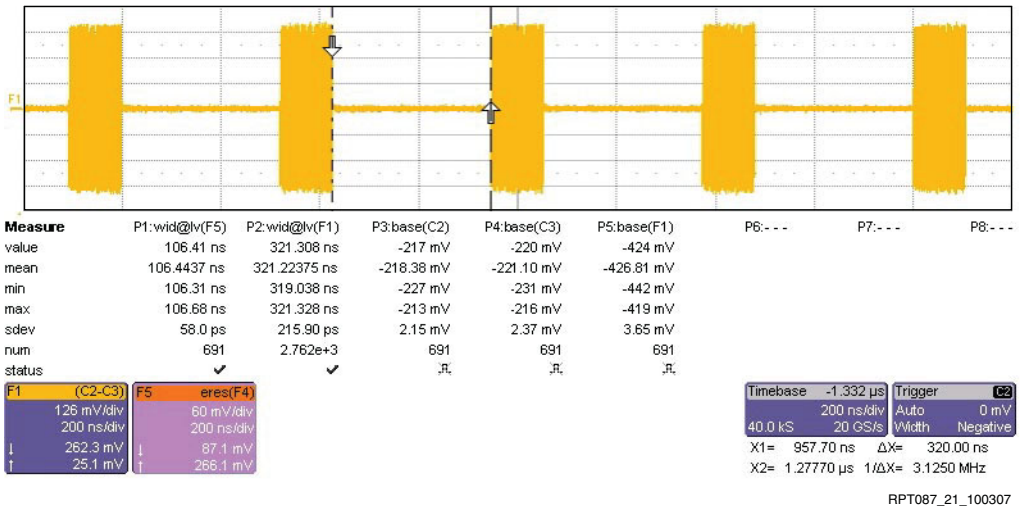

Figure 21: **COMRESET**

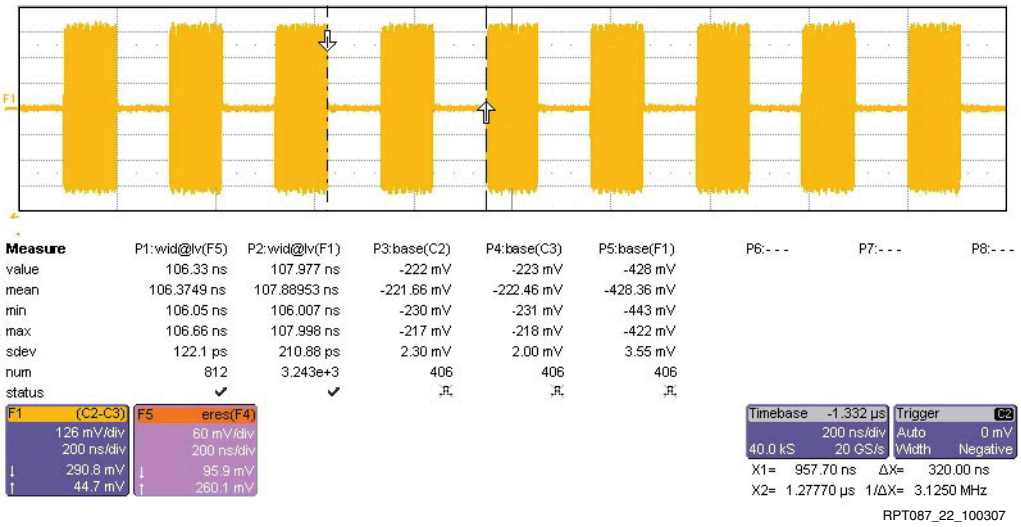

Figure 22: **COMWAKE**

Figure 23 and Table 23 show the OOB burst length distribution.

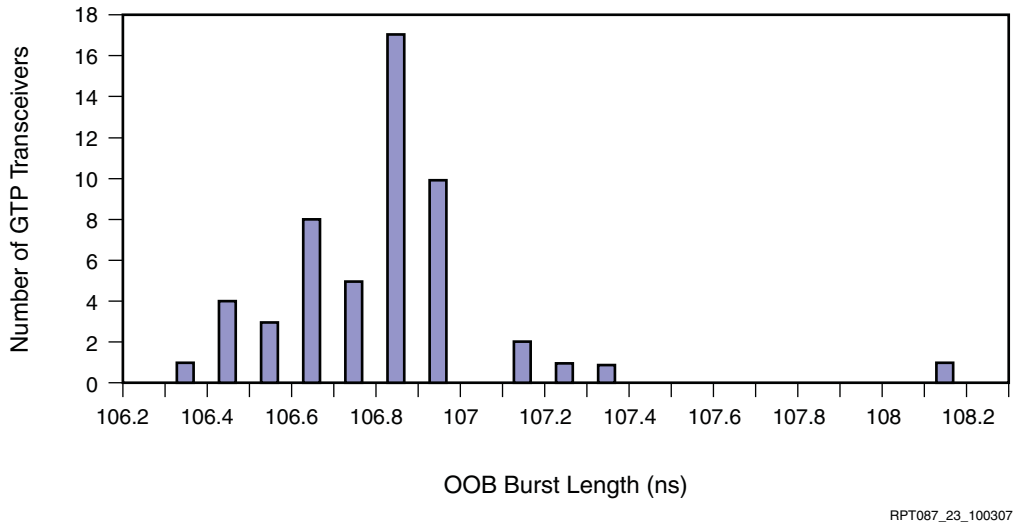

Figure 23: **OOB Burst Length Distribution**

Table 23: **OOB Burst Length Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
106	107	108	107	0.3	ns

Figure 24 and Table 24 show the COMRESET gap length distribution.

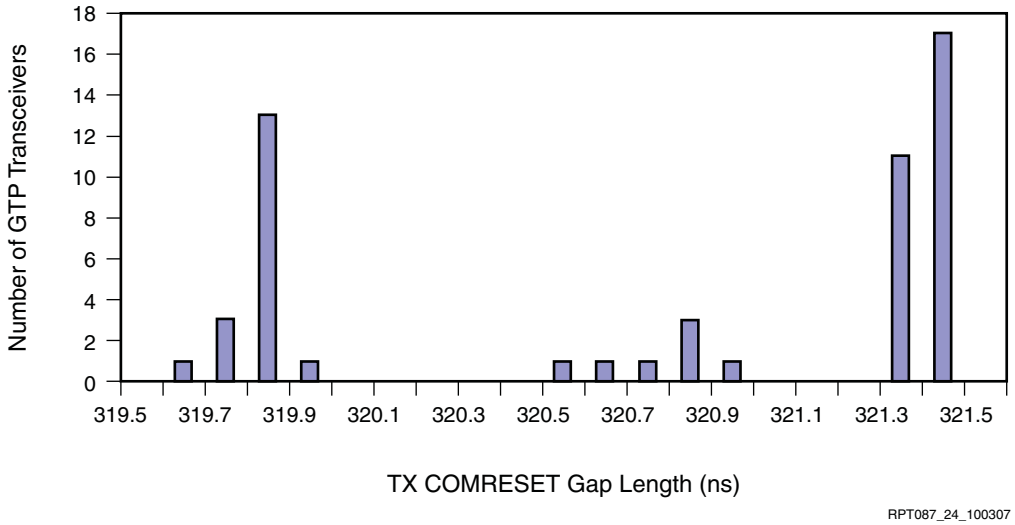

Figure 24: **TX COMRESET Gap Length Distribution**

Table 24: **TX COMRESET Gap Length Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
319.5	320.7	321.3	321.2	0.7	ns

Figure 25 and Table 25 show the COMWAKE gap length distribution.

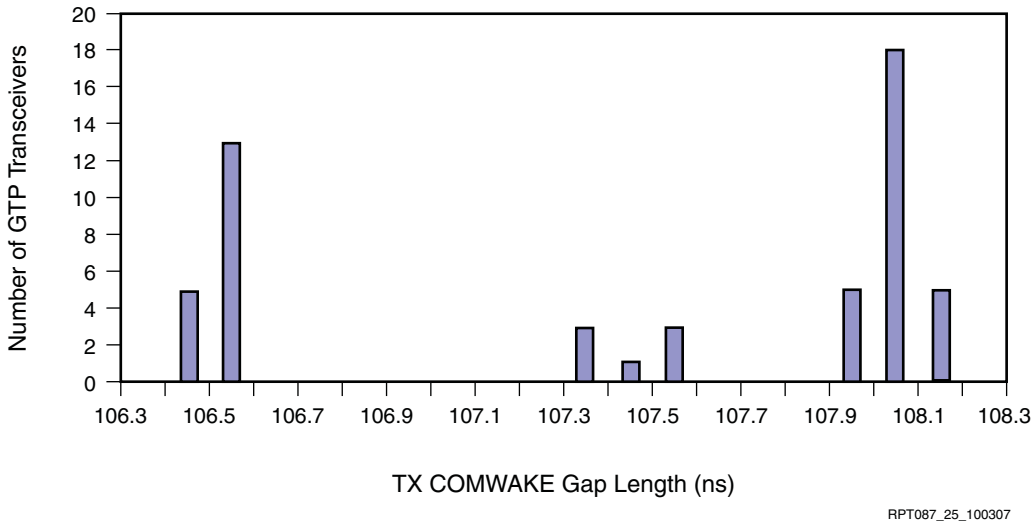

Figure 25: **TX COMWAKE Gap Length Distribution**

Table 25: **TX COMWAKE Gap Length Summary**

Minimum	Average	Maximum	Median	Standard Deviation	Unit
106	107	108	108	0.7	ns

Spread Spectrum Clocking

Serial ATA allows the use of spread spectrum clocking or intentional low frequency modulation of the transmitter clock. The purpose of this modulation is to spread the spectral energy to mitigate any unintentional interference to radio services. The SSC tests of the GTP transceiver were performed separately from the other SATA transmitter and receiver tests. The SSC test setup is shown in Figure 26. Agilent J-BERT N4903A data outputs were connected to the DUT RX, and the DUT was placed in the RX-to-TX far-end physical medium attachment (PMA) loopback mode. Data errors were checked at the Agilent J-BERT, and an Agilent E4405B spectrum analyzer was used to verify the SSC modulation on the input data and reference clock.

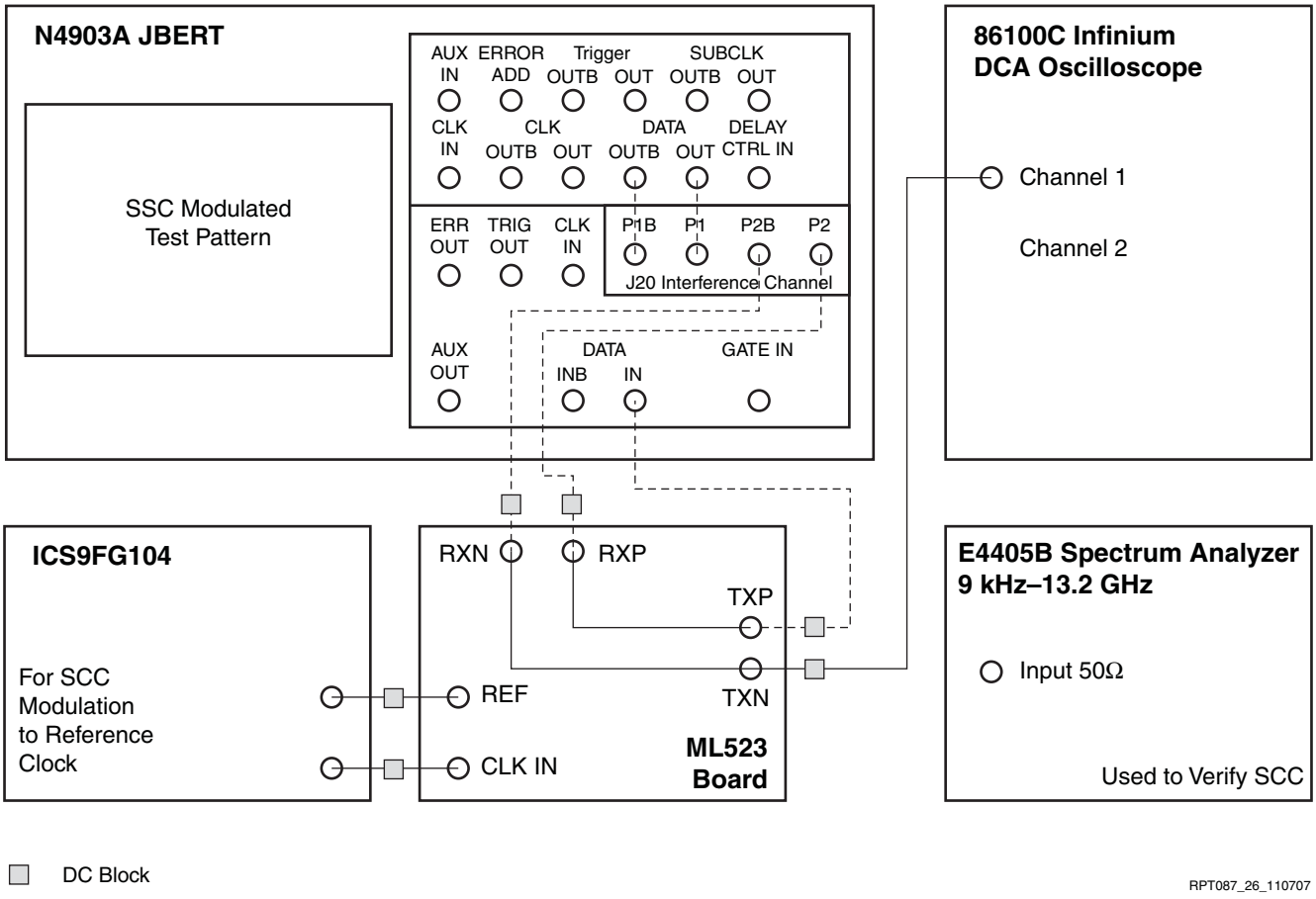

Figure 26: **SSC Test Setup**

SSC Test Signals

The Agilent J-BERT provided a PRBS2^{31}-1 test pattern. The data rate was modulated at 33 KHz from 0 ppm to –5000 ppm (δ) from the nominal data rate in a triangular profile. Figure 27 illustrates the modulation.

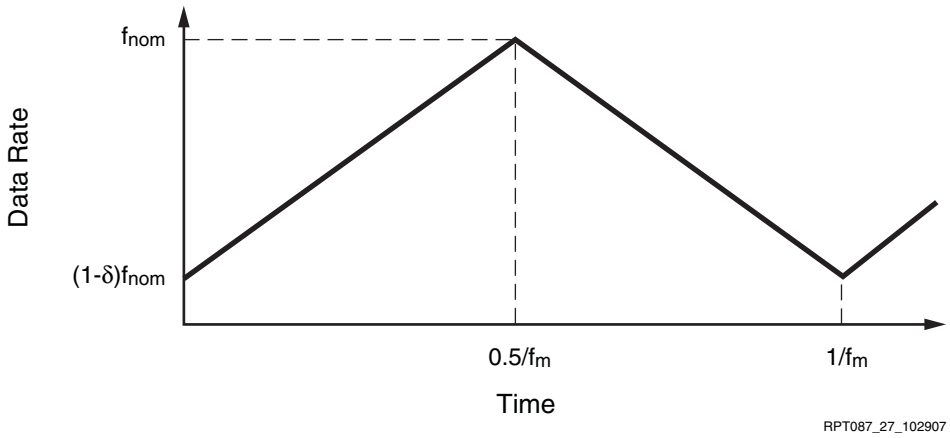

Figure 27: **SSC Profile**

Figure 28 shows the measured spectral fundamental frequency of the spread spectrum modulated data feeding into the GTP receiver. The nominal data frequency of 1.5 GHz was expanded, creating a wider spectral plateau.

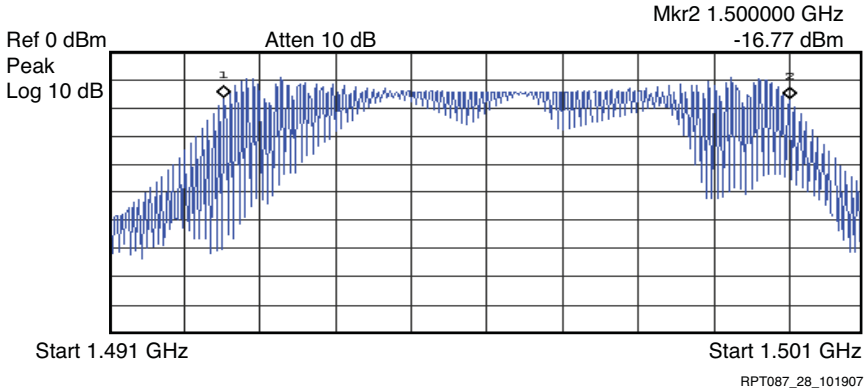

Figure 28: **Spectral Fundamental Frequency of Incoming Data**

The GTP transceiver reference clock was also modulated similarly. The frequency modulation was 33 KHz in a triangular profile. The spread was between 0 to –0.5% from the nominal frequency. An IDT ICS9FG104 frequency generator provided the modulated clock. Figure 29 shows the spectral fundamental frequency of the reference clock. The reference clock maintained a 700 ppm static frequency offset relative to the RX data.

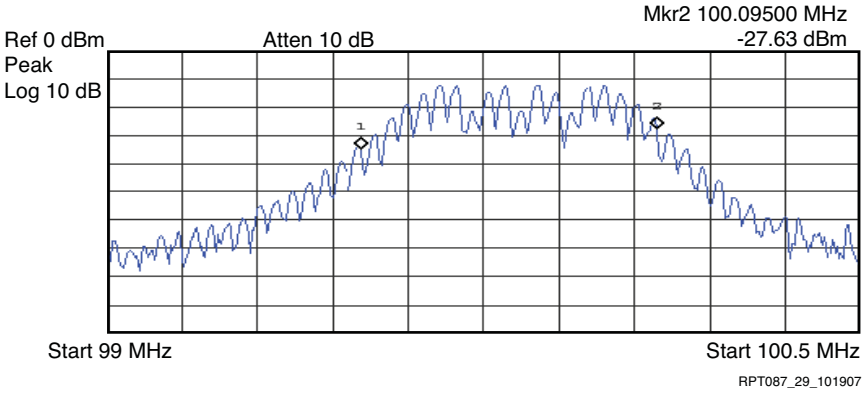

Figure 29: **Spectral Fundamental Frequency of GTP Transceiver Reference Clock**

Test Results

Table 26 summarizes the SATA Generation 2 SSC test results for the GTP transceiver. The table indicates that the GTP transceiver did not create any bit errors during the SSC test and passed under various conditions. The tests covered all processes (slow, typical, and fast) and different temperatures. The reference clock frequency was 100 MHz for all tests, which ran five minutes for each case.

Table 26: **GTP Transceiver SATA Generation 2 SSC Test Summary**

Devices	AVCC (V)	PLL AVCC (V)	AVTTTX (V)	AVTTRX (V)	Temp (°C)	Test Result
Typical-1, Typical-2, Fast-1, Fast-2, Slow-1, Slow-2	0.9	1.08	1.08	1.08	100	Pass
	1	1.2	1.2	1.2	25	Pass
	1.1	1.32	1.32	1.32	–40	Pass

Return Loss

The frequency domain return loss measurements shown in Figure 30 to Figure 33 were made using the University of New Hampshire Interoperability Lab (UNH IOL) guidelines. The four traces represent different GTP receivers with varying PCB trace lengths. The data for the TX and RX impedance balance is not available in this report.

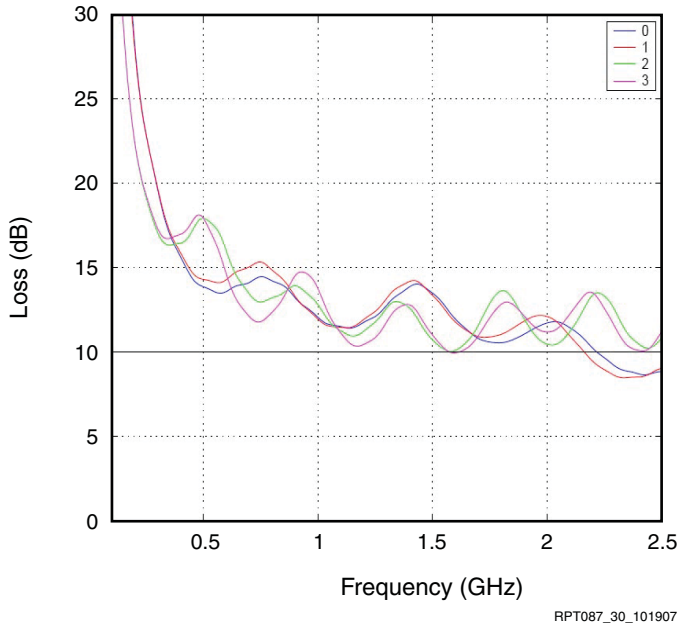

Figure 30: **RX Differential Return Loss vs. Frequency**

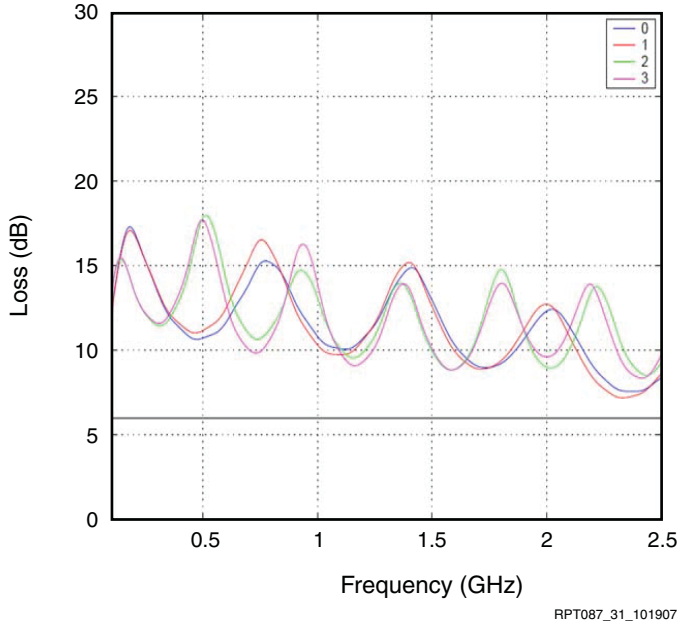

Figure 31: **RX Common Mode Return Loss vs. Frequency**

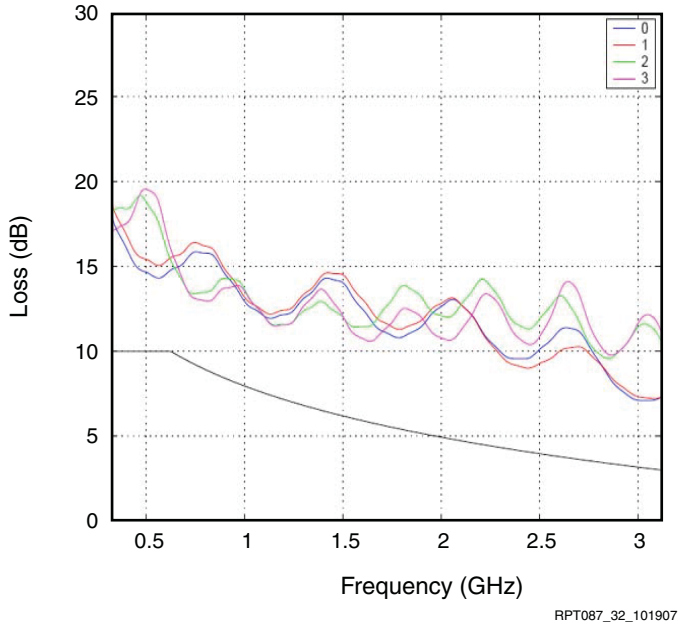

Figure 32: **TX Differential Return Loss vs. Frequency**

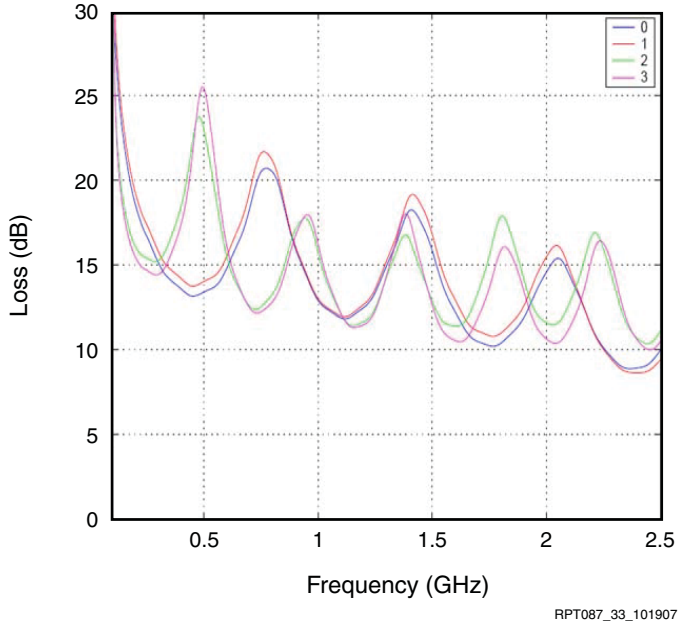

Figure 33: **TX Common Mode Return Loss vs. Frequency**

Transceiver Configuration

Table 27 to Table 29 show SATA GTP transceiver attribute settings used during the characterization. These settings are recommended for achieving optimal performance. These settings are for the GTP0 transceiver. The same settings should be applied for the corresponding attributes in the GTP1 transceiver, if used for SATA.

Table 27: **GTP Receiver Attribute and Port Settings**

Receiver Parameter	Setting	Description
AC_CAP_DIS_0	FALSE	Built-in AC coupling bypass
PLL_DIVSEL_FB	2	PLL feedback divider
PLL_DIVSEL_REF	1	Reference clock divider
PLL_RXDIVSEL_OUT_0	1	RX PLL clock divider
PLL_SATA_0	FALSE	SATA Generation 1 (1.5 Gb/s)/ Generation 2 (3 Gb/s) support
PMA_RX_CFG	09F0089	CDR adjustment
RCV_TERM_GND_0	FALSE	RX termination ground reference
RCV_TERM_MID_0	TRUE	RX termination 2/3 AVTTRX reference
RCV_TERM_VTTRX_0	TRUE	RX termination AVTTRX reference
RXENEQB0	1	RX equalizer

Table 28: **GTP Transmitter Attribute and Port Settings**

Transmitter Attributes	Setting	Description
PLL_TXDIVSEL_OUT_0	1	TX common divider
TX_DIFF_BOOST_0	TRUE	Transmitter boost
TXBUFDIFFCTRL0	001	Pre-driver
TXDIFFCTRL0	100	Main driver
TXPREEMPHASIS0	011	Pre-emphasis

Table 29: **GTP Transceiver OOB Attribute and Port Settings**

OOB Attributes	Setting	Description
COM_BURST_VAL_0	0101	Number of COM sequence bursts transmitted
OOB_CLK_DIVIDER	6	Squelch clock divider
OOBDETECT_THRESHOLD_0	111	OOB detect threshold level
RX_STATUS_FMT_0	SATA	RX status encoding
SATA_BURST_VAL_0	100	Number of bursts required to declare a COM match
SATA_IDLE_VAL_0	100	Number of idles required to declare a COM match
SATA_MAX_BURST_0	7	Maximum OOB burst reject threshold
SATA_MAX_INIT_0	22	Maximum COMRESET idle time allowed
SATA_MAX_WAKE_0	7	Maximum COMWAKE idle time allowed
SATA_MIN_BURST_0	4	Minimum OOB burst reject threshold

Table 29: **GTP Transceiver OOB Attribute and Port Settings *(Continued)***

OOB Attributes	Setting	Description
SATA_MIN_INIT_0	12	Minimum COMRESET idle time allowed
SATA_MIN_WAKE_0	4	Minimum COMWAKE idle time allowed

Appendix A: References

The following references were used in this characterization report:

1. Serial ATA International Organization: Serial ATA Revision 2.6 www.serialata.org.
2. UG225, *ML52x User Guide*.
3. SATA Revision 2.6 Errata ECN #006: $f_{baud}/10$ Jitter Parameter Removal www.sata-io.org/2.6errata_014.zip.
4. RPT056, *Virtex-5 RocketIO GTP Transceiver Characterization Report*.
5. RPT064, *Virtex-5 PCI Express Protocol Standard Characterization Test Report*.
6. DS202, *Virtex-5 Data Sheet: DC and Switching Characteristics*.
7. UG196, *Virtex-5 RocketIO GTP Transceiver User Guide*.
8. Crescent Heart Software Compliance SATA Test Fixtures data sheet http://www.c-h-s.com/TF-SATA.Datasheet.pdf.

Appendix B: Test Equipment

This appendix lists the test equipment used in this characterization report.

Measuring Equipment

The following measuring equipment was used:

- Agilent 86130A BitAlyzer error performance analyzer with SATA and PRBS test patterns
- LeCroy SDA11000 (or SDA6000) serial data analyzer
- Agilent E4438C ESG vector signal generator (for AC common mode noise)
- Agilent J-BERT N4903A high-performance serial BERT
- Agilent E4405B ESA-E series spectrum analyzer
- HP 81130A pulse data generator
- Silicon Thermal CH5050 chiller

Test Fixtures

The following test fixtures were used:

- Xilinx ML523 characterization board, revision A with ML52X power module, revision B
- Crescent Heart Software TF-SATA-NE-ZP SATA compliance test fixture
- Crescent Heart Software TF-SATA-FE-ZP SATA compliance test fixture

- Xilinx quad serial loop, revision B
- Xilinx AC common mode noise injection board

Accessories

The following accessories were used:

- Inmet DC blocks, part number 8037
- Inmet attenuators, part numbers 26AH-20db and 26AH-6db
- Low-loss SMA coaxial cables
- IDT ICS9FG104 frequency generator

Software

The following software was used:

- LeCroy SDA-SATA application software, version 1.2 package
- XBERT software GUI, version 1.1.2 (Xilinx internal)
- XBERT hardware, version 1.1 (Xilinx internal)
- ChipScope Pro Analyzer, version 8.2.02i, build 08202.6.227.120 or newer