Spartan-6 FPGA GTP Transceiver Characterization Report

PCI Express 1.1 (2.5 Gb/s) Electrical Standard

RPT131 (v1.0) October 14, 2010

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/14/10	1.0	Initial Xilinx release.

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Spartan-6 FPGA GTP Transceiver Characterization Report for the PCI Express 1.1 Electrical Standard

Introduction

This characterization report compares the electrical performance of the Spartan®-6 FPGA GTP transceiver against the PCI Express® Revision 1.1 specifications published in the *PCI Express Base Specification, Revision 1.1* and the *PCI Express Card Electromechanical Specification, Revision 1.1*. All testing for this report is based on a line rate of 2.5 Gb/s across voltage, temperature, and worst-case transceiver performance corners.

This report includes test results for these PCI Express, Revision 1.1 specifications:

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Test Conditions

Table 1 and Table 2 show the supply voltage and temperature conditions used in the characterizations, respectively. All combinations of voltage and temperature conditions are used for the test performed.

Table 1: **Supply Voltage Test Conditions**

Condition	MGTAVCC (V)	MGTAVTT (V)
V_{MIN}	1.14	1.14
V_{MAX}	1.26	1.26

Notes:

1. Other FPGA voltages remain at their nominal values during the test.

Table 2: **Temperature Test Conditions**

Condition	Temperature (°C)
T_{-40}	–40
T_0	0
T_{100}	100
T_{125}	125

Transceiver Selection

Xilinx first performs volume generic transceiver characterization across process, voltage, and temperature. Protocol-specific characterization is subsequently performed using representative transceivers from generic characterization.

The chosen Spartan-6 FPGA GTP transceiver channels represent a mixture of transmitters having worst-case and typical performance based on volume generic characterization data. Transceivers with the worst performing transmitter output jitter are selected within the worst-case distribution of the transceivers found in the generic volume characterization. The same transceivers selected for the transmitter output jitter are also used for receiver jitter tolerance. The histograms in this characterization report do not show a true statistical representation normally present in a random (or even typical) population. The histograms are skewed toward the worst-case performance because of the transceiver selection process and are not representative of the typical production silicon.

Summary of Results

Table 3 shows the tested Spartan-6 FPGA GTP transceiver performance results against the *PCI Express Base Specification, Revision 1.1* and the *PCI Express Card Electromechanical Specification, Revision 1.1*. The data reported in this table represents the values obtained under the worst-case voltage, temperature, and performance corner conditions.

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Table 3: **PCI Express 1.1 Characterization Summary of Results for 2.5 Gb/s Line Rate**

Test Name	Parameter	Specification	Worst-Case Test Result	Units	Compliant
Unit Interval(1)	Min	399.88	400.04	ps	Yes
	Max	400.12	400.06	ps	Yes
Template Tests(1)	Max	Zero Mask Failure	Zero	Number of failures	Yes
Peak Differential Output Voltage(1)	Min	360	Programmable	mV	Yes
	Max	1200	Programmable	mV	Yes
Minimum Eye Width(1)	Min	287	288.26	ps	Yes
Median to Maximum Jitter(1)	Max	56.5	56.21	ps	Yes
TX Differential Return Loss	Frequency Profile	See Figure 11		dB	Yes
TX Common Mode Return Loss	Frequency Profile	See Figure 12		dB	Yes
PLL Bandwidth	Min	1.5	6.07	MHz	Yes
	Max	22	13.80	MHz	Yes
PLL Peaking	Max	3	1.12	dB	Yes
RX Input Jitter Tolerance(2)	TJ (maximum)	0.6	> 0.6	UI	Yes
	RJ (minimum)	5.47	8.86	ps RMS	Yes
	SJ at 10.00 MHz(3)	Not defined	0.15	UI	Yes
RX Differential Return Loss	Frequency Profile	See Figure 22		dB	Yes
RX Common Mode Return Loss	Frequency Profile	See Figure 23		dB	Yes

Notes:

1. Part of the Add-in Card Transmitter test for PCI Express, Revision 1.1.
2. The receiver input jitter tolerance requirements is referred to the *PCI Express Base Specification, Revision 1.1* and *PCI Express Card Electromechanical Specification, Revision 1.1.*
3. BER = 10^{-12}.

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Electrical Characterization Details

This section describes the test methodology used to characterize the Spartan-6 FPGA GTP transceiver's performance against the *PCI Express Base Specification, Revision 1.1* and the *PCI Express Card Electromechanical Specification, Revision 1.1*. The Spartan-6 FPGA GTP transceiver under test is configured using the default PCI Express setting generated from the Spartan-6 FPGA GTP Transceiver Wizard, version 1.6. The Spartan-6 FPGA GTP transceiver attribute settings that differ from the Wizard default settings are identified in the "Test Setup and Conditions" table for each test. Table 4 shows the PLL settings used in the characterization. This characterization report is based on the 100 MHz reference clock. The 125 MHz reference clock PLL settings are provided as a comparison.

Table 4: **PLL Settings for the 2.5 Gb/s Line Rate**

Data Rate (Gb/s)	PLL Frequency (GHz)	Reference Clock Frequency (MHz)	Reference Clock Divider: M(1)	PLL Feedback Dividers: N1(2) x N2(3)	PLL Output Divider: D(4)
2.5	1.5	100	2	5 x 5 = 25	1
2.5	1.5	125	1	5 x 2 = 10	1

Notes:

1. M = PLL_DIVSEL_REF.
2. N1 = Controlled by INTDATAWIDTH.
3. N2 = PLL_DIVSEL_FB.
4. D = PLL_[TX/RX]DIVSEL_OUT.

Add-in Card Transmitter Test

Test Methodology

The Add-in Card Transmitter test for the 2.5 Gb/s line rate comprises the unit interval, template tests, peak differential output voltage, eye width, and median to maximum jitter tests. These tests are compared against the *PCI Express Card Electromechanical Specification, Revision 1.1*. The Add-in Card Transmitter specification for the 2.5 Gb/s line rate is defined in Table 5.

Table 5: **Add-in Card Transmitter Specification for the 2.5 Gb/s Line Rate**

Test Name	Specification Range	Units
Unit Interval (UI)	399.88 to 400.12	ps
Template Tests	Zero Eye Mask Failures	Number of failures
Peak Different Output Voltage	360 to 1200	mV
Eye Width	287 (minimum)	ps
Median to Maximum Jitter	56.5 (maximum)	ps

These tests are performed using the test setup shown in Figure 1. An Agilent Infiniium DSA91304A Digital Signal Analyzer installed with a PCI Express automated test application performs the Add-in Card Transmitter test using the test methodology defined in the PCI-SIG® document *PCI Express 2.0 CEM Signal Quality Testing for Add-in Cards using Agilent DSO91304A*, and *DSA91304A 13 GHz Real-Time Oscilloscopes*. Agilent DSA91304A Analyzer calibration is performed prior to data collection.

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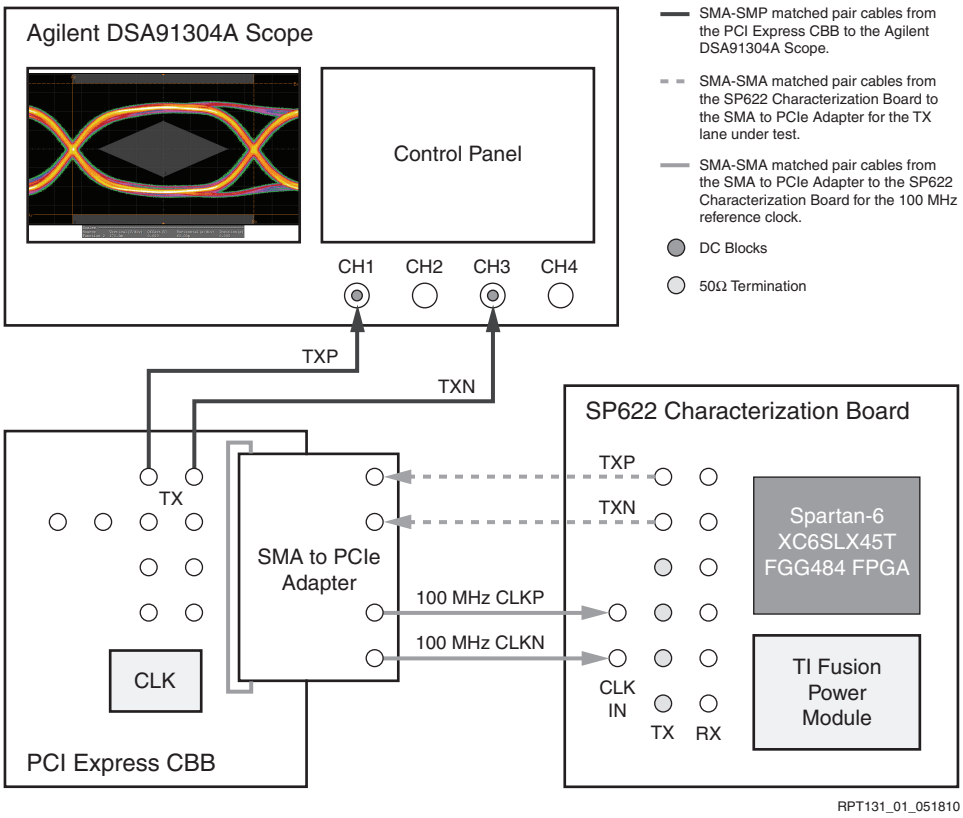

Figure 1: **Add-in Card Transmitter Test Setup Block Diagram**

The Spartan-6 device under test is configured to PCI Express mode and set to transmit the PCI Express compliance pattern on all available TX lanes of the SP622 Spartan-6 FPGA GTP Transceiver Characterization Board. Table 6 defines the test setup and conditions for the Add-in Card Transmitter test.

Table 6: **Add-in Card Transmitter Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent Infiniium DSA91304A Digital Signal Analyzer: • AC coupled using DC blocks.

Software Application	• Agilent N5393B PCI Express Automated Test Application, Version 2.10:
	  • Installed on the Agilent DSA91304A scope to automate the Add-in Card Transmitter test.
	  • PCI-SIG accepted methodology.
	• SIGTEST 3.1.9:
	  • Used only to compare the measurement results with the Agilent PCI Express automated test application.
	  • Uses the setup described in Figure 1.
	  • PCI-SIG accepted methodology.

Voltage	TI Fusion Power Module: • Installed on the SP622 board to change the MGTAVTT and MGTAVCC voltages between V_{MIN} and V_{MAX}.

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Table 6: **Add-in Card Transmitter Test Setup and Conditions *(Cont'd)***

Parameter	Value
Temperature	Temperature Unit: • A socket attached with a temperature controller is used to change the temperature condition of the device under test between T_{-40}, T_0, T_{100}, and T_{125}.
Data Pattern	Transmitting the PCI Express compliance pattern on all available TX lanes of the SP622 board.
FPGA	Spartan-6 FPGA XC6SLX45T FGG484.
Load Boards	• SP622 Spartan-6 FPGA GTP Transceiver Characterization Board, Revision A: • 50Ω terminator on TX channels not under test. • On the various SP622 board channels used, there are about 4 inches of FR4 in the TX paths. • PCI Express Compliance Base Board (CBB), Revision 2.0: • Standard PCI-SIG board for the Add-in Card Transmitter test. • SMA to PCIe® Adapter, Revision D: • Used to connect the SP622 board to the x16 interface of the PCI Express CBB.
Cables	• One pair of matched 50Ω Rosenberger SMA-SMP cables from the PCI Express CBB to the Agilent DSA91304A oscilloscope. • One pair of matched 50Ω SMA-SMA cables from the SMA to PCIe Adapter to the SP622 board for the 100 MHz reference clock. • One pair of matched 50Ω SMA-SMA cables from the SP622 board to the SMA to PCIe Adapter for the TX lane under test.
GTP Transceiver Attributes	• TX Amplitude and Pre-Emphasis: • TXDIFFCTRL = `4'h8` • TXPREEMPHASIS = `3'h4` • PLL Charge Pump Configuration: • PLL_CP_CFG = `8'h21` • Miscellaneous: • PCI_EXPRESS_MODE = TRUE
Reference Clock	100 MHz sourced from the PCI Express CBB.

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Test Results for the 2.5 Gb/s Line Rate

Figure 2 is a transition eye diagram, and Figure 3 is a non-transition eye diagram generated from the Agilent PCI Express automated test application. The Add-in Card Transmitter unit interval test reported UI between 400.04 ps and 400.06 ps, and template tests reported zero eye mask failures.

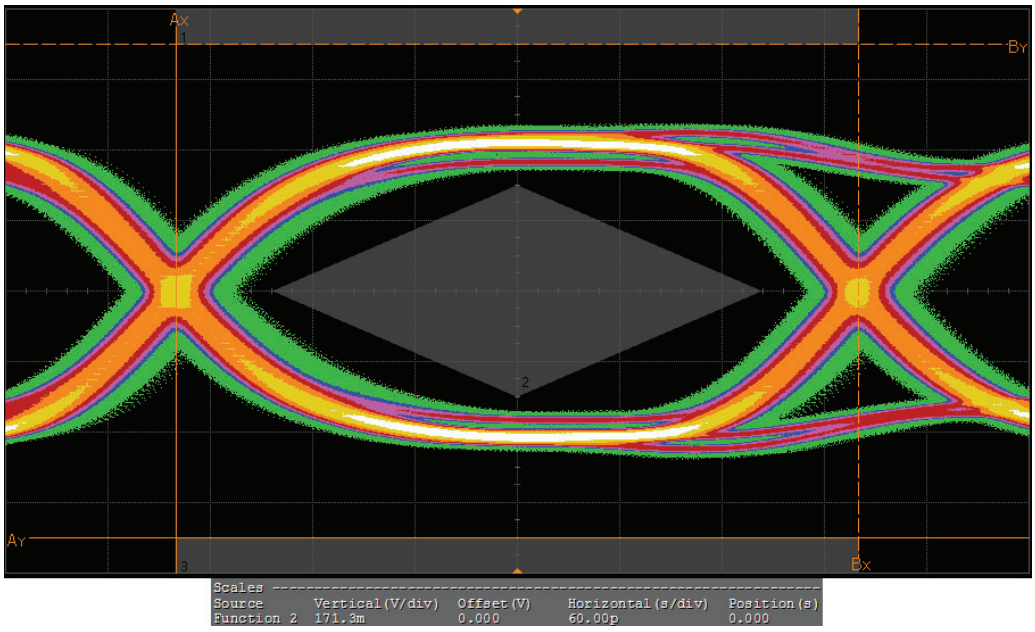

Figure 2: **Transition Eye Diagram for the 2.5 Gb/s Line Rate**

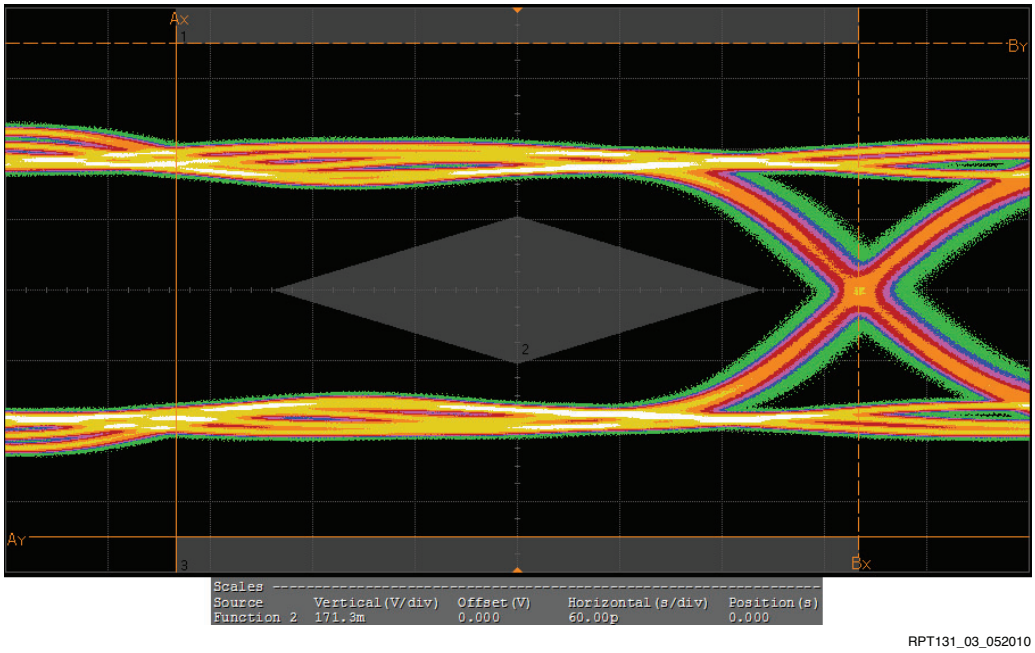

Figure 3: **Non-Transition Eye Diagram for the 2.5 Gb/s Line Rate**

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Figure 4 shows the peak differential output voltage results, Figure 5 shows the eye width results, and Figure 6 shows the median to maximum jitter results at a 2.5 Gb/s line rate with a 100 MHz reference clock. These histogram results are skewed towards the worst-case performance because of the transceiver selection process. The vertical axis of the histogram represents the frequency or number of data points. Additional output jitter margin can be gained by using a 125 MHz reference clock. Table 7 summarizes the maximum and minimum Add-in Card Transmitter test results at the 2.5 Gb/s line rate with a 100 MHz reference clock.

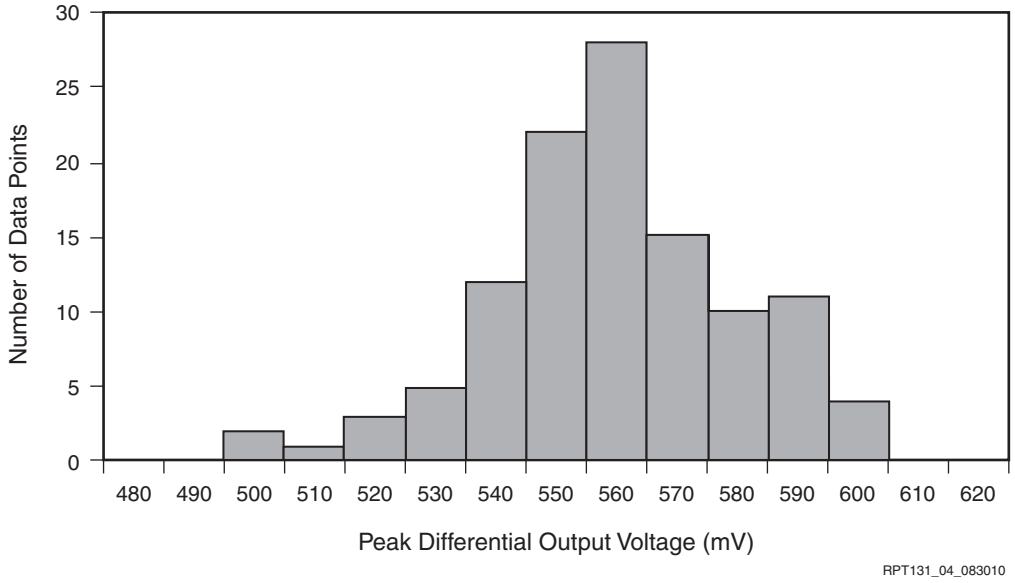

Figure 4: **Peak Differential Output Voltage for the 2.5 Gb/s Line Rate**

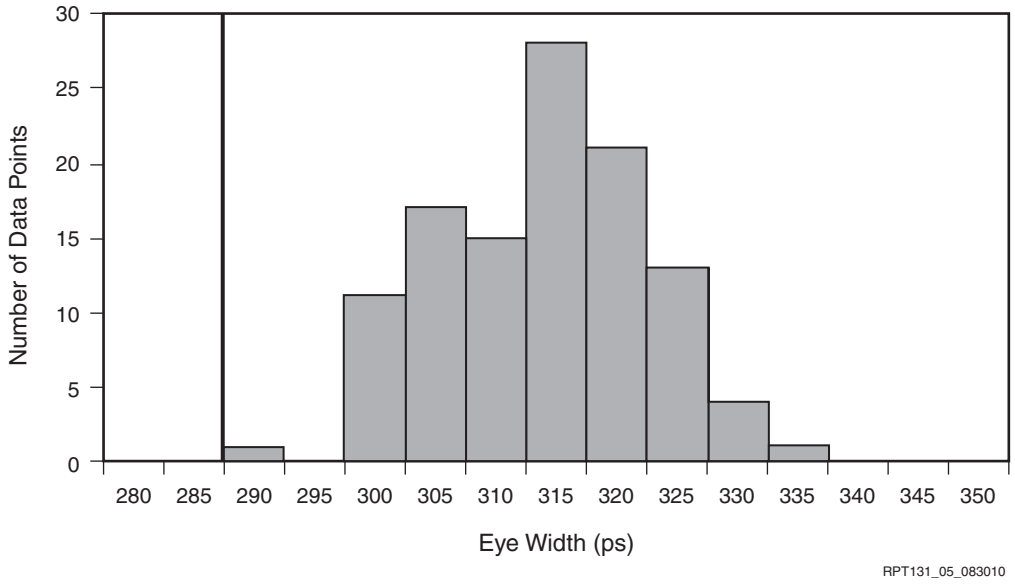

Figure 5: **Eye Width for the 2.5 Gb/s Line Rate**

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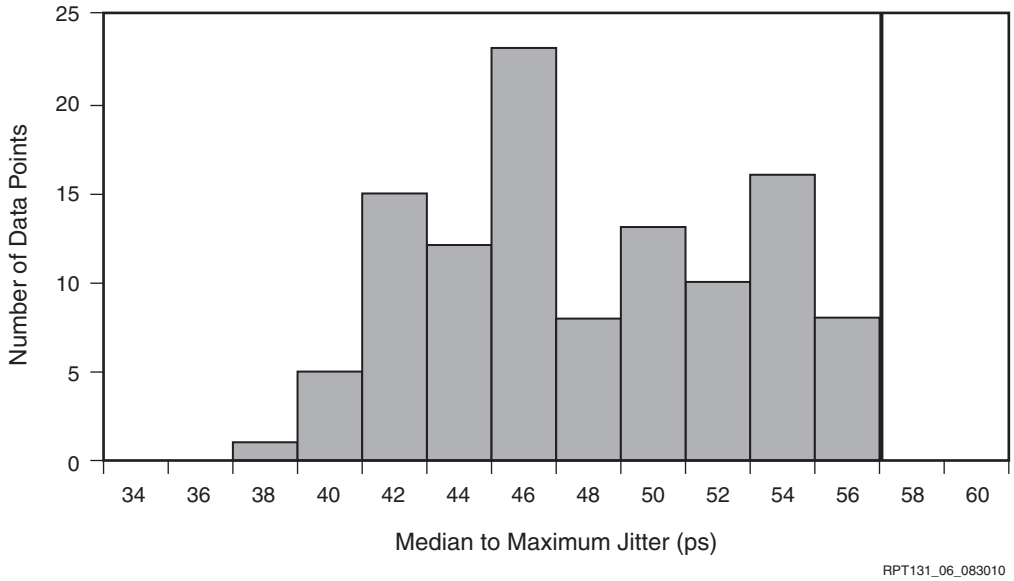

Figure 6: **Median to Maximum Jitter for the 2.5 Gb/s Line Rate**

Table 7: **Minimum and Maximum Test Results for the 2.5 Gb/s Line Rate**

Test Name	Min	Max	Units
Unit Interval (UI)	400.04	400.06	ps
Template Tests	Zero	Zero	Number of failures
Peak Differential Output Voltage	495.4	595.0	mV
Eye Width	288.26	331.74	ps
Median to Max Jitter	36.80	56.21	ps

Notes:

1. The Peak Differential Output Voltage is programmable by setting TXDIFFCTRL and TXPREEMPHASIS.
2. The worst performing transceivers tested can improve the eye width margin by approximately 38 ps with a 125 MHz reference clock.
3. The worst performing transceivers tested can improve the median to maximum jitter margin by approximately 17 ps with a 125 MHz reference clock.
4. The margin gained with a 125 MHz reference clock is based on an external ICS874002AG-02 EVB PCI Express Jitter Attenuator with an onboard ICS874003-05 PCI Express Jitter Attenuator used to convert the 100 MHz reference clock from the PCI Express CBB to 125 MHz. This PCI Express Jitter Attenuator meets the PLL bandwidth and peaking requirements.

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SIGTEST Results for the 2.5 Gb/s Line Rate

Figure 7 shows a transition eye diagram, and Figure 8 shows a non-transition eye diagram generated from the SIGTEST application. The SIGTEST results were used only to compare the measurement results from the Agilent PCI Express automated test application. Figure 9 shows the summary of a SIGTEST result.

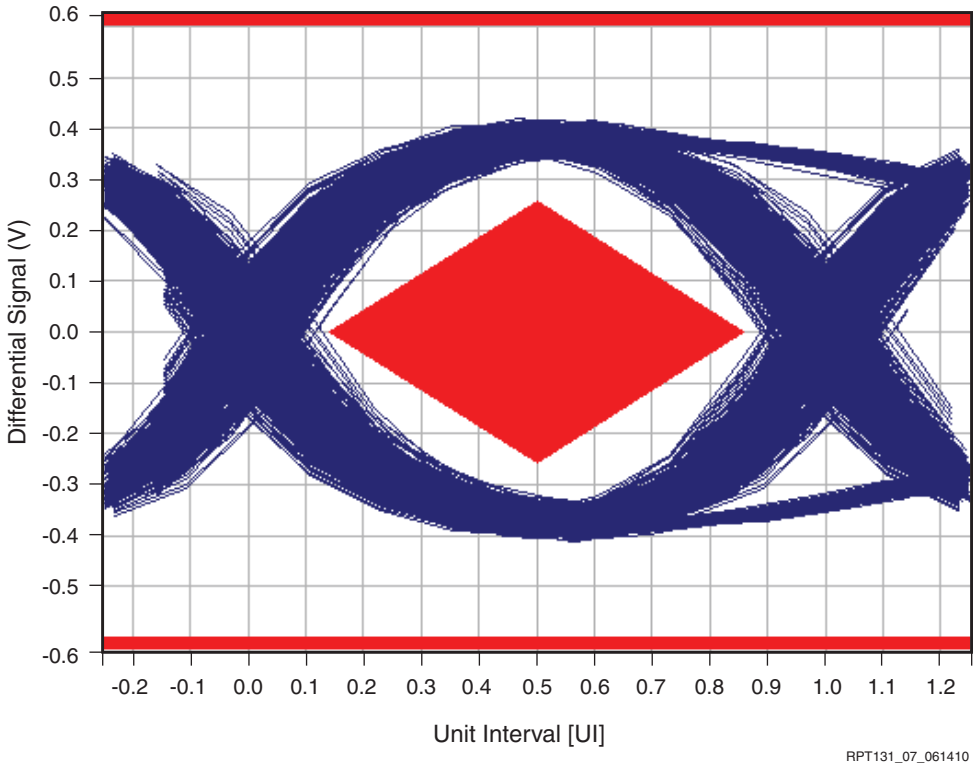

Figure 7: **SIGTEST Transition Eye Diagram for the 2.5 Gb/s Line Rate**

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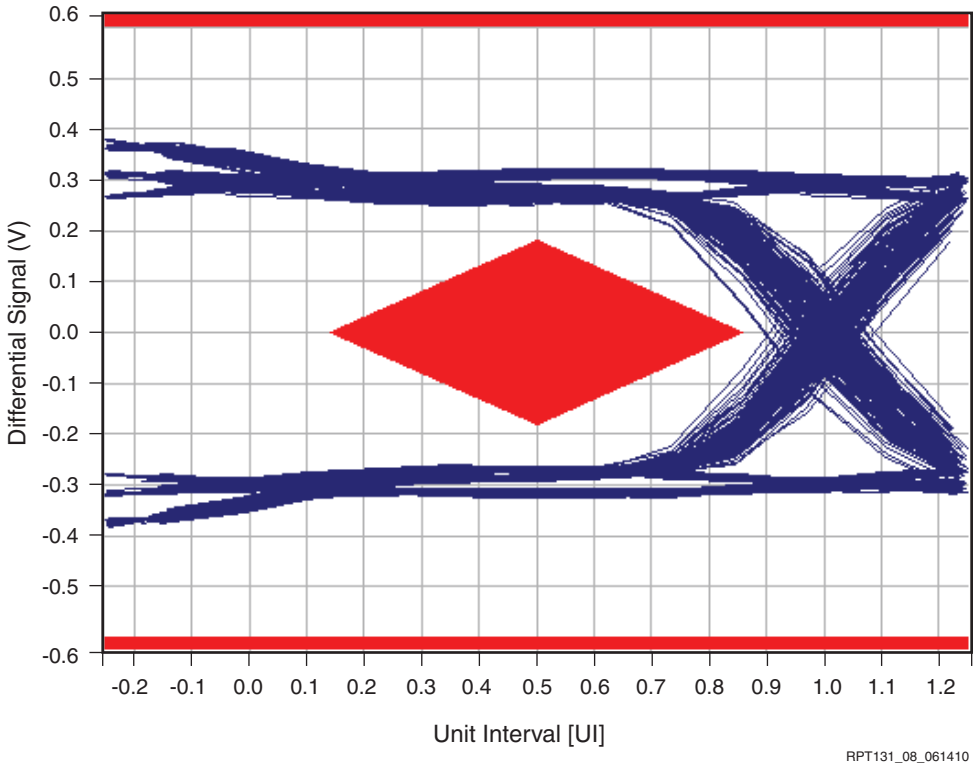

Figure 8: **SIGTEST Non-Transition Eye Signal Diagram for the 2.5 Gb/s Line Rate**

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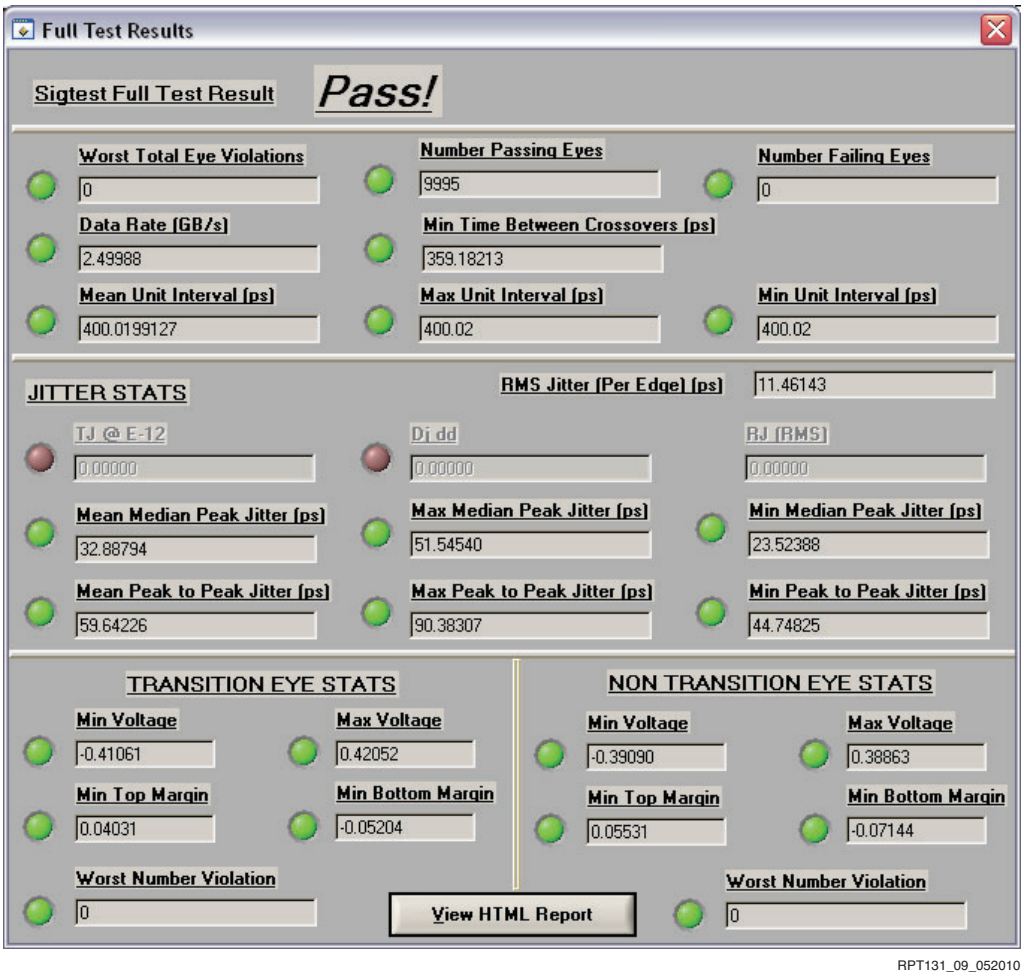

Figure 9: **SIGTEST Result for the 2.5 Gb/s Line Rate**

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Transmitter Differential and Common Mode Return Loss

Test Methodology

The *PCI Express Base Specification, Revision 1.1* defines the transmitter differential and common mode return loss as described in Table 8. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100Ω.

Table 8: **Transmitter Differential and Common Mode Return Loss Specification**

Parameter	Specification Range	Frequency Range	Units
TX Differential Return Loss	10 (minimum)	From 50 MHz to 1.25 GHz	dB
TX Common Mode Return Loss	6 (minimum)	From 50 MHz to 1.25 GHz	dB

The Agilent 8720ES Vector Network Analyzer (VNA) test equipment used for measuring the transmitter differential and common mode return loss interfaces to a host PC through a GPIB interface. Calibration begins after the measurement parameters are set. These VNA measurements are independent of voltage and are accurate up to 11 GHz. Table 9 defines the test setup and conditions. Figure 10 shows the return loss measurement setup.

Table 9: **Transmitter Differential and Common Mode Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 8720ES Vector Network Analyzer
TX Coupling/Termination	Differential, DC coupled into 50Ω to GND
Voltage	Typical Voltage
Temperature	Room Temperature
Load Boards	SP622 Spartan-6 FPGA GTP Transceiver Characterization Board, Revision A
FPGA	Spartan-6 FPGA XC6SLX45T FGG484
Reference Clock	Not necessary for this test
Frequency Sweep	50 MHz to 11 GHz (10 MHz steps)
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency	100 Hz

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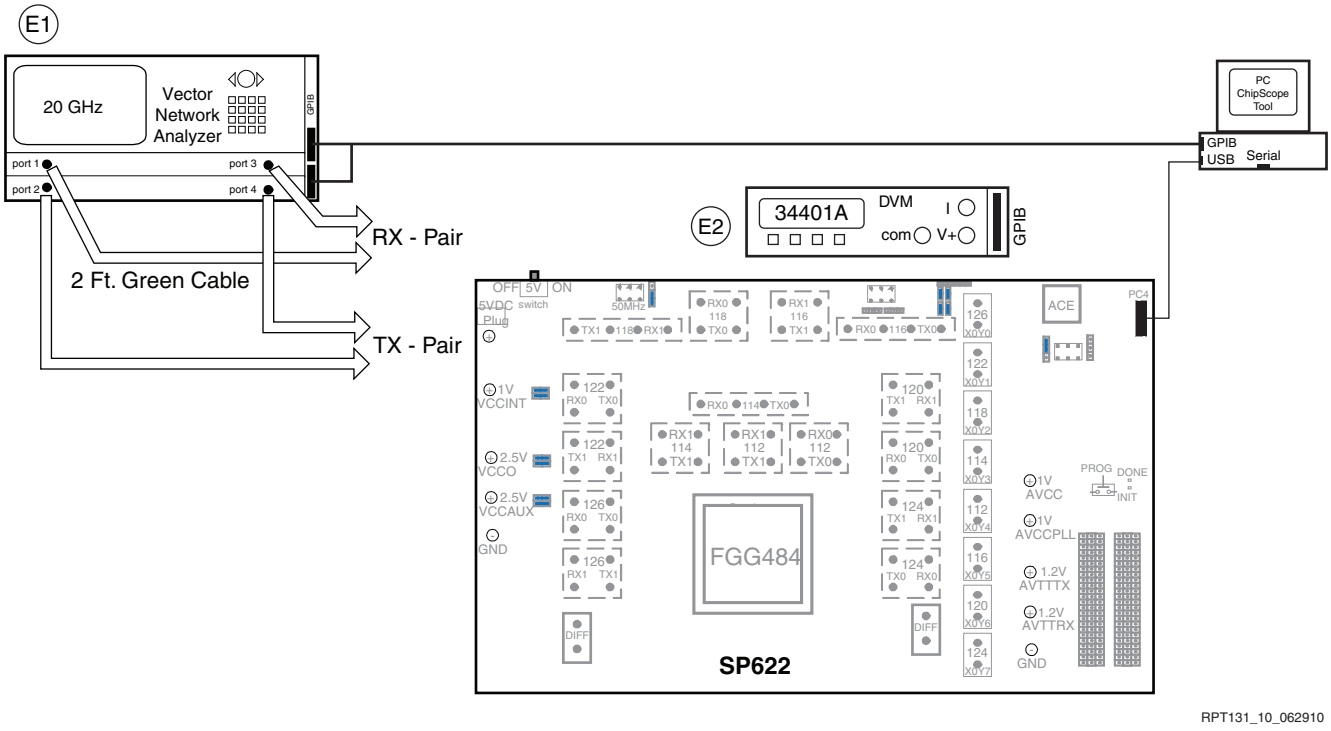

Figure 10: **Transmitter Return Loss Test Setup Block Diagram**

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Test Results for Transmitter Return Loss

Figure 11 describes the transmitter differential return loss measurement, and Figure 12 describes the transmitter common mode output return loss measurement. The return loss results are recorded in negative dB.

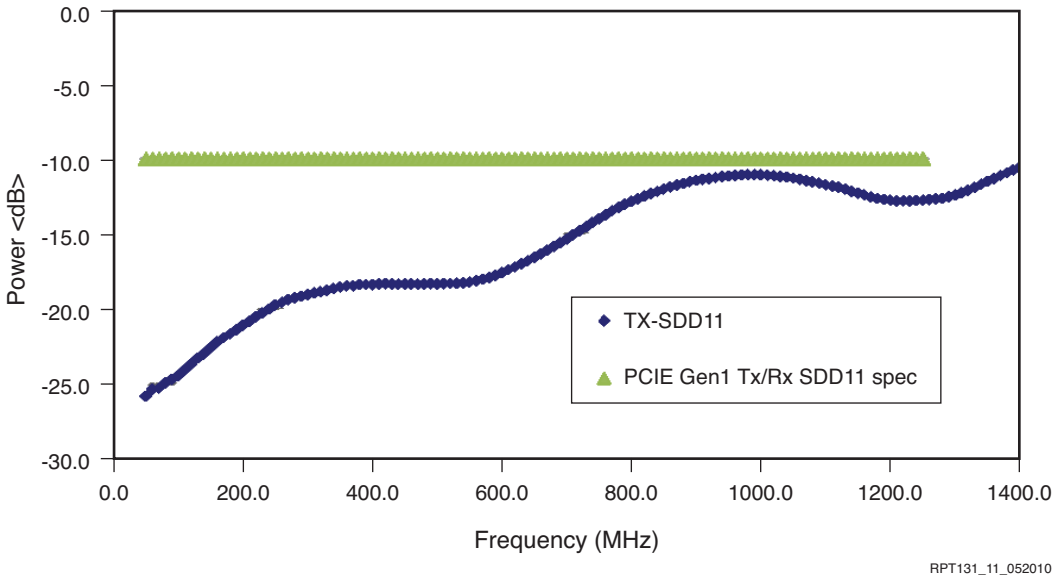

Figure 11: **Transmitter Differential Return Loss Measurement**

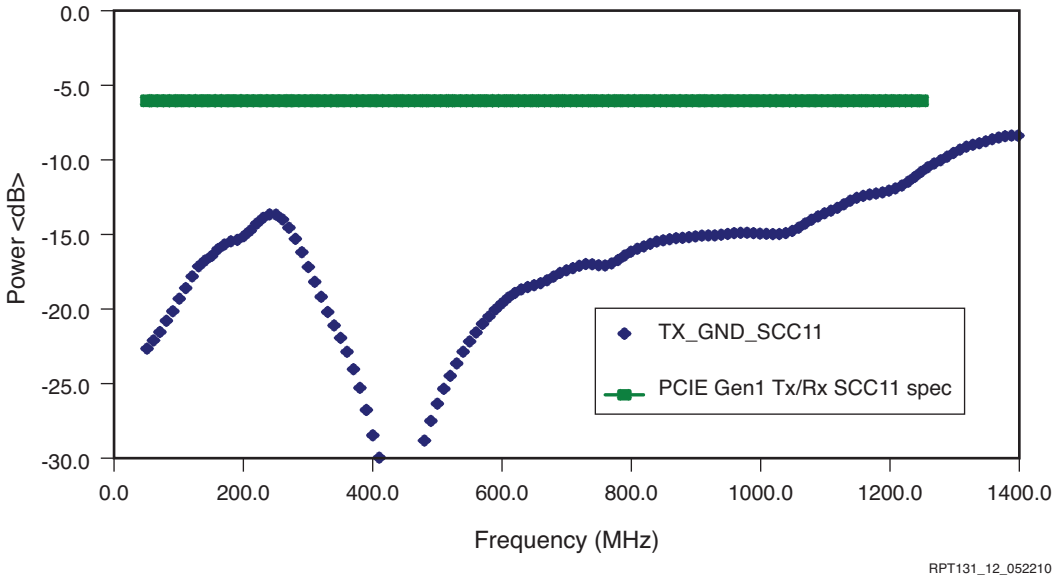

Figure 12: **Transmitter Common Mode Return Loss Measurement**

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PLL Bandwidth Test

Test Methodology

The PLL Bandwidth test consists of PLL bandwidth and peaking measurements. The *PCI Express Base Specification, Revision 1.1* defines the transmitter PLL bandwidth and peaking as described in Table 10.

Table 10: **PLL Bandwidth Specification for the 2.5 Gb/s Line Rate**

Parameter	Specification Range	Units
PLL Bandwidth	From 1.5 to 22	MHz
PLL Peaking	3 (maximum)	dB

This test is performed using the test setup shown in Figure 13. An Agilent J-BERT N4903B Bit Rate Error Tester is used as the clock source, and an Agilent DCA-J 86100C Digital Communication Analyzer with an 86108A Precision Waveform Analyzer is used to perform the PLL Bandwidth test. The Jitter Spectrum Phase Noise (JSPN) application running on an external host PC is used to control the measurement equipment via a GPIB interface. Hardware calibration was completed with the PCIe compliance pattern prior to data collection. The calibration and test procedure methodologies are documented in *PCI Express PLL Loop Bandwidth Test Methodology Users Guide*, *Agilent DCAj 86100C, 86108A Precision Waveform Analyzer*, or *83496B Clock Recovery Module*, and *J-BERT N4903A Bit Error Rate Tester*.

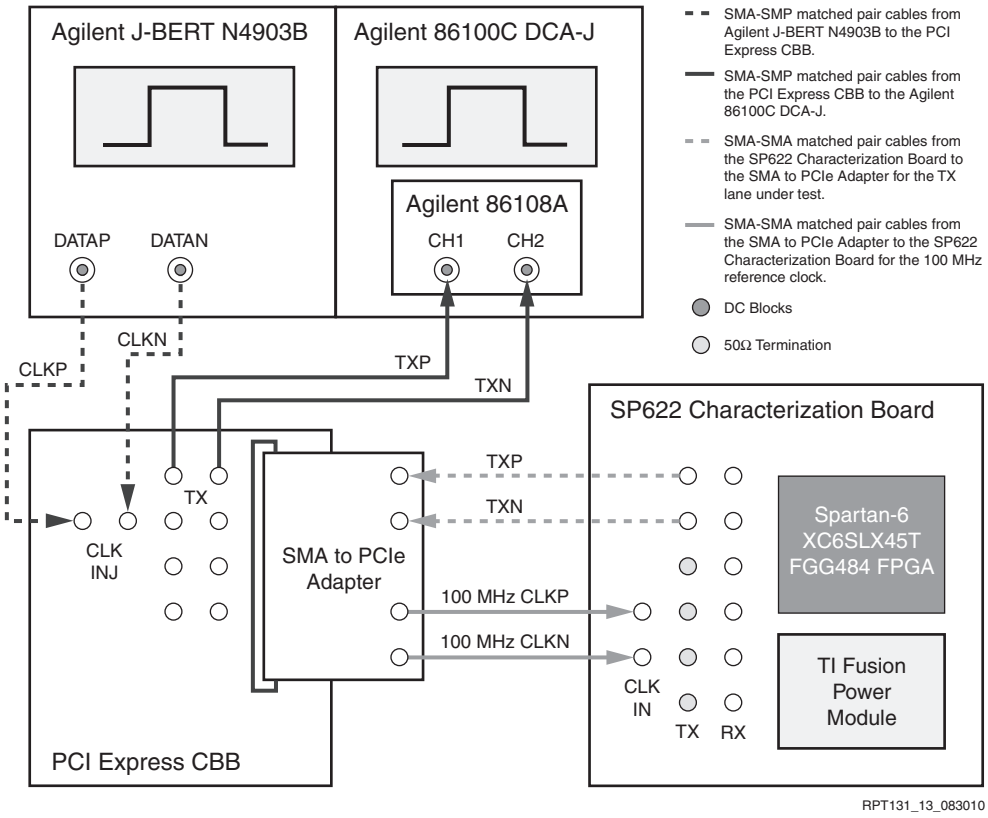

Figure 13: **PLL Bandwidth Test Setup Block Diagram**

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The Spartan-6 device under test is configured to transmit the PCI Express compliance pattern on the TX differential lanes on the SP622 board. This device is configured to the default PCI Express mode with the settings described in Table 11. The test setup and conditions for the PLL Bandwidth test are also defined in Table 11.

Table 11: **PLL Bandwidth Test Setup and Conditions**

Parameter	Value
Measurement Instrument	• Agilent J-BERT N4903B. • Agilent DCA-J 86100C Digital Communication Analyzer with 86108A Precision Waveform Analyzer: • AC coupled using DC blocks.
Software Application	Jitter Spectrum Phase Noise (JSPN) application: • Running on an external host PC to control the measurement instrument via GPIB. • PCI-SIG accepted methodology.
Voltage	TI Fusion Power Module: • Installed on the SP622 board to change the MGTAVTT and MGTAVCC voltages between V_{MIN} and $V_{MAX.}$
Temperature	Temperature Unit: • A socket attached with a temperature controller is used to change the temperature condition of the device under test between T_{-40}, T_0, $T_{100,}$ and $T_{125.}$
Data Pattern	Transmitting the PCI Express compliance pattern on the TX lanes of the SP622 board.
FPGA	Spartan-6 FPGA XC6SLX45T FGG484.

Load Boards	• SP622 Spartan-6 FPGA GTP Transceiver Characterization Board, Revision A:
	  • 50Ω terminator on TX channels not under test.
	  • On the various SP622 board channels used, there are about 4 inches of FR4 in the TX paths.
	• PCI Express Compliance Base Board (CBB) Revision 2.0:
	  • Standard PCI-SIG board for the Add-in Card Transmitter test.
	• SMA to PCIe Adapter, Revision D:
	  • Used to connect the SP622 board to the x16 interface of the PCI Express CBB.

Cables	• One pair of matched 50Ω Rosenberger SMA-SMP cables from the PCI Express CBB to the Agilent DCA-J 86100C. • One pair of matched 50Ω Rosenberger SMA-SMP cables from the Agilent J-BERT N4903B to the PCI Express CBB. • One pair of matched 50Ω SMA-SMA cables from the SMA to PCIe Adapter to the SP622 board for the 100 MHz reference clock. • One pair of matched 50Ω SMA-SMA cables from the SP622 board to the SMA to PCIe Adapter for the TX lane under test.

GTP Transceiver Attributes	• TX Amplitude and Pre-Emphasis:
	  • TXDIFFCTRL = `4'h8`
	  • TXPREEEMPHASIS = `3'h4`
	• PLL Charge Pump Configuration:
	  • PLL_CP_CFG = `8'h21`
	• Miscellaneous:
	  • PCI_EXPRESS_MODE = TRUE

Reference Clock	100 MHz sourced from the Agilent J-BERT N4903B.

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Test Results for the 2.5 Gb/s Line Rate

Figure 14 shows the histogram for the PLL bandwidth, and Figure 15 shows the histogram for PLL peaking. All results are measured across process, voltage, and temperature. Figure 16 shows an example of the jitter transfer function of a PLL bandwidth test. Table 12 summarizes the maximum and minimum test result values.

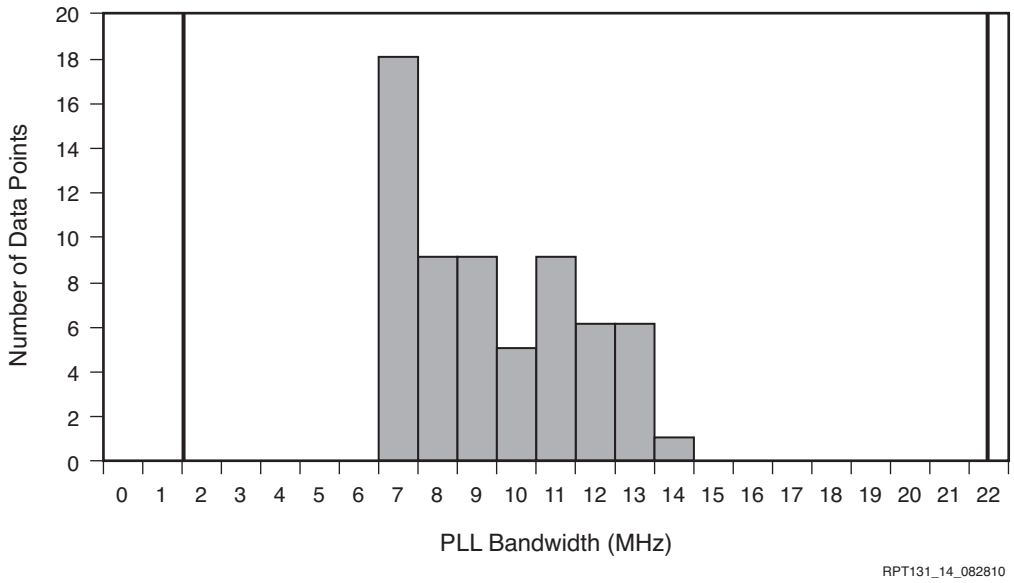

Figure 14: **PLL Bandwidth for the 2.5 Gb/s Line Rate**

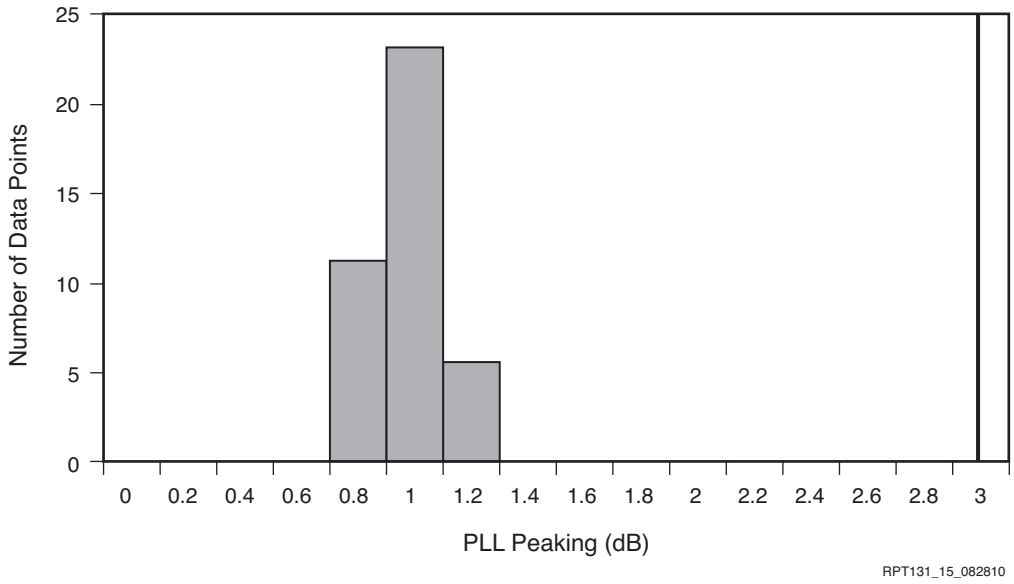

Figure 15: **PLL Peaking for the 2.5 Gb/s Line Rate**

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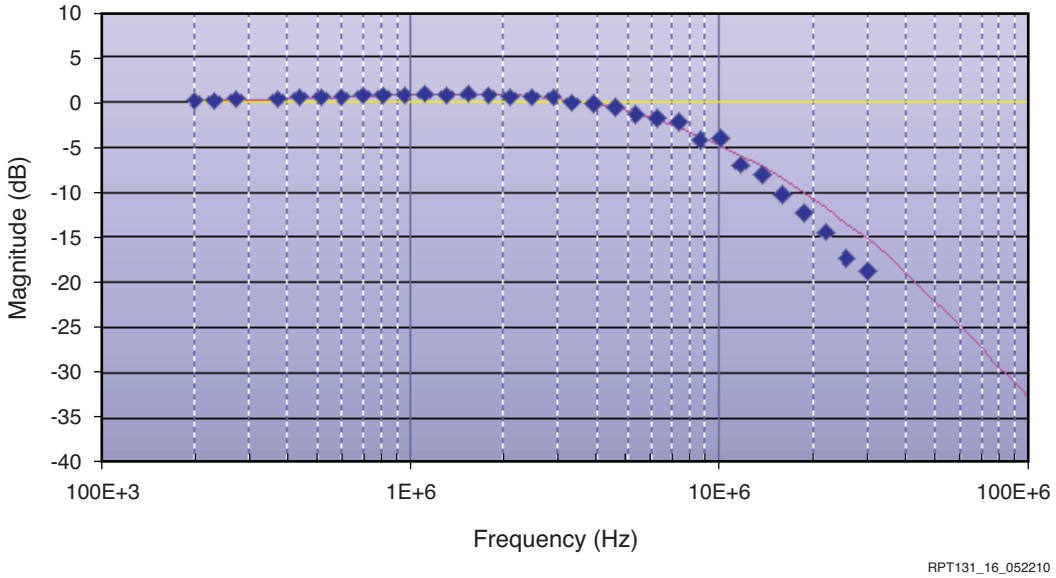

Figure 16: **Jitter Transfer Function for the 2.5 Gb/s Line Rate**

Table 12: **Minimum and Maximum Test Results for the 2.5 Gb/s Line Rate**

Test Name	Min	Max	Units
PLL Bandwidth	6.07	13.80	MHz
PLL Peaking	0.72	1.12	dB

Notes:

1. Hardware calibration with PCIe compliance pattern is performed prior to data collection.
2. These results are confirmed with a BERTScope CRJ 125A-PCIE using the PCI-SIG accepted test procedure documented in *PCI Express (Rev1.1) Test Methodology for PLL Loop Bandwidth Response in Add-in cards*.

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Receiver Input Jitter Tolerance Test

Test Methodology

The receiver input jitter tolerance requirements are derived from the *PCI Express Base Specification, Revision 1.1* and *PCI Express Card Electromechanical Specification, Revision 1.1*. The *PCI Express Base Specification, Revision 1.1* calls for the receiver to be able to meet 0.6 UI of jitter (240 ps at a BER of 10^{-12}) with an effective eye height of 175 mV.

The total jitter (TJ) of 0.6 UI is divided into components of random jitter (RJ) and deterministic jitter (DJ). The specification requires the device under test (DUT) to handle more than 5.47 ps RMS RJ. The rest of the TJ is contributed by DJ. In this test, DJ is added as 50% equalizable jitter, in the form of ISI using 40 inches of FR4 through the BERTScope ISI Board and 50% non-equalizable jitter in the form of Bounded Uncorrelated Jitter (BUJ). In the receiver jitter tolerance test, Sinusoidal Jitter (SJ) is swept from 1 kHz to 80 MHz to show that the receiver still has margin on top of the TJ required by the specification.

The test setup is shown in Figure 17. The CJTPAT pattern is generated from the BERTScope BSA125B-PCIE with various components of jitter injected and signal characteristics described in Table 13. The CJTPAT pattern is used because it is a more strenuous test pattern compared to the PCIe compliance test pattern. The GTP transceiver under test recovers the input data and transmits the pattern back to the Data In (Error Detector) of the BERTScope, where bit errors are measured. This is a synchronous test setup with no PPM offset between the BERTScope data generator and the reference clock provided to the GTP transceiver under test.

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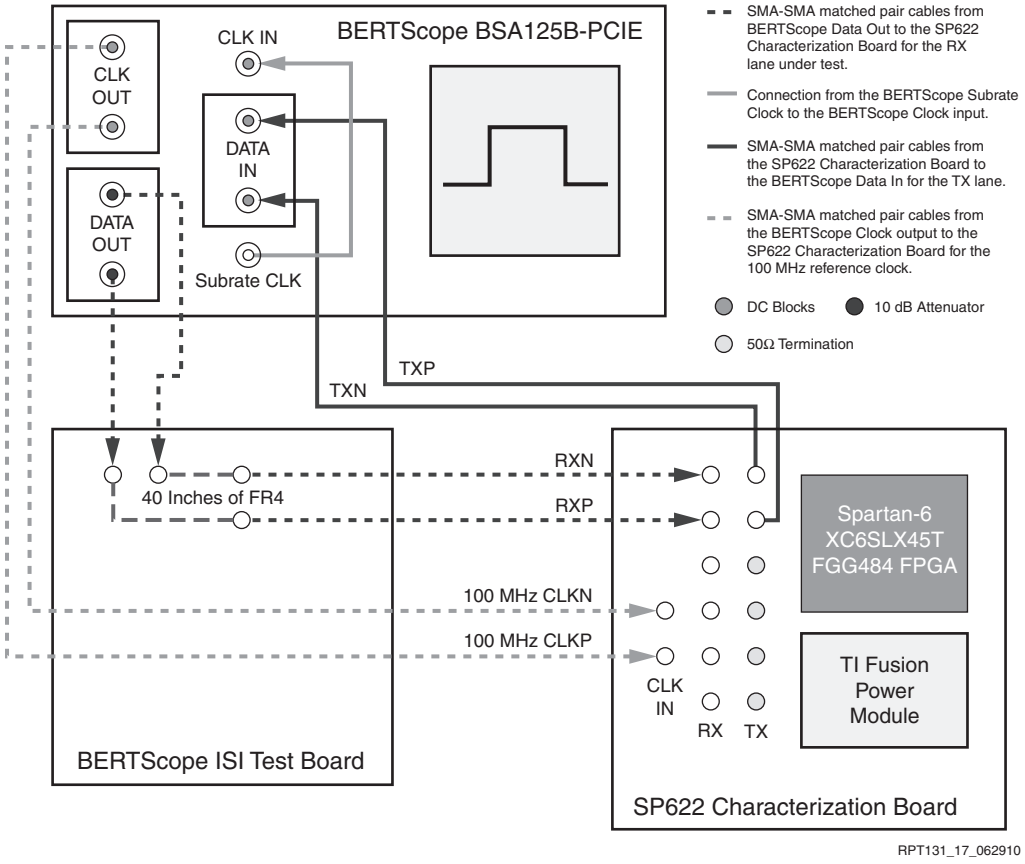

Figure 17: **Receiver Input Jitter Tolerance Test Setup Block Diagram**

Figure 18 shows the jitter injected to the GTP transceiver under test. In addition to all the jitter components added and amplitude settings applied as defined in Table 13, SJ is applied during the test.

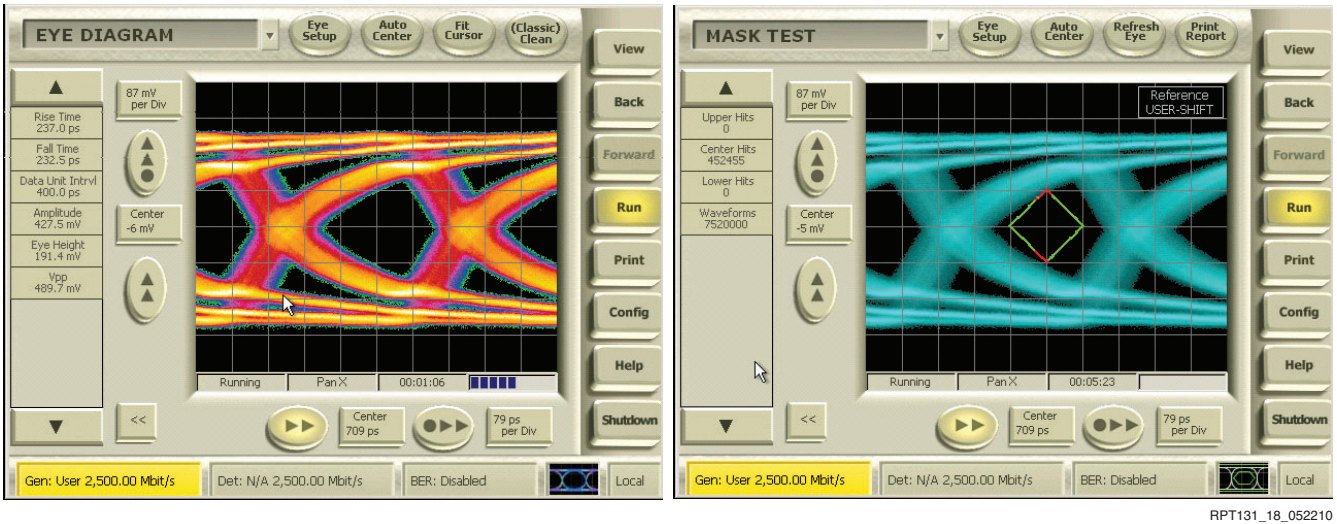

Figure 18: **Eye and Mask Diagrams with Jitter Injected for the 2.5 Gb/s Line Rate**

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Because of board limitations, the measurement is taken with at least four inches of channel between the RXP/RXN FPGA pins and the SMA connectors on the SP622 board. The added channel contributes additional DJ in the form of ISI.

Table 13 defines the test setup and conditions for the Receiver Input Jitter Tolerance test.

Table 13: **Receiver Input Jitter Tolerance Test Setup and Conditions**

Parameter	Value
Measurement Instrument	BERTScope BSA125B-PCIE: • AC coupled using DC blocks.
Voltage	TI Fusion Power Module: • Installed on the SP622 board to change the MGTAVTT and MGTAVCC voltages between V_{MIN} and V_{MAX}.
Temperature	Temperature Unit: • A socket attached with a temperature controller is used to change the temperature condition of the device under test between T_{-40}, T_0, T_{100}, and T_{125}.
Data Pattern	CJTPAT.
FPGA	Spartan-6 FPGA XC6SLX45T FGG484.
Injected Jitter	Sum of: • RJ (1.5 – 100 MHz RMS jitter) = 8.86 ps RMS • BUJ = 69 ps (PRBS7 at 1.999 Gb/s, 100 MHz low pass) • ISI =73 ps • Common mode noise from RX = 150 mV_{PP} (200 MHz) • SJ = Tested to Failure, Frequency Sweep = 1 MHz to 80 MHz
BER	10^{-12} (measured at 10^{-9}, extrapolated to 10^{-12})

Load Boards	• SP622 Spartan-6 FPGA GTP Transceiver Characterization Board, Revision A:
	  • 50Ω terminator on TX channels not under test.
	  • On the various SP622 board channels used, there are about 4 inches of FR4 in the RX paths.
	• BERTScope ISI Test Board:
	  • With a pair of 10 dB attenuators.
	  • Used to add 40 inches of FR4 on the receive path.

Cables	• One pair of matched 50Ω SMA-SMA cables BERTScope to the SP622 board for the 100 MHz reference clock. • One pair of matched 50Ω SMA-SMA cables from the BERTScope to the SP622 board for the RX lane under test. • One pair of matched 50Ω SMA-SMA cables from the SP622 board to the BERTScope for the forwarded data on the TX lane. • SMA-SMA connection from the BERTScope Subrate Clock to the BERTScope Clock input for the 100 MHz clock.

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Table 13: **Receiver Input Jitter Tolerance Test Setup and Conditions *(Cont'd)***

Parameter	Value

GTP Transceiver Attributes	• PLL Charge Pump Configuration:
	  • PLL_CP_CFG = `8'h21`
	• RX Equalizer:
	  • RXEQMIX = `2'b01`
	• RX CDR:
	  • PMA_RX_CFG = `25'h05CE044`
	• RX Termination:
	  • AC_CAP_DIS = FALSE
	  • RCV_TERM_GND = TRUE
	  • RCV_TERM_VTTRX = FALSE
	• Miscellaneous:
	  • PCI_EXPRESS_MODE = TRUE

Reference Clock	100 MHz sourced from the BERTScope.

Notes:

1. PLL_CP_CFG = `8'h00` was also characterized and included in the Receiver Input Jitter Tolerance test results.

Test Results for 2.5 Gb/s Line Rate

Figure 19 shows the receiver jitter tolerance SJ sweep. SJ is applied in addition to all the jitter components and amplitude settings as defined in Table 13.

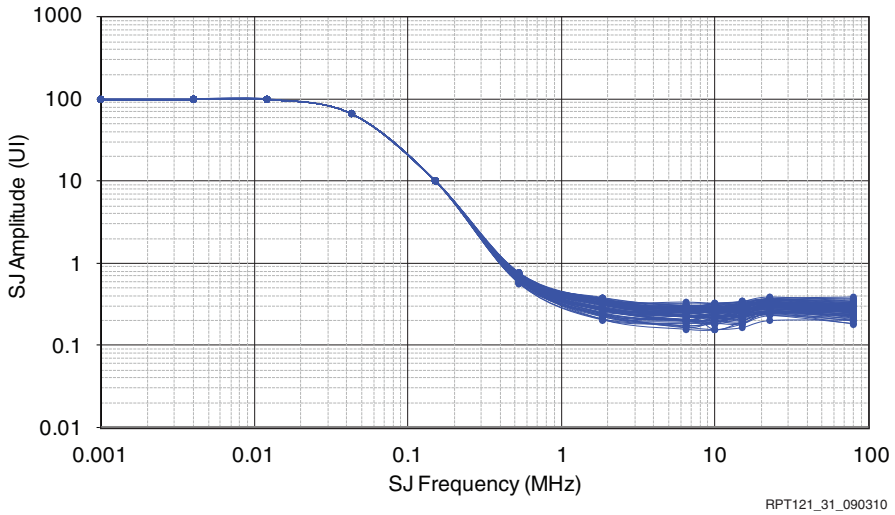

Figure 19: **Receiver Input Jitter Tolerance SJ Sweep for the 2.5 Gb/s Line Rate (CJTPAT, BER = 10^{-12})**

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Figure 20 shows that the SJ at 10.00 MHz. SJ is applied in addition to all of the jitter components and amplitude settings, as defined in Table 13.

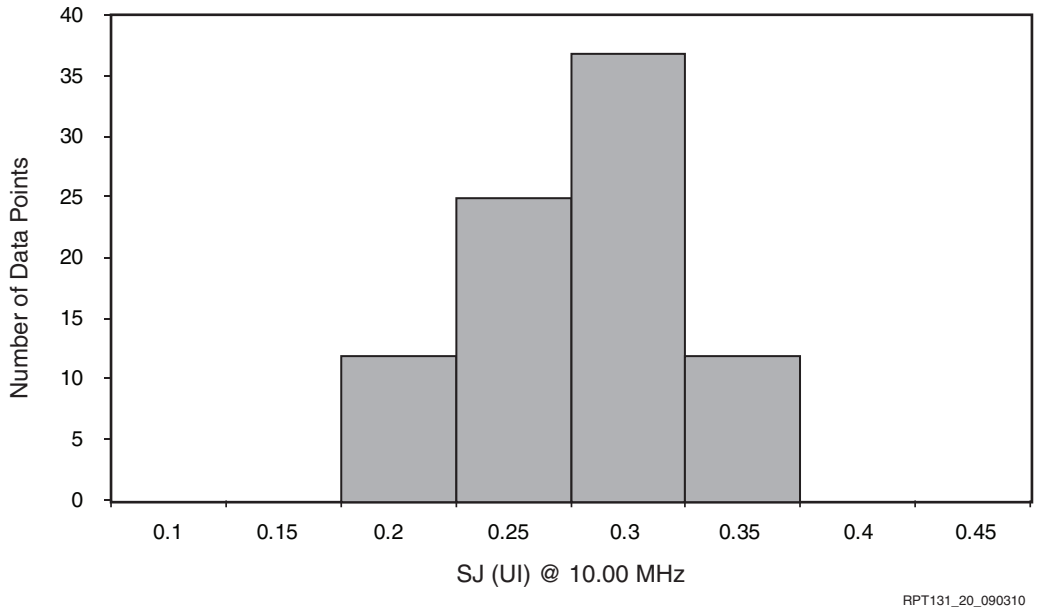

Figure 20: **Receiver Sinusoidal Jitter Tolerance at 10.00 MHz Test Results (CJTPAT, BER = 10^{-12})**

Table 14 shows the minimum receiver SJ tolerance at 10.00 MHz for the transceivers characterized. SJ is applied in addition to all the jitter components and amplitude settings as defined in Table 13.

Table 14: **Receiver Input Jitter Tolerance Test Results for the 2.5 Gb/s Line Rate**

Parameter	Test Condition	BER	Minimum SJ Tolerance	Units
Receiver Jitter Tolerance	SJ at 10.00 MHz	10^{-12}	0.154	UI

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Receiver Differential and Common Mode Return Loss

Test Methodology

The *PCI Express Base Specification, Revision 1.1* defines the receiver differential and common mode return loss as described in Table 15. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100Ω.

Table 15: **Receiver Differential and Common Mode Return Loss Specification**

Parameter	Specification Range	Frequency Range	Units
RX Differential Return Loss	10 (minimum)	From 50 MHz to 1.25 GHz	dB
RX Common Mode Return Loss	6 (minimum)	From 50 MHz to 1.25 GHz	dB

The Agilent 8720ES VNA test equipment used for measuring the receiver differential and common mode return loss interfaces to a host PC through a GPIB interface. Calibration begins after the measurement parameters are set. These VNA measurements are independent of voltage and are accurate up to 11 GHz. Table 16 defines the test setup and conditions. Figure 21 shows the return loss measurement setup.

Table 16: **Receiver Differential and Common Mode Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 8720ES Vector Network Analyzer
RX Coupling/Termination	Differential, DC coupled into 50Ω to GND
Voltage	Typical Voltage
Temperature	Room Temperature
Load Boards	SP622 Spartan-6 FPGA GTP Transceiver Characterization Board, Revision A
FPGA	Spartan-6 FPGA XC6SLX45T FGG484
Reference Clock	Not necessary for this test
Frequency Sweep	50 MHz to 11 GHz (10 MHz steps)
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency	100 Hz

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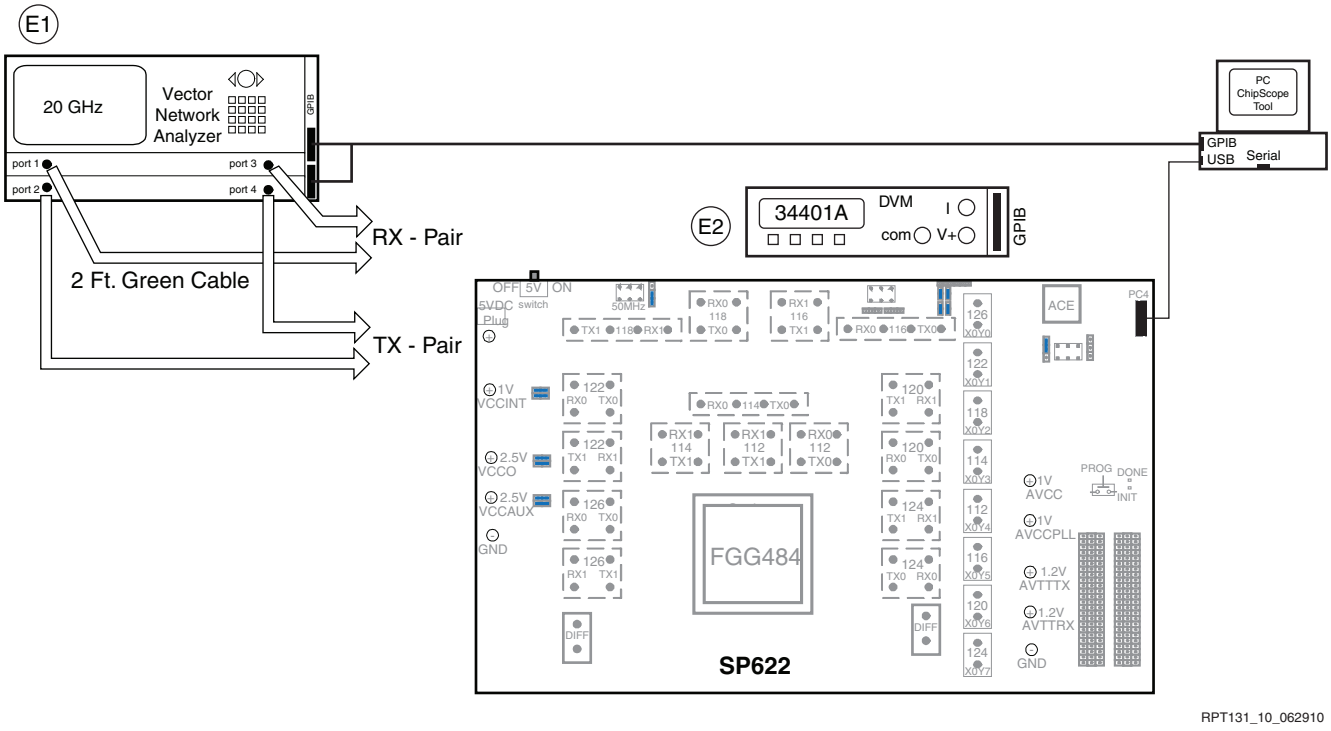

Figure 21: **Receiver Return Loss Test Setup Block Diagram**

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Test Results for Receiver Return Loss

Figure 22 describes the receiver differential return loss measurement, and Figure 23 describes the receiver common mode output return loss measurement. The return loss results are recorded in negative dB.

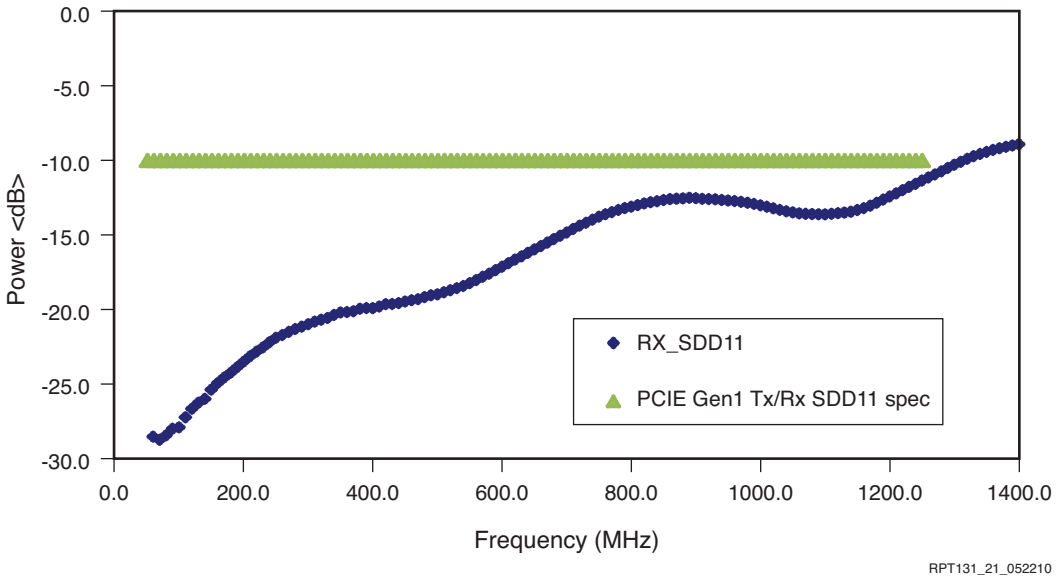

Figure 22: **Receiver Differential Return Loss Measurement**

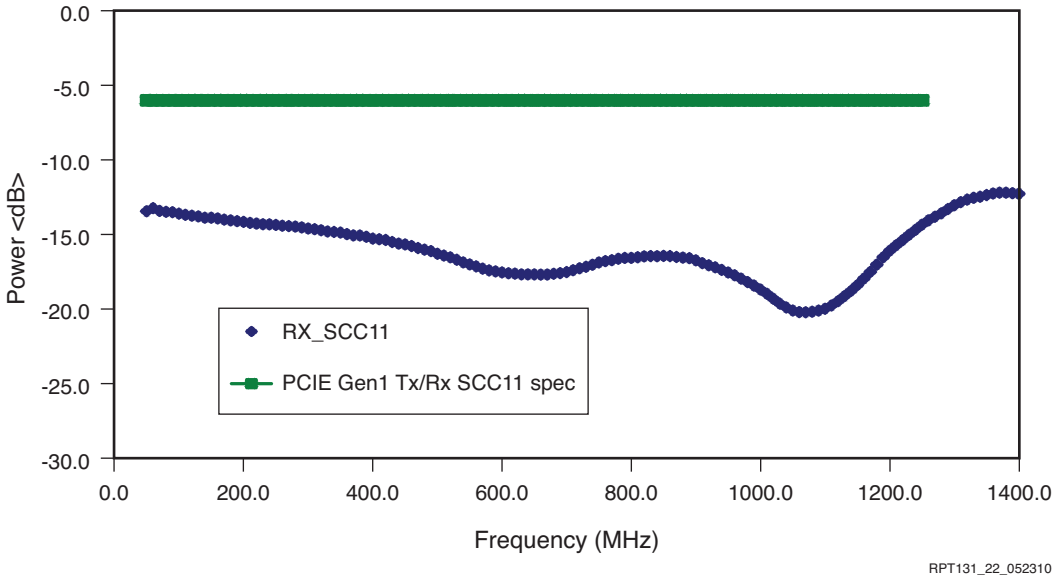

Figure 23: **Receiver Common Mode Return Loss Measurement**

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