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Scaling High-Performance Applications for Low Power and Cost

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As businesses and consumers expect more from portable electronics, the FPGA industry has been compelled to re-think how it serves these low-power, cost-sensitive markets. Application classes like medical and wireless communication devices, when scaled down in size for portability, still need advanced functionality. Small form factors grow an application's market by expanding to the edge of their user network, yet demand high performance to deliver the needed user experience. Portable medical devices, hand-held military communication equipment, and compact network devices must all deliver the performance guaranteed by their service providers.

As the industry's highest performance and lowest power FPGA, the Artix™-7 family redefines how to address cost-sensitive markets. The Artix-7 family utilizes the scalable, optimized architecture of the Xilinx 7 series FPGAs and delivers the industry's highest system performance per watt.

Edge Applications for Market Expansion

Medical devices, software defined radio, mobile communications infrastructure, and a host of other professional grade applications need to deliver high-end user experiences even as they scale down form factor to expand to the edge of their respective markets (see Figure 1). As complex systems that traditionally use high-end FPGAs, these scaled-down *edge applications* need to leverage similarly high-end capabilities in smaller packages. These FPGAs need to deliver high performance and manage power consumption—a difficult balance in terms of silicon technology and architecture.

Figure 1: **Scaling Down Ultrasound for Portability**

The Compounding Effects of Power Consumption

Developers of portable systems or those with limited access to the power grid place much of their attention on minimizing power—but not purely for extending operational time. They also consider the impact power has on cost, form factor, and performance.

As power consumption increases, so do cooling costs and the real estate needed for power management. More regulators, heat sinks, and cooling fans add to board cost and, in turn, require more power to operate, aggravating the energy problem. More components translate into more PCB area, which might be unacceptable for applications demanding a small form factor, and the additional board cost and development time can be prohibitive. In effect, high power consumption has compounding effects on overall product cost.

The other indirect effect is on performance; more switching activity in the logic fabric and across I/Os increases dynamic power. Make-or-break performance requirements can force a system to exceed a desired power budget, or stringent power requirements might not give adequate headroom for performance.

Because of these secondary effects caused by power consumption, selecting the right device can be non-trivial. Some FPGA vendors attempt to serve as many requirements as possible by focusing a technology on either high performance or low power, while in the process neglecting those applications that need to cost-effectively balance both.

Artix-7 Family for High Performance, Reduced Power, and Low Cost

Cost-sensitive markets that need high-end features have been underserved. As a result, they have been forced to move to more expensive mid-range devices or lower-end alternatives. The Artix-7 family focuses much of its innovation on serving these cost-conscious markets that need advanced functionality at the lowest power.

Low Power in a Scalable Optimized Architecture

Based on TSMC's 28 nm high performance, low power (HPL) process, Xilinx 7 series FPGAs offer the ideal balance of power, performance, and capacity. The 7 series consists of:

- Artix-7 devices for low power and low cost
- Kintex™-7 devices for an optimal balance of power and performance
- Virtex®-7 devices for highest performance and capacity

Careful comparisons to TSMC's low power (LP) and high power (HP) processes indicate that the HPL process achieves the lowest power and highest performance when considering the operating range of an FPGA. In principle, an HP process sees performance gains over an HPL process but at levels of static power that are untenable for programmable devices. Conversely, at low leakage points, 28 HPL offers a better performance-power metric than 28 LP, as shown in Figure 2. The ability to extend into a lower leakage region enables a low-power Artix-7 device, for example, to be substituted without switching to a different process.

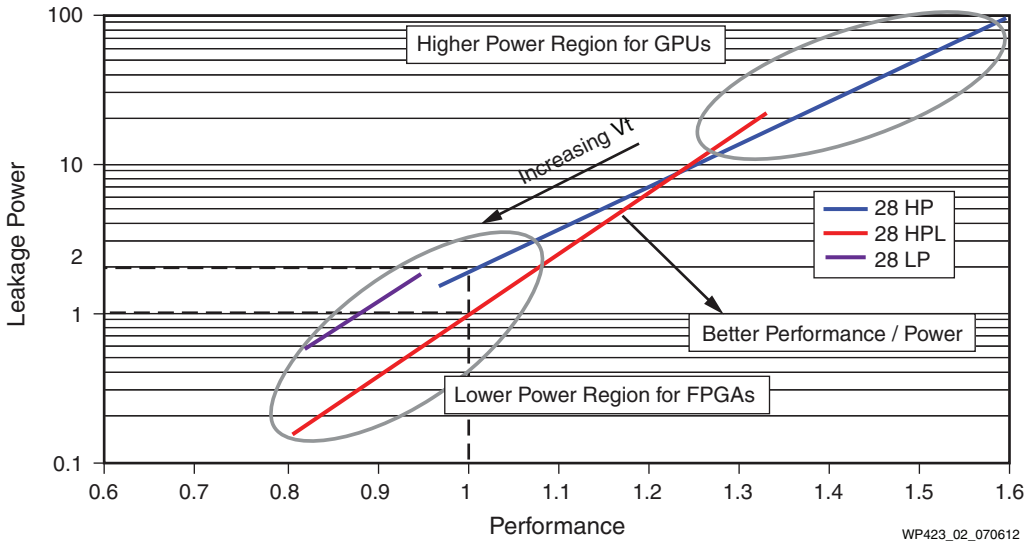

Figure 2: **HPL Process Enables Low Power and High Performance in the Artix-7 FPGA**

By using the HPL process and the same architectural building blocks for Virtex-7, Kintex-7, and Artix-7 FPGAs, the 7 series FPGAs provide easy design migration across families, eliminating time-consuming reoptimization. Targeting an Artix-7 device for an existing product ensures scalability for next-generation systems. Conversely, a high-performance Virtex-7 or Kintex-7 FPGA-based system can be migrated to an Artix-7 FPGA if an application needs to be scaled down to reduce size, cost, or power. For more information, refer to WP373, *Xilinx Redefines Power, Performance, and Design Productivity with Three Innovative 28 nm FPGA Families: Virtex-7, Kintex-7, and Artix-7 Devices*.

The breakthrough of combining the HPL process with the Xilinx 7 series architecture cuts total power consumption by 50% compared to the previous generation (see Figure 3). This provides headroom for additional performance, logic density, I/O bandwidth, and signal processing. Designers have the flexibility to either lower power by 50% or take advantage of greater performance and capacity at previous power budgets. For more information and benchmark data on Artix-7 FPGA power reduction, go to: www.xilinx.com/power.

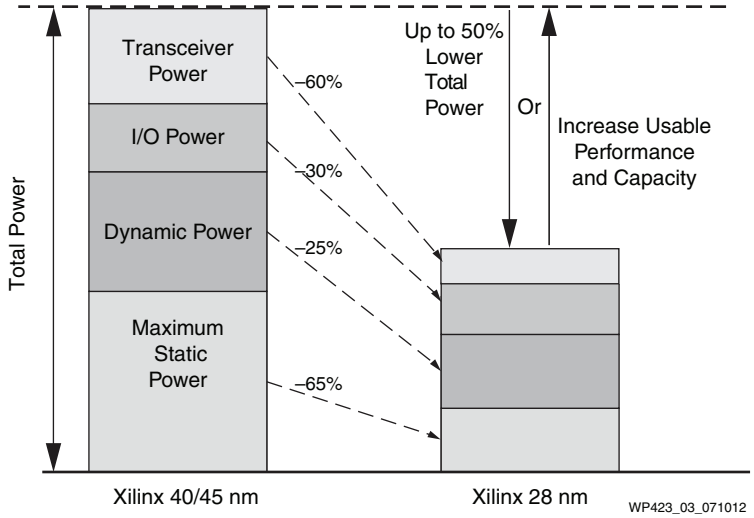

Figure 3: **The 28 nm HPL Process Reduces Power Consumption by 50 Percent**

Logic Fabric Optimized for Power and Performance

As part of its scalability, the 7 series architecture uses the same flexible logic across all families. Configurable logic blocks (CLBs) consist of two slices, each comprised of four 6-input look-up tables (LUTs), four flip-flops, carry-chain logic, and four additional flip-flops that can be configured as latches. There are also dedicated resources that can be used to build large high-speed multiplexers (as opposed to utilizing LUTs).

The 7 series slice architecture is based closely on that in the Virtex-6 and Spartan®-6 families, using the same LUT structure, control logic, enables, and outputs. These similarities between the Spartan-6 and Artix-7 devices provide an easy migration path. For more information, refer to WP405, *Xilinx 7 Series FPGAs: The Logical Advantage*.

With a block RAM-to-logic ratio of up to 18.5 Mb within 360K logic cells, and 1,040 DSP48E1 slices for the same capacity, the Artix-7 FPGA rivals the logic density of mid-range products while still benefiting from lower power and cost. The DSP resources provide up to 1,306 GMACs of DSP performances—3X that of the competition—useful for imaging and communication applications that require extensive processing capacity.

High-Speed Interfaces

Supporting up to sixteen 6.6 Gb/s transceivers that have been optimized for low power, the Artix-7 family offers the fastest line rates for cost-sensitive markets. These transceivers support pre-emphasis and continuous time linear equalization (CTLE) to compensate for signal distortion across transmission channels. With 211 Gb/s of total throughput, the Artix-7 family is a low-cost alternative for bandwidth-sensitive applications that would otherwise require mid-range solutions.

Because memory read/write bandwidth can affect overall system performance, the Artix-7 family offers up to 1,066 Mb/s DDR3 data rates, the highest in the industry for FPGAs in its class. The memory solution consists of a flexible controller and physical layer (PHY) for interfacing designs and AMBA® advanced extensible interface (AXI4) slave interfaces to DDR3 and DDR2 SDRAM devices. The controller supports an array of external memories for flexible system design, for example, streamlined access to video and data storage.

Small Form Factor for Reduced Cost

The Artix-7 family features a 50% smaller package at equivalent density compared to the Spartan-6 family. As low-cost devices move into more compact applications, such as hand-held, software-defined radios, feasibility depends on the device's form factor and the restrictions caused by limited PCB area. Artix-7 devices are offered in various types of low-cost wire-bond packages—from chip-scale packaging with 0.8 mm ball spacing, the smallest form factor, to BGA packaging with 1.0 mm ball spacing, ideal for low-cost PCB manufacturing.

Market Applications

The following examples show how high-performance applications can scale for portability and accessibility. Each example demonstrates how the Artix-7 FPGA enables edge applications to deliver high processing power and bandwidth while benefiting from small form factor and low power consumption.

Portable Ultrasound

For decades ultrasound has been critical to modern medicine, helping doctors gain insights into the inner workings of the body. In recent years, thanks to portability, ultrasound is being used not just in medical facilities but by doctors making house calls or working in remote locations. In fact, portable ultrasound is evolving into a competitive, high-volume market. Because a certain level of image quality is required, the design challenge is balancing image quality, power consumption, cost, and form factor.

Optimized DSP for High Image Quality and Lower Power

Resolution and penetration depth (i.e., depth of the tissue to be examined or treated) depends on the transducer—the device's probing module, as shown in Figure 4. These transducer channels issue sound waves that are ultimately reflected back to generate a 2-D or even 3-D image of various tissue layers of the body. The receiver of the front end of the beamformer—one of the most differentiating components of the system—renders this image, demanding extensive DSP resources.

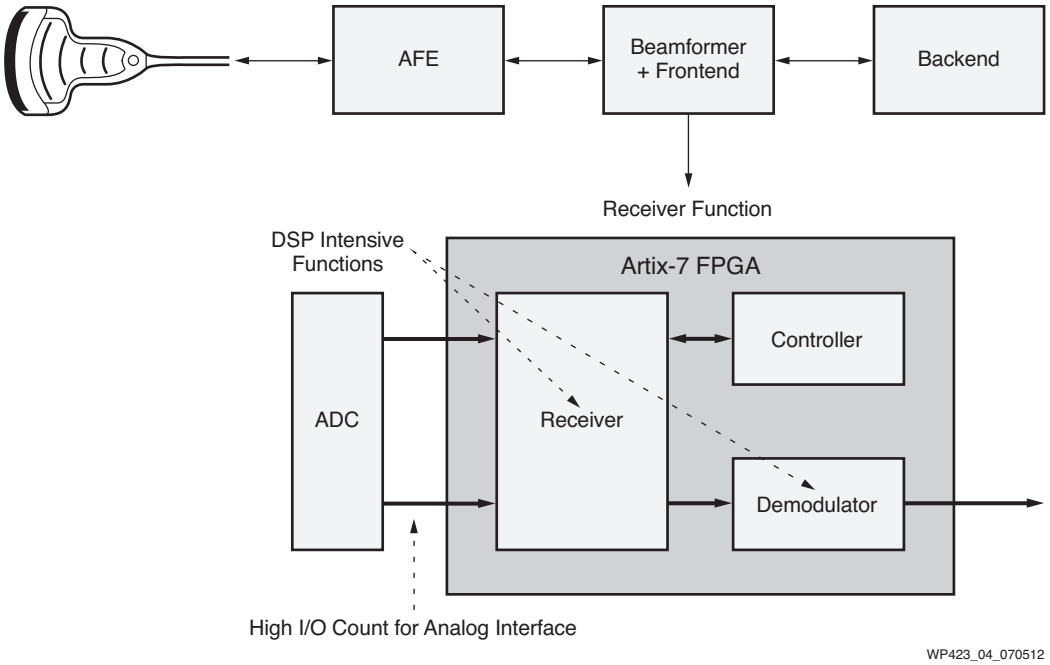

Figure 4: **High DSP Performance and I/O Count for Portable Ultrasound**

The required DSP bandwidth also leads to more power consumption. Because power supplies for medical systems have stringent requirements for safety and quality, success of a product depends equally on battery life and the ability to run on a limited power source.

With up to 1,040 DSP blocks, the Artix-7 FPGA provides 35% more DSP resources than the competition. The DSP slices provide 25x18 systolic elements to enable pre-adder multiply-accumulate engines. They contain low-latency pipeline stages and support pattern detection. Because they are built on the 28 nm process, 7 series DSPs offer improved performance at lower cost and lower power than their predecessor. A competitive comparison of power consumption is shown in Figure 5, with design resources shown in Table 1. Because 592 pins are required to support the 128-channel transducer, the competition is forced to go to its mid-range device.

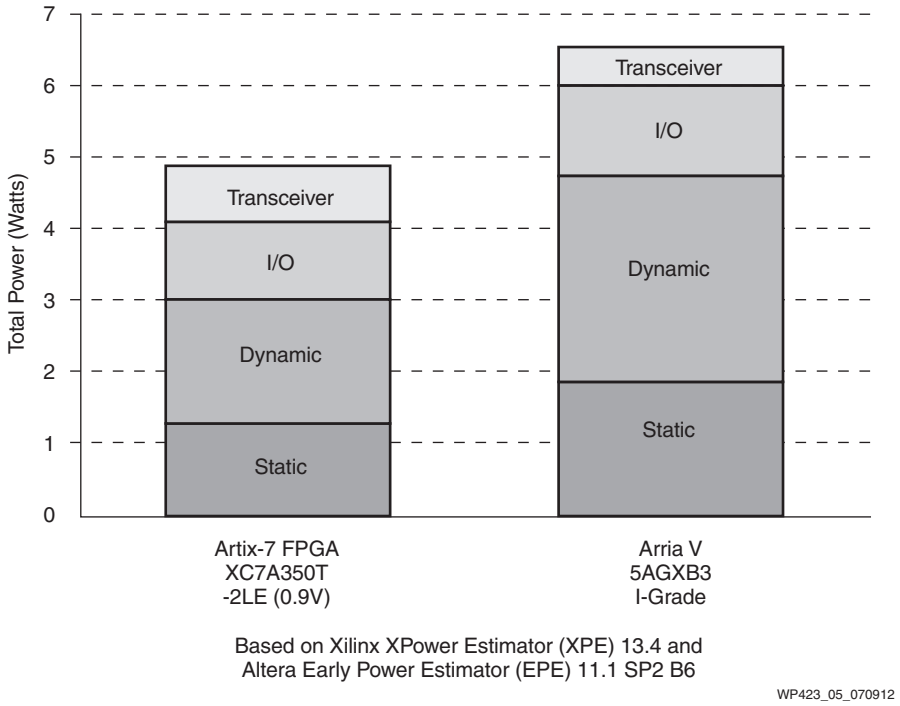

Figure 5: **34% Higher Power Consumption in Competing Device for Portable Ultrasound RX Front-End Beamformer**

Table 1: **Resource Count for Portable Ultrasound RX Beamformer**

Resource Type	Resource Count
Logic Cells	158K
Flip-Flops	114K
Block RAM	3,744 Kb
DSP Blocks	226
PCIe® Blocks	2
Core Frequency	40, 160 MHz
LVDS I/Os	288, 250 Mb/s
LVCMOS I/Os	48, 125 Mb/s
	256, 40 Mb/s
Transceivers	6, 3.125 Gb/s
	2, 2.5 Gb/s
Environment	T_j = 100°C, Max Process

High-Speed Transceivers for Complex Interfaces

The high bandwidth of the front end of the beamformer places a burden on I/O count and throughput between components. A major bottleneck is interfacing to the analog front end, where I/Os interface with parallel digital-to-analog converters (DACs) to transmit signals, and LVDS analog-to-digital converters (ADCs) interface with receive signals. This high number of I/Os complicates routability both in the FPGA and on the PCB.

Fortunately, next-generation portable ultrasound is moving to the JESD204B analog interface standard, which uses a 6.25 Gb/s serial interface to the analog component, minimizing both transmit and receive I/O count. The Artix-7 FPGA supports up to sixteen 6.6 Gb/s transceivers that can interface with the JESD204B standard, reducing pin count dramatically. For future systems—a 128-channel ultrasound device, for example—a 288-pin receive channel can be reduced down to as few as 16 transceiver pins; transmission pin reduction can be even greater. With only 5 Gb/s transceiver support, the competition's low-cost family cannot support this standard, nor can most ASICs on the market today.

For more information, refer to WP378, *Xilinx FPGAs in Portable Ultrasound Systems*.

Military Software-Defined Radio

One of the most ideal fits for the Artix-7 FPGA is in military software-defined radio (SDR). A military SDR network can comprise permanent military bases, mobile command centers, ground and airborne vehicles, individual foot soldiers, and much more. However, SDR systems at the “edge” of the network (worst-case use locations) often require higher transmit power—which typically leads to higher battery drain, increased size and weight (often driven by the need for bigger batteries), and ultimately to higher costs.

In addition, extensive DSP processing capacity is needed to support a variety of radio protocols (each with unique waveform characteristics) for voice, data, and video communication modes. Supporting many protocols is challenging, as is maintaining the required level of security in all protocols. In addition, the SDR must be able to operate reliably from worst-case radio locations within a complex strategic topology as well as in dense radio frequency (RF) spectrum environments that can exacerbate undesired cross-channel interference and receiver desensitization.

SDRs must be designed for:

- The capability to recognize and support encoding/decoding of many different communications protocols
- High-performance waveform processing in all supported protocols
- Small form factors, permitting a high degree of designed-in portability
- Minimal power consumption by the FPGA, providing extended use periods between battery replacement/recharge

DSP Processing Capacity for Wideband Protocol Support

Critical to an SDR is the modem that performs baseband signal preprocessing and RF signal improvements. Because of its parallel processing-based architecture and reconfigurability, an FPGA implementation of the modem is common—and the Artix-7 FPGA is an ideal fit for this application, as shown in Figure 6. With up to 1,040 DSP slices, the Artix-7 device can provide up to 1,306 GMACs of DSP performance—three times that of competing FPGAs, and far greater than any stand-alone DSP processor or GPU.

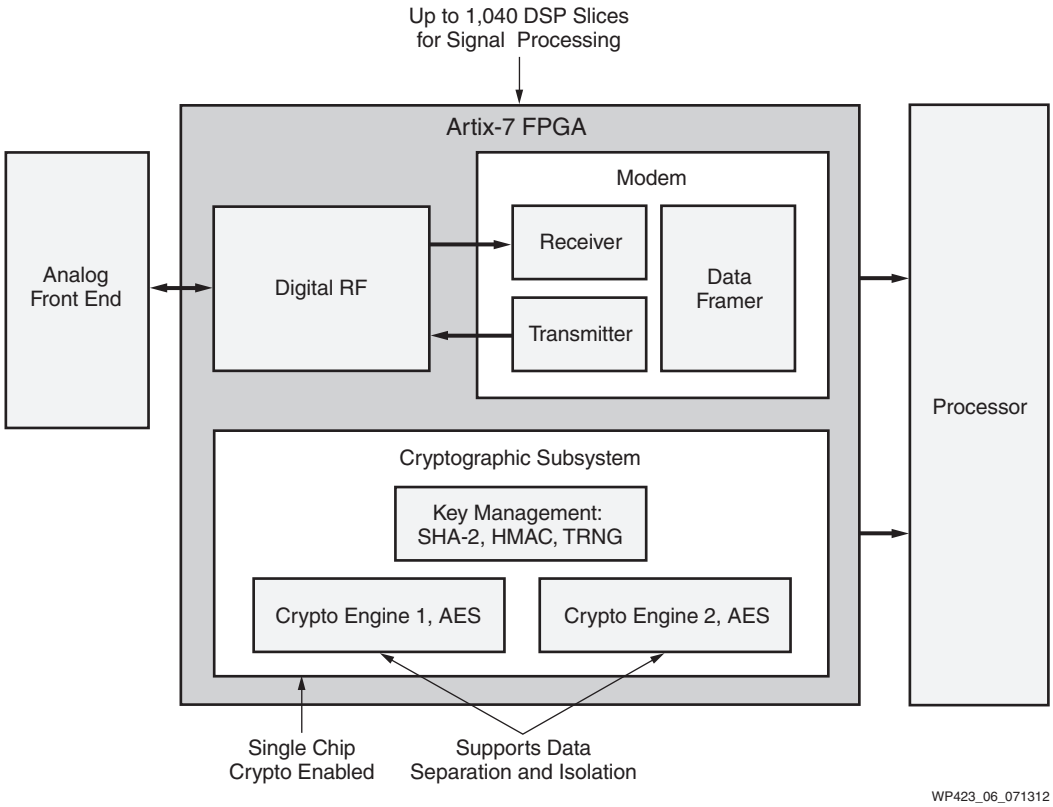

Figure 6: **System Integration for Software-Defined Radio**

Low Power for Long Battery Life

While DSP processing is critical, limitations of battery operation demand just the right performance-to-power balance. The Artix-7 FPGA's performance per watt ensures long battery life while still providing the needed processing capacity. As a matter of comparison, a typical ASSP-based implementation is comprised of a DSP processor and ASSP for the modem function, along with a 3-device Cryptographic engine. The Artix-7 A200T device consumes up to 35% less power than such an implementation.

Small Form Factor for Hand-Held Radio

Size and weight are high priorities when deploying SDRs for foot soldiers. The Artix-7 A100T FPGA is available in a 15x15 mm package with 101,440 logic cells, the industry's smallest FPGA for its capacity. With 215,360 logic cells in a 19x19 mm package, the Artix-7 A200T FPGA is an ideal solution for implementing an SDR modem as well as a cryptographic engine, as represented in Figure 6.

Single-Chip Cryptographic Solution for System Integration

Because security is a major concern in SDR, a key requirement enforced by the National Security Agency is the compartmentalization of encrypted and unencrypted data. Typically, this would require two separate devices, but Xilinx supports an Isolation Design Flow (IDF) that enables multiple physically isolated functions to be implemented within a single FPGA. IDF utilizes a "fence" of unused device components between each function, ensuring the system meets security requirements while still benefiting from single-chip integration.

Wireless Backhaul: High Bandwidth in Urban Locations

Mobile backhaul has come to the forefront within cellular communications networks due to the rapid growth in data traffic. Because the majority of the growth in cellular traffic is happening in urban and suburban areas where fiber media is often not practical, operators plan to boost capacity by deploying small cells at street level in places like lamp posts, traffic lights, and walls of adjoining buildings. To interconnect these small cells in clusters and to connect them to the nearest aggregation points, operators must deploy low-power, low-cost backhaul units, whose microwave radio links can span up to tens of miles.

High-Speed Transceivers for Bandwidth Support

A traditional mobile backhaul unit typically supports several Ethernet links. In wireless mobile backhaul, the traffic is forwarded between Ethernet links and radio channels using an internal Ethernet switch. High-speed transceivers are required at both ends of the unit, as shown in the generic block diagram in Figure 7. As a low-cost alternative, the Artix-7 family delivers maximal bandwidth with its sixteen 6.6 Gb/s transceivers for both Ethernet and RF links using JEDEC JESD204B connectivity to data converters.

Integrating Multi-Chip Functionality onto a Single Device

One half of the backhaul unit contains packet processing, traffic management, and timing synchronization functions. The other half of the unit supports modem channels for signal processing. For modem functionality, two requirements are key:

- Adequate high-performance DSP processing
- High-speed transceivers that interconnect with the data converters to produce high rates of data throughput

The Artix-7 devices have the right mix of logic density, IP support, and DSP resources to support these functions. The Artix-7 A200T device, for example, with 215,360 logic cells, can integrate a backhaul solution composed of all the needed packet processing, traffic management, and timing and synchronization blocks as well as a single high-speed radio channel. The Artix-7 A350T device can support up to two high-speed radio channels, as shown in Figure 7.

A typical ASIC/ASSP-based solution needs a stand-alone Ethernet switch, a traffic manager function in an FPGA, an external timing and synchronization device, one modem device per channel, external PHY for serial connectivity, and a control plane CPU, representing a 7-device solution—versus the Xilinx two-device programmable implementation shown in Figure 7.

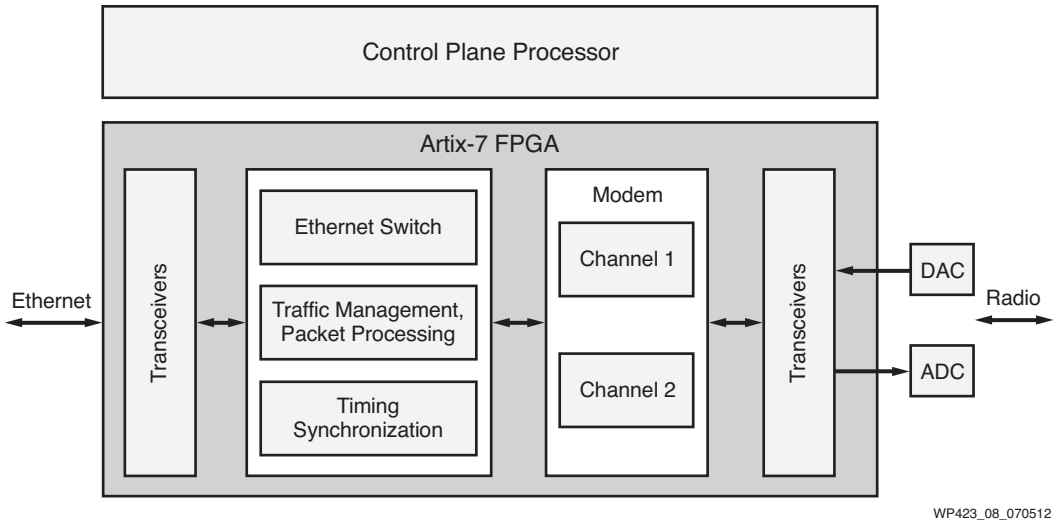

Figure 7: **Integrating Multi-Device Functionality for Microwave Mobile Backhaul**

Low Power in a Small Form Factor

To maintain low visual impact, backhaul units are typically compact, making it challenging to dissipate the heat they generate. By integrating much of the system on a single FPGA, the Artix-7 FPGA solution minimizes dissipation needs, not just by reducing device count, but also by reducing inter-device I/O dissipation. An Artix-7 FPGA based design can reduce power by up to 50% compared to a multi-device solution.

Conclusion

Today, mobile users are demanding that providers expand their networks. Enabling treatment for those who cannot reach a medical facility, equipping foot soldiers with multi-media communication, and ensuring high-speed internet access to those on the periphery of a cellular network are only a few examples of *edge applications* delivering on such requirements.

System developers can only meet such demands by scaling their systems effectively and economically. Rather than opting for mid-range devices, they are looking for lower-power alternatives with similar feature sets, as found in the Artix-7 FPGA. By leveraging the Artix-7 family's highest performance per watt at the lowest cost, applications can improve their reach to the edge of their traditional markets and enter new ones.

For more information, go to:

http://www.xilinx.com/products/silicon-devices/fpga/artix-7/index.htm

Additional Resources

- DS180: 7 Series FPGA Overview
- WP312: Xilinx Next Generation 28 nm FPGA Technology Overview
- WP373: Xilinx Redefines Power, Performance, and Design Productivity with Three Innovative 28 nm FPGA Families: Virtex-7, Kintex-7, and Artix-7 Devices
- WP378: Xilinx FPGAs in Portable Ultrasound Systems
- WP389: Lowering Power at 28 nm with Xilinx 7 Series FPGAs
- WP405: Xilinx 7 Series FPGAs: The Logical Advantage

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/16/12	1.0	Initial Xilinx release.

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