MCB Performance, JTAG Revision Code, Max I_{CCINTQ} and I_{CCAUXQ} and SSO Table Updates for Spartan-6 LX16 and LX45 FPGAs

XCN10024 (v1.2) April 11, 2011 **Product Change Notice**

Overview

The purpose of this notification is to inform Xilinx customers of a change to the Memory Controller Block (MCB) performance, an update to the JTAG ID Revision Code, a change to the maximum I_{CCINTQ} and I_{CCAUXQ} specifications, and an update to the CSG324 Bank 0/2 SSO limit recommendations for "XC" Commercial Spartan®-6 LX16 -2C and Spartan-6 LX45 -2C FPGA production devices.

Description

New V_{CCINT} operating conditions are now required to meet the previous MCB performance specifications for DDR2 interfaces. Operating the MCB over the full V_{CCINT} operating conditions (1.14V to 1.26V) will now result in reduced MCB performance. This change improves the ability of Xilinx to support this product effectively. In addition, the JTAG ID Revision Code field has been incremented from "2" to "3". This JTAG ID Revision Code change has no impact on the form, fit, function, or reliability of affected devices. The Circuit Design Revision Code remains unaffected.

The new Extended Performance mode for the MCB V_{CCINT} Recommended Operating Conditions and the corresponding maximum data rate specification changes for DDR2 interfaces are shown below in Table 1. These changes are also reflected in v2.1 of the Spartan-6 FPGA Family data sheet (DS162) and v2.2 of the Spartan-6 FPGA Memory Controller User Guide (UG388).

The ISE 12.2 (with MIG 3.5) software will provide support for selection and timing validation of the Standard Performance mode and Extended Performance mode for the MCB. Prior to the 12.2 release, these modes can be used by adhering to the correct V_{CCINT} range and ensuring that MIG tool selections are made in compliance with the new performance specifications.

In addition to the MCB performance specification change, all MCB designs, regardless of performance level, will require a bitstream change to update the configuration of IO elements involved in READ data capture.
For more information on the MCB performance and bitstream changes as well as other recent important MCB updates, see the Spartan-6 FPGA answer records dated 6/14/10 posted under the MIG Design Advisories (Xilinx Answer Record #33566).

The JTAG ID Revision Code change does not affect any documentation but can be used to identify material shipped under the old MCB performance specifications. Material with a revision code of "2" meets the previous performance specifications over the full V_{CCINT} range as listed in Table 1, while material with a revision code of "3" or later would adhere to the new performance modes and specifications.

Table 1: **MCB Performance Change for -2 Speed Grade, DDR2 interfaces**

	Original Performance Specification	New Performance Specification	
V_{CCINT} Range	1.14V to 1.26V	Standard Performance V_{CCINT} 1.14V to 1.26V	Extended Performance V_{CCINT} 1.2V to 1.26V
JTAG ID Revision	JTAG ID Revision Code "2"	JTAG ID Revision Code "3" or Later	JTAG ID Revision Code "3" or Later
DDR2	667 Mb/s	625 Mb/s	667 Mb/s

Maximum I_{CCINTQ} and I_{CCAUXQ} specifications for -2 speed grade devices have been changed. XPower Estimator Revision 12.3.1 or newer (available at http://www.xilinx.com/products/design_resources/power_central/index.htm) reports the correct total maximum quiescent power. The total maximum power for -2 speed grade devices was increased by 6% to 20% in Revision 12.1.1, but then decreased by 34% to 41% in Revision 12.3.1, resulting in a net improvement in power since the initial production specifications. These changes are for the maximum power specifications only; there are no changes to the typical power specifications listed in the data sheet.

The Spartan-6 FPGA Family data sheet (DS162) includes recommended maximum SSO limits per Vcco/GND pair. Due to a publication error the data values shown in the CSG324 Bank 0/2 column were incorrect in v1.4 and earlier. The Spartan-6 Family data sheet v1.5 or newer reports the correct recommended SSO limits.

Products Affected

These changes affect all Spartan-6 LX16 and LX45 FPGA products (XC) for -2 speed and C grade temperature as listed below. The standard part numbers affected by this change are listed in Table 2.

Table 2: **Spartan-6 Commercial "XC" FPGA Products Affected**

Xilinx Product	Xilinx Product
XC6SLX16-2CSG225C	XC6SLX45-2CSG324C
XC6SLX16-2CSG324C	XC6SLX45-2FG484C
XC6SLX16-2FT256C	XC6SLX45-2FG676C
XC6SLX16-2FTG256C	XC6SLX45-2FGG484C
	XC6SLX45-2FGG676C

Key Dates and Ordering Information

This change is effective upon release of this PCN.

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support.

Important Notice: Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the Support website (http://www.xilinx.com/support). Register today and personalize your "Documentation and Design Advisory Alerts" area to include Customer Notifications. Xilinx Support provides many benefits, including the ability to receive alerts for new and updated information about specific products, as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to Xilinx Answer Record #18683.

Additional Documentation

DS162, *Spartan-6 FPGA DC and Switching Characteristics*, Data Sheet:
http://www.xilinx.com/support/documentation/data_sheets/ds162.pdf.

UG388, *Spartan-6 FPGA Memory Controller*, User Guide:
http://www.xilinx.com/support/documentation/user_guides/ug388.pdf.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/14/2010	1.0	Initial release.
12/03/2010	1.1	Revised paragraph on maximum ICCINTQ and ICCAUXQ specifications.
04/11/2011	1.2	References to DDR3 interfaces removed from PCN. All production devices, including those shipped prior to this document revision, are now qualified for the original MCB DDR3 performance specifications over the full V_{CCINT} range (1.14V to 1.26V)

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