

Introduction

Thank you for participating in the Xilinx Virtex™-4 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the Virtex-4 XC4VLX25 FPGA. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the XC4VLX25 devices as shown in [Table 1](#).

Table 1: XC4VLX25 FPGA Devices Affected by These Errata

Devices	XC4VLX25CES	JTAG ID: 0, 9
Packages	All	
Speed Grades	All	

Hardware Errata Details (JTAG ID = 0)

This section provides a detailed description of each hardware issue known at the release time of this document for devices where JTAG ID = 0.

FIFO16

The FIFO16 does not correctly generate the ALMOST EMPTY, EMPTY, ALMOST FULL, and FULL flags after the following sequence occurs:

1. Read or Write has reached the threshold value of ALMOST_EMPTY_OFFSET or ALMOST_FULL_OFFSET.
2. A single Read or Write operation is performed, followed by a simultaneous Read or Write operation, when active Read and Write clock edges are very close together.

Unexpected or corrupt data can occur as a result of the flag failures, even if the ALMOST EMPTY or ALMOST FULL flags are not being used.

This issue does not happen in FIFO16 applications where Read and Write never occur simultaneously. Workarounds (downloadable macros) are available for users who are performing simultaneous Read/Writes. Not all workarounds will achieve data sheet performance. See Xilinx answer record 22462 for more details, workaround solutions, and corresponding performance information.

Configuration

JTAG INTEST Instruction is Not Supported

The JTAG INTEST instruction outlined in the Virtex-4 Configuration Guide is not supported.

BSCAN_VIRTEX4 Library Element

When using the BSCAN_VIRTEX4 library element, the RESET signal is not supported. If the BSCAN_VIRTEX4 is instantiated in the design after configuration, the USER2, USER3, and USER4 registers are not available. For further details, check answer record 20129.

JTAG TDO Output

The JTAG TDO output will 3-state on the rising edge of TCK when the JTAG TAP state machine exits the Shift-DR or Shift-IR states. In the event that the last bit shifted out is a "0," the value might be read as a "1" by the next device in the chain if it has a long hold-time requirement on its TDI pin.

Workaround

Provide negative skew on TCK between the Virtex-4 device and the next device in the chain. Refer to answer record 19865.

FRAME_ECC

The FRAME_ECC logic does not correctly calculate bit failures when readback is performed via JTAG, 8-bit SelectMAP™ mode, or 8-bit ICAP.

Workaround

The FRAME_ECC block must be used with ICAP32.

ISERDES or IDELAY

When using an ISERDES or IDELAY element with the attribute IOBDELAY_TYPE set to VARIABLE, the CLKDIV (ISERDES) or CLK (IDELAY) signal is inverted. This imposes a design requirement that the internal routing delay plus the setup delay must be less than one-half the clock cycle.

Workaround

Frequency of operation for resetting or changing the delay value is limited to approximately 200 MHz. Place the logic driving the signals DLYRST, DLYINC, and DLYCE (ISERDES), or RST, INC, and CE (IDELAY) as close as possible to the ISERDES or IDELAY element. This placement makes the delay for these signals in the trace report less than one-half the clock cycle time. For further details, check answer record 20125.

DSP48**CarryIn Input Register**

The CarryIn input register from fabric is not supported (that is, the attribute CARRYINREG = 1).

Workaround

Use the CLB register to replace the CarryIn input register, and set attribute CARRYINREG = 0.

Symmetric Rounding Logic

The DSP48 element supports five different modes of symmetric rounding. All four non-pipelined rounding modes are fully supported. Only the pipelined Round (A x B) mode (that is, when CarryInSel[1:0] = 11) is not supported.

Workaround

Perform the equivalent logic for carry in a CLB, and connect the carry to the CarryIn input of the DSP48 using CarryInSel[1:0] = 00 (set attribute CARRYINREG = 0).

DCM

1. The DCM attribute CLKOUT_PHASE_SHIFT set to the value VARIABLE_CENTER is not supported.
2. If the only clock outputs used from a DCM are CLKFX and/or CLKFX180, and the input clock frequency (CLKIN) is outside of the CLKIN_FREQ_DLL_(HF or LF)_(MS or MR)_MIN/MAX range, then use the macro in answer record 20529 to properly generate the LOCKED signal.
3. For source-synchronous applications, it is best to use the ChipSync™ features for the highest performance and lowest skew. If the DCM must be used, follow the guidelines outlined in answer record 20529 to achieve a CLKIN_CLKFB_PHASE specification of ±300 ps.

Pin-to-Pin Timing

The following tables list the correct pin-to-pin timing for the XC4VLX25CES devices where JTAG ID = 0:.

Table 2: Global Clock Input to Output Delay for LVC MOS25, 12 mA, Fast Slew Rate, With DCM

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
LVC MOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM.						
T _{ICKOFDCM}	Global Clock and OFF with DCM	XC4VLX25	2.60	2.93	3.11	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 3: Global Clock Input to Output Delay for LVC MOS25, 12 mA, Fast Slew Rate, Without DCM

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
LVC MOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> DCM.						
T _{ICKOF}	Global Clock and OFF without DCM	XC4VLX25	6.83	7.82	8.60	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 4: Global Clock Setup and Hold for LVC MOS25 Standard, With DCM

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard. ⁽¹⁾						
T _{PSDCM} / T _{PHDCM}	No Delay Global Clock and IFF ⁽²⁾ with DCM	XC4VLX25	0.80 -0.59	0.87 -0.59	0.97 -0.59	ns

Notes:

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. These measurements include:
CLK0 DCM jitter
IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 5: Global Clock Setup and Hold for LVC MOS25 Standard, With DCM in Source-Synchronous Mode

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, ⁽¹⁾ Using DCM and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Switching Characteristics, page 21 of the Virtex-4 data sheet .						
T _{PSDCM_0} / T _{PHDCM_0}	No Delay Global Clock and IFF ⁽²⁾ with DCM in Source-Synchronous Mode	XC4VLX25	-0.67 0.97	-0.67 1.07	-0.67 1.21	ns

Notes:

1. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CLK0 DCM jitter. Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

Table 6: Global Clock Setup and Hold for LVCMOS25 Standard, Without DCM

Symbol	Description	Device	Speed Grade			Units
			-12	-11	-10	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾						
T _{PSFD} / T _{PHFD}	Full Delay Global Clock and IFF ⁽²⁾ without DCM	XC4VLX25	4.92 -0.35	6.20 -0.37	7.62 -0.62	ns

Notes:

1. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Operational Guidelines

Design Software Requirements (JTAG ID = 0)

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.57 (or later) and Xilinx software ISE 7.1i Service Pack 4 (SP4) or later is required when designing for the devices covered by this errata. Contact Xilinx technical support for SP4 help. Updates are available on the following web page:

http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

The stepping should be set to ES in the constraint file (UCF file)

CONFIG STEPPING = "ES";

- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:

http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations (JTAG ID = 0)

Virtex-II and Virtex-II Pro FPGA Designers

For Virtex-II and Virtex-II Pro designers, the CCLK specification in Virtex-4 devices was changed to LVCMOS 12mA Fast slew rate. Xilinx recommends designing to this new standard.

V_{CCAUX} Power Requirements

During the device configuration sequence, V_{CCAUX} requires 750 mA for up to 4 ms during initialization, followed by 250 mA during the loading of the bitstream. To reduce I_{CCAUX} after configuration, Xilinx recommends the following:

For JTAG Configuration Mode

Use the iMPACT™ or ChipScope™ Pro tools in ISE software to configure these devices.

For Slave Serial Configuration Mode

When generating the bitstream with BitGen, use the option: **-g EngineeringSample:Serial.**

For Slave SelectMAP Configuration Mode

When generating the bitstream with BitGen, use the option: **-g EngineeringSample>SelectMAP8.**

When using Master mode, insert a V_{CCAUX_FIX} module in the design. See answer record 20246.

IDELAY or ISERDES with IOBDELAY_TYPE Design Guidelines

When using IDELAY or ISERDES with IOBDELAY_TYPE set to FIXED or VARIABLE, a pulse must be applied to RST/DLYRST for initialization.

Hardware Errata Details (JTAG ID = 9)

This section provides a detailed description of each hardware issue known at the release time of this document for devices where JTAG ID = 9.

FIFO16

The errata for JTAG ID = 9 is the same as the errata for JTAG ID = 0. See [FIFO16, page 5](#).

Operational Guidelines

Design Software Requirements (JTAG ID = 9)

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.57 (or later) and Xilinx software ISE 7.1i Service Pack 4 (SP4) or later is required when designing for the devices covered by this errata. Contact Xilinx technical support for SP4 help. Updates are available on the following web page:

http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

The stepping should be set to 1 in the constraint file (UCF file)

CONFIG STEPPING = "1";

- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:

http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations (JTAG ID = 9)

Virtex-II and Virtex-II Pro FPGA Designers

For Virtex-II and Virtex-II Pro designers, the CCLK specification in Virtex-4 devices was changed to LVCMOS 12mA Fast slew rate. Xilinx recommends designing to this new standard.

Traceability

The XC4VLX25 is marked as shown in [Figure 1](#).

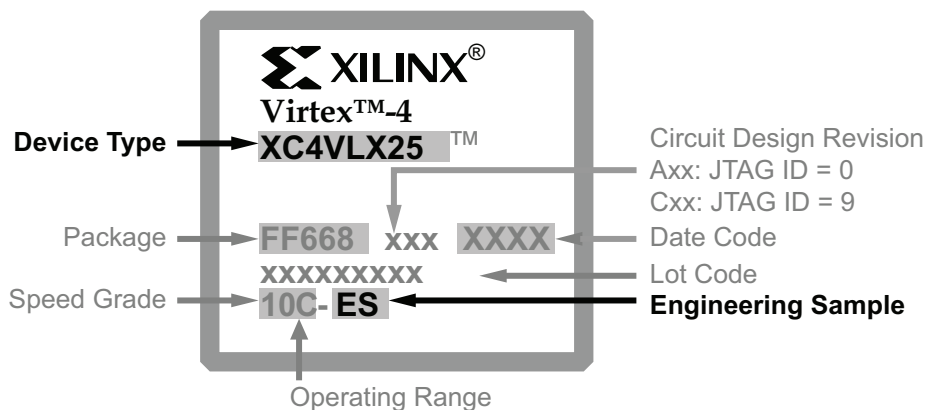


Figure 1: Example XC4VLX25CES Package Marking

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications.

For additional questions regarding these errata, please contact your Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact.htm>.

Obtaining the Most Recent Errata Version

If this document is printed or saved locally in electronic form, check for the most recent release, available to registered users on the Xilinx website at: http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata.

To receive an e-mail alert when this document changes, sign up at:
http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-4 documents:

Virtex-4 Overview (<http://www.xilinx.com/bvdocs/publications/ds112.pdf>)

Virtex-4 Data Sheet (<http://www.xilinx.com/bvdocs/publications/ds302.pdf>)

Virtex-4 User Guide (http://www.xilinx.com/bvdocs/user_guides/ug070.pdf)

XtremeDSP™ Design Guide (http://www.xilinx.com/bvdocs/user_guides/ug073.pdf)

Virtex-4 Configuration Guide (http://www.xilinx.com/bvdocs/user_guides/ug071.pdf)

Virtex-4 Packaging Guide (http://www.xilinx.com/bvdocs/user_guides/ug075.pdf)

Revision History

Date	Version	Description
10/19/04	1.0	Initial release.
3/24/05	1.1	Edited V_{CCAUx} Power Requirements section. Addition of DSP48 CarryIn Input Register section. Added DCM section.
01/25/06	1.2	Added the FIFO16, page 5 errata. Redistributed sections based upon the JTAG ID number. In the JTAG ID = 0 section: Added Pin-to-Pin Timing section. Updated Design Software Requirements (JTAG ID = 0) section. Replaced the LVTTTL I/O standard with LVCMOS I/O standard in the Notes and Recommendations (JTAG ID = 0) section. Removed System Monitor errata because it is no longer in the Virtex-4 data sheet. Added Circuit Design Revision to Figure 1 .