Virtex-4 XC4VFX20CES2/3 and XC4VFX60CES2/3 Errata

EN014 (v1.6) October 24, 2007 **Errata Notification**

Introduction

Thank you for participating in the Xilinx Virtex™-4 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the Virtex-4 XC4VFX20CES2/3 and XC4VFX60CES2/3 devices. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the XC4VFX20CES2/3 and XC4VFX60CES2/3 devices as shown in Table 1.

Table 1: **XC4VFX20 and XC4VFX60 Devices Affected by These Errata**

Devices	XC4VFX20CES2	XC4VFX20CES3	XC4VFX60CES2	XC4VFX60CES3
		XC4VFX20CES3L	XC4VFX60CES2L2(1)	XC4VFX60CES3L
		XC4VFX20CES3R	XC4VFX60CES2R2(1)	XC4VFX60CES3R
			XC4VFX60CES2V2(1)	XC4VFX60CES3L2(1)
				XC4VFX60CES3R2(1)
				XC4VFX60CES3V2(1)
JTAG ID (Revision Code) for all devices(2): 0h, Bh, Dh, or Fh				
Packages	All			
Speed Grades	-10, -11, -12			

Notes:

1. CES3L2, CES3R2, and CES3V2 devices require a different Calibration Block version. Refer to the Calibration Block section in this document.
2. The revision code is located in bits [31:28] of the JTAG ID Code register. See UG071: V*irtex-4 Configuration Guide* for more information.

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

FIFO16

The FIFO16 does not correctly generate the ALMOST EMPTY, EMPTY, ALMOST FULL, and FULL flags after the following sequence occurs:

1. Read or Write has reached the threshold value of ALMOST_EMPTY_OFFSET or ALMOST_FULL_OFFSET.
2. A single Read or Write operation is performed, followed by a simultaneous Read or Write operation, when active Read and Write clock edges are very close together.

Unexpected or corrupt data can occur as a result of the flag failures, even if the ALMOST EMPTY or ALMOST FULL flags are not being used.

This issue does not happen in FIFO16 applications where Read and Write never occur simultaneously. Workarounds (downloadable macros) are available for users who are performing simultaneous Read/Writes. Not all workarounds will achieve data sheet performance. See Xilinx answer record 22462 for more details, workaround solutions, and corresponding performance information.

DSP48

CarryIn Input Register

The CarryIn input register from fabric is not supported (that is, the attribute `CARRYINREG = 1`).

Workaround

Use CLB register to replace CarryIn Input Register, and set attribute `CARRYINREG = 0`.

Symmetric Rounding Logic

The DSP48 element supports five different modes of symmetric rounding. All four non-pipelined rounding modes are fully supported. Only the pipelined Round (A x B) mode (that is, when `CarryInSel[1:0] = 11`) is not supported.

Workaround

Perform the equivalent logic for carry in a CLB, and connect the carry to the CarryIn input of the DSP48 slice using `CarryInSel[1:0] = 00` (set attribute `CARRYINREG = 0`)

DCM

1. The DCM attribute CLKOUT_PHASE_SHIFT set to the value VARIABLE_CENTER is not supported.
2. If the only clock outputs used from a DCM are CLKFX and/or CLKFX180, and the input clock frequency (CLKIN) is outside of the CLKIN_FREQ_DLL_(HF or LF)_(MS or MR)_MIN/MAX range, then use the macro in answer record 20529 to properly generate the LOCKED signal.
3. For source-synchronous applications, it is best to use the ChipSync™ features for the highest performance and lowest skew. If the DCM must be used, follow the guidelines outlined in answer record 20529 to achieve a CLKIN_CLKFB_PHASE specification of ±300 ps.

T_{CONFIG}, DCM_INPUT_CLOCK_STOP, and DCM_RESET Requirements

The following time requirements detailed in the Virtex-4 data sheet apply to the devices listed in this errata:

- T_{CONFIG} – the time to configure devices after V_{CCINT} is applied.
- DCM_INPUT_CLOCK_STOP – the maximum duration of time where CLKIN and CLKFB can be stopped.
- DCM_RESET– the maximum time to reset the DCM.

Workaround

Use design solution in answer record 21127.

FRAME_ECC

FRAME_ECC readback of unused configuration bits in I/O IDELAY frames might indicate readback errors. These are false errors and can be ignored because they have no functional impact.

Workaround

The reference design described in XAPP714 can be used to eliminate this error indication.

Processor Block

Frequency Performance

1) The PPC405 processor core maximum operating frequency is 300 MHz for -10 speed grade and 350 MHz for -11 speed grade.

   Workaround

   Compile code with the Xilinx provided Gnu compiler to achieve full frequency (350 MHz for -10 speed grade; 400 MHz -11 speed grade). For details, see answer record 21075.

   When using all other compilers, the frequency is as stated in item 1.

2) When using the APU controller interface, the maximum operating frequency of the processor block is 275 MHz for -10 speed grade and 300 MHz for -11 speed grade.

For other processor block errata and operational guidelines, please refer to answer record 20658.

RocketIO™ Multi-Gigabit Serial Transceivers

This section provides a detailed description of the Virtex-4 RocketIO™ transceiver issues known at the release time of this document.

Unavailable Pins On CES2 Devices

The RocketIO serial transceiver pins listed in Table 2 are not available. All other RocketIO transceiver pins are available for use. This specific table does not apply to CES3 devices.

Table 2: **Unavailable Pins on CES2 Devices**

Device - Package	MGT Name	Software Location	Pin Name	Pin Location
XC4VFX20CES2 – FF672	MGT110A	GT11_X1Y1	RXPPADA_110	AC1
			RXNPADA_110	AD1
			TXPPADA_110	AF2
			TXNPADA_110	AF3
XC4VFX60CES2 – FF672	MGT110A	GT11_X1Y3	RXPPADA_110	AC1
			RXNPADA_110	AD1
			TXPPADA_110	AF2
			TXNPADA_110	AF3
XC4VFX60CES2 – FF1152	MGT110A	GT11_X1Y3	RXPPADA_110	AC1
			RXNPADA_110	AD1
			TXPPADA_110	AF1
			TXNPADA_110	AG1

Available Transceivers on the Left or Right Side

Some Virtex-4 devices are available with reduced transceiver counts. RocketIO serial transceivers are available on either the left or the right side of the die. The device order numbers have an L or an R after the CES designation to indicate the left or right side of the die. When viewed from the top of a flip-chip packaged device, the MGTs and their pin locations are reversed. In other words, the left-side MGT on the die is a right-side MGT when viewed from top of the package. Table 3 shows the available left or right side transceivers for the FF672 package devices. Table 4 shows the available left or right side transceivers for the FF1152 package devices.

Table 3: **Available Left or Right Side Transceivers -FF672 Package**

	MGT Name	XC4VFX20 FF672			XC4VFX60 FF672		
		Software Location	Pin Name	Pin Location	Software Location	Pin Name	Pin Location
Left-side MGTs: XC4VFX20CES3L or XC4VFX60CES3L XC4VFX60CES3L2	102_A	GT11_X0Y3	RXPPADA_102	A19	GT11_X0Y7	RXPPADA_102	A19
			RXNPADA_102	A20		RXNPADA_102	A20
			TXPPADA_102	A22		TXPPADA_102	A22
			TXNPADA_102	A23		TXNPADA_102	A23
	102_B	GT11_X0Y2	RXPPADB_102	C26	GT11_X0Y6	RXPPADB_102	C26
			RXNPADB_102	D26		RXNPADB_102	D26
			TXPPADB_102	A24		TXPPADB_102	A24
			TXNPADB_102	A25		TXNPADB_102	A25
	103_A				GT11_X0Y5	RXPPADA_103	J26
						RXNPADA_103	K26
						TXPPADA_103	M26
						TXNPADA_103	N26
	103_B				GT11_X0Y4	RXPPADB_103	U26
						RXNPADB_103	V26
						TXPPADB_103	P26
						TXNPADB_103	R26
	105_A	GT11_X0Y1	RXPPADA_105	W26	GT11_X0Y3	RXPPADA_105	W26
			RXNPADA_105	Y26		RXNPADA_105	Y26
			TXPPADA_105	AB26		TXPPADA_105	AB26
			TXNPADA_105	AC26		TXNPADA_105	AC26
	105_B	GT11_X0Y0	RXPPADB_105	AF24	GT11_X0Y2	RXPPADB_105	AF24
			RXNPADB_105	AF23		RXNPADB_105	AF23
			TXPPADB_105	AD26		TXPPADB_105	AD26
			TXNPADB_105	AE26		TXNPADB_105	AE26
	106_A						
	106_B						

Table 3: **Available Left or Right Side Transceivers -FF672 Package*(Continued)***

	MGT Name	XC4VFX20 FF672			XC4VFX60 FF672		
		Software Location	Pin Name	Pin Location	Software Location	Pin Name	Pin Location
Right-side MGTs: XC4VFX20CES2R2 XC4VFX20CES3R or XC4VFX60CES2R2 XC4VFX60CES3R XC4VFX60CES3R2	113_A	GT11_X1Y3	RXPPADA_113	A4	GT11_X1Y7	RXPPADA_113	A4
			RXNPADA_113	A3		RXNPADA_113	A3
			TXPPADA_113	B1		TXPPADA_113	B1
			TXNPADA_113	C1		TXNPADA_113	C1
	113_B	GT11_X1Y2	RXPPADB_113	G1	GT11_X1Y6	RXPPADB_113	G1
			RXNPADB_113	H1		RXNPADB_113	H1
			TXPPADB_113	D1		TXPPADB_113	D1
			TXNPADB_113	E1		TXNPADB_113	E1
	112_A				GT11_X1Y5	RXPPADA_112	N1
						RXNPADA_112	P1
						TXPPADA_112	T1
						TXNPADA_112	U1
	112_B				GT11_X1Y4	RXPPADB_112	AA1
						RXNPADB_112	AB1
						TXPPADB_112	V1
						TXNPADB_112	W1
	110_A	GT11_X1Y1(1)	RXPPADA_110	AC1	GT11_X1Y3 (1)	RXPPADA_110	AC1
			RXNPADA_110	AD1		RXNPADA_110	AD1
			TXPPADA_110	AF2		TXPPADA_110	AF2
			TXNPADA_110	AF3		TXNPADA_110	AF3
	110_B	GT11_X1Y0	RXPPADB_110	AF7	GT11_X1Y2	RXPPADB_110	AF7
			RXNPADB_110	AF8		RXNPADB_110	AF8
			TXPPADB_110	AF4		TXPPADB_110	AF4
			TXNPADB_110	AF5		TXNPADB_110	AF5
	109_A						
	109_B						

Notes:

1. This location is not supported in XC4VFX20 and XC4VFX60 CES2R devices.

Table 4: **Available Left or Right Side Transceivers -FF1152 Package**

	MGT Name	XC4VFX60 FF1152		
		Software Location	Pin Name	Pin Location
Left-side MGTs: XC4VFX60CES2L2 XC4VFX60CES3L XC4VFX60CES3L2	102_A	GT11_X0Y7	RXPPADA_102	A31
			RXNPADA_102	A32
			TXPPADA_102	D34
			TXNPADA_102	E34
	102_B	GT11_X0Y6	RXPPADB_102	J34
			RXNPADB_102	K34
			TXPPADB_102	F34
			TXNPADB_102	G34
	103_A	GT11_X0Y5	RXPPADA_103	R34
			RXNPADA_103	T34
			TXPPADA_103	V34
			TXNPADA_103	W34
	103_B	GT11_X0Y4	RXPPADB_103	AC34
			RXNPADB_103	AD34
			TXPPADB_103	Y34
			TXNPADB_103	AA34
	105_A	GT11_X0Y3	RXPPADA_105	AF34
			RXNPADA_105	AG34
			TXPPADA_105	AJ34
			TXNPADA_105	AK34
	105_B	GT11_X0Y2	RXPPADB_105	AP32
			RXNPADB_105	AP31
			TXPPADB_105	AL34
			TXNPADB_105	AM34
	106_A	GT11_X0Y1	RXPPADA_106	AP26
			RXNPADA_106	AP25
			TXPPADA_106	AP23
			TXNPADA_106	AP22
	106_B	GT11_X0Y0	RXPPADB_106	AP18
			RXNPADB_106	AP17
			TXPPADB_106	AP21
			TXNPADB_106	AP20

Table 4: **Available Left or Right Side Transceivers -FF1152 Package *(Continued)***

	MGT Name	XC4VFX60 FF1152		
		Software Location	Pin Name	Pin Location
Right-side MGTs: XC4VFX60CES2R2 XC4VFX60CES3R XC4VFX60CES3R2	113_A	GT11_X1Y7	RXPPADA_113	A7
			RXNPADA_113	A6
			TXPPADA_113	A4
			TXNPADA_113	A3
	113_B	GT11_X1Y6	RXPPADB_113	F1
			RXNPADB_113	G1
			TXPPADB_113	C1
			TXNPADB_113	D1
	112_A	GT11_X1Y5	RXPPADA_112	M1
			RXNPADA_112	N1
			TXPPADA_112	R1
			TXNPADA_112	T1
	112_B	GT11_X1Y4	RXPPADB_112	Y1
			RXNPADB_112	AA1
			TXPPADB_112	U1
			TXNPADB_112	V1
	110_A	GT11_X1Y3 (1)	RXPPADA_110	AC1
			RXNPADA_110	AD1
			TXPPADA_110	AF1
			TXNPADA_110	AG1
	110_B	GT11_X1Y2	RXPPADB_110	AL1
			RXNPADB_110	AM1
			TXPPADB_110	AH1
			TXNPADB_110	AJ1
	109_A	GT11_X1Y1	RXPPADA_109	AP6
			RXNPADA_109	AP7
			TXPPADA_109	AP9
			TXNPADA_109	AP10
	109_B	GT11_X1Y0	RXPPADB_109	AP14
			RXNPADB_109	AP15
			TXPPADB_109	AP11
			TXNPADB_109	AP12

Notes:

1. This location is not supported in XC4VFX60 CES2R devices.

Analog Voltage Supply Values

AVCCAUXTX must be set to 1.1V ± 3%.

AVCCAUXRX (both A and B) must be set to 1.1V ± 3%.

For additional information on recommended regulators, see Xilinx answer record 21739.

Analog Receiver Range

The receiver is tested at 622 Mb/s and 1.25 Gb/s using the digital CDR mode, and at 1.25 Gb/s, 2.5 Gb/s, and 3.125 Gb/s using the analog CDR mode. Operation above 3.125 Gb/s is not supported in the devices covered by this errata (Table 1).

8B/10B Encoding

Data transmitted/received with the devices covered by this errata (Table 1) must be 8B/10B encoded when using the analog CDR mode for 1.25 Gb/s, 2.5 Gb/s, and 3.125 Gb/s rates.

Total Jitter Generation

At MGTCLK frequencies of 156 MHz and below, the transceivers can exhibit total wide-band jitter generation greater than 0.35UI.

Calibration Block

A programmable Calibration block, written in Verilog and VHDL, is available from Xilinx. This block must be used with these devices. See answer record 22477 for details on obtaining this block.

Attributes

Certain attribute settings need to be changed from the ISE software 7.1i SP4 default settings. See Xilinx answer record 21672 for the most up to date attribute setting details.

Temperature Range

The devices covered by this errata (Table 1) are certified for use at 25°C junction to 85°C junction temperature. Junction temperatures below 25°C are not supported.

32-Bit Comma Detection (SONET Alignment)

Receive data alignment is not maintained when the ENPCOMMAALIGN fabric port is deasserted (pulled Low) while operating with the 32-bit SONET aligner enabled. SONET alignment (A1A1A2A2) is enabled by setting the attribute COMMA32 = TRUE. This errata does not affect the normal byte alignment block. This block *does* maintain alignment on deassertion of ENPCOMMAALIGN.

Internal Clock Divider Restriction

TXUSRCLK must be sourced from the fabric for 1-byte and 2-byte interface modes on both MGTA and MGTB. Although the internal clock divider (divide by 2 or 4) can be used to internally generate TXUSRCLK, the TXUSRCLK2 divider cannot be used in the transmitter of MGTA or MGTB for 1-byte and 2-byte interface modes.

8B/10B Encoder TXKERR Port

The TXKERR output port incorrectly indicates the correctness of K-characters on the transmit data bus. It indicates invalid K-characters as valid and valid K-characters as invalid. The output of this port should be ignored.

Static Operating Behavior

Under certain and specific conditions, transceivers might cease to correctly transmit or receive data when all three of the following conditions are met:

1. Power has been applied to the FPGA.
2. Transitions are not occurring in the transmit and/or the receive direction.
3. Conditions (1) and (2) persist for more than 400 cumulative hours at 85°C T_j or more than 2,000 cumulative hours at 60°C T_j.

To view detailed information on this topic, see Xilinx answer record 22471.

Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.57 (or later) and Xilinx software ISE 7.1i Service Pack 4 (SP4) or later is required when designing for the devices covered by this errata. Contact the Xilinx technical support for SP4 support. Updates are available on the following web page:

  http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

  The Stepping should be set to ES in the constraint file (UCF file):

  CONFIG STEPPING = “ES”;

- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:

  http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations

Virtex-II and Virtex-II Pro FPGA Designers

For Virtex-II and Virtex-II Pro designers, the CCLK specification in Virtex-4 devices was changed to LVCMOS 12mA Fast slew rate. Xilinx recommends designing to this new standard.

Traceability

Examples of package markings for the devices listed in Table 1 appear in Figure 1 and Figure 2.

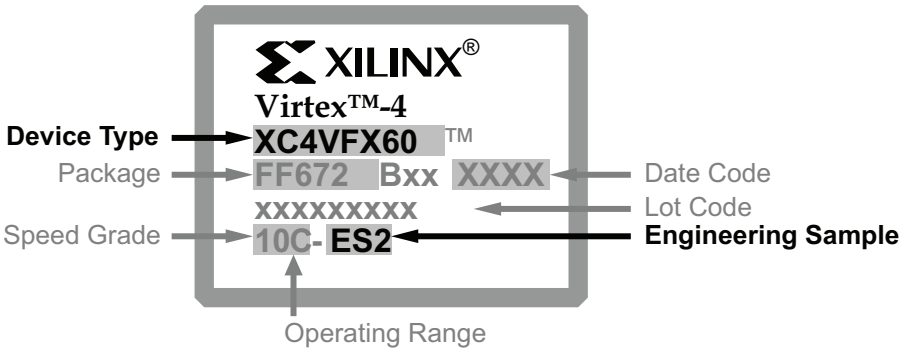

Figure 1: **Example XC4VFX60CES2 Package Marking**

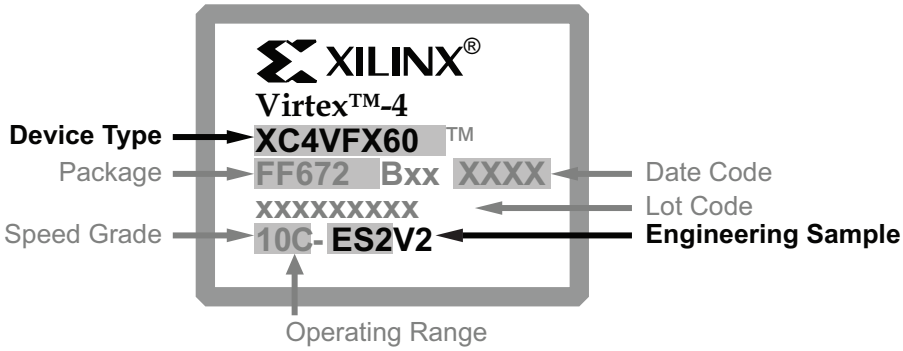

Figure 2: **Example XC4VFX60CES2V2 Package Marking**

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications.

For additional questions regarding these errata, please contact your Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Obtaining the Most Recent Errata Version

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To receive an e-mail alert when this document changes, sign up at: http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-4 documents:

Virtex-4 Overview (http://www.xilinx.com/bvdocs/publications/ds112.pdf)

Virtex-4 Data Sheet (http://www.xilinx.com/bvdocs/publications/ds302.pdf)

Virtex-4 User Guide (http://www.xilinx.com/bvdocs/user guides/ug070.pdf)

XtremeDSP™ Design Guide (http://www.xilinx.com/bvdocs/user guides/ug073.pdf)

Virtex-4 Configuration Guide (http://www.xilinx.com/bvdocs/user guides/ug071.pdf)

Virtex-4 Packaging Guide (http://www.xilinx.com/bvdocs/user guides/ug075.pdf)

Virtex-4 RocketIO Multi-Gigabit Transceiver Guide (http://www.xilinx.com/bvdocs/user guides/ug076.pdf)

PowerPC 405 Processor Block Reference Guide (http://www.xilinx.com/bvdocs/user guides/ug018.pdf)

Revision History

Date	Version	Description
04/25/05	1.0	Initial release.
06/23/05	1.1	Revised designation of devices from CES to CES2. Change the Design Software Requirements to ISE7.1i (SP3). Corrected the RocketIO software table to GT11. Added FRAME_ECC errata information.
07/06/05	1.2	Added a new section, Analog Voltage Supply Values, and made text changes.
08/22/05	1.3	Revised information under the Analog Receiver Range heading, added the 8B/10B Encoding and Temperature Range sections, and removed the *PCS HCLKOUT Output* section. Updated the Design Software Requirements to require speed specification 1.57 and ISE7.1i (SP4) software.
10/11/05	1.4	Added CES3 device functionality. Revised Analog Receiver Range and 8B/10B Encoding sections. Added Internal Clock Divider Restriction and 32-Bit Comma Detection (SONET Alignment) errata.
04/05/06	1.5	• Updated Table 1, Table 3, and Table 4. • Added the FIFO16 errata. • Replaced the LVTTL I/O standard with LVCMOS I/O standard in the Notes and Recommendations section. • Removed System Monitor errata because it is no longer in the Virtex-4 data sheet. Added Available Transceivers on the Left or Right Side section. • Added T_{CONFIG}, DCM_INPUT_CLOCK_STOP, and DCM_RESET Requirements, Static Operating Behavior, and 8B/10B Encoder TXKERR Port sections. • Updated the Analog Voltage Supply Values and the Attributes sections.
10/24/07	1.6	Updated JTAG information in Table 1 and added Note 2. Updated copyright and legal disclaimer.

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