# Virtex-4 XC4VSX25CES Errata

EN018 (v1.1) February 23, 2006 **Errata Notification**

## Introduction

Thank you for participating in the Xilinx Virtex™-4 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the Virtex-4 XC4VSX25 FPGA. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

## Devices

These errata apply to the XC4VSX25 devices as shown in Table 1.

*Table 1:* **XC4VSX25 FPGA Devices Affected by These Errata**

| | | |
|---|---|---|
| Devices | XC4VSX25CES | JTAG ID (Revision Code): 2, 0 |
| Packages | All | |
| Speed Grades | All | |

## Hardware Errata Details (JTAG ID = 2)

This section provides a detailed description of each hardware issue known at the release time of this document for devices where JTAG ID = 2.

### FIFO16

The FIFO16 does not correctly generate the ALMOST EMPTY, EMPTY, ALMOST FULL, and FULL flags after the following sequence occurs:

1. Read or Write has reached the threshold value of ALMOST EMPTY OFFSET or ALMOST FULL OFFSET.
2. A single Read or Write operation is performed, followed by a simultaneous Read or Write operation, when active Read and Write clock edges are very close together.

Unexpected or corrupt data can occur as a result of the flag failures, even if the ALMOST_EMPTY or ALMOST_FULL flags are not being used.

This issue does not happen in FIFO16 applications where Read and Write never occur simultaneously. Workarounds (downloadable macros) are available for users who are performing simultaneous Read/Writes. Not all workarounds will achieve data sheet performance. See Xilinx answer record 22462 for more details, workaround solutions, and corresponding performance information.

## Operational Guidelines

### Design Software Requirements (JTAG ID = 2)

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.57 (or later) and Xilinx software ISE 7.1i Service Pack 4 (SP4) or later is required when designing for the devices covered by this errata. Contact Xilinx technical support for SP4 help. Updates are available on the following web page:

  http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

The stepping should be set to "1" in the constraint file (UCF file)

CONFIG STEPPING = "1";

- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:
  http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

### Notes and Recommendations (JTAG ID = 2)

#### *Virtex-II and Virtex-II Pro FPGA Designers*

For Virtex-II and Virtex-II Pro designers, the CCLK specification in Virtex-4 devices was changed to LVCMOS 12mA Fast slew rate. Xilinx recommends designing to this new standard.

## Hardware Errata Details (JTAG = 0)

This section provides a detailed description of each hardware issue known at the release time of this document.

### FIFO16

The errata for JTAG ID = 0 is the same as the errata for JTAG ID = 2. See FIFO16, page 1.

### DSP48

#### *CarryIn Input Register*

The CarryIn input register from fabric is not supported (that is, the attribute `CARRYINREG = 1`).

**Workaround**

Use the CLB register to replace the CarryIn input register, and set attribute `CARRYINREG = 0`.

#### *Symmetric Rounding Logic*

The DSP48 element supports five different modes of symmetric rounding. All four non-pipelined rounding modes are fully supported. Only the pipelined Round (A x B) mode (that is, when `CarryInSel[1:0] = 11`) is not supported.

**Workaround**

Perform the equivalent logic for carry in a CLB, and connect the carry to the CarryIn input of the DSP48 using `CarryInSel[1:0] = 00` (set attribute `CARRYINREG = 0`).

### DCM

1. The DCM attribute CLKOUT_PHASE_SHIFT set to the value VARIABLE_CENTER is not supported.
2. If the only clock outputs used from a DCM are CLKFX and/or CLKFX180, and the input clock frequency (CLKIN) is outside of the CLKIN_FREQ_DLL_(HF or LF)_(MS or MR)_MIN/MAX range, then use the macro in answer record 20529 to properly generate the LOCKED signal.
3. For source-synchronous applications, it is best to use the ChipSync™ features for the highest performance and lowest skew. If the DCM must be used, follow the guidelines outlined in answer record 20529 to achieve a CLKIN_CLKFB_PHASE specification of ±300 ps.

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http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

The Stepping should be set to "ES" in the constraint file (UCF file):

CONFIG STEPPING = "ES";

- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:

http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

### Notes and Recommendations

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## Traceability

The XC4VSX25 is marked as shown in Figure 1.

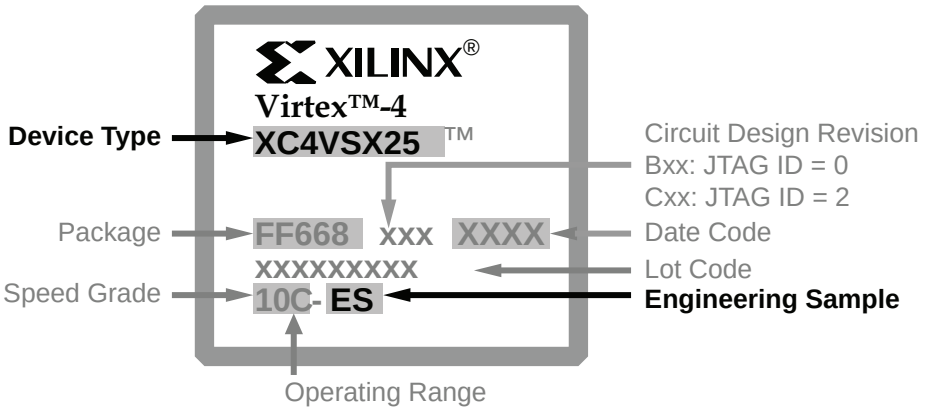


*Figure 1:* **Example XC4VSX25CES Package Marking**

## Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications.

For additional questions regarding these errata, please contact your Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

## Obtaining the Most Recent Errata Version

If this document is printed or saved locally in electronic form, check for the most recent release, available to registered users on the Xilinx website at: http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata.

To receive an e-mail alert when this document changes, sign up at: http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-4 documents:

Virtex-4 Overview (http://www.xilinx.com/bvdocs/publications/ds112.pdf)

Virtex-4 Data Sheet (http://www.xilinx.com/bvdocs/publications/ds302.pdf)

Virtex-4 User Guide (http://www.xilinx.com/bvdocs/user guides/ug070.pdf)

XtremeDSP™ Design Guide (http://www.xilinx.com/bvdocs/user guides/ug073.pdf)

Virtex-4 Configuration Guide (http://www.xilinx.com/bvdocs/user guides/ug071.pdf)

Virtex-4 Packaging Guide (http://www.xilinx.com/bvdocs/user guides/ug075.pdf)

## Revision History

| Date | Version | Description |
|---|---|---|
| 04/12/05 | 1.0 | Initial release. |
| 02/23/06 | 1.1 | • Added JTAG: 2.<br>• Added the FIFO16 section.<br>• Updated Design Software Requirements section.<br>• Replaced the LVTTL I/O standard with LVCMOS I/O standard in the Notes and Recommendations section.<br>• Updated Figure 1.<br>• Removed System Monitor errata because it is no longer in the Virtex-4 data sheet. |