Virtex-4 XC4VFX20CES4, XC4VFX60CES4, XC4VFX100CES4, and XC4VFX140CES4 Errata

EN042 (v1.2) October 6, 2006 **Errata Notification**

Introduction

Thank you for participating in the Xilinx Virtex™-4 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the Virtex-4 XC4VFX20CES4, XC4VFX60CES4, XC4VFX100CES4, and XC4VFX140CES4 FPGAs. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the XC4VFX20CES4, XC4VFX60CES4, XC4VFX100CES4, and XC4VFX140CES4 devices, as shown in Table 1.

Table 1: **Devices Affected by These Errata**

Devices	XC4VFX20CES4	JTAG ID (Revision Code): 2
	XC4VFX60CES4	JTAG ID (Revision Code): 2
	XC4VFX100CES4	JTAG ID (Revision Code): 0
	XC4VFX140CES4	JTAG ID (Revision Code): 0
Packages	All	
Speed Grades	-10, -11	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

HBM ESD Protection

HBM passing voltage for M0, M2, CS, and RDWR pins is 1.25 kV. All other pins that are not RocketIO™ device pins meet the 2 kV specification.

FIFO16

The FIFO16 does not correctly generate the ALMOST EMPTY, EMPTY, ALMOST FULL, and FULL flags after the following sequence occurs:

1. Read or Write has reached the threshold value of ALMOST EMPTY OFFSET or ALMOST FULL OFFSET.
2. A single Read or Write operation is performed, followed by a simultaneous Read or Write operation, when active Read and Write clock edges are very close together.

Unexpected or corrupt data can occur as a result of the flag failures, even if the ALMOST EMPTY or ALMOST FULL flags are not being used.

This issue does not happen in FIFO16 applications where Read and Write never occur simultaneously. Workarounds (downloadable macros) are available for users who are performing simultaneous Read/Writes. Not all workarounds achieve data sheet performance. See Xilinx answer record 22462 for more details, workaround solutions, and corresponding performance information.

Processor Block

APU Controller

The APU Controller can hang after a specific sequence of instructions. A detailed description of this issue along with hardware and software workarounds are described in Xilinx answer record 23720.

For other processor block errata and operational guidelines, please refer to Xilinx answer record 20658.

RocketIO Multi-Gigabit Serial Transceivers

This section provides a detailed description of the Virtex-4 RocketIO transceiver issues known at the release time of this document.

8B/10B Encoding

Data transmitted and received with the devices covered by this errata (Table 1) must be 8B/10B encoded when using the analog CDR mode for 1.25 Gb/s, 2.5 Gb/s, and 3.125 Gb/s rates.

Analog CDR Operating Range Limitation

MGT operation in the Analog CDR mode at line rates between 2.15 Gb/s–2.48 Gb/s is not supported. Valid operating configurations are created by the Virtex-4 RocketIO Wizard 1.1 and above, which is obtained by following the instructions described in Xilinx answer record 22845.

Analog Receiver Range

The receiver is tested at 622 Mb/s and 1.25 Gb/s using the digital CDR mode, and at 1.25 Gb/s, 2.5 Gb/s, and 3.125 Gb/s using the analog CDR mode. Operation above 3.125 Gb/s is not supported in the devices covered by this errata (Table 1).

Attribute Settings

Certain attribute settings need to be changed from the ISE software defaults, which are described in Xilinx answer record 21672. These attributes are set automatically when using the ISE 8.1i Virtex-4 RocketIO Wizard 1.1 or later, which is obtained by following instructions described in Xilinx answer record 22845.

Digital Receiver: Buffer Bypass Mode

Buffer Bypass Mode cannot be used in conjunction with the Digital Receiver. Due to this restriction, the Buffered Mode must be used with the Digital Receiver. The Digital Receiver attributes must be set as shown in Table 2 for Buffered Mode operation.

Table 2: **Digital Receiver Attributes**

Attribute	Buffered Mode Value
RX_BUFFER_USE	TRUE
RXCLK0_FORCE_PMACLK	TRUE
DIGRX_SYNC_MODE	FALSE

See the "Digital Receiver" section of the Virtex-4 RocketIO Multi-Gigabit Transceiver Guide (http://www.xilinx.com/bvdocs/userguides/ug076.pdf) for more details regarding these attributes.

CDM ESD Protection

The CDM ESD for the RocketIO pins (TXN, TXP, RXN, RXP, AVCCAUXRX, GNDA, AVCCAUXTX, VTRX, VTTX, AVCCAUXMGT, MGTCLKP, and MGTCLKN) deviates from the product definition of 250V. The XC4VFX20 and XC4VFX60 devices meet a level of 150V. The XC4VFX100 and XC4VFX140 devices meet a level of 100V.

Xilinx recognizes the present level of RocketIO pin ESD is lower than Xilinx internal standards. Xilinx continues to evaluate ESD requirements for high-speed serial interconnects and is committed to providing best-in-class ESD.

Reference Clock

The MGTCLK input pins in the devices covered by this errata (Table 1) have a maximum frequency of 400 MHz with a minimum peak-to-peak differential input voltage of 250 mV.

RXPCSHCLKOUT and TXPCSHCLKOUT Ports

The RXPCSHCLKOUT and TXPCSHCLKOUT MGT output clock ports are not supported in the devices covered by this errata (Table 1).

RXSIGDET – Receive Out-of-Band (Receive OOB) Signaling

The RXCDRLOS attribute does not function with the resolution and accuracy stated in the Virtex-4 RocketIO Multi-Gigabit Transceiver Guide (http://www.xilinx.com/bvdocs/userguides/ug076.pdf). Refer to Xilinx application note XAPP732 for further details.

SYNCLK1OUT and SYNCLK2OUT Ports

The GT11CLK output ports SYNCLK1OUT and SYNCLK2OUT to BUFG, PMCD, and DCM are supported in the devices covered by this errata (Table 1) as shown in Table 3.

Table 3: **SYNCLK1OUT and SYNCLK2OUT to BUFG, PMCD, and DCM**

Connection To	Maximum Frequency (MHz)
BUFG	375
DCM, PMCD	290

Static Operating Behavior

Under certain and specific conditions, transceivers might cease to correctly transmit or receive data when all three of the following conditions are met:

1. Power has been applied to the FPGA.
2. Transitions are not occurring in the transmit and/or the receive direction.
3. Conditions (1) and (2) persist for more than 400 cumulative hours at 85°C T_J or more than 2,000 cumulative hours at 60°C T_J.

This is only a concern for transceivers that are expected to transmit or receive in the future. Transceivers that are never used require no action. To view detailed information on this topic, please see Xilinx answer record 22471.

Related to the static operating behavior, a programmable Calibration Block, available in Verilog and VHDL, might need to be used with these devices. To determine if a Calibration Block is necessary, please see Xilinx answer record 22477.

Total Jitter Generation

At MGTCLK frequencies of 156.25 MHz and below, the transceivers can exhibit total wide-band jitter generation greater than 0.35 UI. MGTCLK frequencies of 200 MHz or higher are recommended.

TXENOOB Port – Transmit OOB (Out-of-Band) Signaling

The peak-to-peak amplitude of the differential output pins (TXP/TXN) can be higher than 65 mV when TXENOOB is asserted. Xilinx answer record 23481 discusses possible workarounds.

Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the speed specifications and Xilinx development software installations shown inTable 4.

Table 4: **Minimum Speed Specification and Xilinx ISE Software Version**

Speed Grade	Speed Specification	Xilinx ISE Version
-10	v1.58	8.1i Service Pack 2 (SP2)
-11	v1.62	8.2i Service Pack 3 (SP3)

- Contact the Xilinx technical support for ISE support. Updates are available on the following web page:
  http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp
  The Stepping should be set to "0" or "SCD1" in the constraint file (UCF file):
  CONFIG STEPPING = "0";
  or
  CONFIG STEPPING = “SCD1”;
  By using these values, the ISE software inserts a small macro to remove the DCM_INPUT_CLOCK_STOP requirement.
- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:
  http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations

Virtex-II and Virtex-II Pro FPGA Designers

For Virtex-II and Virtex-II Pro designers, the CCLK specification in Virtex-4 devices was changed to LVCMOS 12 mA *Fast* slew rate. Xilinx recommends designing to this new standard.

Traceability

The XC4VFX60CES4 is marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

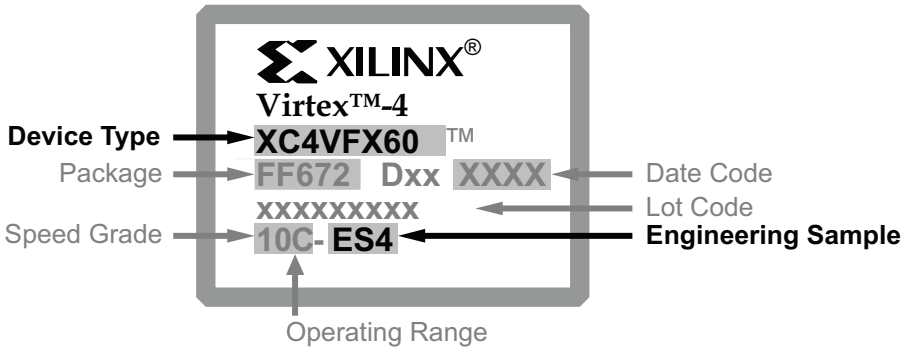

Figure 1: **Example XC4VFX60CES4 Package Marking**

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications.

For additional questions regarding these errata, please contact your Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Obtaining the Most Recent Errata Version

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To receive an e-mail alert when this document changes, sign up at: http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-4 documents:

Virtex-4 Overview (http://www.xilinx.com/bvdocs/publications/ds112.pdf)

Virtex-4 Data Sheet (http://www.xilinx.com/bvdocs/publications/ds302.pdf)

Virtex-4 User Guide (http://www.xilinx.com/bvdocs/userguides/ug070.pdf)

XtremeDSP™ Design Guide (http://www.xilinx.com/bvdocs/userguides/ug073.pdf)

Virtex-4 Configuration Guide (http://www.xilinx.com/bvdocs/userguides/ug071.pdf)

Virtex-4 Packaging Guide (http://www.xilinx.com/bvdocs/userguides/ug075.pdf)

Virtex-4 RocketIO Multi-Gigabit Transceiver Guide (http://www.xilinx.com/bvdocs/userguides/ug076.pdf)

PowerPC™ 405 Processor Block Reference Guide (http://www.xilinx.com/bvdocs/userguides/ug018.pdf)

Revision History

Date	Version	Description
02/13/06	1.0	Initial Xilinx release.
06/21/06	1.1	Added HBM ESD Protection. Under RocketIO Multi-Gigabit Serial Transceivers: put all headings in alphabetical order, added additional sections, Analog CDR Operating Range Limitation, Digital Receiver: Buffer Bypass Mode, CDM ESD Protection, Reference Clock, RXPCSHCLKOUT and TXPCSHCLKOUT Ports, RXSIGDET – Receive Out-of-Band (Receive OOB) Signaling, SYNCLK1OUT and SYNCLK2OUT Ports, and TXENOOB Port – Transmit OOB (Out-of-Band) Signaling, and changed section Total Jitter Generation.Updated the stepping settings under Design Software Requirements.
10/06/06	1.2	Updated the Analog CDR Operating Range Limitation and Attribute Settings section. Added XC4VFX140CES4 device information throughout document. Updated the Speed Specification in the Design Software Requirements section.