Figure 1: ML300 CPU Virtex-II Pro Based Block Diagram

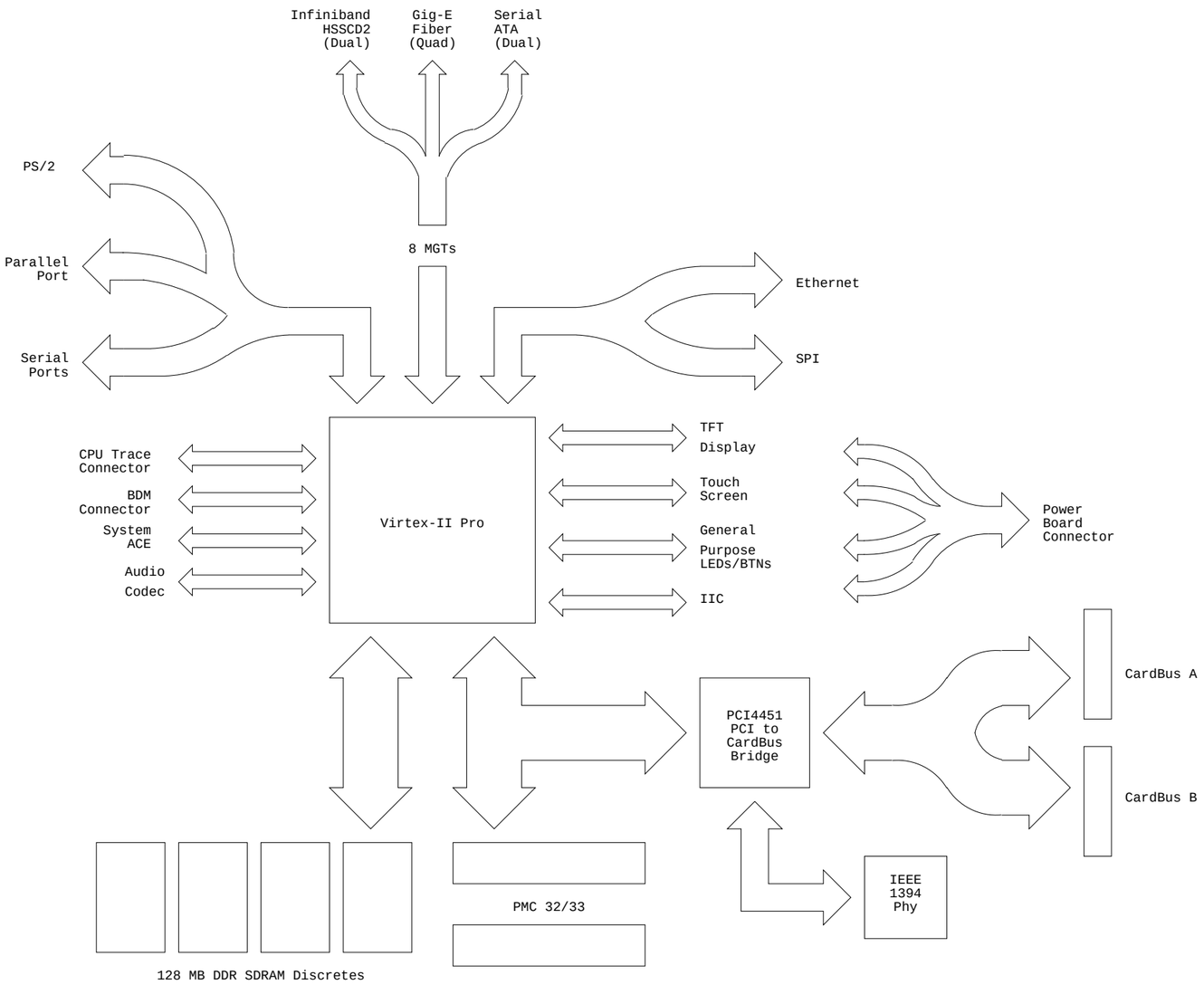

Table 1: ML300 CPU Virtex-II Pro Based Table of Contents

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
Board Block Diagram
and Table of Contents

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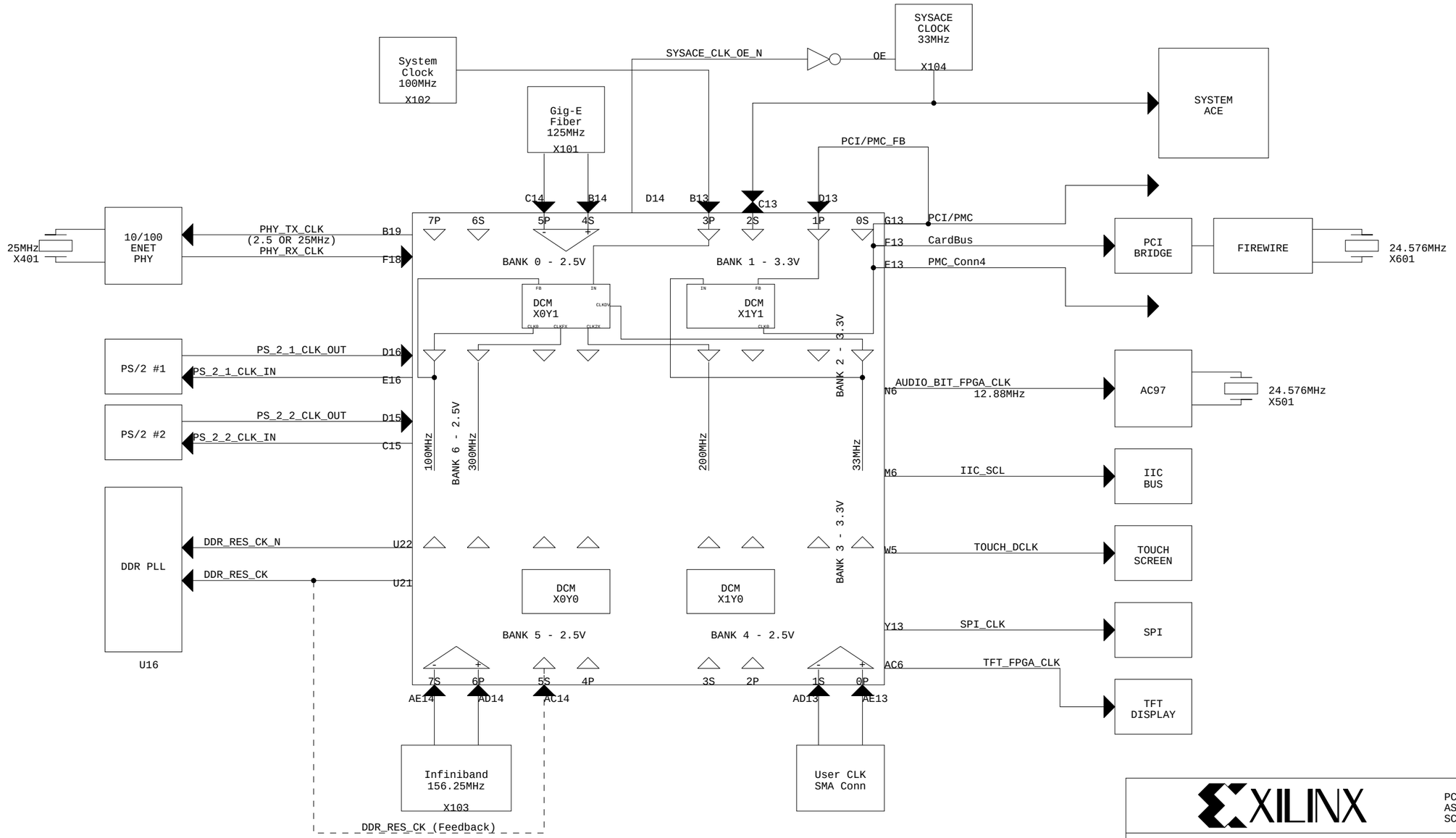
Figure 2: ML300 CPU
Virtex-II Pro Based
Clocking Distribution Diagram



Notes:
1. Internal clocking structure is design dependent

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PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
Clock Distribution Diagram

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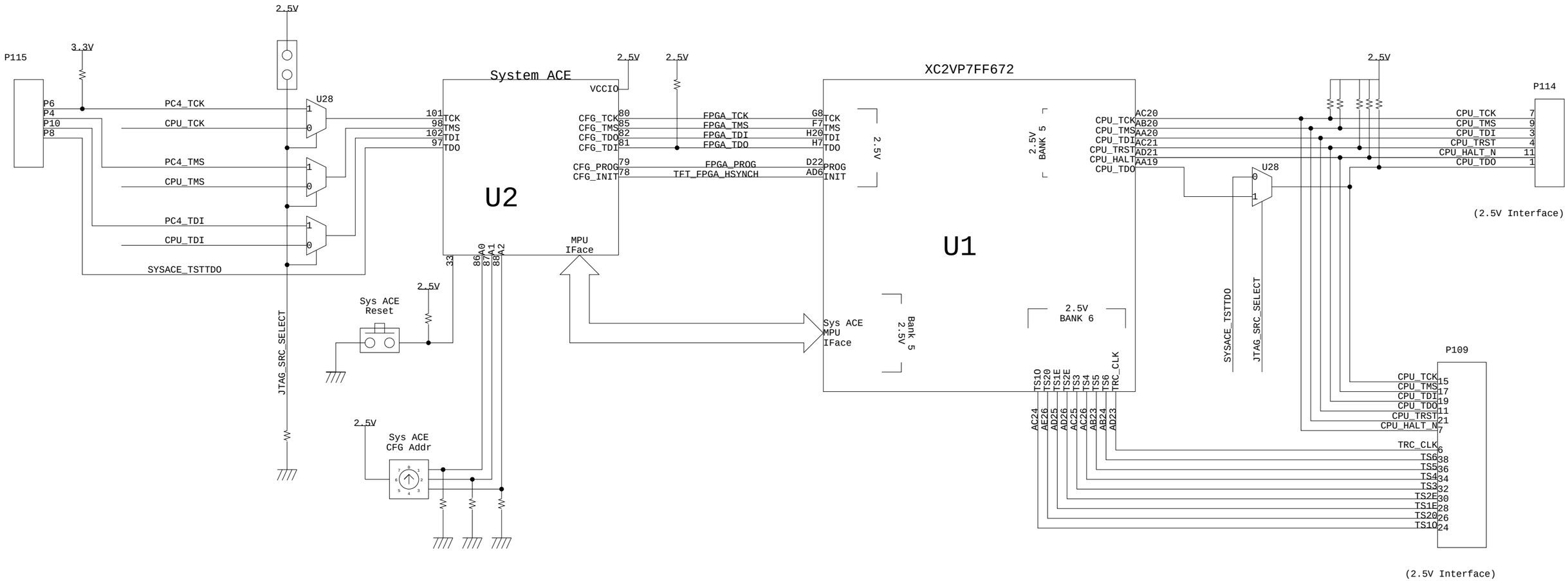
Figure 3: ML300 CPU
Virtex-II Pro Based
LOGICAL Configuration Diagram



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PCB: 1280285
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Title: ML300_CPU

JTAG / System ACE / Debug Diagram

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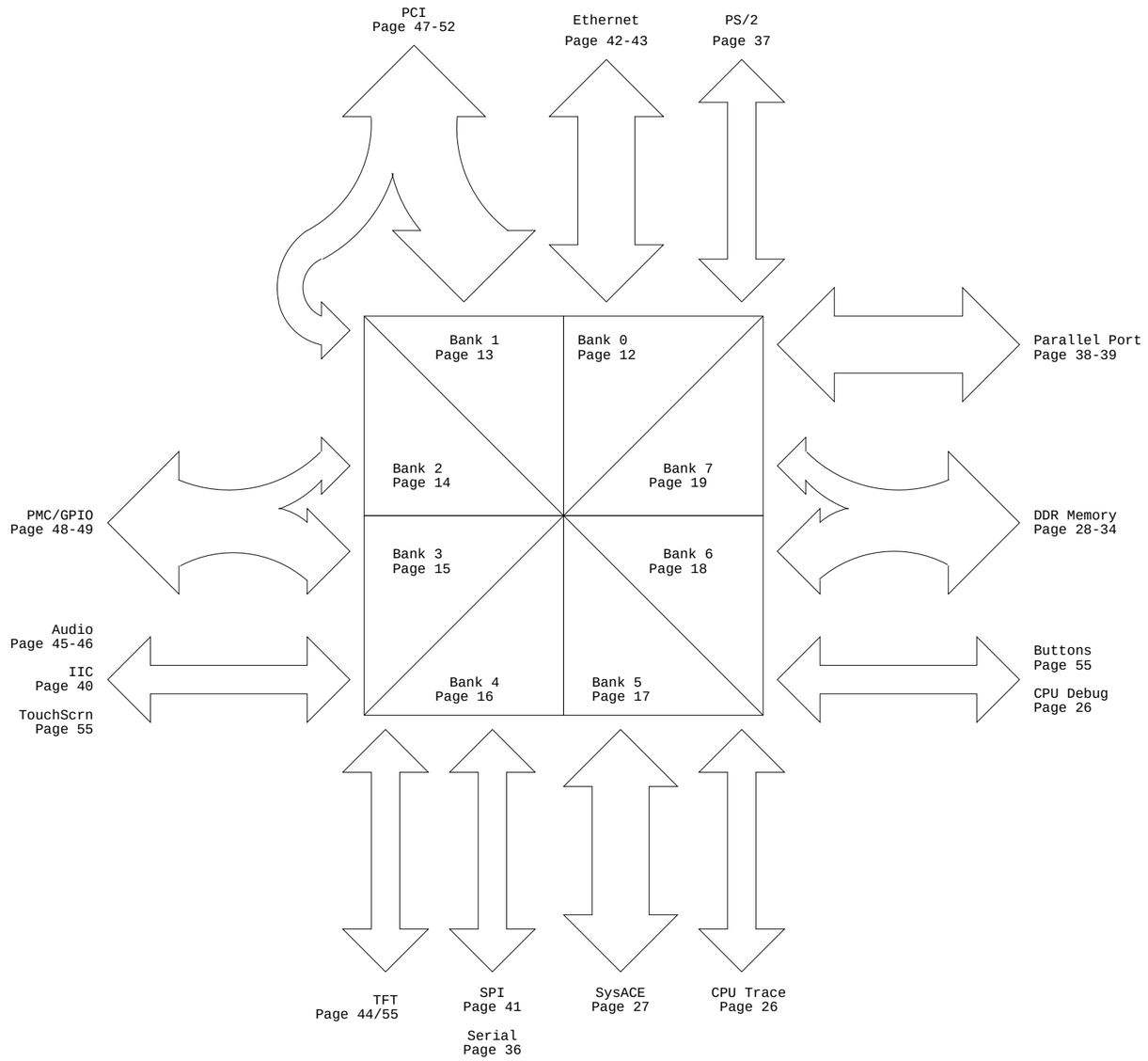
Figure 4: ML300 CPU
Virtex-II Pro Based
FPGA Bankout Diagram



MGT BLOCKS
- Banks 0 and 1 - Page 22
- Banks 4 and 5 - Page 21

MISC FPGA Pins
- Page 20

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Title: ML300_CPU
FPGA Banking

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Table 2: ML300 CPU
Virtex-II Pro Based
Part Index

IC Index (U*)

RefDes	Page	Description
U1	12-22	XC2VP7-FF672
U2	27	System ACE
U3	24	LT1963ES8 MGT VTT Linear Regulator
U4	13	PCI VCCO Linear Regulator
U6	30	HYB25D256800AT-7 DDR Chip
U7	30	HYB25D256800AT-7 DDR Chip
U8	30	HYB25D256800AT-7 DDR Chip
U9	30	HYB25D256800AT-7 DDR Chip
U14	29	SSTV16857 DDR Register
U15	29	SSTV16857 DDR Register
U16	28	CDCV857 DDR Clock Replicator
U19	37	74C914 PS/2 Buffer
U20	38	QS34XV245 Par Port Clamp Diode
U21	39	SN74LVC161284DGGR Par Port XCVR
U22	39	SN74CBT16210DGGR Par Port LED Buf
U26	42	LXT971_LQFP64 Ethernet Phy
U27	44	74ALVC164245 TFT Level Shifter
U28	44	74ALVC164245 TFT Level Shifter
U50	47	QS32X2245 PCI Clamp Diode
U51	47	QS32X2245 PCI Clamp Diode
U52	47	QS32X2245 PCI Clamp Diode
U53	47	QS316211 PCI Clamp Diode
U58	53	TPS2216A PCMCIA Power Regulator
U59	54	TSB41AB1 IEE1394 (Firewire) Phy
U60	26	74ALVC157A JTAG/Trace MUX
U101	24	LT1963-25EQ MGT VCC Linear Reg
U251	40	MAX1617 FPGA IIC Temp Sensor
U252	40	LM76CNM_3 IIC Ambient Temp Sensor
U253	40	24LC32A IIC EEPROM
U254	41	25LC160_SN SPI EEPROM
U255	40	MAX6683 IIC Power Monitor
U256	40	MAX6652 IIC Power Monitor
U270	36	MAX3388E UART Transceiver
U271	36	MAX3388E UART Transceiver
U500	45	AD1885 Audio Codec
U501	46	LM4835 Audio Amplifier
U502	40	DS1845 IIC Audio Volume Trimpot
U601	50	PCI4451GFN PCMCIA to PCI Bridge
U802	48	QS32X2245 PMC Clamp Diode
U912	48	QS32X2245 PMC Clamp Diode
U913	48	QS32X2245 PMC Clamp Diode
U914	48	QS32X2245 PMC Clamp Diode
U1001	33	ML6554 DDR Switching Regulator

Diodes/Transistors (D*/Q*)

RefDes	Page	Description
D601	47	Clamp Diode VCC Diode
D602	47	Clamp Diode VCC Diode
D603	47	Clamp Diode VCC Diode
D604	47	Clamp Diode VCC Diode
D605	54	Fire Wire VCC Diode
D801	48	Clamp Diode VCC Diode
D901	48	Clamp Diode VCC Diode
D902	48	Clamp Diode VCC Diode
D903	48	Clamp Diode VCC Diode
Q101	20	Re-drive FPGA Done for LED
Q103	13	System ACE Clock OE FET
Q401	35	Re-drive Illum Signals for LEDs
Q402	35	Re-drive Illum Signals for LEDs
Q403	37	Dual FET for PS/2 Transceivers
Q404	37	Dual FET for PS/2 Transceivers
Q405	35	Re-drive Illum Signals for LEDs

Header Index (J*)

RefDes	Page	Description
J1	16	SMA User Clock P-side
J2	16	SMA User Clock N-side
J101	55	HDR 2x32 Digital Connector #1
J102	55	HDR 2x32 Digital Connector #2
J103	55	HDR 2x25 Power Connector
J104	49	PMC Connector #1
J105	49	PMC Connector #2
J106	49	PMC Connector #4
J204	26	HDR 1x2 JTAG MUX Select
J505	46	Audio Left Speaker Jack
J506	46	Audio Right Speaker Jack

Port Index (P*)

RefDes	Page	Description
P101	39	DB25 Parallel Port
P102	23	GIGE-R14K-ST11 Quad Fiber XCVR
P103	42	RJ45 Ethernet Port w/LEDs
P104	37	Shielded Minidin-6 PS/2 Port
P105	37	Shielded Minidin-6 PS/2 Port
P106	36	DB9 Serial Port
P107	36	DB9 Serial Port
P108	54	1394A Firewire Connector
P109	26	Trace/Debug Connector (Mictor-38)
P110	51	FCI71240-340CA Cardbus Top
P110	51	FCI71240-340CA Cardbus Bottom
P111	21	HSSCD2 (Infiniband) MGT Connector
P112	21	HSSCD2 (Infiniband) MGT Connector
P113	27	System ACE Compact Flash
P114	26	HDR 2x8 CPU Debug Connector
P115	26	HDR 2mm 2x7 JTAG Connector
P116	46	Stereo Jack Headphone/Line Out
P117	45	Stereo Jack Microphone In
P118	45	Stereo Jack Line In
P119	21	Serial ATA Connector (Host)
P120	21	Serial ATA Connector (Device)

LED Index (DS*)

RefDes	Page	Description
DS101	20	LED0603 Blue Done LED
DS102	35	Dual LED OPB Bus Error
DS103	35	Dual LED PLB Bus Error
DS201	27	LED0603 Red System ACE Error
DS202	27	LED0603 Green System ACE Status
DS203	27	LED0603 Red INIT LED
DS401	35	Round LED Blue Illumination
DS402	35	Round LED Blue Illumination
DS403	35	Round LED Blue Illumination
DS404	35	Round LED Blue Illumination
DS405	35	Round LED Blue Illumination
DS406	35	Round LED Blue Illumination
DS407	39	LED0603 Yellow Par Port Direction
DS408	39	LED0603 Yellow Par Port User Def 3
DS409	39	LED0603 Yellow Par Port User Def 1
DS410	39	LED0603 Yellow Par Port NWait
DS411	39	LED0603 Yellow Par Port Interrupt
DS412	39	LED0603 Green Par Port Data0
DS413	39	LED0603 Yellow Par Port NAStrobe
DS414	39	LED0603 Yellow Par Port Ninit
DS415	39	LED0603 Yellow Par Port User Def 2
DS416	39	LED0603 Yellow Par Port NDStrobe
DS417	39	LED0603 Yellow Par Port Nwrite
DS418	39	LED0603 Yellow Par Port High Drain
DS419	39	LED0603 Green Par Port Data1
DS420	39	LED0603 Green Par Port Data2
DS421	39	LED0603 Green Par Port Data3
DS422	39	LED0603 Green Par Port Data4
DS423	39	LED0603 Green Par Port Data5
DS424	39	LED0603 Green Par Port Data6
DS425	39	LED0603 Green Par Port Data7
DS426	42	LED0603 Green Ethernet Link Speed
DS427	35	Round LED Blue Illumination
DS428	35	Round LED Blue Illumination
DS429	35	Round LED Blue Illumination
DS430	35	Round LED Blue Illumination

Oscillator Index (X*)

RefDes	Page	Description
X101	12	EG2121/LV1145B Gig-E Clock 125MHz
X102	13	Half Size Osc System Clock 100MHz
X103	17	EG2121/LV1145B S-ATA/HSSCD2 Clock 156.25MHz
X104	13	Half Size Osc SysACE Clock 33MHz
X401	42	MA506 Ethenet Clock 25MHz
X501	45	MA506 Audio Clock 24.576MHz
X601	54	MA506 Firewire Clock 24.576 MHz

XILINX

PCB: 1280285
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SCH: 0381135

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SEMICONDUCTORS

QTY	REFDES	PKG	MANUFACTURE PN	MANUFACTURE	DESCRIPTION
8	D601,D602,D603,D604,D801,D901,D902,D903	SOD-323	1N4148WS-7	Diodes Inc	Diode, SMD
1	D605	MELF	1N5819M-13	Diodes Inc	Diode, SMD
11	DS101,DS401,DS402,DS403,DS404,DS405,DS406,DS427,DS428,DS429,DS430	0603	LTST-C190CBKT	Lite-On	LED, BLUE, SMD
2	DS102,DS103	LED_DUAL	LNJ115W8PRA	Panasonic	LED, Dual Red/Green, SMD
2	DS201,DS203	0603	SML-LX0603IW-TR	Lumex	LED, Red, SMD
10	DS202,DS412,DS419,DS420,DS421,DS422,DS423,DS424,DS425,DS426	0603	SML-LX0603GW-TR	Lumex	LED, Green, SMD
11	DS407,DS408,DS409,DS410,DS411,DS413,DS414,DS415,DS416,DS417,DS418	0603	SML-LX0603YW-TR	Lumex	LED, Yellow, SMD
5	Q101,Q103,Q401,Q402,Q405	SOT23	BSS138	Fairchild	Diode, SMD
2	Q403,Q404	SOT363	MMDT3904-7	Diodes Inc	Transistor, Dual NPN
1	U1	FF672	XC2VP7-6FF672C	Xilinx	IC, FPGA, XC2VP7-6FF672C
1	U2	TQFP144	XCCACE-TQ144I	Xilinx	IC, Logic, SystemACE
1	U3	LINEAR_SO8	LT1963ES8	Linear Tech	IC, Linear, Voltage Reg, 1.5A, Adjustable, LDO
1	U4	LINEAR_SO8	LT1763CS8	Linear Tech	IC, Linear, Voltage Reg, 500mA, Adjustable, LDO
4	U6,U7,U8,U9	TSOP_66	HYB25D256800AT-7	Infineon	IC, Memory, DDR SDRAM, 256Mbit
2	U14,U15	TVSOP48	SN74SSTV16857DGVR	TI	IC, Logic, 14 bit register, SSTL2, Dual Phase Clock
1	U16	TSSOP48	CDCV857DGGR	TI	IC, Analog, Phase Lock Loop
1	U19	SOIC14	DM74AS1034AM	National	IC, Logic, Hex Driver
1	U20	MILLIPAQ80	QS34XV245Q3	IDT	IC, Logic, Quickswitch, 32 bit
1	U21	TSSOP48	SN74LVC161284DGGR	TI	IC, Logic, IEEE-1284 Driver & Level Translator
1	U22	TSSOP48	SN74CBTD16210DGGR	TI	IC, Logic, Bus Switch, 20 bit, Level Translator
1	U26	LQFP64	DJLXT971ALCA4834105	Intel	IC, Logic, Ethernet PHY
2	U27,U28	TSSOP48	SN74ALVC164245DGGR	TI	IC, Logic, Transceiver, 16 bit
7	U50,U51,U52,U802,U912,U913,U914	QVSOP40	QS32X2245Q2	IDT	IC, Logic, Quickswitch, 16 bit
1	U53	TSSOP56	QS316211PA	IDT	IC, Logic, Quickswitch, 24 bit
1	U58	DAP32	TPS2216ADAP	TI	IC, Analog, Power Switch for PCMCIA
1	U59	S-PQFP-G48	TSB41AB1PHP	TI	IC, Logic, IEEE-1394a PHY
1	U60	TSSOP16	SN74LVC157APWR	TI	IC QUAD, 2-1 DATA SEL/MUX
1	U101	5-DD	LT1963EQ-25	Linear Tech	IC, Linear, Voltage Reg, 1.5A, 2.5V, LDO
1	U251	QSOP16	MAX1617AMEE	Maxim	IC, Linear, IIC Remote Diode Temperature Sensor
1	U252	SOP8	LM76CNM-3	National	IC, Linear, IIC Temperature Sensor
1	U253	SOIC8	24LC32A/SN	Microchip	IC, Memory, IIC EPROM, 32K
1	U254	SOIC8	25LC160/SN	Microchip	IC, Memory, SPI EPROM, 16K
1	U255	10_UMAX	MAX6683AUB	Maxim	IC, Logic, System Monitor, 1.8V, 2.5V, 5V
1	U256	10_UMAX	MAX6652AUB	Maxim	IC, Logic, System Monitor, 12V, 2.5V, 3.3V
2	U270,U271	TSSOP24	MAX3388ECUG	Maxim	IC, Analog, RS-232 Level Translator
1	U500	LQFP48	AD1885JST	Analog	IC, Logic, AC97 Audio Codec, SMD
1	U501	TSSOP28	LM4835MTE	National	IC, Analog, Audio Amplified, 1W
1	U502	TSSOP14	DS1845E-010/T&R	Dallas Semi	IC, Analog, Potentiometer, IIC controlled, dual
1	U601	S-PBGA-N256	PCI4451GFN	TI	IC, Logic, PCI to PCMCIA / CardBus Bridge
1	P102		R14K-ST11	Stratos Lightwave	IC, Optical Transceiver, Gigabit Etherent, 4X

OSCILATORS / CRYSTALS

QTY	REFDES	FREQUENCY	MANUFACTURE PN	MANUFACT	DESCRIPTION
1	X101	125.000 MHZ	LV11B003-125.0M	Pletronics	Oscillator, SMT
1	X102	100.000 MHZ	EH1325HSTS-100.000M	Ecliptek	Oscillator, TH, Half Size
1	X103	156.250 MHZ	LV11B004-156.25M	Pletronics	Oscillator, SMT
1	X104	33.000 MHz	EH1325HSTS-33.000M	Ecliptek	Oscillator, TH, Half Size
1	X401	25.000 MHZ	MA-506 25.000M-C0	Epson	Crystal, 25.000 MHz, MA_506
2	X501,X601	24.576 MHZ	MA-506 24.576M-C0	Epson	Crystal, 24.576 MHz, MA_506

ML300 CPU - BOM

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CAPACITORS

QTY	REFDES	VALUE	TOL	VOLT	KIND	PKG	MANUFACTURE PN	MANUFACTURE
2	C542,C543	220UF	10%	10V	TANT	X	T491X227K010AS	Kemet
5	C1001,C1002,C1003,C1008,C1009	220UF	20%	6.3V	TANT	D	EEJ-L0JD227R	Panasonic
1	C191	100UF	20%	10V	TANT	D	ECS-T1AD107R	Panasonic
8	C787,C788,C789,C790,C791,C792,C793,C794	47UF	20%	6.3V	TANT	B	ECS-T0JX476R	Panasonic
6	C188,C192,C197,C673,C675,C795	33UF	20%	10V	TANT	B	ECS-T1AX336R	Panasonic
1	C356	22UF	20%	6.3V	TANT	A	ECS-T0JY226R	Panasonic
3	C674,C796,C797	10UF	20%	20V	TANT	C	ECS-T1DC106R	Panasonic
5	C512,C519,C522,C528,C537	10UF	20%	16V	TANT	B	ECS-T1CX106R	Panasonic
23	C16,C18,C21,C189,C230,C231,C317,C318,C319,C320,C321,C322,C323,C324,C335,C336,C337,C338, C339,C340,C346,C352,C1028	10UF	20%	10V	TANT	A	ECS-T1AY106R	Panasonic
2	C103,C106	10UF	+80/-20	6.3V	CERAMIC	0805	ECJ-2FF0J106Z	Panasonic
8	C180,C181,C182,C183,C184,C185,C186,C187	22UF	12%	6.3V	CERAMIC	1206	C1206C226Z9VACTU	Kemet
12	C775,C776,C777,C778,C779,C780,C781,C783,C784,C785,C786,C1012	4.7UF	10%	16V	TANT	A	T491A475K016AS	Kemet
7	C516,C517,C525,C526,C527,C534,C538	1UF	10%	20V	TANT	A	T491A105K020AS	Kemet
2	C10,C19	1UF	+80/-20	10V	CERAMIC	0603	ECJ-1VF1A105Z	Panasonic
2	C532,C533	0.33UF	10%	35V	TANT	A	T491A334K035AS	Kemet
5	C501,C502,C503,C504,C506	0.33UF	10%	16V	CERAMIC	0805	ECJ-2YB1C334K	Panasonic
32	C120,C121,C122,C123,C124,C125,C126,C127,C128,C129,C130,C131,C132,C133,C134,C135,C140,C141, C142,C143,C144,C145,C146,C147,C148,C149,C150,C151,C152,C153,C154,C155	0.22UF	10%	25V	CERAMIC	0805	ECJ-2YB1E224K	Panasonic
12	C270,C271,C272,C273,C274,C275,C276,C277,C278,C279,C678,C682	0.22UF	10%	10V	CERAMIC	0603	ECJ-1VB1A224K	Panasonic
205	C9,C11,C12,C13,C17,C20,C22,C23,C102,C105,C193,C194,C195,C196,C215,C216,C217,C218,C219, C220,C221,C222,C223,C224,C225,C226,C227,C228,C229,C250,C252,C253,C254,C255,C280,C281,C301, C302,C303,C304,C305,C306,C307,C308,C309,C310,C311,C312,C313,C314,C315,C325,C326,C327,C328, C329,C330,C331,C332,C333,C334,C341,C342,C343,C344,C345,C347,C348,C349,C350,C351,C353,C354, C355,C357,C358,C359,C360,C361,C362,C363,C364,C365,C511,C513,C520,C521,C523,C524,C529,C530, C531,C535,C536,C541,C676,C677,C679,C680,C681,C690,C693,C697,C698,C701,C702,C703,C704,C705, C706,C707,C708,C709,C710,C711,C712,C713,C714,C715,C716,C717,C718,C719,C720,C721,C722,C723, C724,C725,C726,C727,C728,C729,C730,C731,C732,C733,C734,C735,C736,C737,C738,C739,C740,C741, C742,C743,C744,C745,C746,C747,C748,C749,C750,C751,C752,C753,C754,C755,C756,C757,C758,C759, C760,C761,C762,C763,C764,C765,C766,C767,C768,C769,C770,C771,C772,C773,C774,C801,C802,C803, C804,C805,C806,C807,C808,C809,C1004,C1005,C1011,C1013,C1014,C1015,C1016,C1017,C1018,C1019, C1020,C1021,C1022,C1023,C1024,C1025,C1026,C1027	0.1UF	+80/-20	16V	CERAMIC	0402	ECJ-0EF1C104Z	Panasonic
31	C5,C26,C112,C113,C114,C115,C116,C117,C118,C119,C156,C157,C158,C159,C160,C161,C164,C165, C166,C167,C168,C169,C172,C173,C176,C177,C686,C688,C689,C691,C696	0.01UF	10%	16V	CERAMIC	0402	C0402C103K4RACTU	Kemet
2	C539,C540	68000PF	10%	10V	CERAMIC	0402	ECJ-0EB1A683K	Panasonic
1	C518	47000PF	10%	10V	CERAMIC	0402	ECJ-0EB1A473K	Panasonic
1	C251	2200PF	10%	25V	CERAMIC	0402	C0402C222K3RACTU	Kemet
3	C1,C2,C3	1000PF	10%	2000V	CERAMIC	1812	1808B102K202NT	Novacap
11	C14,C15,C24,C25,C101,C104,C687,C692,C694,C695,C1010	1000PF	10%	50V	CERAMIC	0402	ECJ-0EB1H102K	Panasonic
2	C507,C508	470PF	10%	25V	CERAMIC	0402	ECJ-0EB1E471K	Panasonic
4	C4,C6,C514,C515	270PF	5%	50V	CERAMIC	0603	ECJ-1VC1H271J	Panasonic
1	C685	220PF	5%	50V	CERAMIC	0402	ECJ-0EC1H221J	Panasonic
2	C1006,C1007	30PF	5%	50V	CERAMIC	0402	ECU-E1H300JCQ	Panasonic
2	C509,C510	22PF	5%	50V	CERAMIC	0402	ECJ-0EC1H220J	Panasonic
2	C7,C8	18PF	5%	50V	CERAMIC	0402	ECJ-0EC1H180J	Panasonic
2	C683,C684	12PF	5%	50V	CERAMIC	0402	ECJ-0EC1H120J	Panasonic
1	C366	10PF	5%	50V	CERAMIC	0402	ECJ-0EC1H100D	Panasonic

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RESISTORS

QTY	REFDES	VALUE	TOL	WATT	PKG	MANUFACTURE PN	MANUFACTURE
2	R512,R633	1M	5%	1/16W	0402	ERJ-2GEJ105X	Panasonic
1	R634	402K	1%	1/16W	0402	ERJ-2RKF4023X	Panasonic
4	R538,R539,R1002,R1005	100K	1%	1/16W	0402	ERJ-2RKF1003X	Panasonic
3	R514,R515,R516	47.0K	1%	1/16W	0402	9C04021A4702FLHF3	Yageo America
1	R676	43.0K	1%	1/16W	0402	9C04021A4302FLHF3	Yageo America
1	R450	22.1K	1%	1/16W	0402	ERJ-2RKF2212X	Panasonic
10	R518,R519,R520,R521,R523,R524,R525,R526,R527,R528	20.0K	1%	1/16W	0402	ERJ-2RKF2002X	Panasonic
25	R170,R222,R223,R224,R225,R250,R251,R252,R254,R255,R407,R408,R415,R418,R513,R619,R620,R621,R622,R641,R642, R833,R945,R946,R947	10.0K	1%	1/16W	0402	ERJ-2RKF1002X	Panasonic
1	R501	6.80K	1%	1/16W	0402	9C04021A6801FLHF3	Phycomp
1	R637	6.34K	1%	1/16W	0402	ERJ-2RKF6341X	Panasonic
1	R632	5.10K	1%	1/16W	0402	9C04021A5101FLHF3	Yageo America
46	R125,R129,R133,R180,R208,R209,R210,R211,R212,R217,R218,R221,R260,R261,R262,R263,R264,R409,R410,R411,R414, R439,R444,R462,R463,R464,R465,R491,R495,R496,R498,R499,R503,R504,R505,R506,R507,R508,R509,R624,R628,R647, R659,R675,R702,R1006	4.7K	5%	1/16W	0402	ERJ-2GEJ472X	Panasonic
1	R510	2.00K	1%	1/16W	0402	ERJ-2RKF2001X	Panasonic
4	R412,R413,R416,R417	1.80K	1%	1/16W	0402	9C04021A1801FLHF3	Yageo America
15	R167,R213,R214,R215,R216,R269,R535,R536,R629,R638,R639,R643,R644,R645,R1001	1.00K	1%	1/16W	0402	ERJ-2RKF1001X	Panasonic
1	R166	487R	1%	1/16W	0402	ERJ-2RKF4870X	Panasonic
1	R171	330R	1%	1/16W	0402	9C04021A3300FLHF3	Yageo America
3	R253,R441,R443	200R	1%	1/16W	0402	ERJ-2RKF2000X	Panasonic
8	R146,R147,R148,R149,R150,R151,R152,R153	180R	1%	1/16W	0402	9C04021A1800FLHF3	Yageo America
23	R105,R106,R113,R114,R419,R420,R421,R422,R423,R424,R425,R426,R427,R428,R429,R430,R431,R432,R433,R434,R435, R436,R437	130R	1%	1/16W	0402	ERJ-2RKF1300X	Panasonic
16	R107,R119,R120,R121,R122,R123,R124,R169,R174,R175,R176,R179,R265,R266,R1003,R1004	100R	1%	1/16W	0402	ERJ-2RKF1000X	Panasonic
11	R127,R401,R402,R403,R404,R405,R406,R466,R467,R468,R469	64.9R	1%	1/16W	0402	ERJ-2RKF64R9X	Panasonic
7	R183,R185,R268,R630,R631,R635,R636	56.2R	1%	1/16W	0402	ERJ-2RKF56R2X	Panasonic
5	R184,R186,R220,R625,R626	51.1R	1%	1/16W	0402	ERJ-2RKF51R1X	Panasonic
16	R302,R303,R304,R305,R309,R310,R315,R316,R317,R318,R440,R442,R445,R446,R447,R448	49.9R	1%	1/16W	0402	ERJ-2RKF49R9X	Panasonic
1	R182	38.3R	1%	1/8W	0805	9C08052A38R3FKHFT	Yageo America
1	R181	26.1R	1%	1/8W	0805	9C08052A26R1FKHFT	Yageo America
8	R108,R172,R173,R219,R307,R308,R438,R1007	25.5R	1%	1/16W	0402	ERJ-2RKF25R5X	Panasonic
7	R301,R306,R311,R312,R313,R314,R319	22.1R	1%	1/16W	0402	ERJ-2RKF22R1X	Panasonic
11	R449,R452,R453,R454,R455,R456,R457,R458,R459,R460,R461	20.0R	1%	1/16W	0402	ERJ-2RKF20R0X	Panasonic
2	R533,R534	0R	5%	1/10W	0805	ERJ-6GEY0R00V	Panasonic
15	R134,R135,R136,R137,R138,R139,R140,R141,R168,R226,R227,R451,R623,R627,R640	0R	5%	1/16W	0402	ERJ-2GE0R00X	Panasonic
35	RP302,RP303,RP304,RP308,RP311,RP315,RP316,RP317,RP318,RP319,RP320,RP321,RP322,RP323,RP324,RP325,RP326, RP327,RP328,RP332,RP347,RP348,RP350,RP351,RP353,RP354,RP356,RP357,RP359,RP360,RP361,RP362,RP363,RP910, RP914	22R	5%	1/16W	8PIN	742C083220JTR	CTS
17	RP329,RP330,RP331,RP336,RP338,RP339,RP340,RP341,RP344,RP345,RP346,RP349,RP352,RP355,RP358,RP365,RP603	47R	5%	1/16W	8PIN	EXB-E10C470J	Panasonic
2	RP401,RP402	4.7K	5%	1/16W	8PIN	742C083472JTR	CTS
5	RP601,RP602,RP604,RP605,RP606	4.7K	5%	1/16W	8PIN	EXB-E10C472J	Panasonic

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OTHER

QTY	REFDES	VALUE	TOL	PKG	MANUFACTURE PN	MANUFACTURE	
1	F601	1.1A		2920	SMD100-2	RayChem	Fuse, 1.1A, SMD, Self Healing
33	FB101,FB102,FB103,FB104,FB105,FB106,FB107,FB108,FB109,FB110, FB111,FB112,FB113,FB114,FB115,FB116,FB117,FB118,FB119,FB120, FB121,FB122,FB123,FB124,FB125,FB126,FB127,FB128,FB129,FB130, FB131,FB132,FB601	1000_OHM		0805	BLM21AH102SN1D	Murata	Ferrite Bead, SMD
8	FB133,FB134,FB135,FB136,FB137,FB138,FB139,FB140	47UH	10%	1210	ELJ-PA470KF	Panasonic	Inductor, SMD
8	FB141,FB403,FB405,FB406,FB501,FB502,FB603,FB605	125_OHM		1812	CTCB1812-125S	CTParts	Ferrite Bead, SMD
8	FB301,FB302,FB402,FB404,FB602,FB604,FB606,FB607	60_OHM		1210	CTCB1210-600S	CTParts	Ferrite Bead, SMD
1	L1001	3.3UH		DO3316	DO3316P-332	Coilcraft	Inductor, SMD
1	T401			SOIC16	TG110-S050N2	Halo	Transformer, Ethernet Pulse
1	PCB1					Ambitech	ML300_CPU Printed Circuit Board
1	PCB1b					Axiom	ML300_CPU Printed Circuit Board Assembly
1	ML300_SERNUM_LABEL					Axiom	Label, Polyimide, ML300 Serial Number
1	ML300_MACID_LABEL					Axiom	Label, Polyimide, MAC BASE ADDR

HARDWARE

QTY	DESCRIPTION	MANU PN	MANU
6	Hardware, Screw, 4-40 x 3/8, Pan Head, SS	MS51957-15	Olander
4	Hardware, Screw, 2-56 x 3/4, Pan Head, SS	2C75PPMS	Olander
2	Hardware, Screw, 2-56 x 3/8, Pan Head, SS	2C37PPMS	Olander
12	Hardware, Washer, Flat 4-40 SS	620C4L	Olander
6	Hardware, Washer, Lock, 4-40 SS	4NSLWS	Olander
6	Hardware, Nut, 4-40, SS	4CHNTS	Olander
6	Hardware, Washer, Lock 2-56 SS	2NSLWS	Olander
6	Hardware, Washer, Flat 2-56 SS	620C2	Olander
6	Hardware, Nut, 2-56, SS, Small	2CSHNS	Olander

DO NOT POPULATE PARTS

QTY	REFDES	STATE	PKG
2	R531,R532	DNP	805
8	R130,R256,R257,R258,R259,R267,R502,R649	DNP	402
2	J505,J506	DNP	SIP2
3	E601,E603,E605	DNP	BOWTIE_OPEN
3	E602,E604,E606	DNP	BOWTIE_CLOSED
6	MH1,MH2,MH3,MH4,MH5,MH6	DNP	JACK_109_280
4	MH7,MH8,MH9,MH10	DNP	JACK_116_280
34	TP101,TP102,TP104,TP105,TP106,TP107,TP108,TP214,TP215,TP216,TP217, TP218,TP219,TP220,TP221,TP254,TP255,TP256,TP301,TP302,TP415,TP416, TP419,TP421,TP423,TP424,TP425,TP426,TP427,TP501,TP607,TP650,TP1001	DNP	TESTPOINT

CONNECTORS

QTY	REFDES	MANUFACTURE PN	MANUFACTURE	DESCRIPTION
2	J1,J2	901-144-8RFX	Amphenol-RF Division	Connector, SMA, Straight
2	J101,J102	EW-32-11-G-D-400	Samtec	Connector, Through Hole, Male
1	J103	EW-25-11-G-D-400	Samtec	Connector, Through Hole, Male
3	J104,J105,J106	71439-2164	Molex	Connector, PCI Mezzanine, Main Board
1	J204	22-12-2024	Molex	Header, Right Angle, 2 pin
1	P101	745783-4	AMP	Connector, DB25, Female
1	P103	569564-1	AMP	Connector, RJ45, Thru-Hole
2	P104,P105	MD-60SM	CUI Inc	Connector, MiniDIN6, Shielded, P/S2
2	P106,P107	747250-4	AMP	Connector, DB9, Male
1	P108	53462-0611	Molex	Connector, IEEE-1394A
1	P109	67089-1	AMP	Connector, Mictor, Edge Launch, 38 pin
1	P110	71240-340CA	FCI	Connector, Assembly, Dual PCMCIA with Left side eject
2	P110a, P110b	73277-101000	FCI	Connector, PCMCIA SMT Connector
2	P111,P112	1364532-1	AMP	Connector, HSSDC2, SMD
1	P113	N7E50-7516HG-50	3M	Connector, Compact Flash, SMD
1	P113a	7E50-9316-04	3M	Ejector, Compact Flash
1	P114	PZC08DBAN	Sullins Electric	Header, 2x8, 100mil, right angle
1	P115	87333-1420	Molex	Header, 2X7, 2mm
3	P116,P117,P118	35RASMT4BHNTR	Switchcraft	Connector, Stereo Phone Jack
2	P119,P120	67490-9221	Molex	Connector, Serial ATA, SMD
3	TP1,TP2,TP3	10-109-3-1	Concord Electronics	Testpoint, Turret
2	X102a, X104a	1108800	Aries	Socket, 8 pin DIP

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```
NET_CLASS DATA
{
NET_CLASS AUDIO_DIG_FPGA
{
NET AUDIO_BIT_FPGA_CLK
NET AUDIO_FPGA_SYNCH
NET AUDIO_FPGA_CS0
NET AUDIO_FPGA_SDATA_OUT
NET AUDIO_FPGA_SDATA_IN
NET AUDIO_FPGA_RESET_N
}
NET_CLASS AUDIO_DIG_PMC
{
NET AUDIO_PMC_BIT_CLK
NET AUDIO_PMC_SYNCH
NET AUDIO_PMC_CS0
NET AUDIO_PMC_SDATA_OUT
NET AUDIO_PMC_SDATA_IN
NET AUDIO_PMC_RESET_N
}
NET_CLASS AUDIO_DIG_COMP
{
NET AUDIO_BIT_CLK
NET AUDIO_SYNCH
NET AUDIO_SDATA_OUT
NET AUDIO_SDATA_IN
NET AUDIO_RESET_N
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NET_CLASS CARDBUSA
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NET CARDBUSA_CAD3
NET CARDBUSA_CAD2
NET CARDBUSA_CAD1
NET CARDBUSA_CAD0
NET CARDBUSA_CAD15
NET CARDBUSA_CAD14
NET CARDBUSA_CAD13
NET CARDBUSA_CAD12
NET CARDBUSA_CAD19
NET CARDBUSA_CAD18
NET CARDBUSA_CAD17
NET CARDBUSA_CAD16
NET CARDBUSA_CAD23
NET CARDBUSA_CAD22
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NET CARDBUSA_CAD6
NET CARDBUSA_CAD5
NET CARDBUSA_CAD4
NET CARDBUSA_CAD11
NET CARDBUSA_CAD10
NET CARDBUSA_CAD9
NET CARDBUSA_CAD8
NET CARDBUSA_CTRDY
NET CARDBUSA_CDEVSEL
NET CARDBUSA_CSTOP
NET CARDBUSA_CBLOCK
NET CARDBUSA_CVS1
NET CARDBUSA_CCBE3
NET CARDBUSA_CCBE2
NET CARDBUSA_CCBE1
NET CARDBUSA_CCBE0
NET CARDBUSA_CCLKRUN
NET CARDBUSA_CIRDY
NET CARDBUSA_CCLK
NET CARDBUSA_CSERR
NET CARDBUSA_CRST
NET CARDBUSA_CVS2
NET CARDBUSA_CFRAME
NET CARDBUSA_CINT
NET CARDBUSA_CGNT
NET CARDBUSA_CPERR
NET CARDBUSA_CPAR
NET CARDBUSA_CCD2
NET CARDBUSA_CCD1
NET CARDBUSA_CSTSCHG
NET CARDBUSA_CAUDIO
NET CARDBUSA_CREQ
NET CARDBUSA_RSV_A18
NET CARDBUSA_RSV_D2
NET CARDBUSA_RSV_D14
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NET CARDBUSB_CAD3
NET CARDBUSB_CAD2
NET CARDBUSB_CAD1
NET CARDBUSB_CAD0
NET CARDBUSB_CAD15
NET CARDBUSB_CAD14
NET CARDBUSB_CAD13
NET CARDBUSB_CAD12
NET CARDBUSB_CAD19
NET CARDBUSB_CAD18
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NET CARDBUSB_CAD9
NET CARDBUSB_CAD8
NET CARDBUSB_CTRDY
NET CARDBUSB_CDEVSEL
NET CARDBUSB_CSTOP
NET CARDBUSB_CBLOCK
NET CARDBUSB_CVS1
NET CARDBUSB_CCBE3
NET CARDBUSB_CCBE2
NET CARDBUSB_CCBE1
NET CARDBUSB_CCBE0
NET CARDBUSB_CCLKRUN
NET CARDBUSB_CIRDY
NET CARDBUSB_CCLK
NET CARDBUSB_CSERR
NET CARDBUSB_CRST
NET CARDBUSB_CVS2
NET CARDBUSB_CFRAME
NET CARDBUSB_CINT
NET CARDBUSB_CGNT
NET CARDBUSB_CPERR
NET CARDBUSB_CPAR
NET CARDBUSB_CCD2
NET CARDBUSB_CCD1
NET CARDBUSB_CSTSCHG
NET CARDBUSB_CAUDIO
NET CARDBUSB_CREQ
NET CARDBUSB_RSV_A18
NET CARDBUSB_RSV_D2
NET CARDBUSB_RSV_D14
}
NET_CLASS CPU_DEBUG
{
NET CPU_HALT_N
NET CPU_TDO
NET CPU_TCK
NET CPU_TMS
NET CPU_TDI
NET CPU_TRST
}
NET_CLASS DDR_ADDR_FPGA
{
NET DDR_FPGA_A06
NET DDR_FPGA_A05
NET DDR_FPGA_A04
NET DDR_FPGA_A03
NET DDR_FPGA_A02
NET DDR_FPGA_A01
NET DDR_FPGA_A00
NET DDR_FPGA_A12
NET DDR_FPGA_A11
NET DDR_FPGA_A10
NET DDR_FPGA_A09
NET DDR_FPGA_A08
NET DDR_FPGA_A07
}
```

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NET_CLASS DDR_CLK_FPGA
{
NET DDR_FPGA_CK_N
NET DDR_FPGA_CK
}
NET_CLASS DDR_DM_FPGA
{
NET DDR_FPGA_DM3
NET DDR_FPGA_DM2
NET DDR_FPGA_DM1
NET DDR_FPGA_DM0
}
NET_CLASS DDR_DATA_FPGA
{
NET DDR_FPGA_DQ03
NET DDR_FPGA_DQ02
NET DDR_FPGA_DQ01
NET DDR_FPGA_DQ00
NET DDR_FPGA_DQ07
NET DDR_FPGA_DQ06
NET DDR_FPGA_DQ05
NET DDR_FPGA_DQ04
NET DDR_FPGA_DQ11
NET DDR_FPGA_DQ10
NET DDR_FPGA_DQ09
NET DDR_FPGA_DQ08
NET DDR_FPGA_DQ15
NET DDR_FPGA_DQ14
NET DDR_FPGA_DQ13
NET DDR_FPGA_DQ12
NET DDR_FPGA_DQ19
NET DDR_FPGA_DQ18
NET DDR_FPGA_DQ17
NET DDR_FPGA_DQ16
NET DDR_FPGA_DQ23
NET DDR_FPGA_DQ22
NET DDR_FPGA_DQ21
NET DDR_FPGA_DQ20
NET DDR_FPGA_DQ27
NET DDR_FPGA_DQ26
NET DDR_FPGA_DQ25
NET DDR_FPGA_DQ24
NET DDR_FPGA_DQ31
NET DDR_FPGA_DQ30
NET DDR_FPGA_DQ29
NET DDR_FPGA_DQ28
}
NET_CLASS DDR_DQS_FPGA
{
NET DDR_FPGA_DQS3
NET DDR_FPGA_DQS2
NET DDR_FPGA_DQS1
NET DDR_FPGA_DQS0
}
NET_CLASS DDR_CNTL_FPGA
{
NET DDR_FPGA_CKE
NET DDR_FPGA_RAS_N
NET DDR_FPGA_CAS_N
NET DDR_FPGA_BA1
NET DDR_FPGA_BA0
NET DDR_FPGA_CS_N
NET DDR_FPGA_WE_N
}
NET_CLASS DDR_ADDR_MEM
{
NET DDR_MEM_A06
NET DDR_MEM_A05
NET DDR_MEM_A04
NET DDR_MEM_A03
NET DDR_MEM_A02
NET DDR_MEM_A01
NET DDR_MEM_A00
NET DDR_MEM_A12
NET DDR_MEM_A11
NET DDR_MEM_A10
NET DDR_MEM_A09
NET DDR_MEM_A08
NET DDR_MEM_A07
}
NET_CLASS DDR_DM_MEM
{
NET DDR_MEM_DM3
NET DDR_MEM_DM2
NET DDR_MEM_DM1
NET DDR_MEM_DM0
}
```

```
NET_CLASS DDR_DATA_MEM
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NET DDR_MEM_DQ07
NET DDR_MEM_DQ06
NET DDR_MEM_DQ05
NET DDR_MEM_DQ04
NET DDR_MEM_DQ03
NET DDR_MEM_DQ02
NET DDR_MEM_DQ01
NET DDR_MEM_DQ00
NET DDR_MEM_DQ15
NET DDR_MEM_DQ14
NET DDR_MEM_DQ13
NET DDR_MEM_DQ12
NET DDR_MEM_DQ11
NET DDR_MEM_DQ10
NET DDR_MEM_DQ09
NET DDR_MEM_DQ08
NET DDR_MEM_DQ23
NET DDR_MEM_DQ22
NET DDR_MEM_DQ21
NET DDR_MEM_DQ20
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NET DDR_MEM_DQ18
NET DDR_MEM_DQ17
NET DDR_MEM_DQ16
NET DDR_MEM_DQ31
NET DDR_MEM_DQ30
NET DDR_MEM_DQ29
NET DDR_MEM_DQ28
NET DDR_MEM_DQ27
NET DDR_MEM_DQ26
NET DDR_MEM_DQ25
NET DDR_MEM_DQ24
}
NET_CLASS DDR_DQS_MEM
{
NET DDR_MEM_DQS3
NET DDR_MEM_DQS2
NET DDR_MEM_DQS1
NET DDR_MEM_DQS0
}
NET_CLASS DDR_CNTL_MEM
{
NET DDR_MEM_RAS_N
NET DDR_MEM_CAS_N
NET DDR_MEM_CKE
NET DDR_MEM_BA1
NET DDR_MEM_BA0
NET DDR_MEM_CS_N
NET DDR_MEM_WE_N
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NET_CLASS DDR_CLK_MEM
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NET DDR_MEM_CK1_N
NET DDR_MEM_CK1
NET DDR_MEM_CK0_N
NET DDR_MEM_CK0
NET DDR_MEM_CK3_N
NET DDR_MEM_CK3
NET DDR_MEM_CK2_N
NET DDR_MEM_CK2
NET DDR_MEM_CK5_N
NET DDR_MEM_CK5
NET DDR_MEM_CK4_N
NET DDR_MEM_CK4
NET DDR_PLL_FB_IN_N
NET DDR_PLL_FB_IN
}
NET_CLASS DDR_CLK_PLL
{
NET DDR_PLL_CK2_N
NET DDR_PLL_CK2
NET DDR_PLL_CK1_N
NET DDR_PLL_CK1
NET DDR_PLL_CK0_N
NET DDR_PLL_CK0
NET DDR_PLL_CK5_N
NET DDR_PLL_CK5
NET DDR_PLL_CK4_N
NET DDR_PLL_CK4
NET DDR_PLL_CK3_N
NET DDR_PLL_CK3
NET DDR_PLL_FB_OUT_N
NET DDR_PLL_FB_OUT
}
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NET_CLASS DDR_ADDR_REG
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NET DDR_REG_A06
NET DDR_REG_A05
NET DDR_REG_A04
NET DDR_REG_A03
NET DDR_REG_A02
NET DDR_REG_A01
NET DDR_REG_A00
NET DDR_REG_A12
NET DDR_REG_A11
NET DDR_REG_A10
NET DDR_REG_A09
NET DDR_REG_A08
NET DDR_REG_A07
}
NET_CLASS DDR_CNTL_REG
{
NET DDR_REG_CKE
NET DDR_REG_RAS_N
NET DDR_REG_CAS_N
NET DDR_REG_BA1
NET DDR_REG_BA0
NET DDR_REG_CS_N
NET DDR_REG_WE_N
}
NET_CLASS DDR_ADDR_RES
{
NET DDR_RES_A06
NET DDR_RES_A05
NET DDR_RES_A04
NET DDR_RES_A03
NET DDR_RES_A02
NET DDR_RES_A01
NET DDR_RES_A00
NET DDR_RES_A12
NET DDR_RES_A11
NET DDR_RES_A10
NET DDR_RES_A09
NET DDR_RES_A08
NET DDR_RES_A07
}
NET_CLASS DDR_CLK_RES
{
NET DDR_RES_CK_N
NET DDR_RES_CK
}
NET_CLASS DDR_DATA_RES
{
NET DDR_RES_DQ03
NET DDR_RES_DQ02
NET DDR_RES_DQ01
NET DDR_RES_DQ00
NET DDR_RES_DQ07
NET DDR_RES_DQ06
NET DDR_RES_DQ05
NET DDR_RES_DQ04
NET DDR_RES_DQ11
NET DDR_RES_DQ10
NET DDR_RES_DQ09
NET DDR_RES_DQ08
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NET DDR_RES_DQ14
NET DDR_RES_DQ13
NET DDR_RES_DQ12
NET DDR_RES_DQ19
NET DDR_RES_DQ18
NET DDR_RES_DQ17
NET DDR_RES_DQ16
NET DDR_RES_DQ23
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NET DDR_RES_DQ21
NET DDR_RES_DQ20
NET DDR_RES_DQ27
NET DDR_RES_DQ26
NET DDR_RES_DQ25
NET DDR_RES_DQ24
NET DDR_RES_DQ31
NET DDR_RES_DQ30
NET DDR_RES_DQ29
NET DDR_RES_DQ28
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NET_CLASS DDR_DQS_RES
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NET DDR_RES_DQS3
NET DDR_RES_DQS2
NET DDR_RES_DQS1
NET DDR_RES_DQS0
}
NET_CLASS DDR_CNTL_RES
{
NET DDR_RES_CKE
NET DDR_RES_RAS_N
NET DDR_RES_CAS_N
NET DDR_RES_BA1
NET DDR_RES_BA0
NET DDR_RES_CS_N
NET DDR_RES_WE_N
}
NET_CLASS PMC_FPGA_CONN4
{
NET FPGA_PMC_CONN4_IO14
NET FPGA_PMC_CONN4_IO12
NET FPGA_PMC_CONN4_IO10
NET FPGA_PMC_CONN4_IO21
NET FPGA_PMC_CONN4_IO19
NET FPGA_PMC_CONN4_IO17
NET FPGA_PMC_CONN4_IO15
NET FPGA_PMC_CONN4_IO22
NET FPGA_PMC_CONN4_IO20
NET FPGA_PMC_CONN4_IO18
NET FPGA_PMC_CONN4_IO16
NET FPGA_PMC_CONN4_IO29
NET FPGA_PMC_CONN4_IO27
NET FPGA_PMC_CONN4_IO25
NET FPGA_PMC_CONN4_IO23
NET FPGA_PMC_CONN4_IO30
NET FPGA_PMC_CONN4_IO28
NET FPGA_PMC_CONN4_IO26
NET FPGA_PMC_CONN4_IO24
NET FPGA_PMC_CONN4_IO37
NET FPGA_PMC_CONN4_IO35
NET FPGA_PMC_CONN4_IO33
NET FPGA_PMC_CONN4_IO31
NET FPGA_PMC_CONN4_IO38
NET FPGA_PMC_CONN4_IO36
NET FPGA_PMC_CONN4_IO34
NET FPGA_PMC_CONN4_IO32
NET FPGA_PMC_CONN4_IO45
NET FPGA_PMC_CONN4_IO43
NET FPGA_PMC_CONN4_IO41
NET FPGA_PMC_CONN4_IO39
NET FPGA_PMC_CONN4_IO46
NET FPGA_PMC_CONN4_IO44
NET FPGA_PMC_CONN4_IO42
NET FPGA_PMC_CONN4_IO40
NET FPGA_PMC_CONN4_IO53
NET FPGA_PMC_CONN4_IO51
NET FPGA_PMC_CONN4_IO49
NET FPGA_PMC_CONN4_IO47
NET FPGA_PMC_CONN4_IO54
NET FPGA_PMC_CONN4_IO52
NET FPGA_PMC_CONN4_IO50
NET FPGA_PMC_CONN4_IO48
NET FPGA_PMC_CONN4_IO61
NET FPGA_PMC_CONN4_IO59
NET FPGA_PMC_CONN4_IO57
NET FPGA_PMC_CONN4_IO55
NET FPGA_PMC_CONN4_IO62
NET FPGA_PMC_CONN4_IO60
NET FPGA_PMC_CONN4_IO58
NET FPGA_PMC_CONN4_IO56
NET FPGA_PMC_CONN4_IO13
NET FPGA_PMC_CONN4_IO11
NET FPGA_PMC_CONN4_IO9
}
NET_CLASS IIC_FPGA
{
NET IIC_FPGA_SCL
NET IIC_FPGA_SDA
}
NET_CLASS IIC_PMC
{
NET IIC_PMC_SCL
NET IIC_PMC_SDA
}
```

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
Net Classes
Page 1 of 2

Date: October 17th, 2002	Ver: 1.00
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ML300 CPU - Net Classes

Page 1 of 2

```
NET_CLASS PCI_FPGA_CONN
{
NET PCI_FPGA_AD06
NET PCI_FPGA_AD04
NET PCI_FPGA_AD03
NET PCI_FPGA_AD01
NET PCI_FPGA_AD07
NET PCI_FPGA_CBE0
NET PCI_FPGA_AD05
NET PCI_FPGA_M66EN
NET PCI_FPGA_AD11
NET PCI_FPGA_AD12
NET PCI_FPGA_AD08
NET PCI_FPGA_AD13
NET PCI_FPGA_AD14
NET PCI_FPGA_AD15
NET PCI_FPGA_AD10
NET PCI_FPGA_AD19
NET PCI_FPGA_CBE2
NET PCI_FPGA_AD16
NET PCI_FPGA_AD17
NET PCI_FPGA_AD20
NET PCI_FPGA_AD21
NET PCI_FPGA_AD22
NET PCI_FPGA_AD18
NET PCI_FPGA_AD31
NET PCI_FPGA_AD26
NET PCI_FPGA_AD27
NET PCI_FPGA_AD28
NET PCI_FPGA_PMC_GNT
NET PCI_FPGA_PMC_REQ
NET PCI_FPGA_AD29
NET PCI_FPGA_AD30
NET PCI_FPGA_PRS2
NET PCI_FPGA_BM3
NET PCI_FPGA_BUS_RST
NET PCI_FPGA_BM4
NET PCI_FPGA_AD24
NET PCI_FPGA_AD25
NET PCI_FPGA_AD23
NET PCI_FPGA_CBE3
NET PCI_FPGA_INTC
NET PCI_FPGA_INTB
NET PCI_FPGA_PRS1
NET PCI_FPGA_INTD
NET PCI_FPGA_SB0
NET PCI_FPGA_SDONE
NET PCI_FPGA_CBE1
NET PCI_FPGA_PAR
NET PCI_FPGA_CB_GNT
NET PCI_FPGA_CB_REQ
NET PCI_FPGA_GBL_RST
NET PCI_FPGA_PMC_TRST
NET PCI_FPGA_PMC_TCK
NET PCI_FPGA_PMC_TDO
NET PCI_FPGA_PMC_TDI
NET PCI_FPGA_INTA
NET PCI_FPGA_PMC_TMS
NET PCI_FPGA_AD02
NET PCI_FPGA_ACK64
NET PCI_FPGA_AD00
NET PCI_FPGA_REQ64
NET PCI_FPGA_DEVSEL
NET PCI_FPGA_PERR
NET PCI_FPGA_LOCK
NET PCI_FPGA_SERR
NET PCI_FPGA_FRAME
NET PCI_FPGA_TRDY
NET PCI_FPGA_IRDY
NET PCI_FPGA_STOP
}
NET_CLASS CLK_27MHZ_COMP
{
NET FPGA_PMC_CONN4_IO61
NET PCI_PORT_CLK_PMC
NET PCI_PORT_CLK_CB
}
NET_CLASS CLK_27MHZ_FPGA
{
NET PCI_PORT_CLK_PMC
NET PCI_PORT_CLK_CB
}

NET_CLASS PCI_PORT_CONN
{
NET PCI_PORT_AD06
NET PCI_PORT_AD04
NET PCI_PORT_AD03
NET PCI_PORT_AD01
NET PCI_PORT_AD07
NET PCI_PORT_CBE0
NET PCI_PORT_AD05
NET PCI_PORT_M66EN
NET PCI_PORT_AD11
NET PCI_PORT_AD12
NET PCI_PORT_AD08
NET PCI_PORT_AD13
NET PCI_PORT_AD14
NET PCI_PORT_AD15
NET PCI_PORT_AD10
NET PCI_PORT_AD19
NET PCI_PORT_CBE2
NET PCI_PORT_AD16
NET PCI_PORT_AD17
NET PCI_PORT_AD20
NET PCI_PORT_AD21
NET PCI_PORT_AD22
NET PCI_PORT_AD18
NET PCI_PORT_AD31
NET PCI_PORT_AD26
NET PCI_PORT_AD27
NET PCI_PORT_AD28
NET PCI_PORT_PMC_GNT
NET PCI_PORT_PMC_REQ
NET PCI_PORT_AD29
NET PCI_PORT_AD30
NET PCI_PORT_PRS2
NET PCI_PORT_BM3
NET PCI_PORT_BUS_RST
NET PCI_PORT_BM4
NET PCI_PORT_AD24
NET PCI_PORT_AD25
NET PCI_PORT_AD23
NET PCI_PORT_CBE3
NET PCI_PORT_INTC
NET PCI_PORT_INTB
NET PCI_PORT_PRS1
NET PCI_PORT_INTD
NET PCI_PORT_SBO
NET PCI_PORT_SDONE
NET PCI_PORT_CBE1
NET PCI_PORT_PAR
NET PCI_PORT_CB_GNT
NET PCI_PORT_CB_REQ
NET PCI_PORT_GBL_RST
NET PCI_PORT_PMC_TRST
NET PCI_PORT_PMC_TCK
NET PCI_PORT_PMC_TDO
NET PCI_PORT_PMC_TDI
NET PCI_PORT_INTA
NET PCI_PORT_PMC_TMS
NET PCI_PORT_AD02
NET PCI_PORT_ACK64
NET PCI_PORT_AD00
NET PCI_PORT_REQ64
NET PCI_PORT_DEVSEL
NET PCI_PORT_PERR
NET PCI_PORT_LOCK
NET PCI_PORT_SERR
NET PCI_PORT_FRAME
NET PCI_PORT_TRDY
NET PCI_PORT_IRDY
NET PCI_PORT_STOP
}
NET_CLASS ENET_PHY_COMP
{
NET PHY_TX_ER_TMP
NET PHY_TX_CLK_TMP
NET PHY_COL_TMP
NET PHY_CRS_TMP
NET PHY_RXD3_TMP
NET PHY_RXD2_TMP
NET PHY_RXD1_TMP
NET PHY_RXD0_TMP
NET PHY_RX_DV_TMP
NET PHY_RX_CLK_TMP
NET PHY_RX_ER_TMP
}

NET_CLASS ENET_PHY
{
NET PHY_RXD3
NET PHY_RXD2
NET PHY_RXD1
NET PHY_RXD0
NET PHY_RX_DV
NET PHY_RX_CLK
NET PHY_RX_ER
NET PHY_SLEEP
NET PHY_PAUSE
NET PHY_PWRDN
NET PHY_MDIO
NET PHY_MDC
NET PHY_COL
NET PHY_CRS
NET PHY_MDINT
NET PHY_RESET
NET PHY_SLW0
NET PHY_SLW1
NET PHY_TX_ER
NET PHY_TX_CLK
NET PHY_TX_EN
NET PHY_TXD0
NET PHY_TXD1
NET PHY_TXD2
NET PHY_TXD3
}
NET_CLASS PMC_PMC_CONN4
{
NET PMC_CONN4_IO21
NET PMC_CONN4_IO19
NET PMC_CONN4_IO17
NET PMC_CONN4_IO15
NET PMC_CONN4_IO22
NET PMC_CONN4_IO20
NET PMC_CONN4_IO18
NET PMC_CONN4_IO16
NET PMC_CONN4_IO29
NET PMC_CONN4_IO27
NET PMC_CONN4_IO25
NET PMC_CONN4_IO23
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NET PMC_CONN4_IO24
NET PMC_CONN4_IO37
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NET PMC_CONN4_IO31
NET PMC_CONN4_IO38
NET PMC_CONN4_IO36
NET PMC_CONN4_IO34
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NET PMC_CONN4_IO45
NET PMC_CONN4_IO43
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NET PMC_CONN4_IO39
NET PMC_CONN4_IO46
NET PMC_CONN4_IO44
NET PMC_CONN4_IO42
NET PMC_CONN4_IO40
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NET PMC_CONN4_IO51
NET PMC_CONN4_IO49
NET PMC_CONN4_IO47
NET PMC_CONN4_IO54
NET PMC_CONN4_IO52
NET PMC_CONN4_IO50
NET PMC_CONN4_IO48
NET PMC_CONN4_IO61
NET PMC_CONN4_IO59
NET PMC_CONN4_IO57
NET PMC_CONN4_IO55
NET PMC_CONN4_IO62
NET PMC_CONN4_IO60
NET PMC_CONN4_IO58
NET PMC_CONN4_IO56
NET PMC_CONN4_IO14
NET PMC_CONN4_IO12
NET PMC_CONN4_IO10
NET FPGA_PMC_CONN4_IO13
NET PMC_CONN4_IO11
NET PMC_CONN4_IO9
}

NET_CLASS PS2_1
{
NET PS2_1_DATA_OUT
NET PS2_1_DATA_IN
NET PS2_1_CLK_OUT
NET PS2_1_CLK_IN
}
NET_CLASS PS2_2
{
NET PS2_2_DATA_OUT
NET PS2_2_DATA_IN
NET PS2_2_CLK_OUT
NET PS2_2_CLK_IN
}
NET_CLASS SYSACE_FLASH
{
NET SYSACE_CFA05
NET SYSACE_CFA04
NET SYSACE_CFA03
NET SYSACE_CFA02
NET SYSACE_CFA01
NET SYSACE_CFA00
NET SYSACE_CFA10
NET SYSACE_CFA09
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NET SYSACE_CFA07
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NET SYSACE_CFD14
NET SYSACE_CFD13
NET SYSACE_CFD12
NET SYSACE_CFD11
NET SYSACE_CFD10
NET SYSACE_CFCD1
NET SYSACE_CFCD2
NET SYSACE_CFREG
NET SYSACE_CFWAIT
NET SYSACE_CFRDBSY
NET SYSACE_CFWE
NET SYSACE_CFDE
}
NET_CLASS SYSACE_MPU
{
NET SYSACE_MPA03
NET SYSACE_MPA02
NET SYSACE_MPA01
NET SYSACE_MPA00
NET SYSACE_MPA06
NET SYSACE_MPA05
NET SYSACE_MPA04
NET SYSACE_MPD04
NET SYSACE_MPD03
NET SYSACE_MPD02
NET SYSACE_MPD01
NET SYSACE_MPD00
NET SYSACE_MPD09
NET SYSACE_MPD08
NET SYSACE_MPD07
NET SYSACE_MPD06
NET SYSACE_MPD05
NET SYSACE_MPD15
NET SYSACE_MPD14
NET SYSACE_MPD13
NET SYSACE_MPD12
NET SYSACE_MPD11
NET SYSACE_MPD10
NET SYSACE_MPBRDY
NET SYSACE_MPIRQ
NET SYSACE_MPCE
NET SYSACE_MPWE
NET SYSACE_MPDE
}

NET_CLASS SYSACE_JTAG_2V5
{
NET SYSACE_TSTTDO
NET SYSACE_TSTTMS_2V5
NET SYSACE_TSTTCK_2V5
NET SYSACE_TSTTDI_2V5
}
NET_CLASS SYSACE_JTAG_3V3
{
NET SYSACE_TSTTMS_3V3
NET SYSACE_TSTTCK_3V3
NET SYSACE_TSTTDI_3V3
}
NET_CLASS TFT_CNTL_FPGA
{
NET TFT_FPGA_DPS
NET TFT_FPGA_DE
NET TFT_FPGA_VSYNC
NET TFT_FPGA_HSYNC
NET TFT_FPGA_CLK
}
NET_CLASS TFT_CLR_FPGA
{
NET TFT_FPGA_B5
NET TFT_FPGA_B4
NET TFT_FPGA_B3
NET TFT_FPGA_B2
NET TFT_FPGA_B1
NET TFT_FPGA_B0
NET TFT_FPGA_G5
NET TFT_FPGA_G4
NET TFT_FPGA_G3
NET TFT_FPGA_G2
NET TFT_FPGA_G1
NET TFT_FPGA_G0
NET TFT_FPGA_R5
NET TFT_FPGA_R4
NET TFT_FPGA_R3
NET TFT_FPGA_R2
NET TFT_FPGA_R1
NET TFT_FPGA_R0
}
NET_CLASS TFT_CNTL_LCD
{
NET TFT_LCD_DPS
NET TFT_LCD_DE
NET TFT_LCD_VSYNC
NET TFT_LCD_HSYNC
NET TFT_LCD_CLK
}
NET_CLASS TFT_CLR_LCD
{
NET TFT_LCD_B5
NET TFT_LCD_B4
NET TFT_LCD_B3
NET TFT_LCD_B2
NET TFT_LCD_B1
NET TFT_LCD_B0
NET TFT_LCD_G5
NET TFT_LCD_G4
NET TFT_LCD_G3
NET TFT_LCD_G2
NET TFT_LCD_G1
NET TFT_LCD_G0
NET TFT_LCD_R5
NET TFT_LCD_R4
NET TFT_LCD_R3
NET TFT_LCD_R2
NET TFT_LCD_R1
NET TFT_LCD_R0
}
NET_CLASS CPU_TRACE
{
NET TS6
NET TS5
NET TS4
NET TS3
NET TS2E
NET TS1E
NET TS2O
NET TS1O
NET TRC_CLK
}
```

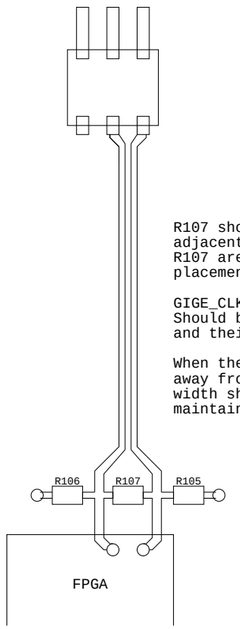
ML300 CPU - Net Classes
Page 2 of 2

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
Net Classes
Page 2 of 2

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 11 of 55	Drawn By BP

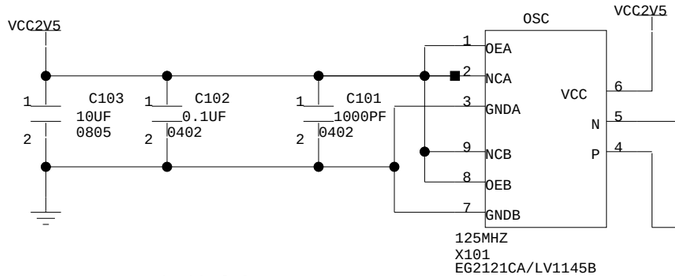


R107 should be Placed immediately adjacent to the FPGA. R105 and R107 are for DC Current, so placement is not critical.

GIGE_CLK_P and GIGE_CLK_N Should be routed differentially, and their tracelengths matched.

When the traces need to deviate away from eachother, the trace width should be modified, to maintain a controlled impedance.

C101, C102 and C103 should be Placed immediately adjacent to X101



NOTE: 62.5MHz osc is ideal for GIG-E
125MHz osc must divide by 2 internally

Total tracelength GIGE_CLK_P = GIGE_CLK_N
These Traces are should be routed as
100 Ohm differential signals.

Test Clock using LineSim

ML300 CPU - V2P7 Bank 0 PS/2, Ethernet

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

2VP7 Bank 0
Ethernet and PS/2

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 12 of 55	Drawn By BP

V2P7_BANK1
FF672
(DIE DOWN)

VCC3V3

OSC: 1 OE, 8 VCC, 4 GND, 5 OUT

This resistor should be placed close to the Oscillators

R172 25.5R 0402

X102
100MHZ

For DIP8 oscillators for System Clock and Sys ACE Clock, series R (R172 and R173, respectively) should be immediately adj. to the output pin, and parallel Rs (R179/R174 and R176/R175, respectively) should be immediately adjacent to the FPGA.

The clock signal should go to the FPGA, and then terminate at the parallel Rs as shown below (Ref des for the System Clock are shown, for System Ace, they are shown in parentheses)

VCC3V3

R1006 4.70K 0402

OSC: 1 OE, 8 VCC, 4 GND, 5 OUT

This resistor should be placed close to the Oscillators

R173 25.5R 0402

33.000MHZ
X104

SYSACE_CLK

Q103
BSS138

SYSACE_CLK_OE

SYSACE_CLK_OE_N

R180 4.70K 0402

Needed to prevent 3.3V on a 2.5V FPGA IO pin

VCC2V5

R179 100R 0402

R176 100R 0402

CLK_100MHZ_OSC

SYSACE_CLK

R174 100R 0402

R175 100R 0402

These resistor should be placed close to the FPGA

PCI_PORT_CLK_CB

PCI_PORT_CLK_PMC

R1007 0402 25.5R

PCI_PORT_CLK_CB_TMP

PCI_PORT_CLK_PMC_TMP

R108 0402 25.5R

PCI_FPGA_PMC_TMS

FPGA_PMC_CONN4_IO[0:63]

FPGA_PMC_CONN4_IO61	E13	MGT 7
FPGA_PMC_CONN4_IO51	H12	
FPGA_PMC_CONN4_IO62	C12	
FPGA_PMC_CONN4_IO60	D12	
FPGA_PMC_CONN4_IO59	E12	
FPGA_PMC_CONN4_IO57	F12	
FPGA_PMC_CONN4_IO58	D11	
FPGA_PMC_CONN4_IO55	E11	
FPGA_PMC_CONN4_IO53	G12	
FPGA_PMC_CONN4_IO49	G11	
FPGA_PMC_CONN4_IO56	D10	
FPGA_PMC_CONN4_IO45	E10	
FPGA_PMC_CONN4_IO47	F11	MGT 9
FPGA_PMC_CONN4_IO43	F10	
FPGA_PMC_CONN4_IO41	H11	
FPGA_PMC_CONN4_IO39	G10	
FPGA_PMC_CONN4_IO54	C9	
FPGA_PMC_CONN4_IO52	D9	
FPGA_PMC_CONN4_IO37	F9	
FPGA_PMC_CONN4_IO35	G9	
FPGA_PMC_CONN4_IO50	A8	
FPGA_PMC_CONN4_IO48	B8	
FPGA_PMC_CONN4_IO46	C8	
FPGA_PMC_CONN4_IO44	D8	
FPGA_PMC_CONN4_IO33	E9	
FPGA_PMC_CONN4_IO31	E8	
FPGA_PMC_CONN4_IO30	F8	
FPGA_PMC_CONN4_IO42	D7	
FPGA_PMC_CONN4_IO28	E7	
FPGA_PMC_CONN4_IO40	C6	
FPGA_PMC_CONN4_IO38	D6	
FPGA_PMC_CONN4_IO36	A3	
FPGA_PMC_CONN4_IO34	B3	

B13	B13_PAD040_IO_L75N_1/GCLK3P	
C13	C13_PAD041_IO_L75P_1/GCLK2S	
D13	D13_PAD042_IO_L74N_1/GCLK1P	
E13	E13_PAD043_IO_L74P_1/GCLK0S	
F13	F13_PAD044_IO_L73N_1	
G13	G13_PAD045_IO_L73P_1	
H13	H13_PAD046_IO_L69N_1/VREF_1	
H12	H12_PAD047_IO_L69P_1	
C12	C12_PAD048_IO_L68N_1	
D12	D12_PAD049_IO_L68P_1	
E12	E12_PAD050_IO_L67N_1	
F12	F12_PAD051_IO_L67P_1	
D11	D11_PAD052_IO_L45N_1/VREF_1	
E11	E11_PAD053_IO_L45P_1	
G12	G12_PAD054_IO_L44N_1	
G11	G11_PAD055_IO_L44P_1	
D10	D10_PAD056_IO_L43N_1	
E10	E10_PAD057_IO_L43P_1	
F11	F11_PAD058_IO_L39N_1	
F10	F10_PAD059_IO_L39P_1	
H11	H11_PAD060_IO_L38N_1	
G10	G10_PAD061_IO_L38P_1	
C9	C9_PAD062_IO_L37N_1	
D9	D9_PAD063_IO_L37P_1	
F9	F9_PAD064_IO_L09N_1/VREF_1	
G9	G9_PAD065_IO_L09P_1	
A8	A8_PAD066_IO_L08N_1	
B8	B8_PAD067_IO_L08P_1	
C8	C8_PAD068_IO_L07N_1	
D8	D8_PAD069_IO_L07P_1	
E9	E9_PAD070_IO_L06N_1	
E8	E8_PAD071_IO_L06P_1	
F8	F8_PAD072_IO_L05_1/No_Pair	
D7	D7_PAD073_IO_L03N_1/VREF_1	
E7	E7_PAD074_IO_L03P_1	
C6	C6_PAD075_IO_L02N_1	
D6	D6_PAD076_IO_L02P_1	
A3	A3_PAD077_IO_L01N_1/VRP_1	
B3	B3_PAD078_IO_L01P_1/VRN_1	
C7	C7_VCCO_1	
H9	H9_VCCO_1	
C10	C10_VCCO_1	
H10	H10_VCCO_1	
J11	J11_VCCO_1	
J12	J12_VCCO_1	
J13	J13_VCCO_1	

U1
DEVICE=XC2VP7-6FF672C
PKG_TYPE=FF672
PARTS=1
LEVEL=STD

VCC5

LT1763CS8: 8 IN, 5 SHDN, 1 OUT, 4 NC, 2 ADJ, 6 GND_6, 3 GND_3, 7 GND_7

U4

VCC3_PCI

NC

R182 38.3R 0805

R181 26.1R 0805

C197 33UF B

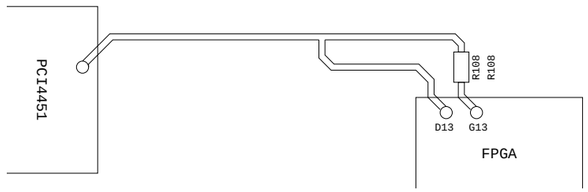
C801 0.1UF 0402

VCC3_PCI is a power line so should be thick or a plane

The Clock line to the Cardbus PCI4451 (R108) and the PMC Connectors (R1007) should have their Series Rs immediately adjacent to the FPGA.

The Feebackpath for Cardbus (to D13) should go half way to the PCI4451, before coming back to the FPGA. The length to the PCI4451 should equal the feedback loop.

The Cardbus layout is shown below.



XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

2VP7 Bank 1
PMC General Purpose IO

Date: October 17th, 2002	Ver: 1.00
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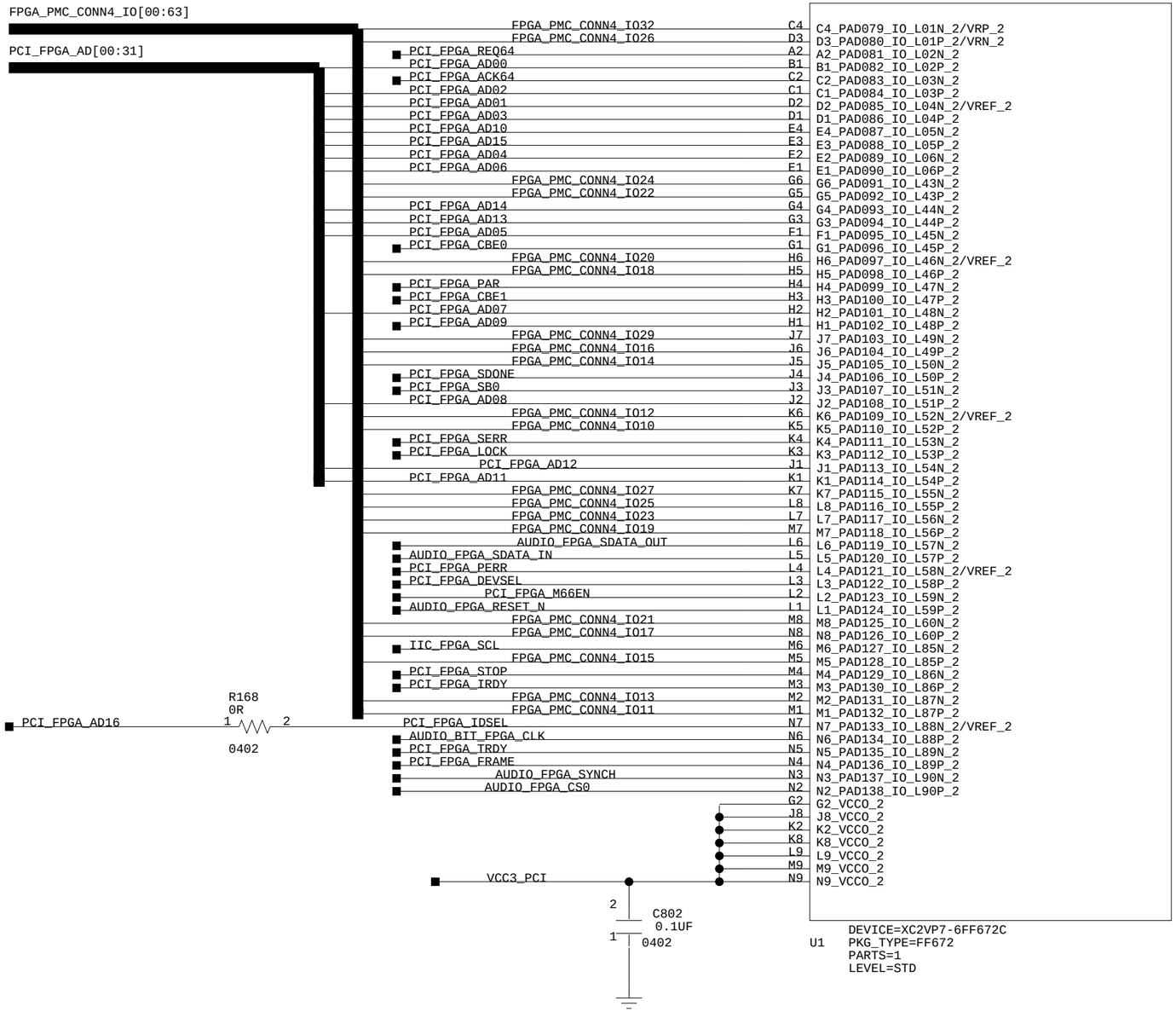
ML300 CPU - V2P7 Bank 1
PMC General Purpose IO

V2P7_BANK2
FF672
(DIE DOWN)



XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

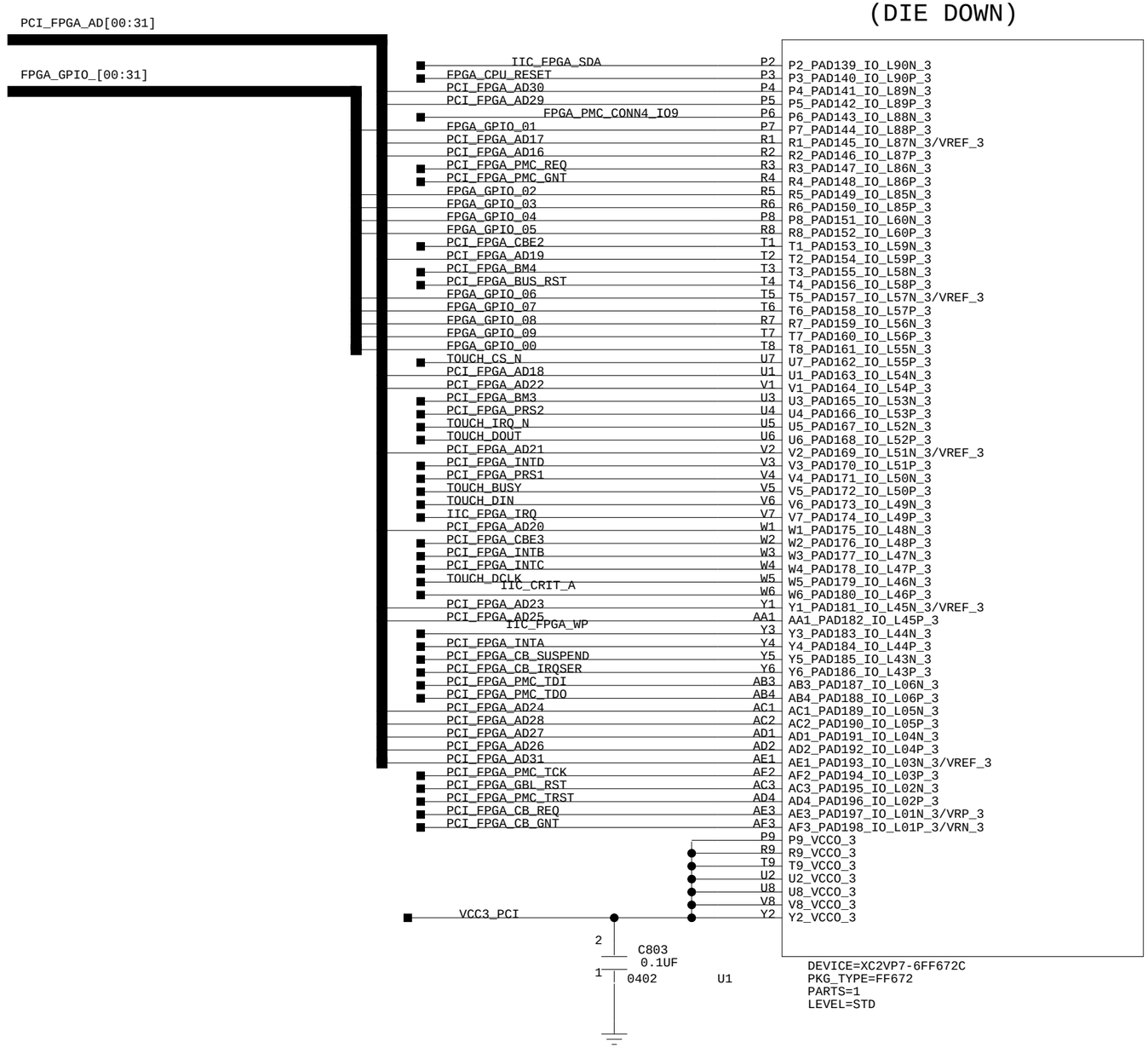
2VP7 Bank 2
PMC GPIO and PCI

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 14 of 55	Drawn By BP

ML300 CPU - V2P7 Bank 2
PMC GPIO and PCI

Touchscreen

The Touchscreen is on the ML300_PWR_IO board,
and the connection is shown on page 55.



ML300 CPU - V2P7 Bank 3
IIC, Audio, PMC GPIO, PCI and TouchScrn

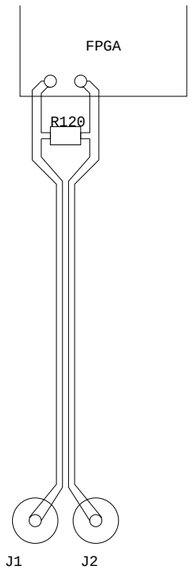
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

2VP7 Bank 3
IIC, Audio, PCI and Touch

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 15 of 55	Drawn By BP



R120 shouldbe placed immediately
adjacent to the FPGA

USER_MGT_CLK_P and USER_MGT_CLK_N
Should be routed differentially,
and their tracelengths matched.

When the traces need to deviate
away from eachother, the trace
width should be modified, to
maintain a controlled impedance.

V2P7_BANK4
FF672
(DIE DOWN)

VCC2V5

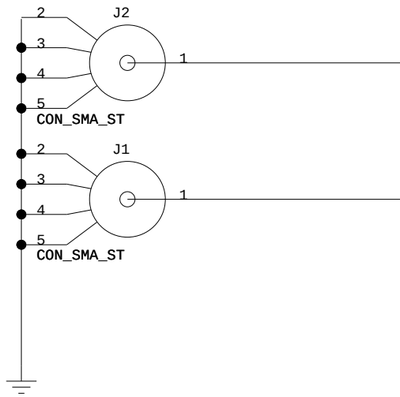
	W9	W9_VCCO_4
	AD7	AD7_VCCO_4
	V11	V11_VCCO_4
	V12	V12_VCCO_4
	V13	V13_VCCO_4
	W10	W10_VCCO_4
	AD10	AD10_VCCO_4
To TFT Conn Through 3.3V Level Shifter page 44	TFT_FPGA_CLK	AC6
	TFT_FPGA_HSYNC	AD6
	TFT_FPGA_VSYNC	AB7
	TFT_FPGA_R0	AC7
	TFT_FPGA_R1	AA7
	TFT_FPGA_R2	AA8
	TFT_FPGA_R3	Y8
	TFT_FPGA_R4	AB8
	TFT_FPGA_R5	AB9
	TFT_FPGA_G0	AC8
	TFT_FPGA_G1	AD8
	TFT_FPGA_G2	AE8
	TFT_FPGA_G3	AF8
	TFT_FPGA_DPS	Y9
	TFT_FPGA_G4	AA9
	TFT_FPGA_G5	AC9
	TFT_FPGA_B0	AD9
	TFT_FPGA_B1	Y10
	TFT_FPGA_B2	W11
	TFT_FPGA_B3	AA10
	TFT_FPGA_B4	AA11
		MGT 16
	TFT_FPGA_B5	AB10
	TFT_FPGA_DE	AC10
Serial Ports MAX3388E page 36	RTS2_FPGA	Y11
	CTS2_FPGA	Y12
	TXD2_FPGA	AB11
	RXD2_FPGA	AC11
	RTS1_FPGA	AA12
	CTS1_FPGA	AB12
	TXD1_FPGA	AC12
	RXD1_FPGA	AD12
2.5V SPI 25LC160 page 41	SPI_CLK	W12
	SPI_DATA_IN	W13
		MGT 18
	SPI_DATA_OUT	Y13
	FPGA_GPIO_11	AA13
	FPGA_GPIO_12	AB13
	FPGA_GPIO_13	AC13
	USER_MGT_CLK_N	AD13
	USER_MGT_CLK_P	AE13

	W9_PAD199_IO_L01N_4/DOUT	
	AD6_PAD200_IO_L01P_4/INIT_B	
	AB7_PAD201_IO_L02N_4/D0	
	AC7_PAD202_IO_L02P_4/D1	
	AA7_PAD203_IO_L03N_4/D2	
	AA8_PAD204_IO_L03P_4/D3	
	Y8_PAD205_IO_L05_4/No_Pair	
	AB8_PAD206_IO_L06N_4/VRP_4	
	AB9_PAD207_IO_L06P_4/VRN_4	
	AC8_PAD208_IO_L07N_4	
	AD8_PAD209_IO_L07P_4/VREF_4	
	AE8_PAD210_IO_L08N_4	
	AF8_PAD211_IO_L08P_4	
	Y9_PAD212_IO_L09N_4	
	AA9_PAD213_IO_L09P_4/VREF_4	
	AC9_PAD214_IO_L37N_4	
	AD9_PAD215_IO_L37P_4	
	Y10_PAD216_IO_L38N_4	
	W11_PAD217_IO_L38P_4	
	AA10_PAD218_IO_L39N_4	
	AA11_PAD219_IO_L39P_4	
	AB10_PAD220_IO_L43N_4	
	AC10_PAD221_IO_L43P_4	
	Y11_PAD222_IO_L44N_4	
	Y12_PAD223_IO_L44P_4	
	AB11_PAD224_IO_L45N_4	
	AC11_PAD225_IO_L45P_4/VREF_4	
	AA12_PAD226_IO_L67N_4	
	AB12_PAD227_IO_L67P_4	
	AC12_PAD228_IO_L68N_4	
	AD12_PAD229_IO_L68P_4	
	W12_PAD230_IO_L69N_4	
	W13_PAD231_IO_L69P_4/VREF_4	
	Y13_PAD232_IO_L73N_4	
	AA13_PAD233_IO_L73P_4	
	AB13_PAD234_IO_L74N_4/GCLK3S	
	AC13_PAD235_IO_L74P_4/GCLK2P	
	AD13_PAD236_IO_L75N_4/GCLK1S	
	AE13_PAD237_IO_L75P_4/GCLK0P	

U1

DEVICE=XC2VP7-6FF672C
PKG_TYPE=FF672
PARTS=1
LEVEL=STD

FPGA_GPIO_[00:31]



Matched Trace Lengths

R120
100R
1%
0402
2

This resistor should be
placed close to the FPGA
See figure above.

Total tracelength GIGE_CLK_LVPCL_P + GIGE_CLK_P = GIGE_CLK_LVPCL_N + GIGE_CLK_N

These Traces are should be routed as 100 Ohm differential signals, 8mil track, 10mil spacing

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

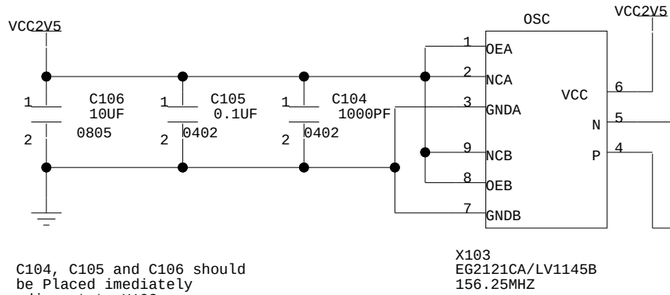
Title: ML300_CPU

2VP7 Bank 4
TFT LCD, Serial and SPI

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 16 of 55	Drawn By BP

ML300 CPU - V2P7 Bank 4
TFT LCD, Serial, SPI

V2P7_BANK5
FF672
(DIE DOWN)



C104, C105 and C106 should be Placed imediately adjacent to X103

Matched Trace Lengths

This resistor should be placed close to the FPGA

INFINBAND_CLK_N

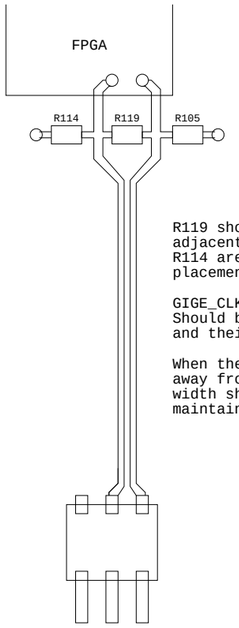
INFINBAND_CLK_P

R119 100R 0402

R114 130R 0402

R113 130R 0402

These resistor provide for LVPECL to LVDS Conversion, so use for the ED2121 CA OSC. DNP when using the LV1145B, as is an LVDS differential oscillator, and doesn't need.



R119 should be Placed immediately adjacent to the FPGA. R113 and R114 are for DC Current, so placement is not critical.

GIGE_CLK_P and GIGE_CLK_N Should be routed differentially, and their tracelengths matched.

When the traces need to deviate away from eachother, the trace width should be modified, to maintain a controlled impedance.

VTTDDR

R309 49.9R 0402

DDR_RES_CK

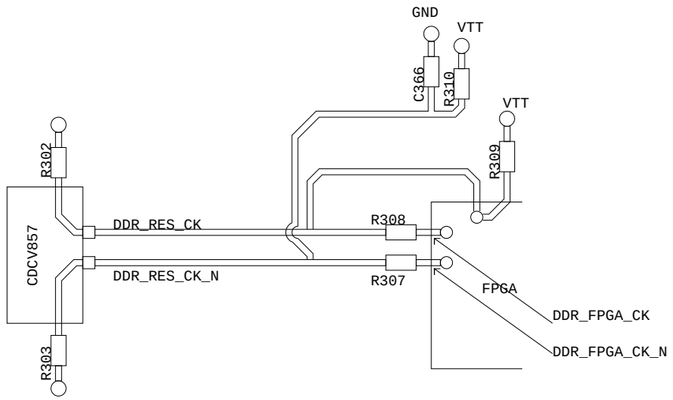
DDR_RES_CK_N

See Diagram Below

VTTDDR

R310 49.9R 0402

C366 10PF 0402



The Clock traces to the DDR PLL (CDCV857) must be matched tracelength. The Length of the feedback loop (i.e. length from FPGA back to FPGA) for the DDR_XXX_CK net should match the net to DDR Clk Replicator

The Negative DDR Clock signal should be routed s.t. the tracelength matches that of the positive DDR Clock net, and the length to the load cap (C366) and term R (R310) match the length of the feedback loop.

See Page 28 for the DDR Clock Replicator

FPGA_GPIO_14	AB14	AB14_PAD241_IO_L74P_5/GCLK4P	
FPGA_GPIO_15	AA14	AA14_PAD242_IO_L73N_5	
SYSACE_MPDE	Y14	Y14_PAD243_IO_L73P_5	
		MGT 19	
SYSACE_MPWE	W14	W14_PAD244_IO_L69N_5/VREF_5	
SYSACE_MPA00	W15	W15_PAD245_IO_L69P_5	
SYSACE_MPA01	AD15	AD15_PAD246_IO_L68N_5	
SYSACE_MPA02	AC15	AC15_PAD247_IO_L68P_5	
SYSACE_MPA03	AB15	AB15_PAD248_IO_L67N_5	
SYSACE_MPD00	AA15	AA15_PAD249_IO_L67P_5	
SYSACE_MPD01	AC16	AC16_PAD250_IO_L45N_5/VREF_5	
SYSACE_MPD02	AB16	AB16_PAD251_IO_L45P_5	
SYSACE_MPD03	Y15	Y15_PAD252_IO_L44N_5	
SYSACE_MPD04	Y16	Y16_PAD253_IO_L44P_5	
SYSACE_MPD05	AC17	AC17_PAD254_IO_L43N_5	
SYSACE_MPD06	AB17	AB17_PAD255_IO_L43P_5	
		MGT 21	
SYSACE_MPD07	AA16	AA16_PAD256_IO_L39N_5	
SYSACE_MPD08	AA17	AA17_PAD257_IO_L39P_5	
SYSACE_MPD09	W16	W16_PAD258_IO_L38N_5	
SYSACE_MPD10	Y17	Y17_PAD259_IO_L38P_5	
SYSACE_MPD11	AD18	AD18_PAD260_IO_L37N_5	
SYSACE_MPD12	AC18	AC18_PAD261_IO_L37P_5	
SYSACE_MPD13	AA18	AA18_PAD262_IO_L09N_5/VREF_5	
SYSACE_MPD14	Y18	Y18_PAD263_IO_L09P_5	
SYSACE_MPD15	AF19	AF19_PAD264_IO_L08N_5	
SYSACE_MPA04	AE19	AE19_PAD265_IO_L08P_5	
SYSACE_MPA05	AD19	AD19_PAD266_IO_L07N_5/VREF_5	
SYSACE_MPA06	AC19	AC19_PAD267_IO_L07P_5	
SYSACE_MPCE	AB18	AB18_PAD268_IO_L06N_5/VRP_5	
SYSACE_MPIRQ	AB19	AB19_PAD269_IO_L06P_5/VRN_5	
SYSACE_MPBRDY	Y19	Y19_PAD270_IO_L05_5/No_Pair	
CPU_TDO_TMP	AA19	AA19_PAD271_IO_L03N_5/D4	
CPU_TDI	AA20	AA20_PAD272_IO_L03P_5/D5	
CPU_TCK	AC20	AC20_PAD273_IO_L02N_5/D6	
CPU_TMS	AB20	AB20_PAD274_IO_L02P_5/D7	
CPU_HALT_N	AD21	AD21_PAD275_IO_L01N_5/RDWR_B	
CPU_TRST	AC21	AC21_PAD276_IO_L01P_5/CS_B	
	V14	V14_VCCO_5	
	V15	V15_VCCO_5	
	V16	V16_VCCO_5	
VCC2V5	W17	W17_VCCO_5	
	W18	W18_VCCO_5	
	AD17	AD17_VCCO_5	
	AD20	AD20_VCCO_5	

U1

DEVICE=XC2VP7-6FF672C
PKG_TYPE=FF672
PARTS=1
LEVEL=STD

ML300 CPU - V2P7 Bank 5
System ACE, CPU Debug

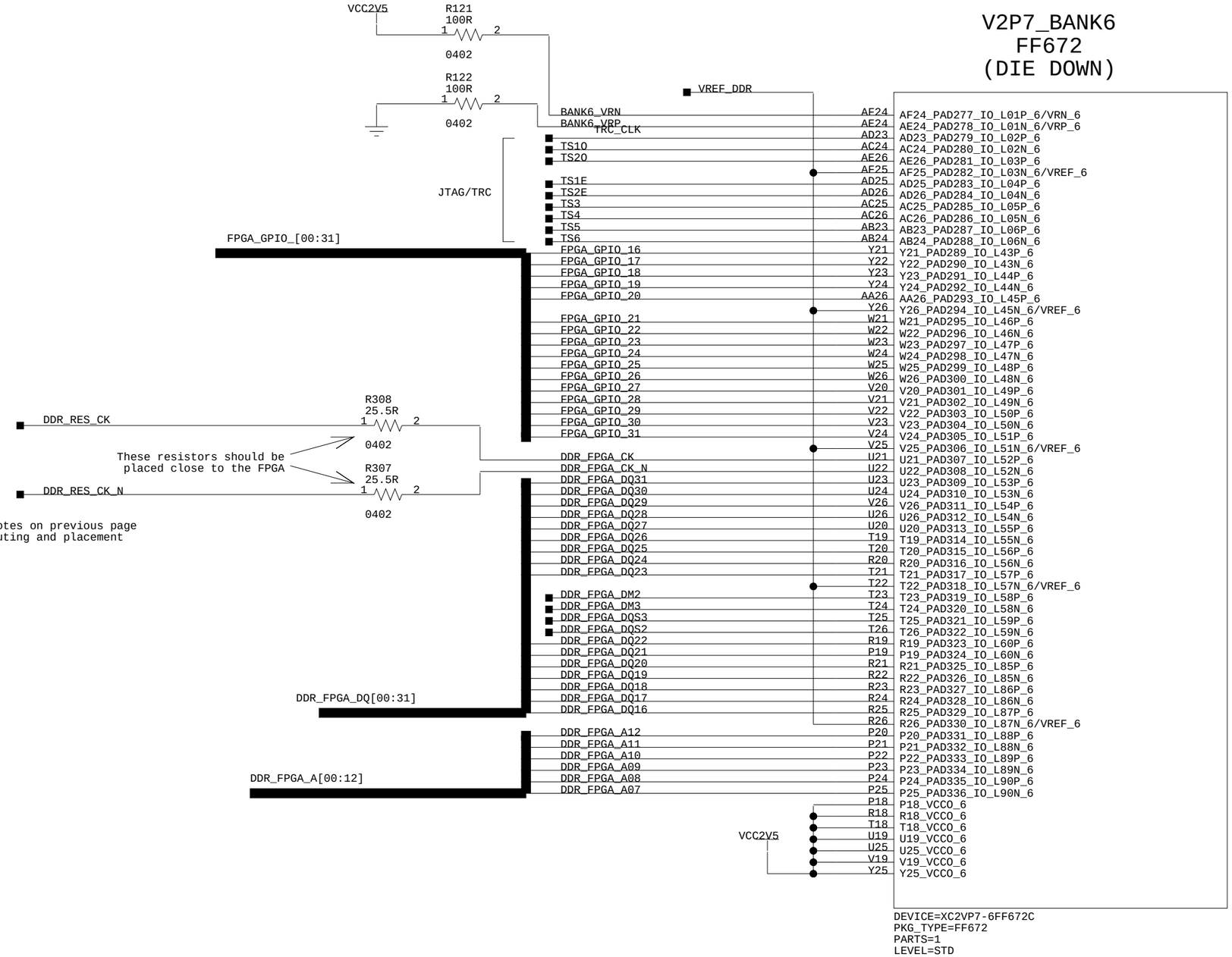
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

2VP7 Bank 5
System ACE and CPU Debug

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 17 of 56	Drawn By BP



V2P7_BANK6
FF672
(DIE DOWN)

ML300 CPU - V2P7 Bank 6
CPU Trace, DDR

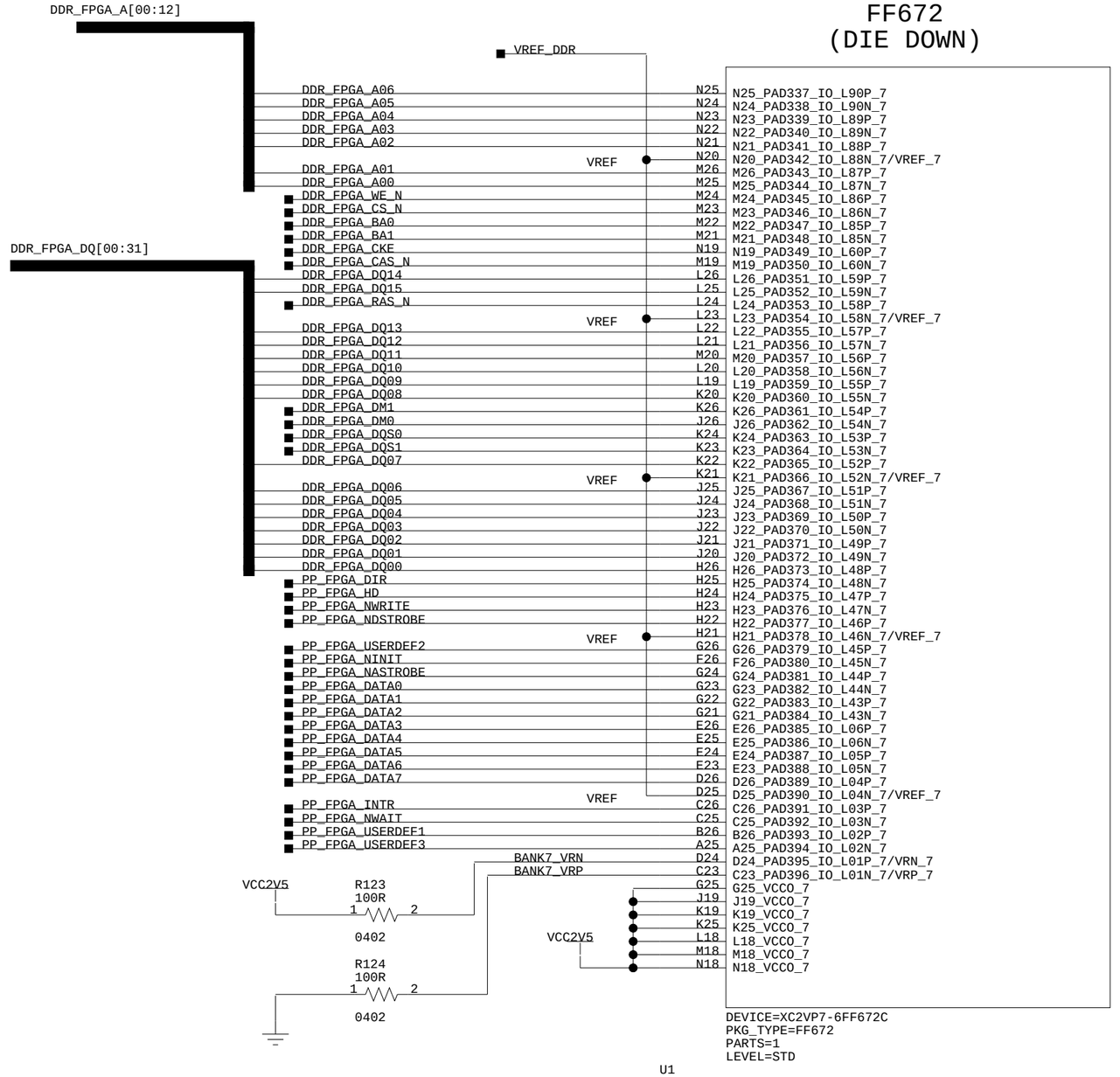
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

2VP7 Bank 6
CPU Trace and DDR

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 18 of 55	Drawn By BP



XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

2VP7 Bank 7
DDR and Parallel Port

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 19 of 55	Drawn By BP

ML300 CPU - V2P7 Bank 7
DDR and Parallel Port

These signals (FPGA_DXP, FPGA_DXN) should be routed as differential signals to the MAX11617AMEE (U251), and isolated from other signals as much as possible

DEVICE=XC2VP7-6FF672C
PKG_TYPE=FF672
PARTS=1
LEVEL=STD

VCC1V5

W19 W19_VCCINT
V18 V18_VCCINT
V17 V17_VCCINT
V10 V10_VCCINT
U18 U18_VCCINT
U16 U16_VCCINT
U11 U11_VCCINT
T17 T17_VCCINT
T10 T10_VCCINT
L17 L17_VCCINT
L10 L10_VCCINT
K18 K18_VCCINT
K16 K16_VCCINT
K11 K11_VCCINT
J18 J18_VCCINT
J17 J17_VCCINT
J10 J10_VCCINT
H19 H19_VCCINT
W8 W8_VCCINT
V9 V9_VCCINT
U9 U9_VCCINT
K9 K9_VCCINT
J9 J9_VCCINT
H8 H8_VCCINT

VCC2V5

AF14 AF14_VCCAUX
AF13 AF13_VCCAUX
AE25 AE25_VCCAUX
P26 P26_VCCAUX
N26 N26_VCCAUX
B25 B25_VCCAUX
AE2 AE2_VCCAUX
A14 A14_VCCAUX
A13 A13_VCCAUX
P1 P1_VCCAUX
N1 N1_VCCAUX
B2 B2_VCCAUX

VCC2V5

R125 4.70K 0402

R129 4.70K 0402

R133 4.70K 0402

R130 DNP 0402

R169 100R 0402

TP102

TP104

TP101

FPGA_DXP F20 F20_DXP
FPGA_DXN G19 G19_DXN
FPGA_PWRDWN_B AC5 AC5_PWRDWN_B
FPGA_HSWAP E21 E21_HSWAP_EN
FPGA_D5_RSVD D5 D5_RSVD
E6 E6_VBATT
FPGA_VBATT
FPGA_MODE_2 AB21 AB21_M2
FPGA_MODE_1 W20 W20_M1
FPGA_MODE_0 AC22 AC22_M0
FPGA_PROG_B D22 D22_PROG_B
FPGA_DONE AB6 AB6_DONE
FPGA_CCLK W7 W7_CCLK
FPGA_TMS F7 F7_TMS
FPGA_TCK G8 G8_TCK
FPGA_TDI H20 H20_TDI
FPGA_TDO H7 H7_TDO

V2P7_MISC
FF672
(DIE DOWN)

U1

C3 C3_GND
D4 D4_GND
E5 E5_GND
F6 F6_GND
G7 G7_GND
Y7 Y7_GND
AA6 AA6_GND
AB5 AB5_GND
AC4 AC4_GND
AD3 AD3_GND
C24 C24_GND
D23 D23_GND
E22 E22_GND
F21 F21_GND
G20 G20_GND
K10 K10_GND
K12 K12_GND
K13 K13_GND
K14 K14_GND
K15 K15_GND
K17 K17_GND
L11 L11_GND
L12 L12_GND
L13 L13_GND
L14 L14_GND
L15 L15_GND
L16 L16_GND
M10 M10_GND
M11 M11_GND
M12 M12_GND
M13 M13_GND
M14 M14_GND
M15 M15_GND
M16 M16_GND
M17 M17_GND
N10 N10_GND
N11 N11_GND
N12 N12_GND
N13 N13_GND
N14 N14_GND
N15 N15_GND
N16 N16_GND
N17 N17_GND
P10 P10_GND
P11 P11_GND
P12 P12_GND
P13 P13_GND
P14 P14_GND
P15 P15_GND
P16 P16_GND
P17 P17_GND
R10 R10_GND
R11 R11_GND
R12 R12_GND
R13 R13_GND
R14 R14_GND
R15 R15_GND
R16 R16_GND
R17 R17_GND
T11 T11_GND
T12 T12_GND
T13 T13_GND
T14 T14_GND
T15 T15_GND
T16 T16_GND
U10 U10_GND
U12 U12_GND
U13 U13_GND
U14 U14_GND
U15 U15_GND
U17 U17_GND
Y20 Y20_GND
AA21 AA21_GND
AB22 AB22_GND
AC23 AC23_GND
AD24 AD24_GND

Done LED

VCC5

R127 64.9R 0402

BLUE DS101

DONE_LED

See Page 35 for placement of DS101

VCC2V5

R171 330R 0402

Q101 BSS138

FPGA_DONE

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

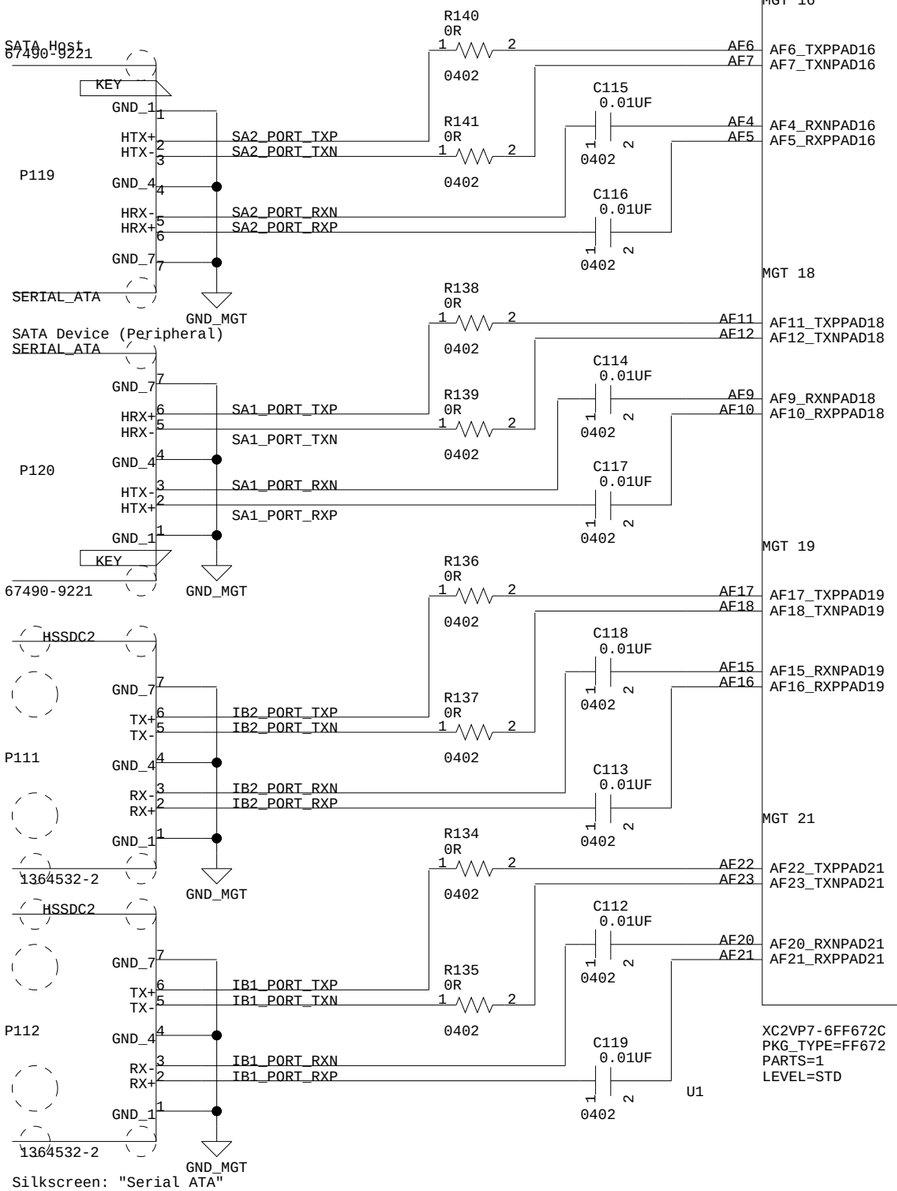
Title: ML300_CPU
2VP7 Misc / Config

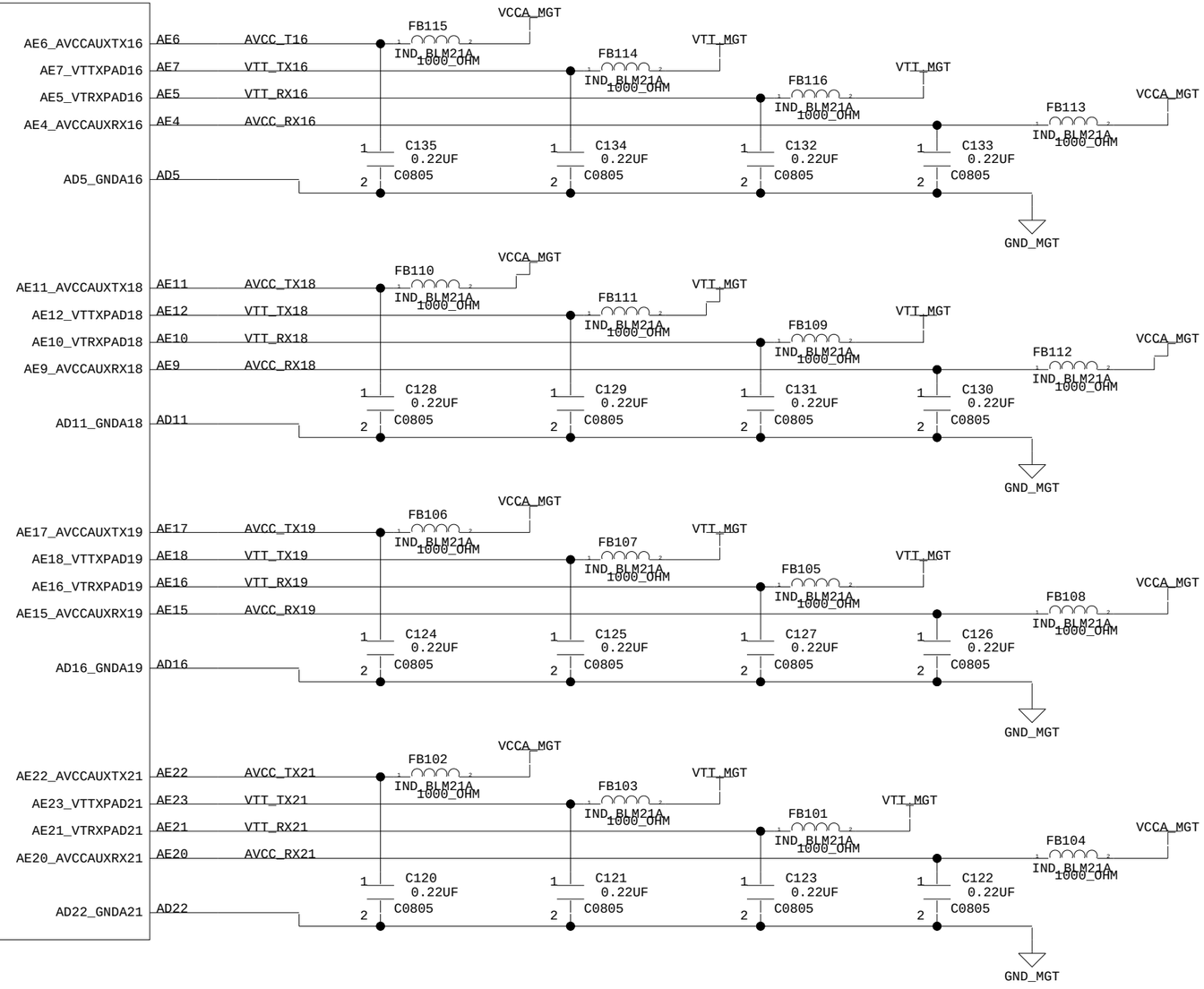
Date: October 17th, 2002
Ver: 1.00
Sheet Size: B
Rev: A
Sheet 20 of 55
Drawn By BP

ML300 CPU - V2P7 Auxiliary Miscellaneous/Config

Silkscreen: "HSSCD2"

V2P7_MGT_BOTTOM
FF672
(DIE DOWN)





Silkscreen: "Serial ATA"

NOTES

1. Each of the pairs must be matched trace length, such that

   GIGEX_XX_P + GIGEX_XX_CONN_P = GIGEX_XX_N + GIGEX_XX_CONN_N

1. Each of the pairs must be 100 ohm controlled differential impedance
   - track width XX mils
   - track spacing XX mils

3. Put res on transmit lines (TX) near the connector,
   Caps on receive lines (RX) near the FPGA,

4. Serial ATA Connectors shown flipped to more easily
   map to the V2Pro MGT pinout

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

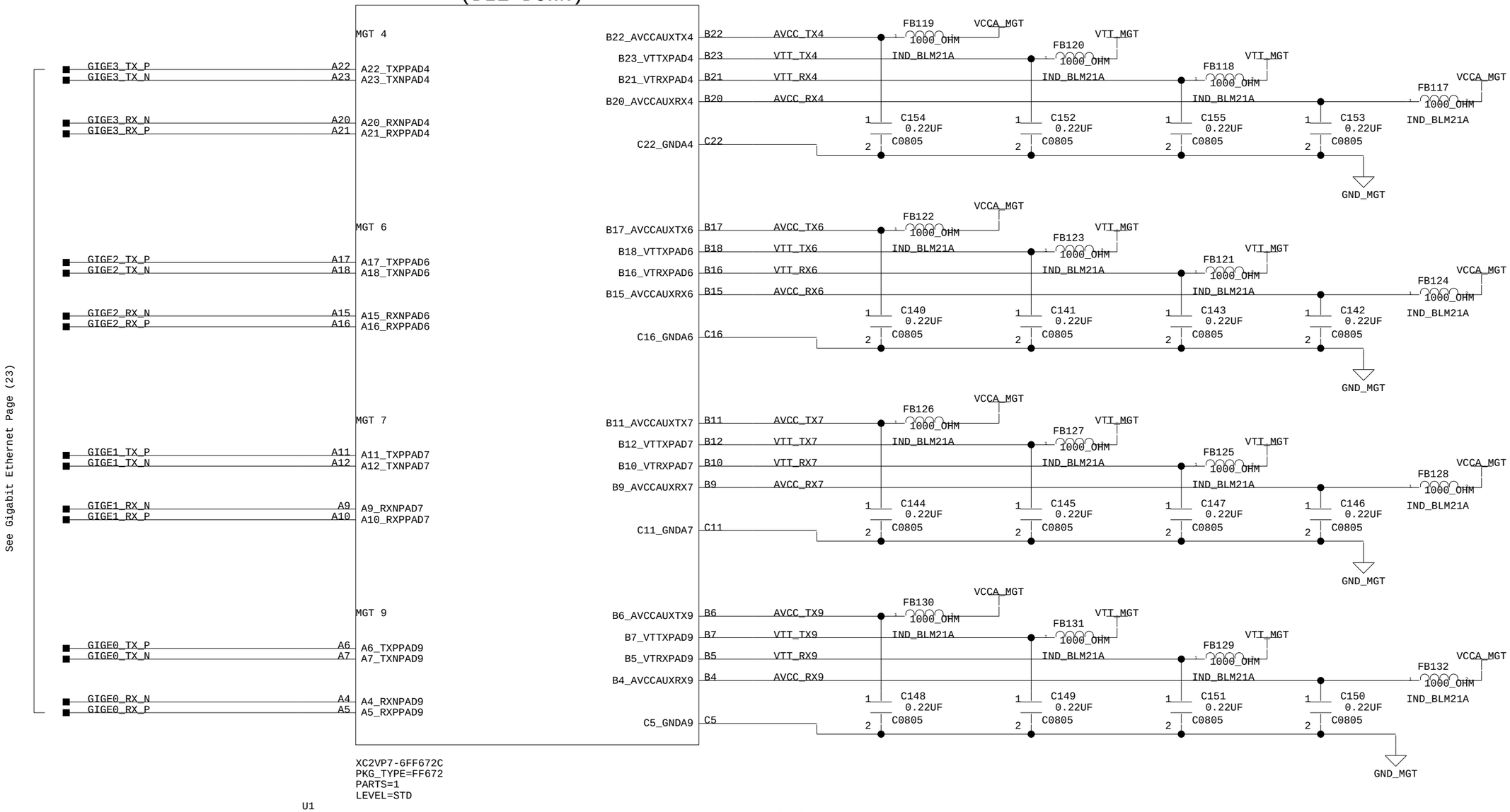
2VP7 MGT Bottom
HSSCD2 and Serial ATA

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 21 of 55	Drawn By BP

ML300 CPU

V2P7 MGT Bottom

V2P7_MGT_TOP
FF672
(DIE DOWN)



All 0.22UF caps on this page are 0805.

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

2VP7 MGT Top
Gigabit Ethernet Fiber

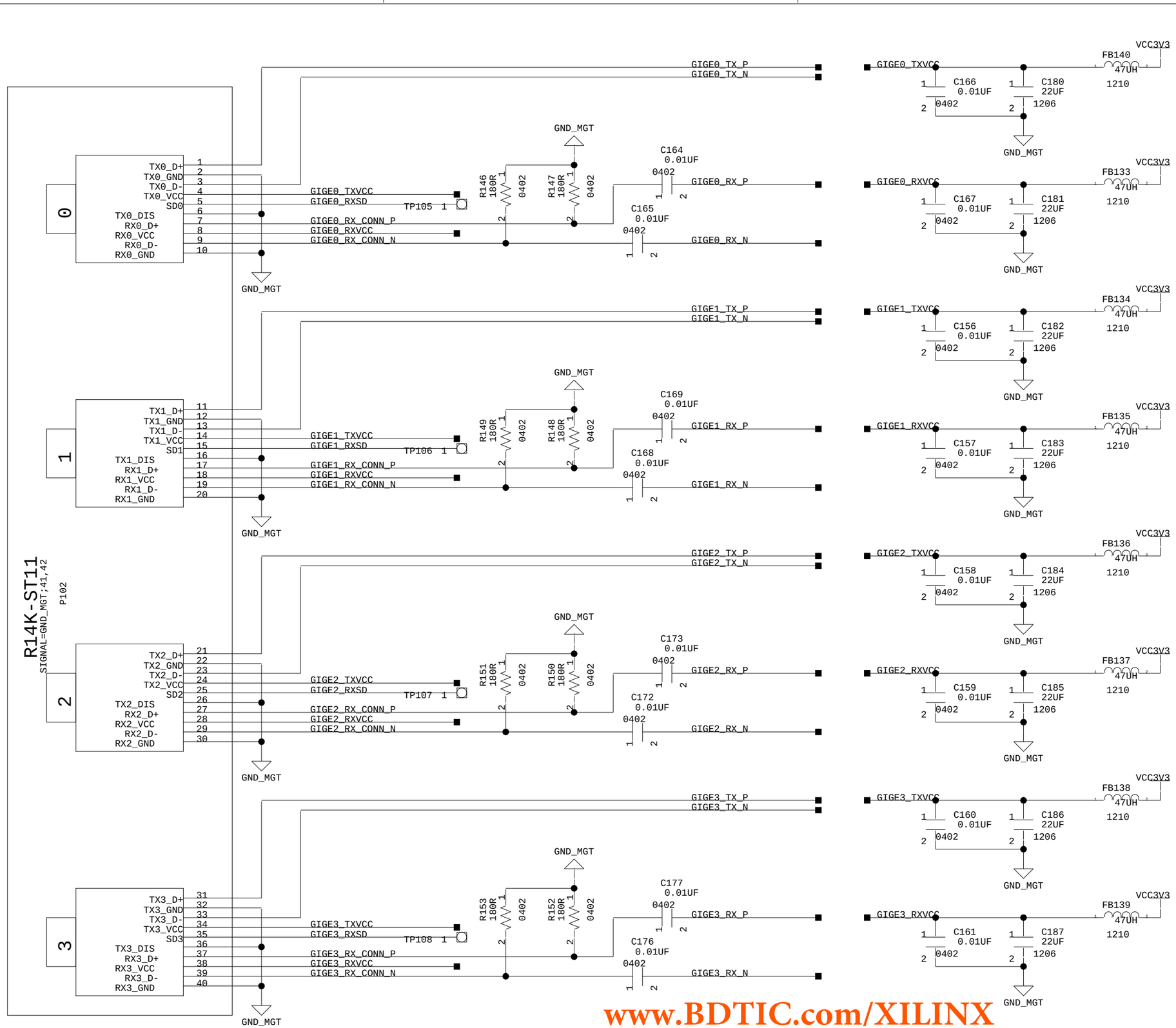
Date: October 17th, 2002 | Ver: 1.00

Sheet Size: B | Rev: A

Sheet 22 of 55 | Drawn By BP

ML300 CPU

V2P7 MGT Top



NOTES

1. Each of the pairs must be matched trace length, such that GIGEX_XX_P + GIGEX_XX_CONN_P = GIGEX_XX_N + GIGEX_XX_CONN_N

2. Each of the pairs must be 100 ohm controlled differential impedance
   - track width XX mils
   - track spacing XX mils

3. Put Caps on receive lines (RX) adjacent to the FPGA.

4. TxVCC and RxVCC supply filters designed to filter out 50KHz-100KHz supply to R14K-ST11, a frequency of of sensitivity for the R14K-ST11

ML300 CPU
V2P7 MGT Top
Fiber XCVR

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

Gigabit Ethernet Fiber Transceiver
MGT Top

Date: October 17th, 2002	Ver: 1.00
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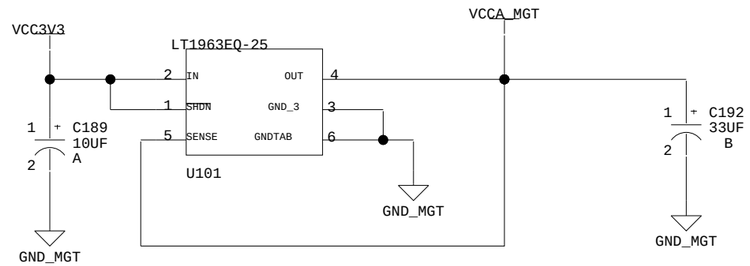
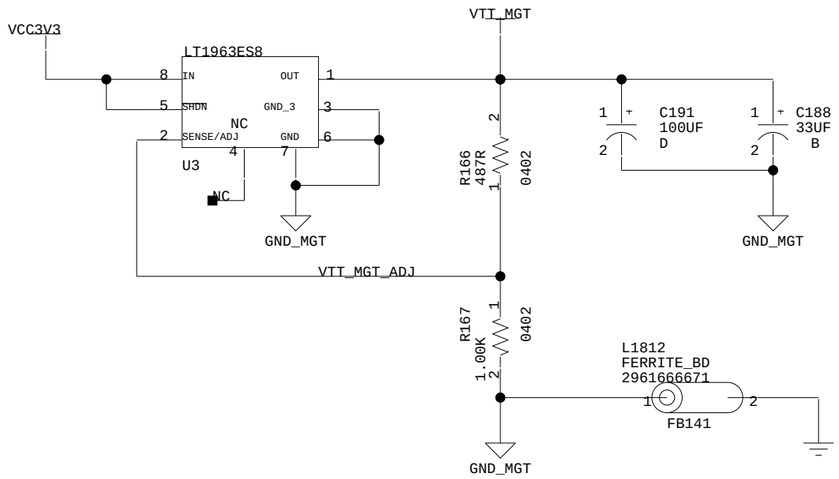
MGT VCCA Linear Regulator



MGT VTT Linear Regulator



ML300 CPU
MGT Power

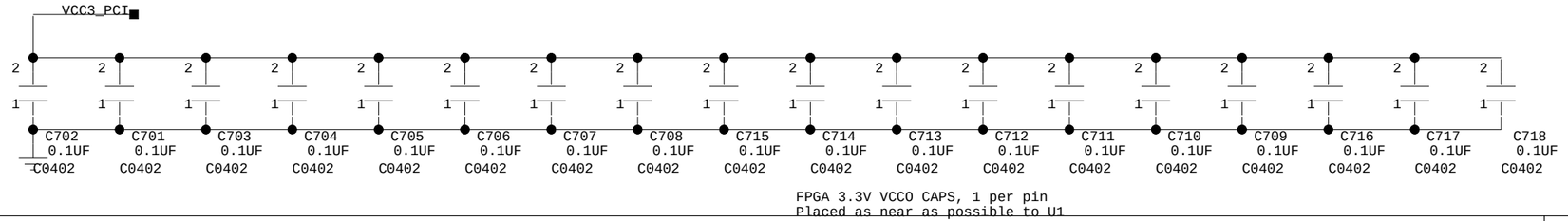
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

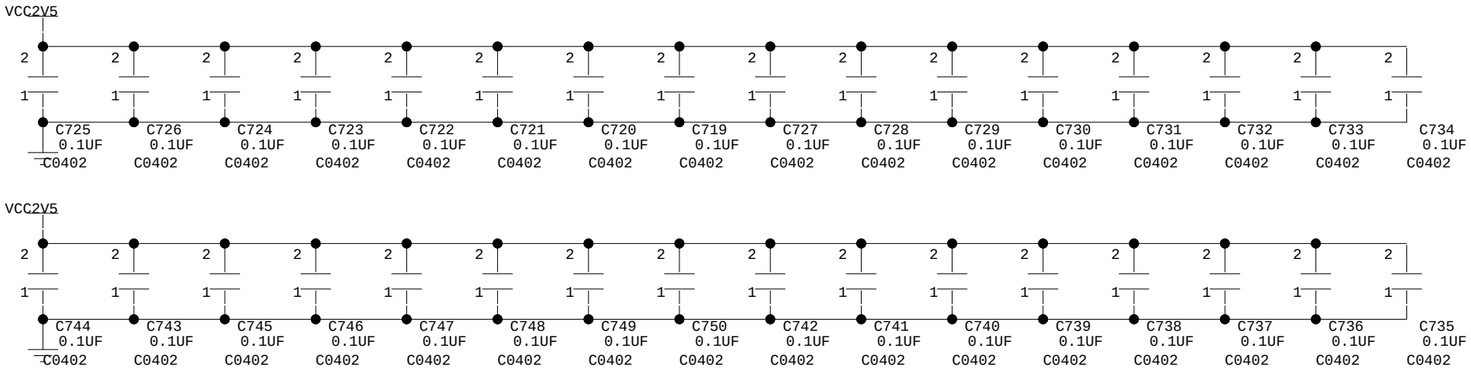
Title: ML300_CPU

MGT Power Supplies

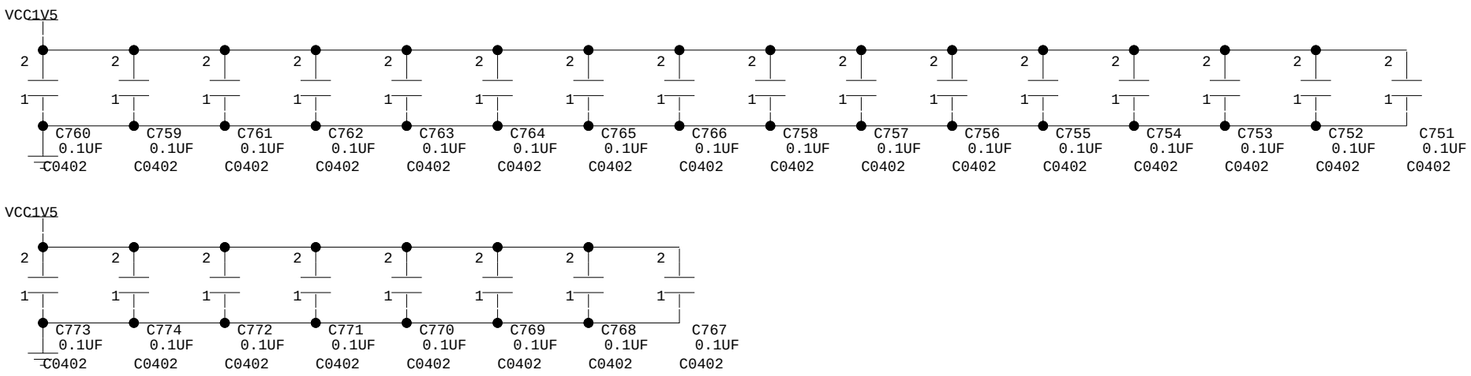
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 24 of 55	Drawn By BP



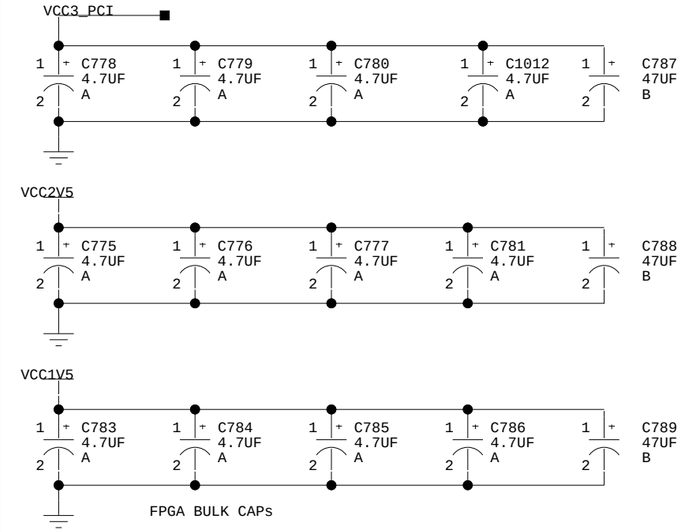
FPGA 3.3V VCCO CAPS, 1 per pin
Placed as near as possible to U1



FPGA VCCO, VCCAUX CAPS, 1 per pin
Placed as near as possible to U1



FPGA VCORE CAPS, 1 per pin
Placed as near as possible to U1



FPGA BULK CAPs
Placed as near as possible to U1

ML300 CPU V2P7
Bypass Capacitors

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

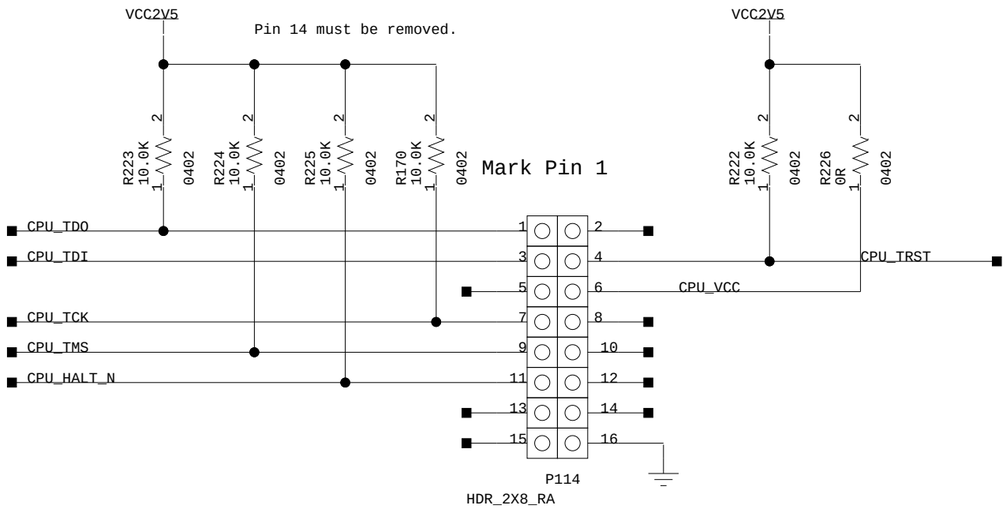
Title: ML300_CPU
V2P7 Bypass Capacitors

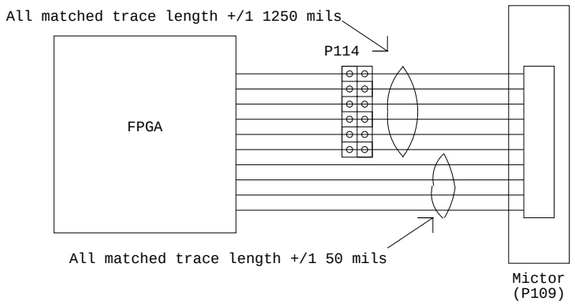
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 25 of 55	Drawn By GB

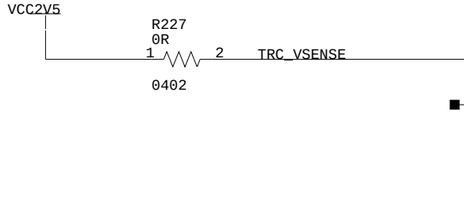
There are two sets of signals between the FPGA
and the Mictor 38:

1. Bussed to include the 2X8 header above.
   These are the CPU Debug and should be +/- 1250 mils
   The Header should be located between the Mictor
   and FPGA, so the FPGA and Mictor are the endpoints

2. Only connected to the Mictor and FPGA.
   These are the CPU Trace and should be +/- 50 mils

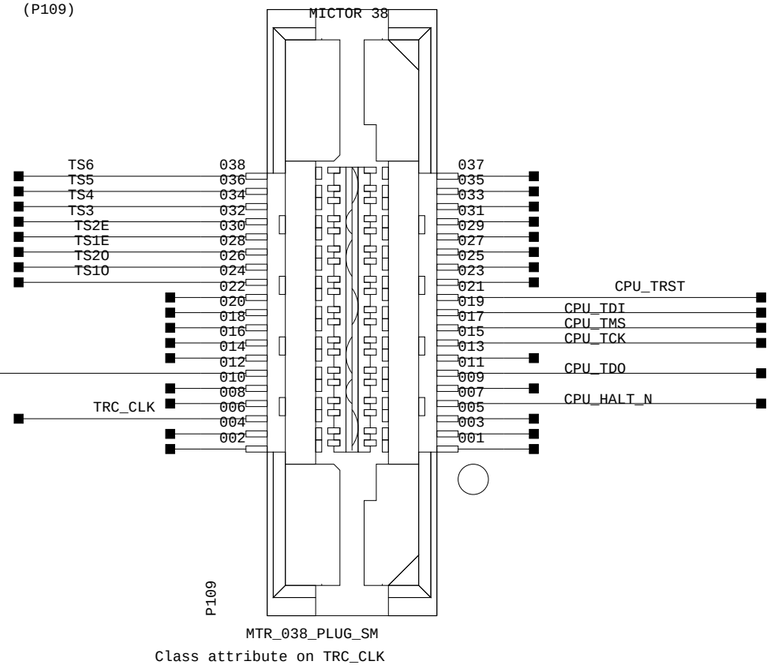






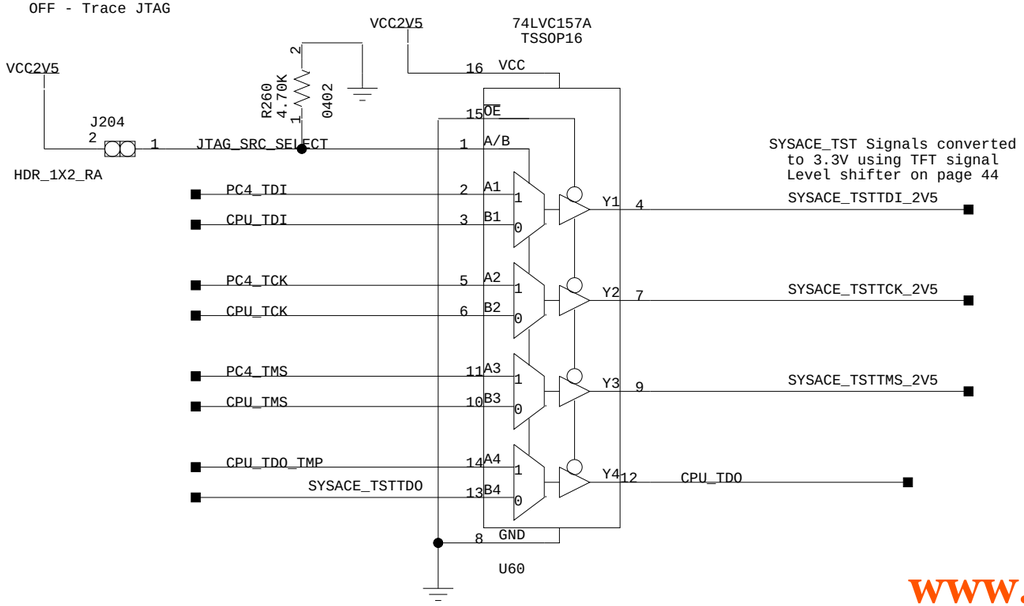
Mark Pin 1

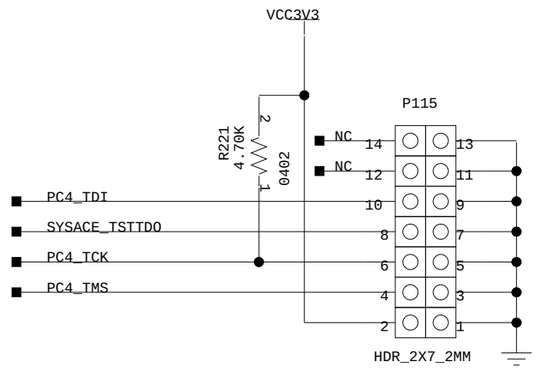
Silkscreen:



Class attribute on TRC_CLK

J204:
ON - PC4 JTAG
OFF - Trace JTAG





ML300 CPU
V2P7 Bank 5/6 (17/18)
Trace + Debug

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
CPU Debug and Trace

Date: October 17th, 2002
Ver: 1.00
Sheet Size: B
Rev: A
Sheet 26 of 55
Drawn By BP

VCC2V5

C215 0.1UF 0402 · C217 0.1UF 0402 · C218 0.1UF 0402 · C221 0.1UF 0402 · C220 0.1UF 0402 · C219 0.1UF 0402 · C222 0.1UF 0402

C230 10UF A

VCC3V3

C229 0.1UF 0402 · C228 0.1UF 0402 · C227 0.1UF 0402 · C226 0.1UF 0402 · C223 0.1UF 0402 · C224 0.1UF 0402 · C225 0.1UF 0402 · C216 0.1UF 0402

C231 10UF A

VCC2V5 · VCC3V3

VCCL_10 · VCCL_15 · VCCL_25 · VCCL_57 · VCCL_84 · VCCL_94 · VCCL_99 · VCCL_126

VCCH_1 · VCCH_17 · VCCH_37 · VCCH_55 · VCCH_92 · VCCH_73 · VCCH_109 · VCCH_128

SYSACE_RESET_N

R217 4.70K 0402 — VCC2V5

TP221

to Power Board

RESET_N · POR_BYPASS · POR_TEST · POR_RESET

VCC3V3

R212 4.70K 0402

ACEFLASH

CFCD2	13	SYSACE_CFCD2	25 25_CD2
CFD10	12	SYSACE_CFD10	49 49_D10
CFD09	11	SYSACE_CFD09	48 48_D09
CFD02	8	SYSACE_CFD02	23 23_D02
CFD08	7	SYSACE_CFD08	47 47_D08
CFD01	6	SYSACE_CFD01	22 22_D01
CFD00	5	SYSACE_CFD00	21 21_D00
CFA00	4	SYSACE_CFA00	20 20_A00
CFREG	3	SYSACE_CFREG	44 44_REG
CFA01	142	SYSACE_CFA01	19 19_A01
CFA02	141	SYSACE_CFA02	18 18_A02
CFWAIT	140	SYSACE_CFWAIT	42 42_WAIT
CFA03	139	SYSACE_CFA03	17 17_A03
CFA04	137	SYSACE_CFA04	16 16_A04
CFA05	135	SYSACE_CFA05	15 15_A05
CFA06	134	SYSACE_CFA06	14 14_A06
CFGRSVD	133	SYSACE_CFRDBSY	37 37_RDY/BSY
CFA07	132	SYSACE_CFA07	12 12_A07
CFWE	131	SYSACE_CFWE	36 36_WE
CFA08	130	SYSACE_CFA08	11 11_A08
CFA09	125	SYSACE_CFA09	10 10_A09
CFOE	123	SYSACE_CFDE	9 9_OEI
CFA10	121	SYSACE_CFA10	8 8_A10
CFCE2	138	SYSACE_CFCE2	32 32_CE2
CFCE1	119	SYSACE_CFCE1	7 7_CE1I
CFD15	118	SYSACE_CFD15	31 31_D15
CFD07	117	SYSACE_CFD07	6 6_D07
CFD14	116	SYSACE_CFD14	30 30_D14
CFD06	115	SYSACE_CFD06	5 5_D06
CFD13	114	SYSACE_CFD13	29 29_D13
CFD05	113	SYSACE_CFD05	4 4_D05
CFD12	106	SYSACE_CFD12	28 28_D12
CFD04	105	SYSACE_CFD04	3 3_D04
CFD11	104	SYSACE_CFD11	27 27_D11
CFD03	103	SYSACE_CFD03	2 2_D03
CFCD1	103	SYSACE_CFCD1	26 26_CD1

SYSTEMACE
TQFP144
(DIE DOWN)

DEVICE=XCCACE-TQ144I
TQFP144
PARTS=1
LEVEL=STD

U2

SYSACE_MPBRDY 39 MPBRDY
SYSACE_MPIRQ 41 MPIRQ
SYSACE_MPCE 42 MPCE
SYSACE_MPA06 43 MPA06
SYSACE_MPA05 44 MPA05
SYSACE_MPA04 45 MPA04
SYSACE_MPD15 47 MPD15
SYSACE_MPD14 48 MPD14
SYSACE_MPD13 49 MPD13
SYSACE_MPD12 50 MPD12
SYSACE_MPD11 51 MPD11
SYSACE_MPD10 52 MPD10
SYSACE_MPD09 53 MPD09
SYSACE_MPD08 56 MPD08
SYSACE_MPD07 58 MPD07
SYSACE_MPD06 59 MPD06
SYSACE_MPD05 60 MPD05
SYSACE_MPD04 61 MPD04
SYSACE_MPD03 62 MPD03
SYSACE_MPD02 63 MPD02
SYSACE_MPD01 65 MPD01
SYSACE_MPD00 66 MPD00
SYSACE_MPA03 67 MPA03
SYSACE_MPA02 68 MPA02
SYSACE_MPA01 69 MPA01
SYSACE_MPA00 70 MPA00
SYSACE_MPWE 76 MPWE
SYSACE_MPOE 77 MPOE

CFGINIT 78 · CFGPROG 79 · CFGTCK 80 · CFGTDI 81 · CFGTDO 82 · CFGTMS 85 · CFGADDR0 86 · CFGADDR1 87 · CFGADDR2 88 · CFGMODEPIN 89 · CLK 93 · STATLED 95 · ERRLED 96 · TSTTDO 97 · TSTTMS 98 · TSTTCK 101 · TSTTDI 102

GND_35 · GND_26 · GND_18 · GND_9 · GND_144 · GND_136 · GND_129 · GND_120 · GND_111 · GND_46 · GND_54 · GND_64 · GND_83 · GND_75 · GND_91 · GND_100 · GND_112 · GND_110

VCC3V3

38_VCC 38 · 13_VCC 13

R213 1.00K 0402 — R216 1.00K 0402

35_IOWR 35 · 34_IORD 34

46_BVD1 46 · 45_BVD2 45 · 40_VS2 40 · 33_VS1 33 · 24_WP 24 · 43_INPACK 43

TP215 · TP216 · TP217 · TP218 · TP219 · TP220

39_CSEL 39 · 41_RESET 41

R215 1.00K 0402 — R214 1.00K 0402

50_GND 50 · 1_GND 1

SHIELD S1 S2

P113

TP214

FPGA_INIT_LED

R268 56.2R 0402

DS203 RED LED0603

VCC2V5

R208 4.70K 0402

(Init Signal)
TFT_FPGA_HSYNC

to FPGA
From Power Board

FPGA_PROG_B
FPGA_TCK
FPGA_TDO
FPGA_TDI
FPGA_TMS

SYSACE_CFGADDR0
SYSACE_CFGADDR1
SYSACE_CFGADDR2

R210 4.70K 0402 · R211 4.70K 0402 · R209 4.70K 0402

VCC2V5

R218 4.70K 0402

SYSACE_CFGMODEPIN

NOTE: See Page 35 for
mounting locations of
DS201, DS202 and DS203

VCC2V5

R265 100R 0402 — SYSACE_CLK

R266 100R 0402

Place these
resistors
as close to
System ACE
as possible

VCC2V5

Silkscreen "System ACE" "Status LED" — DS202 GREEN — R219 25.5R 0402 — SYSACE_STATLED

Silkscreen "System ACE" "Error LED" — DS201 RED — R220 51.1R 0402 — SYSACE_ERRLED

SYSACE_TSTTDI_3V3
SYSACE_TSTTCK_3V3
SYSACE_TSTTMS_3V3
SYSACE_TSTTDO

To Level
Shifter and
MUX, then
to JTAG and
Trace Conns

ML300 CPU
V2P7 Bank 5 (17)
System ACE

XILINX

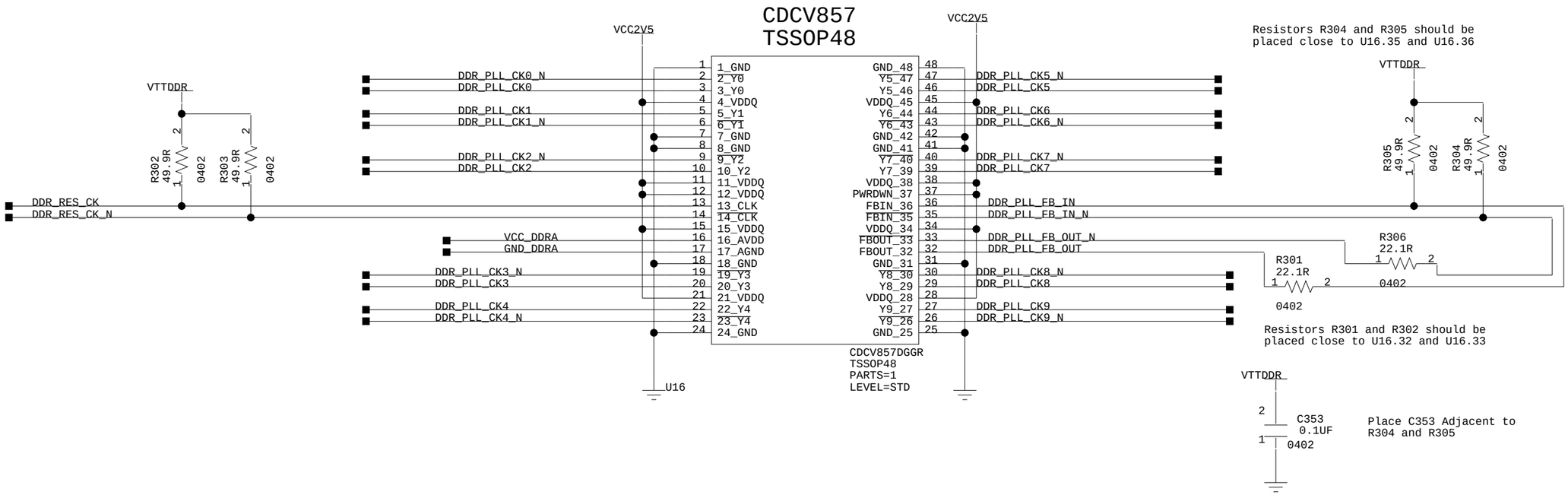
PCB: 1280285
ASM: 0431182
SCH: 0381135

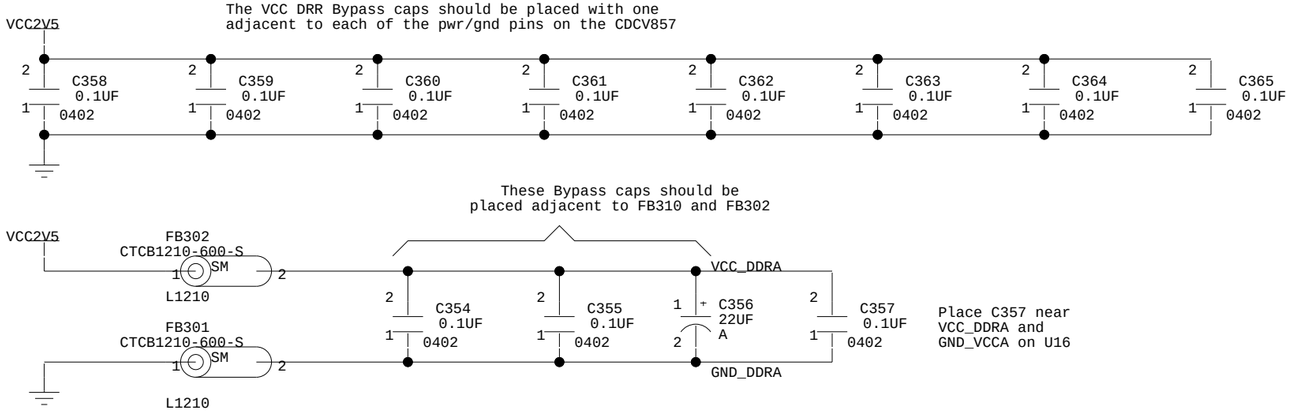
Title: ML300_CPU
System ACE

Date: October 17th, 2002 — Ver: 1.00
Sheet Size: B — Rev: A
Sheet 27 of 55 — Drawn By BP

All of the CLK pairs should be match tracelength
DDR_CLK_PLL Class on DDR_PLL_CK0, 3 and 6

See diagram on Page 17 for routing of clock
signals to FPGA





ML300 CPU
DDR Clock Replicator

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
DDR SDRAM - Clock PLL

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 28 of 55	Drawn By BP

DDR_ADDR_REG Class on DDR_REG_A00 and A07
DDR_ADDR_FPGA Class on DDR_RES_A00 and A07

RP359 22R CTS742
RP360 22R CTS742
RP361 22R CTS742
RP362 22R CTS742
RP363 22R CTS742

DDR_FPGA_A00
DDR_FPGA_A01
DDR_FPGA_A02
DDR_FPGA_A03
DDR_FPGA_A04
DDR_FPGA_A05
DDR_FPGA_A06
DDR_FPGA_A07
DDR_FPGA_A08
DDR_FPGA_A09
DDR_FPGA_A10
DDR_FPGA_A11
DDR_FPGA_A12
DDR_FPGA_WE_N
DDR_FPGA_CS_N
DDR_FPGA_BA0
DDR_FPGA_BA1
DDR_FPGA_CAS_N
DDR_FPGA_RAS_N
DDR_FPGA_CKE

VTTDDR

RP330 47R EXB-E10C
RP331 47R EXB-E10C
RP329 47R EXB-E10C

DDR_RES_A00
DDR_RES_A01
DDR_RES_A02
DDR_RES_A03
DDR_RES_A04
DDR_RES_A05
DDR_RES_A06
DDR_RES_A07
DDR_RES_A08
DDR_RES_A09
DDR_RES_A10
DDR_RES_A11
DDR_RES_A12
DDR_RES_WE_N
DDR_RES_CS_N
DDR_RES_BA0
DDR_RES_BA1
DDR_RES_CAS_N
DDR_RES_RAS_N
DDR_RES_CKE

SSTV16857
TVS0P48

D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14
CLK_N
CLK
RST_N
VREF
VDD_45 VDD_37 VDD_28
GND_46 GND_36 GND_27
VDDQ_4 VDDQ_9 VDDQ_12 VDDQ_16 VDDQ_21
GND GND_8 GND_13 GND_17 GND_22
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14

SN74SSTV16857DGVR
TVSOP48
PARTS=1
LEVEL=STD

U14

DDR_REG_A00
DDR_REG_A01
DDR_REG_A02
DDR_REG_A03
DDR_REG_A04
DDR_REG_A05
DDR_REG_A06
DDR_REG_A07
DDR_REG_A08
DDR_REG_A09
DDR_REG_A10
DDR_REG_A11
DDR_REG_A12
NC

DDR_MEM_CK4_N
DDR_MEM_CK4
VREF_DDR
VCC2V5

DDR_CNTL_REG Class on DDR_REG_WE_N
DDR_CNTL_FPGA Class on DDR_RES_WE_N

SSTV16857
TVS0P48

SN74SSTV16857DGVR
TVSOP48
PARTS=1
LEVEL=STD

U15

DDR_REG_WE_N
DDR_REG_CS_N
DDR_REG_BA0
DDR_REG_BA1
DDR_REG_CAS_N
DDR_REG_RAS_N
DDR_REG_CKE

DDR_MEM_CK5_N
DDR_MEM_CK5

NEED TO CHANGE DDR_REG_WE_N
SO ATTRIBUTE IS "CLASS" NOT "DDR"

NOTES:

1. All Traces are 50 ohm Controlled impedance.
2. Termination Rs to DDR componenets are shown on on page 31.
3. Series and Parallel termination resistors on this page should be placed as close as possible to the DDR chips.
4. the 0.1UF caps should be placed at each VCC pins of both of the SSTV16859.
5. For details of tracelengths control, see page 56, Classes 1-8.

VCC2V5
C341 0.1UF 0402
C342 0.1UF 0402
C343 0.1UF 0402
C344 0.1UF 0402
C345 0.1UF 0402
C346 10UF A
C347 0.1UF 0402
C348 0.1UF 0402
C349 0.1UF 0402
C350 0.1UF 0402
C351 0.1UF 0402
C352 10UF A

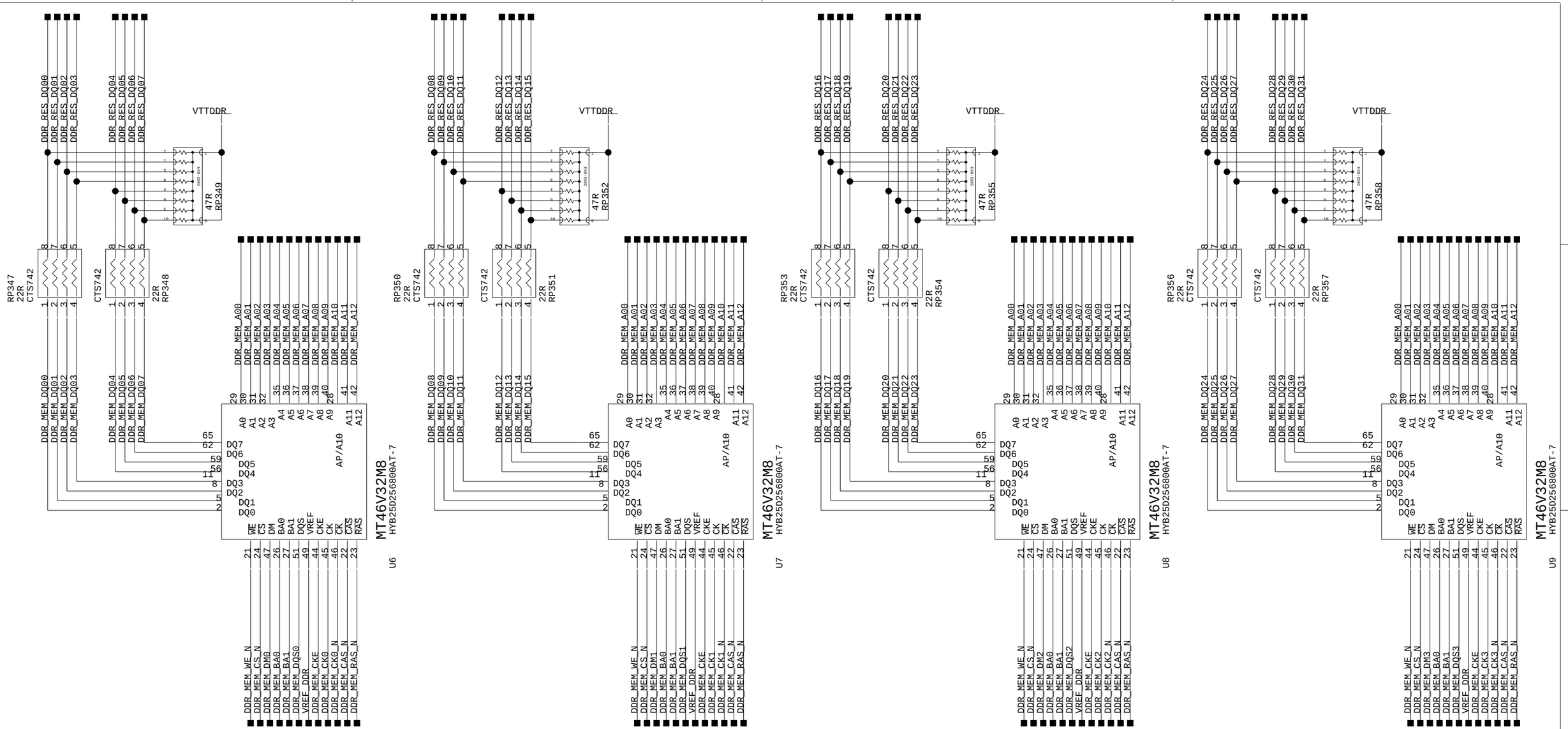
ML300 CPU
V2P7 Bank 6/7 (18/19)
Registers for DDR SDRAM

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
DDR SDRAM - Registers

Date: October 17th, 2002 | Ver: 1.00
Sheet Size: B | Rev: A
Sheet 29 of 56 | Drawn By BP



Silkscreen: "DDR SDRAM - 4 of 8x32M"

NOTES:

1. All Traces are 50 ohm Controlled impedance.
2. For details of tracelengths control, see page 56, Classes 1-8.
3. Series and Parallel termination resistors on this page should be placed as close as possible to the DDR chips.
4. See page 34 for placement of bypass caps
5. Rest of Data path termination Rs shown on page 32

ML300 CPU

V2P7 Bank 6/7 (18/19)

DDR SDRAM Chips

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

DDR SDRAM - Components

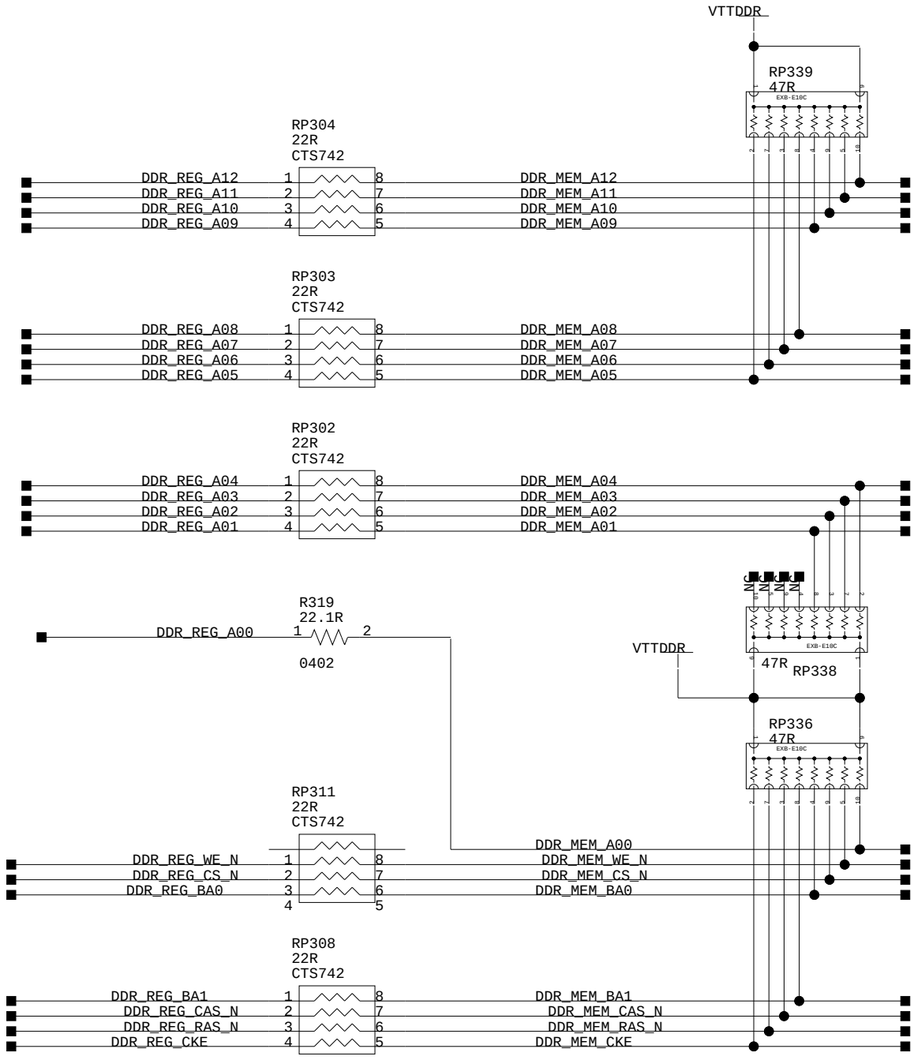
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 30 of 56	Drawn By BP

NOTES:

1. Series termination resistors on this page should be placed as close as possible to the DDR registers (U14 and U15)

2. Parallel termination resistors on this page should be placed after the DDR chips relative to the DDR registers.

3. For details of tracelengths control, see page 56, Classes 1-8.



ML300 CPU

DDR Termination for DDR SDRAM

From Registers to Chips

XILINX

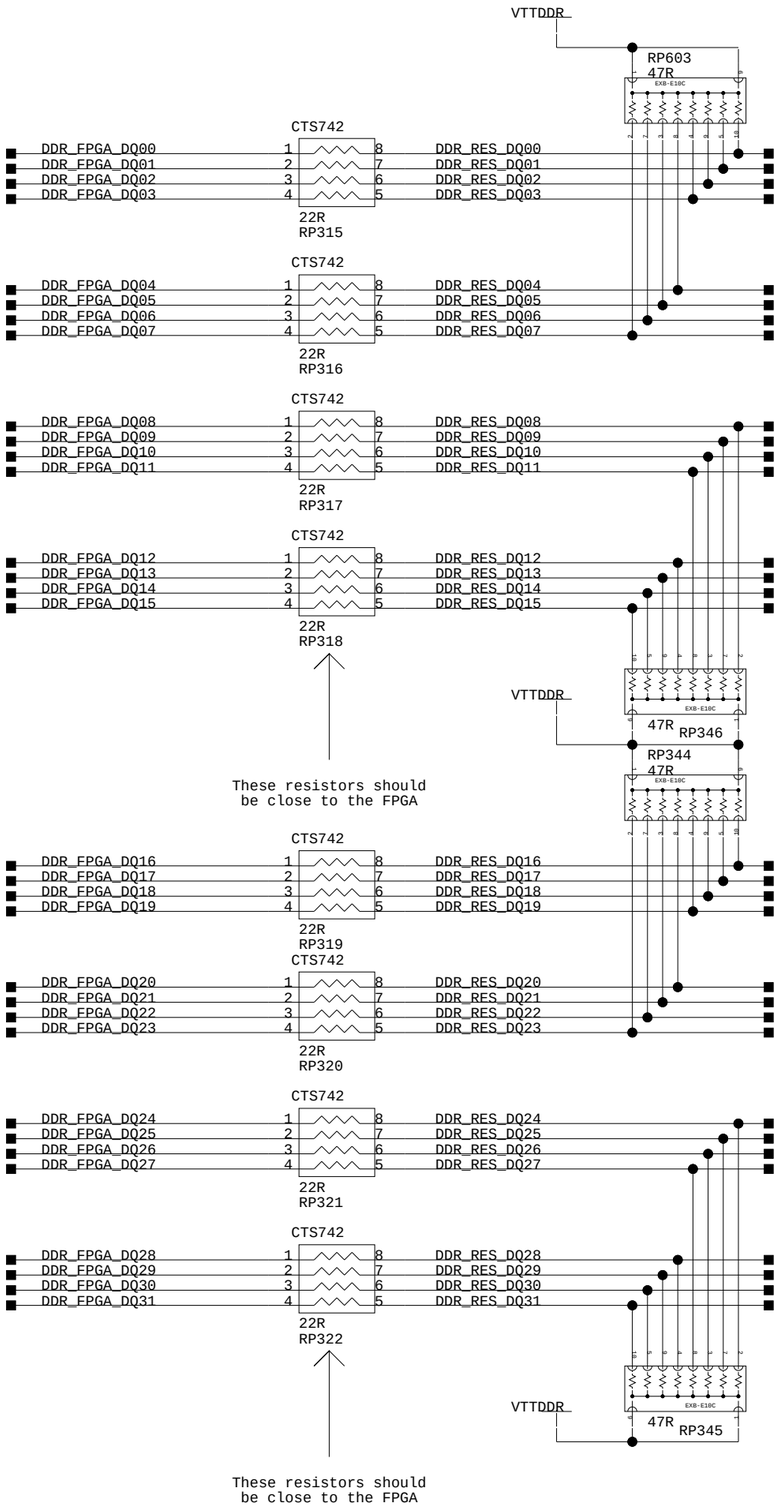
PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

DDR SDRAM - Termination (1 of 2)

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 31 of 56	Drawn By BP

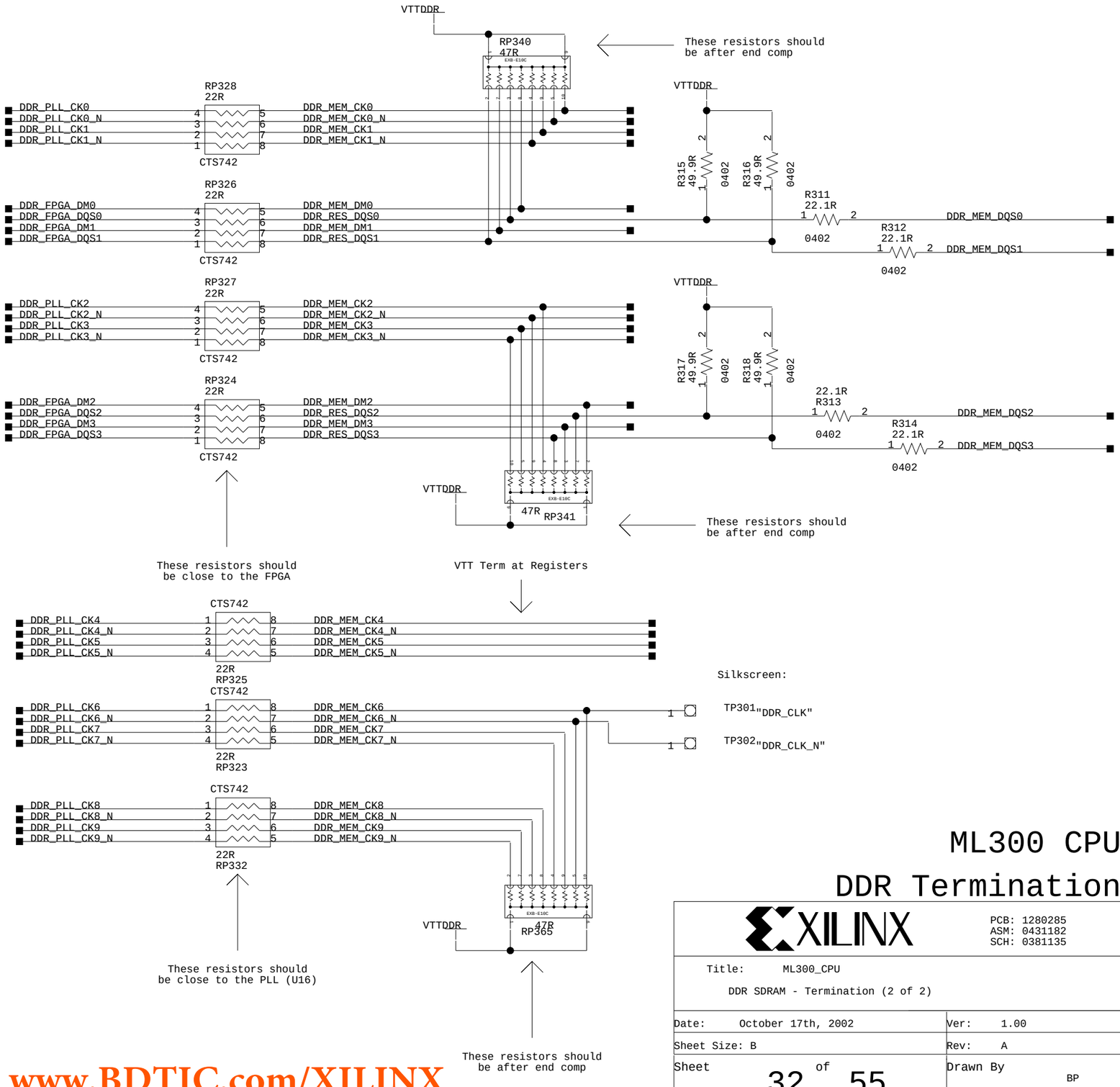
DDR_DATA_FPGA Class is on
DDR_FPGA_DQ00,04,08,12,16,20,24,28 and DM0



These resistors should
be close to the FPGA

These resistors should
be close to the FPGA

DDR_CLK_MEM Class is on DDR_MEM_CK0, 2, 4, and 6
DDR_CNTL_FPGA (DQS0-DQS3) Class is on DDR_FPGA_DQS0



These resistors should
be close to the PLL (U16)

VTT Term at Registers

These resistors should
be after end comp

Silkscreen:

TP301 "DDR_CLK"

TP302 "DDR_CLK_N"

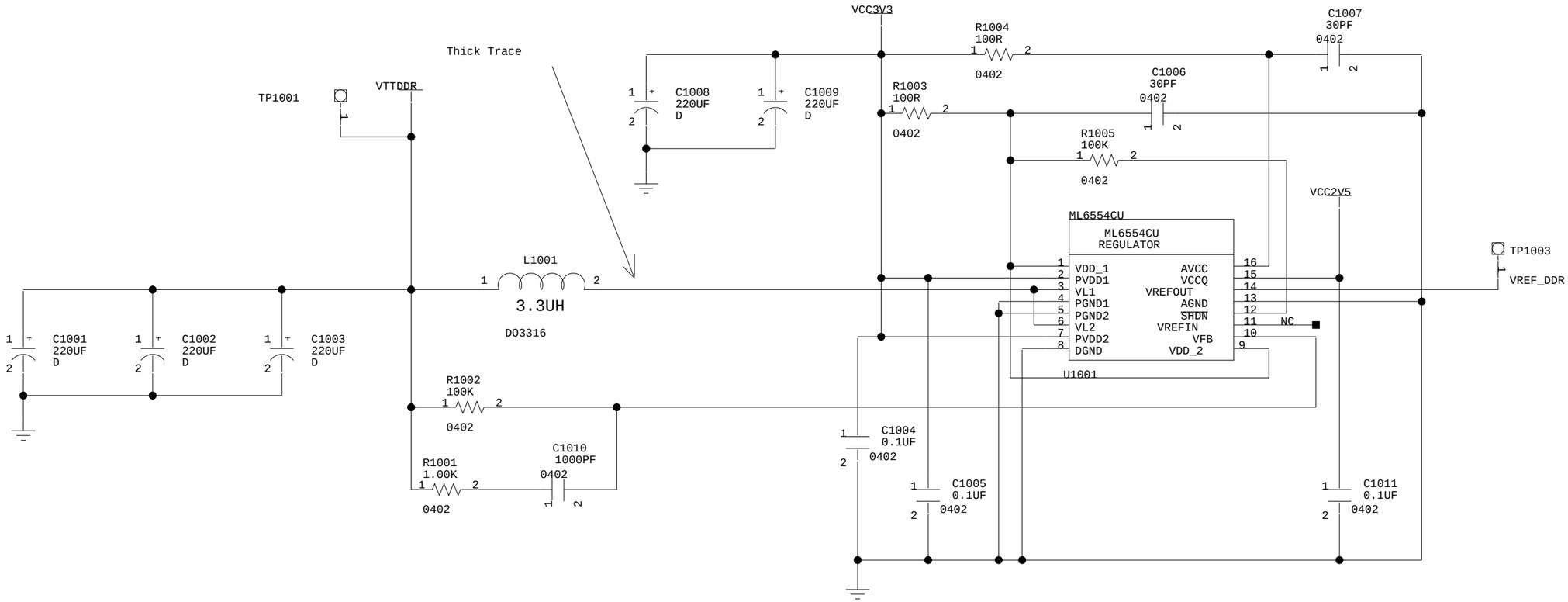
ML300 CPU
DDR Termination

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU DDR SDRAM - Termination (2 of 2)	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 32 of 55	Drawn By BP

DDR VTT & VREF



ML300 CPU
DDR Regulator

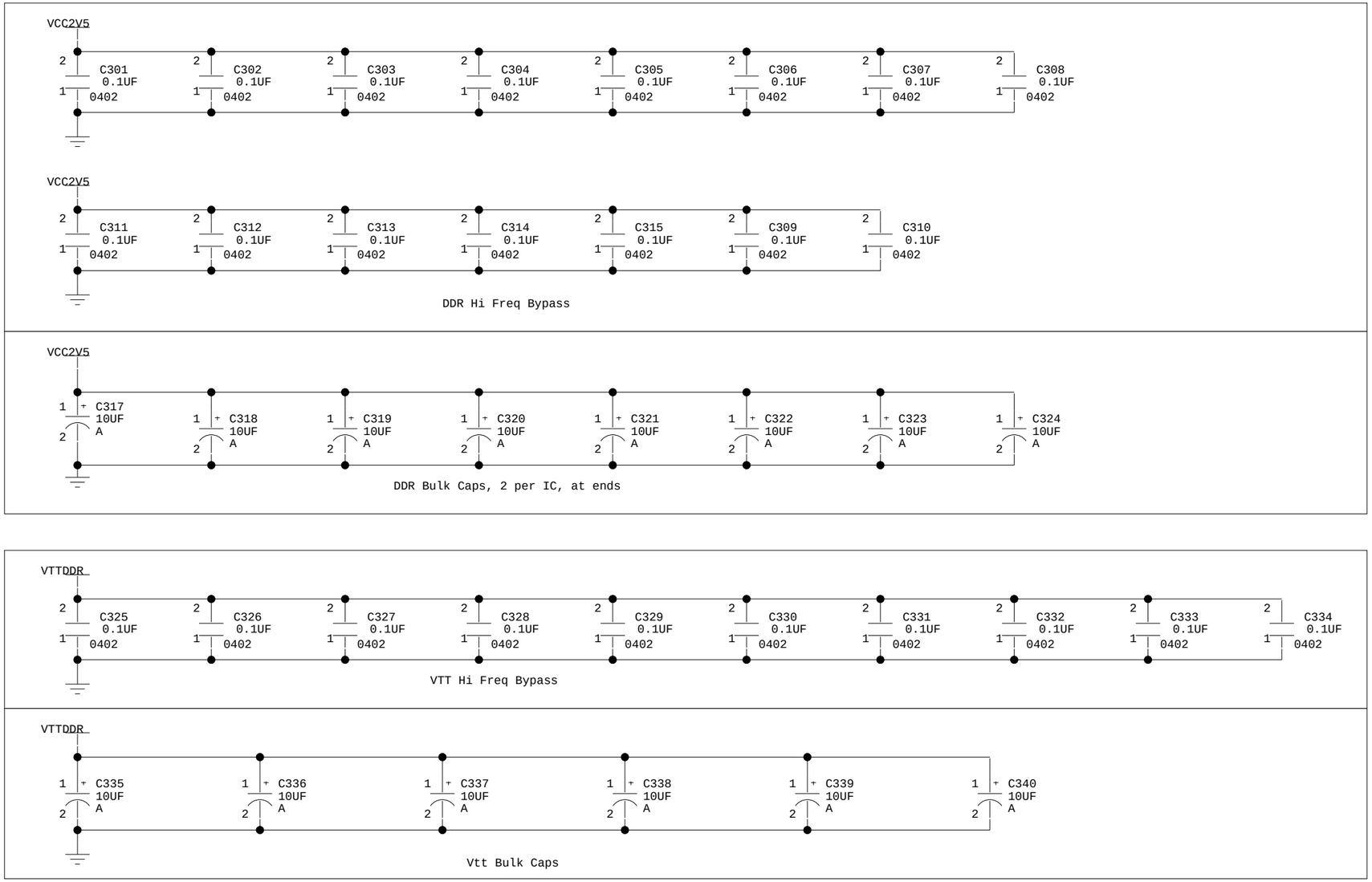
XILINX

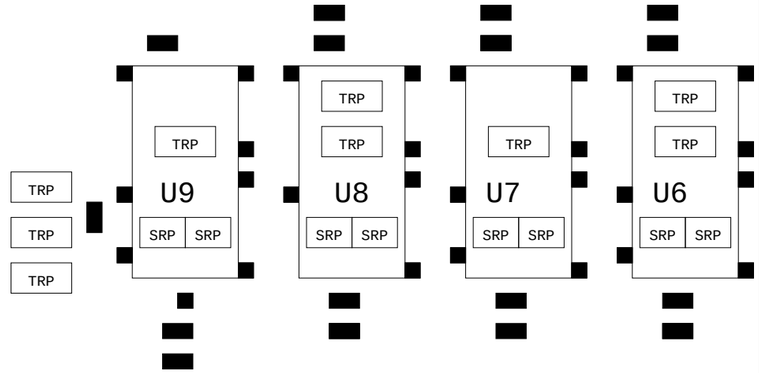
PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

Voltage Regulator for DDR SDRAM

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 33 of 55	Drawn By BP





LAYOUT FOR DDR, CAPS, RPs
(X-Ray View to Bottom Side)

DDR Bulk Caps

DDR HF Bypass Caps (MLC)

VTT Bulk Caps

VTT HF Bypass Caps (MLC)

TRP — Termination Resistor Pack

SRP — Series Resistor Pack

ML300 CPU
DDR Bypass Capacitors

XILINX

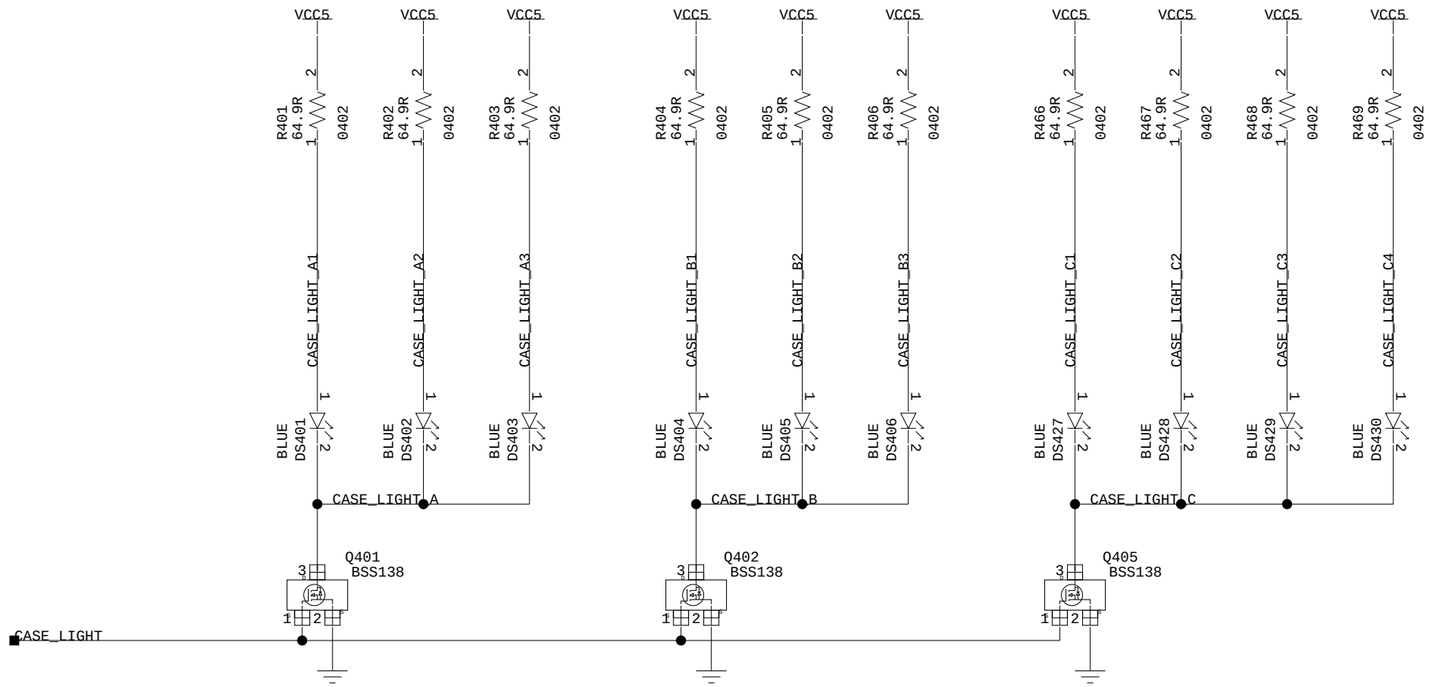
PCB: 1280285
ASM: 0431182
SCH: 0381135

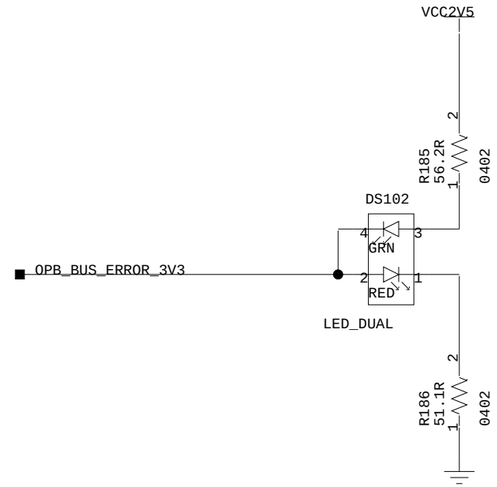
Title: ML300_CPU

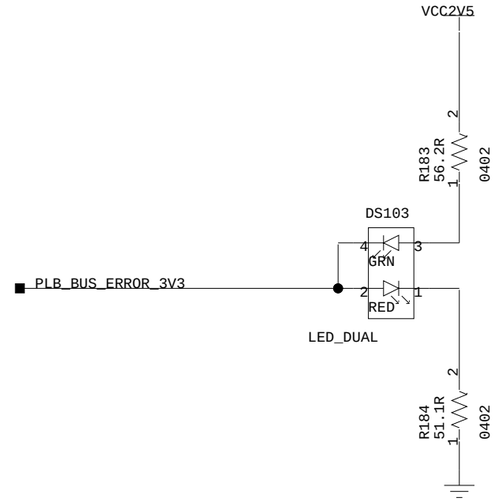
DDR SDRAM - Bypass Caps

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 34 of 55	Drawn By GB

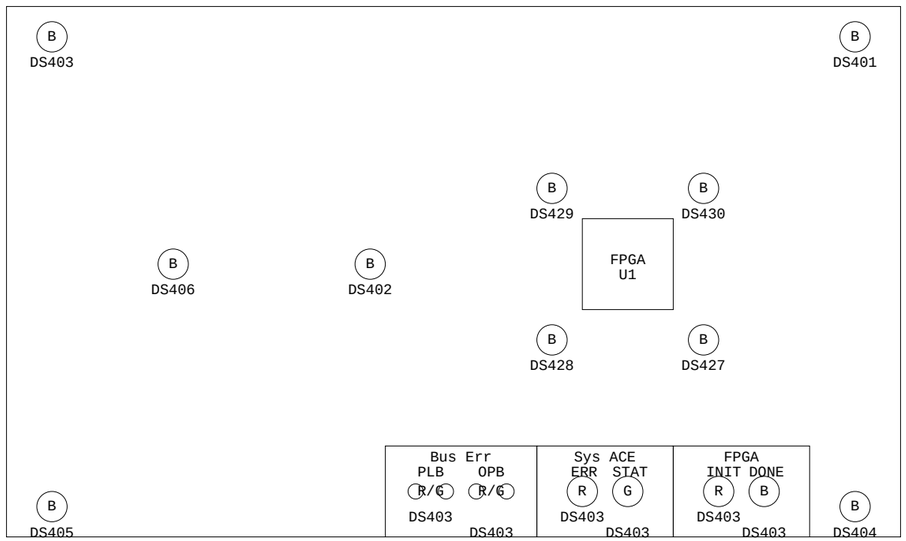
Illumination LEDs







LED placement on Solder side of board (not X-Ray)



B BLUE 0603 LED

R RED 0603 LED

G GREEN 0603 LED

R/G DUAL COLOR LED

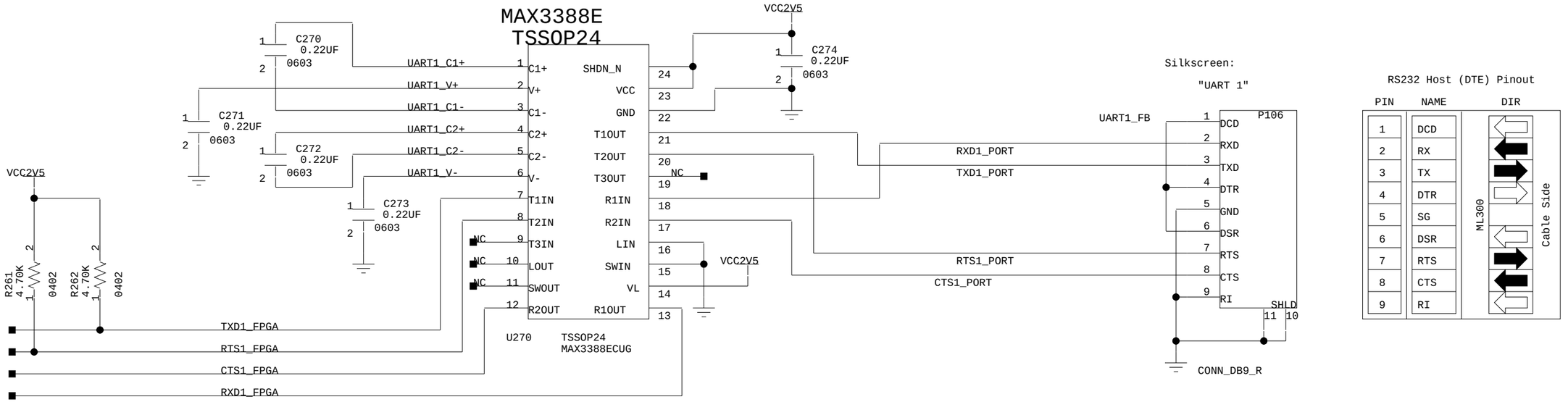
ML300 CPU
Illumination LEDs

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
Illumination LEDs

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 35 of 55	Drawn By BP



ML300 CPU
V2P7 Bank 4 (16)
Serial Ports

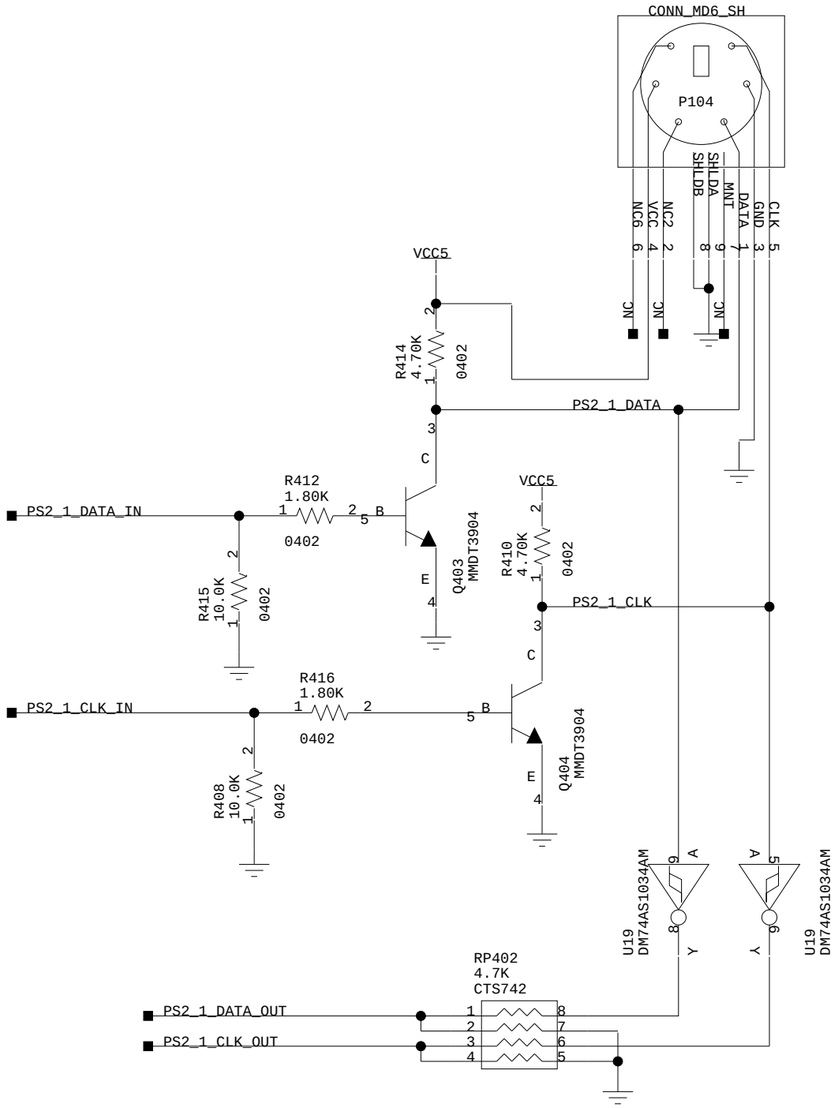
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

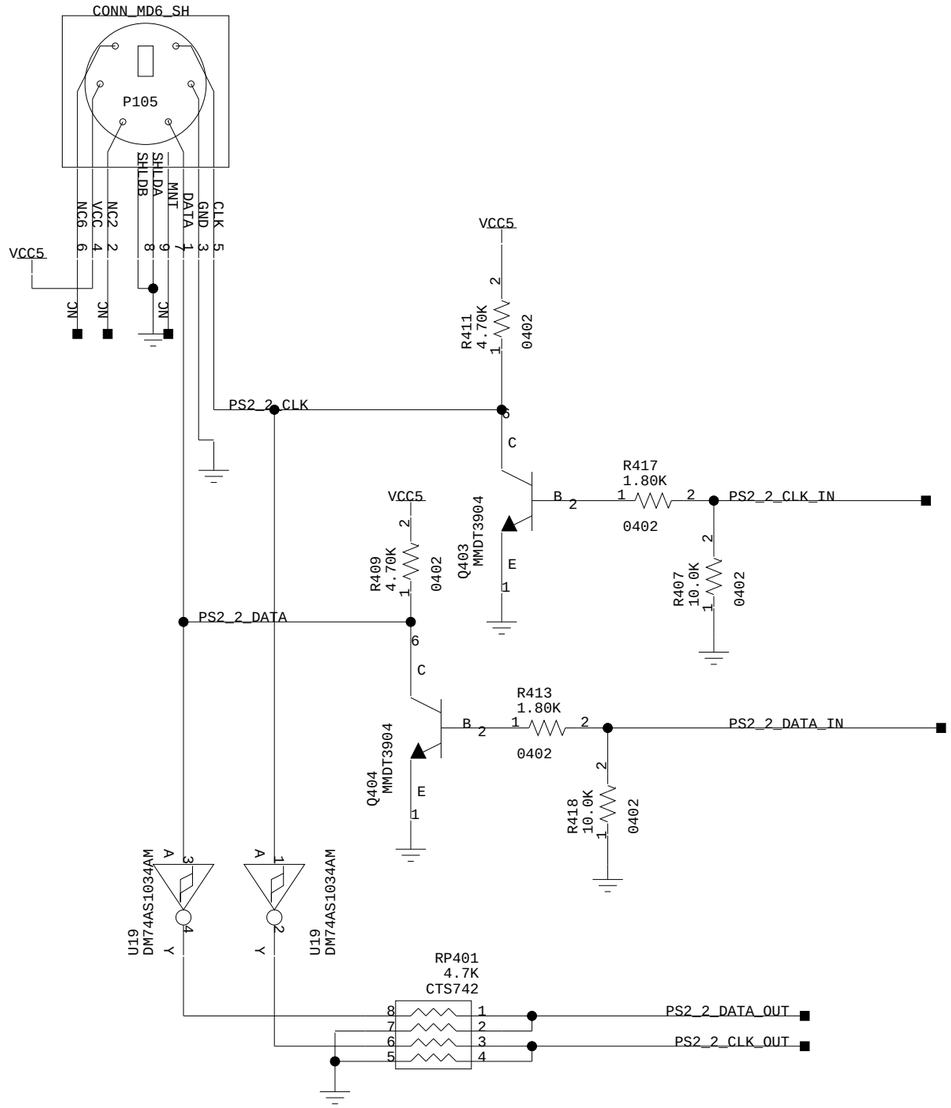
Title: ML300_CPU
Serial Ports

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 36 of 55	Drawn By BP

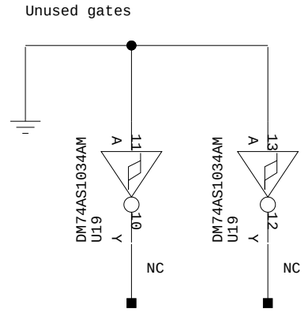
Silkscreen:
"PS2 #1"
"Mouse"



Silkscreen:
"PS2 #2"
"Keyboard"



Unused gates



PS2 NOTES:

1. PS2 uses open collector. Use NPN transistor to bring the signal up to 5V levels
2. The Signal to the connector is fed back to the FPGA through a voltage divider for signals from peripheral.

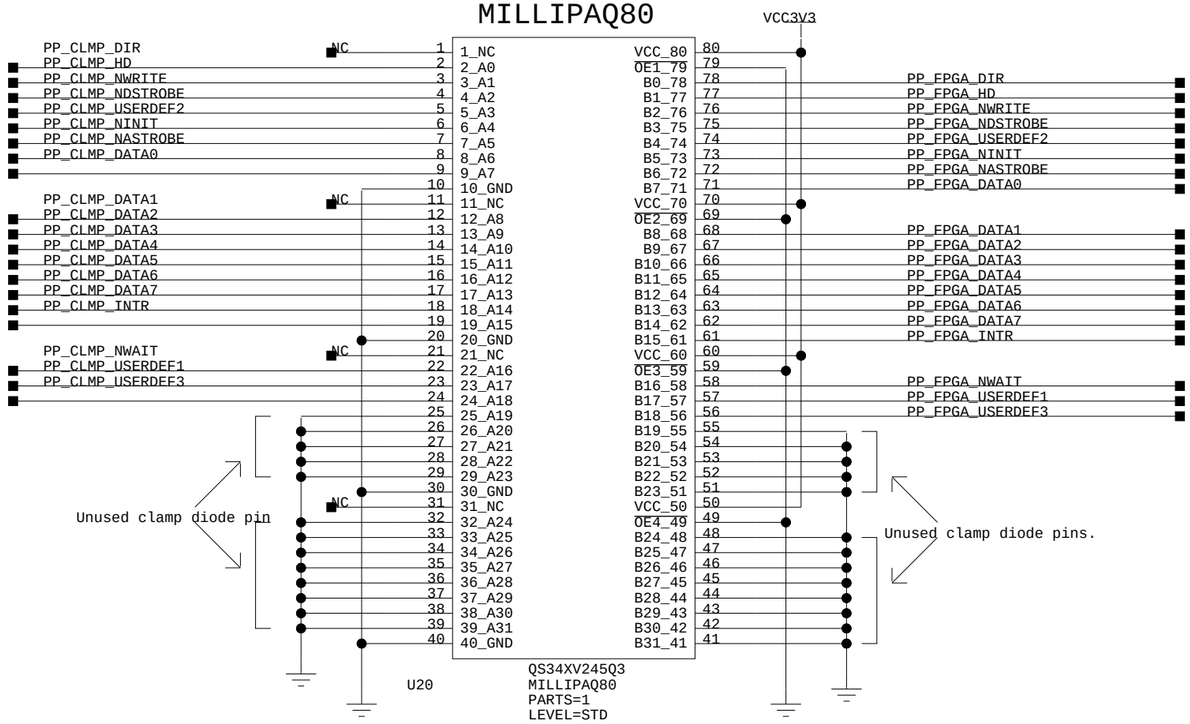
ML300 CPU
V2P7 Bank 0 (12)
PS/2 Ports

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
PS/2 Ports

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 37 of 55	Drawn By BP



ML300 CPU

V2P7 Bank 7 (19)

Parallel Port Level Shifter

XILINX

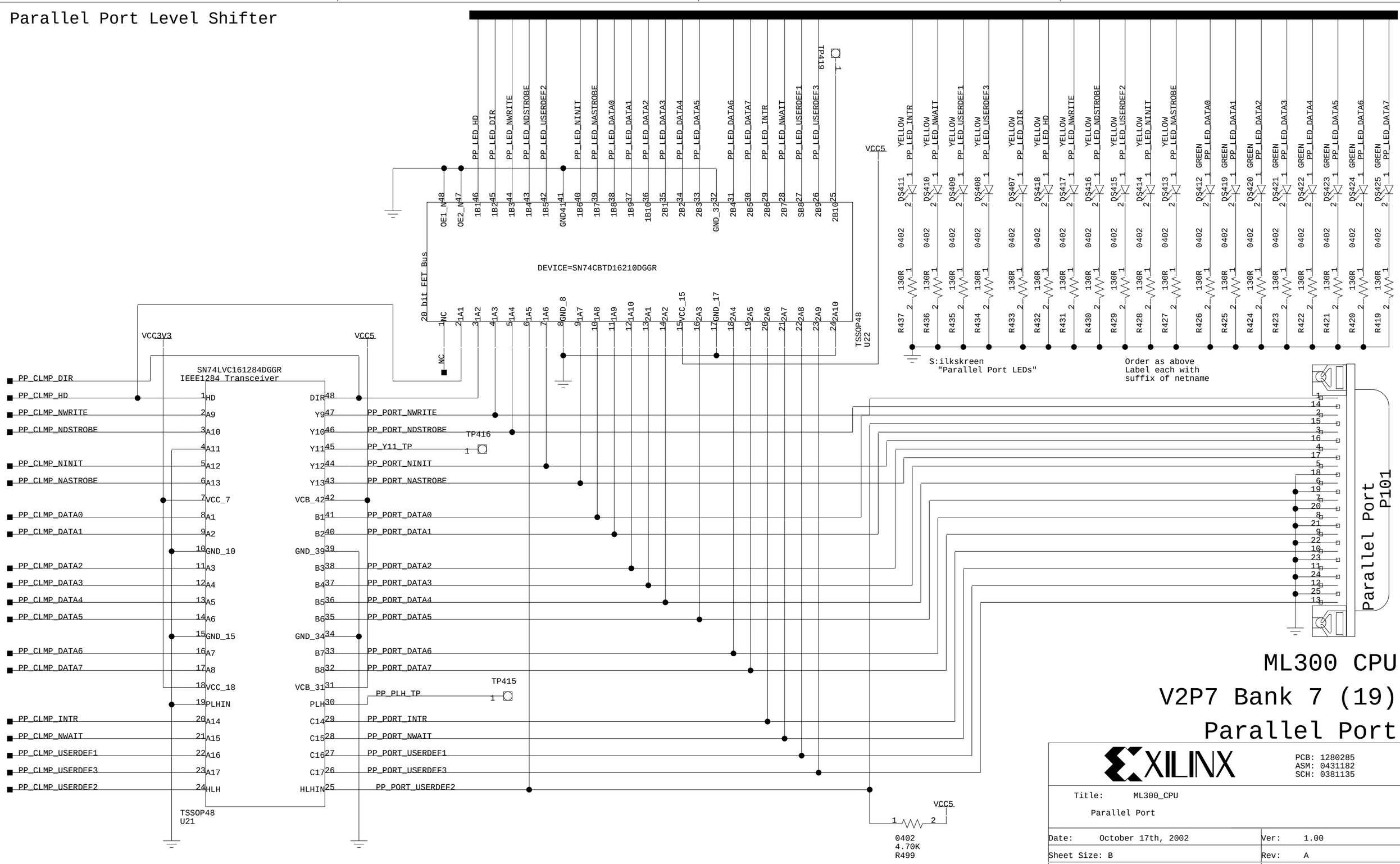
PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

Parallel Port Level Shifter

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 38 of 55	Drawn By GB

Parallel Port Level Shifter



ML300 CPU

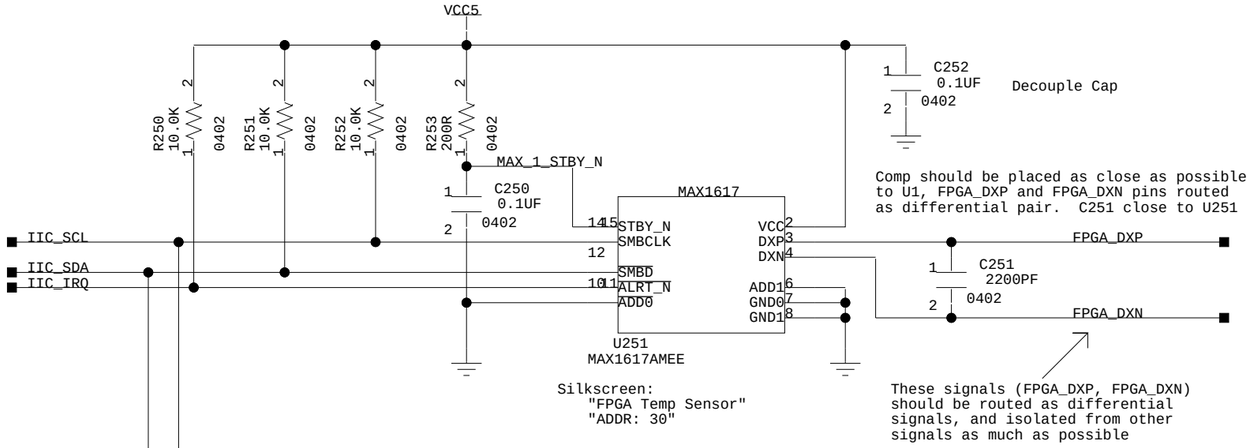
V2P7 Bank 7 (19)

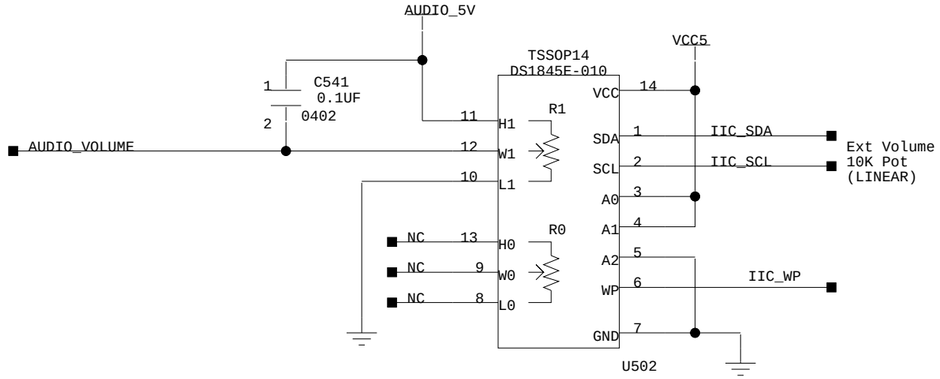
Parallel Port

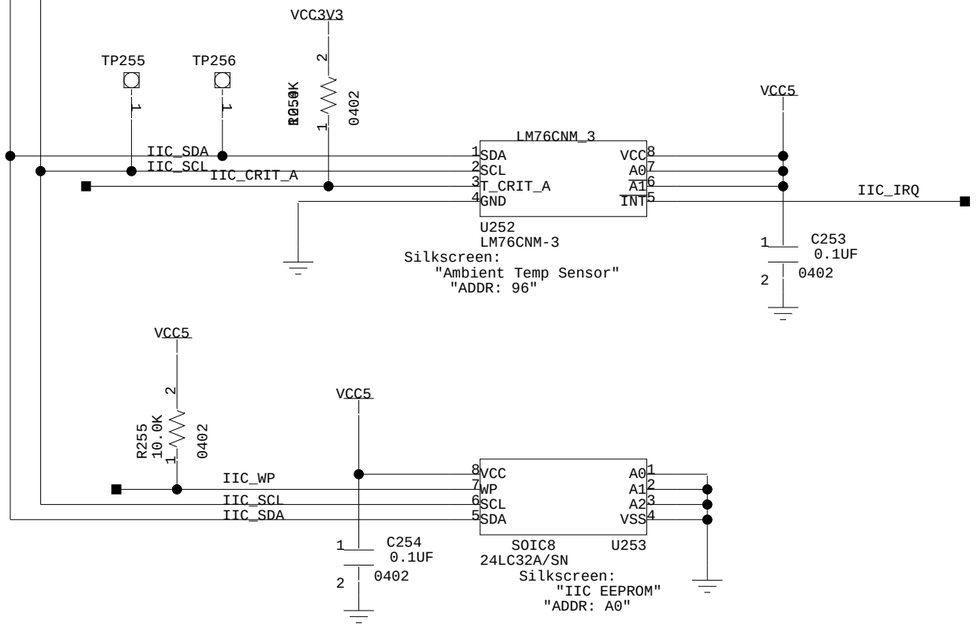
XILINX

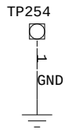
PCB: 1280285
ASM: 0431182
SCH: 0381135

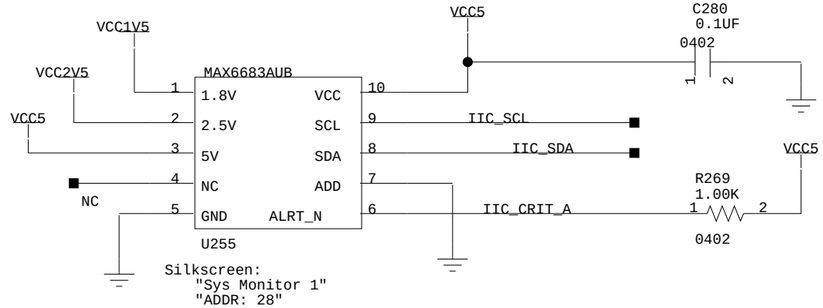
Title: ML300_CPU Parallel Port	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 39 of 55	Drawn By BP

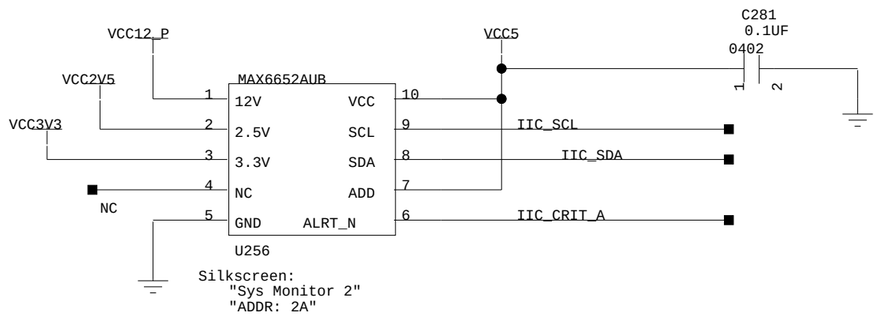












IC	BOARD	REF	DESCRIPTION	ADDR
MAX6683AUB	ML300_CPU	U255	System Monitor 1	28/29
MAX6652AUB	ML300_CPU	U256	System Monitor 2	2A/2B
MAX6652AUB	ML300_PWR_IO	U4	System Monitor 4	2E/2F
MAX6683AUB	ML300_PWR_IO	U2	System Monitor 3	2C/2D
MAX1617	ML300_CPU	U251	FPGA Die/Ambient Temp	30/31
LM76CNM_3	ML300_CPU	U252	Ambient Temp	96/97
24LC32A/SN	ML300_CPU	U253	32Kbit EEPROM	A0/A1
DS1845E-010	ML300_CPU	U502	Audio Trimpot	A6/A7
DS1845E-010	ML300_PWR_IO	U3	TFT Touchscreen Trimpot	AC/AD
X1226S8	ML300_PWR_IO	U24	Real Time Clock 4Kbit EEPROM	AE/AF
X1226S8	ML300_PWR_IO	U24	Real Time Clock RTC	DE/DF

NOTES:
1. The IIC Bus has devices on both the CPU and PWR_IO boards.

ML300 CPU
Bank 3 (15) - IIC Bus

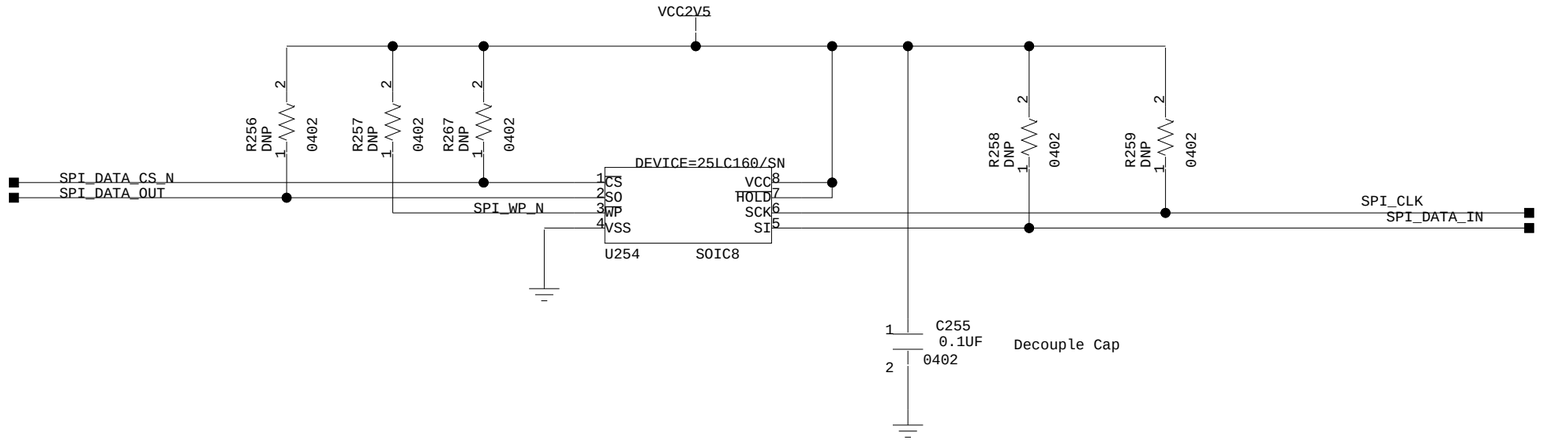
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
IIC Bus

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 40 of 56	Drawn By BP

SPI ROM 2.5V- 5.5V



ML300 CPU

Bank 4 (16)

SPI

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

SPI Bus

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 41 of 55	Drawn By BP

Connector is bottom view

Silkscreen:
"Ethernet Port"

Silkscreen:
"Ethernet Port"

RJ45

Silkscreen:
"Full/Coll LED"
CON_AMP_569564

Silkscreen: "Ethernet Magnetics"

Silkscreen: "Ethernet Phy"

Silkscreen:
"GND"

Place at edge of PCB
Silkscreen:
"PHY 10/100 100=ON"

LXT971_LQFP64
LQFP64
(DIE DOWN)

DEVICE=DJLXT971ALCA4834105
PKG_TYPE=LQFP64
PARTS=1
LEVEL=STD

U26

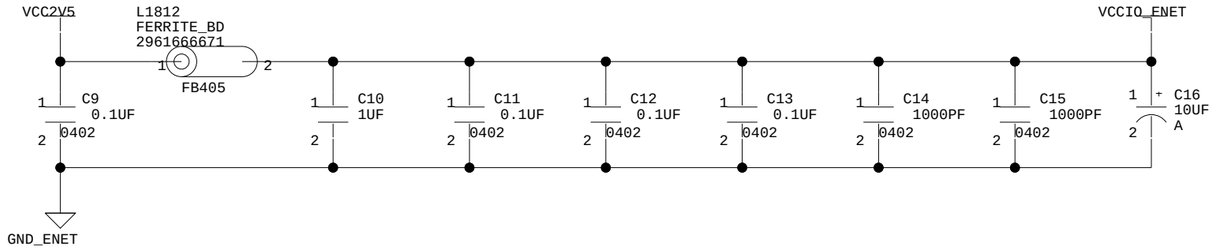
TG110-S050N2

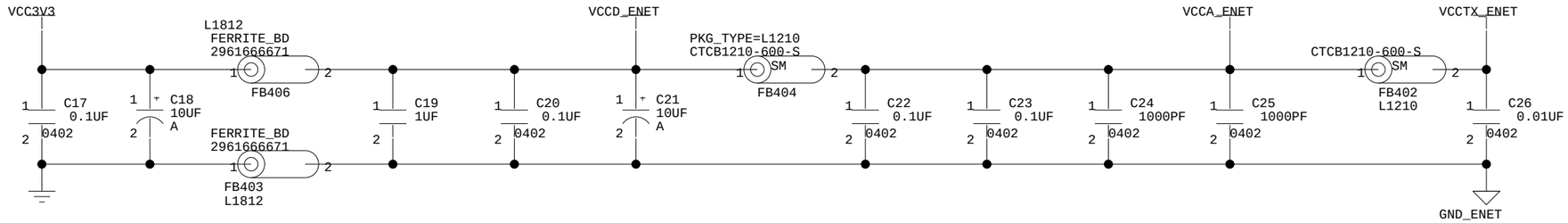
ML300 CPU
Bank 0 (12)
Ethernet PHY

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU Ethernet Phy	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 42 of 55	Drawn By BP





ML300 CPU

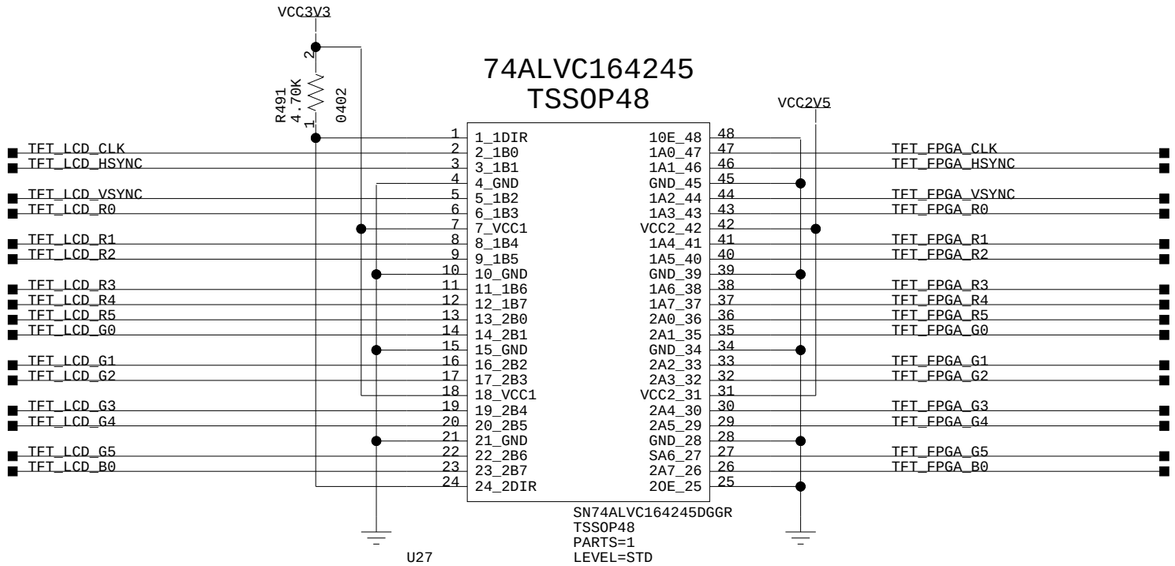
Ethernet Power Filter

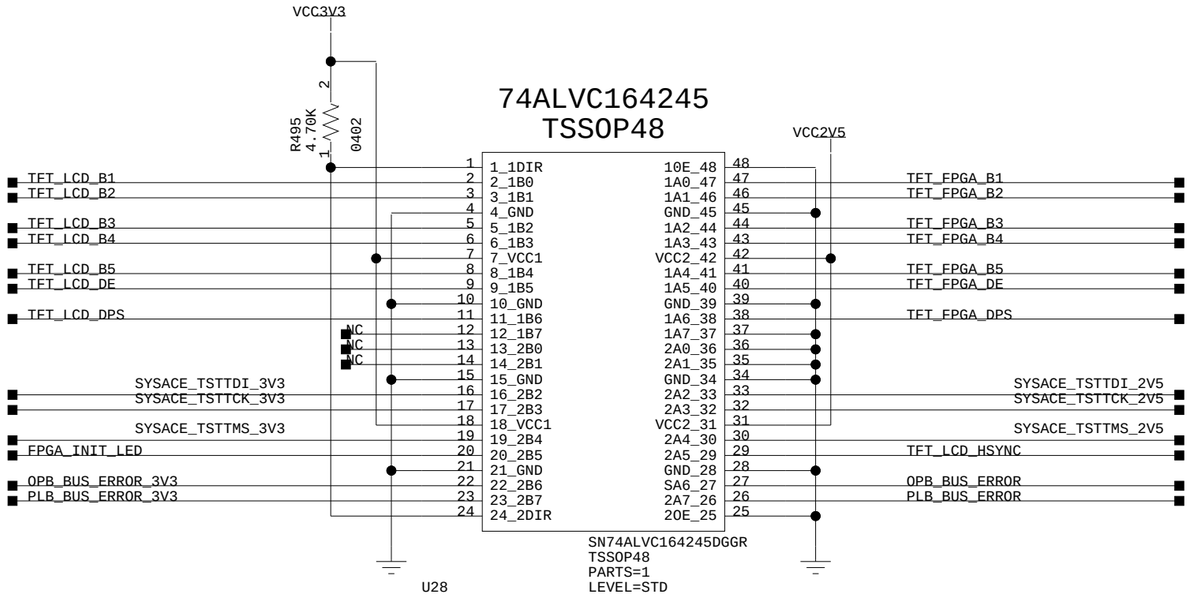
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU Ethernet Power	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 43 of 55	Drawn By BP

LCD Level Shifters - 2.5V to 3.3V





ML300 CPU
V2P7 Bank 4 (16)
TFT LCD

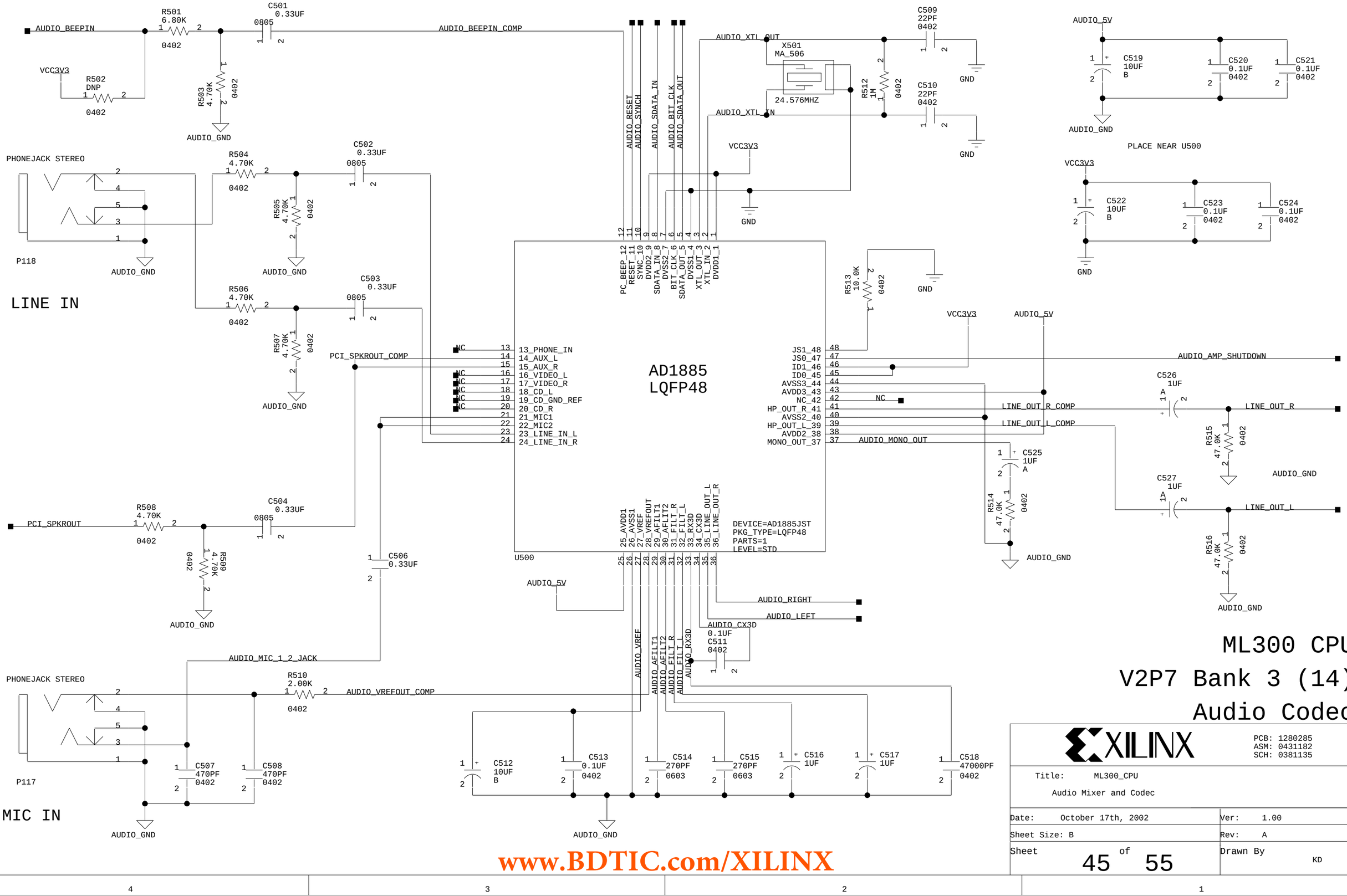
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

TFT LCD - Level Shifter and Conn

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 44 of 55	Drawn By BP



Rs Out	Rs In	Function
RS531 RS532	RS533 RS534	Headphone (Default)
RS533 RS534	RS531 RS532	Line

AUDIO_5V

C528 10UF B

C529 0.1UF 0402

C530 0.1UF 0402

C531 0.1UF 0402

AUDIO_GND

DEVICE=LM4835MTE

TSSOP28

6	VDD1		
16	VDD2		
27	VDD3		
4	MODE		
13	A_FB		
12	A_IN	A_L1	19
22	BYPASS	A_L2	18
9	B_FB	OUT_A_MINUS	17
10	B_IN	OUT_A_PLUS	15
2	SHUTDOWN	HP_IN	21
5	MUTE	OUT_B_PLUS	28
11	BEEP	OUT_B_MINUS	26
3	INTERNAL_GAIN_SELECT	B_R2	25
		B_R1	24
		VOLUME	7
1	GND1		
8	GND2		
14	GND3		
20	GND4		
23	GND5		

U501

AUDIO_LEFT — R518 20.0K 0402 — C532 0.33UF A — R519 20.0K 0402

AUDIO_RIGHT — R520 20.0K 0402 — C533 0.33UF A — R521 20.0K 0402

AUDIO_AMP_SHUTDOWN

AUDIO_BYPASS — C534 1UF A

R523 20.0K 0402 — R524 20.0K 0402 — C539 68000PF 0402

R526 20.0K 0402 — R527 20.0K 0402 — C540 68000PF 0402 — R528 20.0K 0402

AUDIO_OUT_A_MINUS — C542 220UF X — L SPKR — PKG_TYPE=HDR_1X2 J505 DNP

AUDIO_OUT_A_PLUS — R533 0R 0805

LINE_OUT_HP — R539 100K 0402 — R534 0R 0805

AUDIO_OUT_B_PLUS

AUDIO_OUT_B_MINUS — J506 DNP — R SPKR — C543 220UF X

LINE_OUT_L — R531 DNP 0805

LINE_OUT_R — R532 DNP 0805

R535 1.00K 0402 — R536 1.00K 0402

AUDIO_VOLUME

Volume of Audio codec is controlled by an IIC trimpot - see page 40.
Audio IIC Trimpot Addr is "A6"

AUDIO_5V — R538 100K 0402

PHONEJACK STEREO

KEEP GND INTO LOTS OF COPPER

P116

HEADPHONE/
LINE OUT

FAT TRACE

AUDIO_GND

Place near FB501/502

VCC5 — C535 0.1UF 0402 — C536 0.1UF 0402 — GND

VCC5 — FERRITE_BD 2961666671 FB501 L1812 — C537 10UF B — GND

AUDIO_5V — C538 1UF A — AUDIO_GND

FERRITE_BD 2961666671 FB502 L1812

ANALOG GND SHOULD BE SEGREGATED PLANE

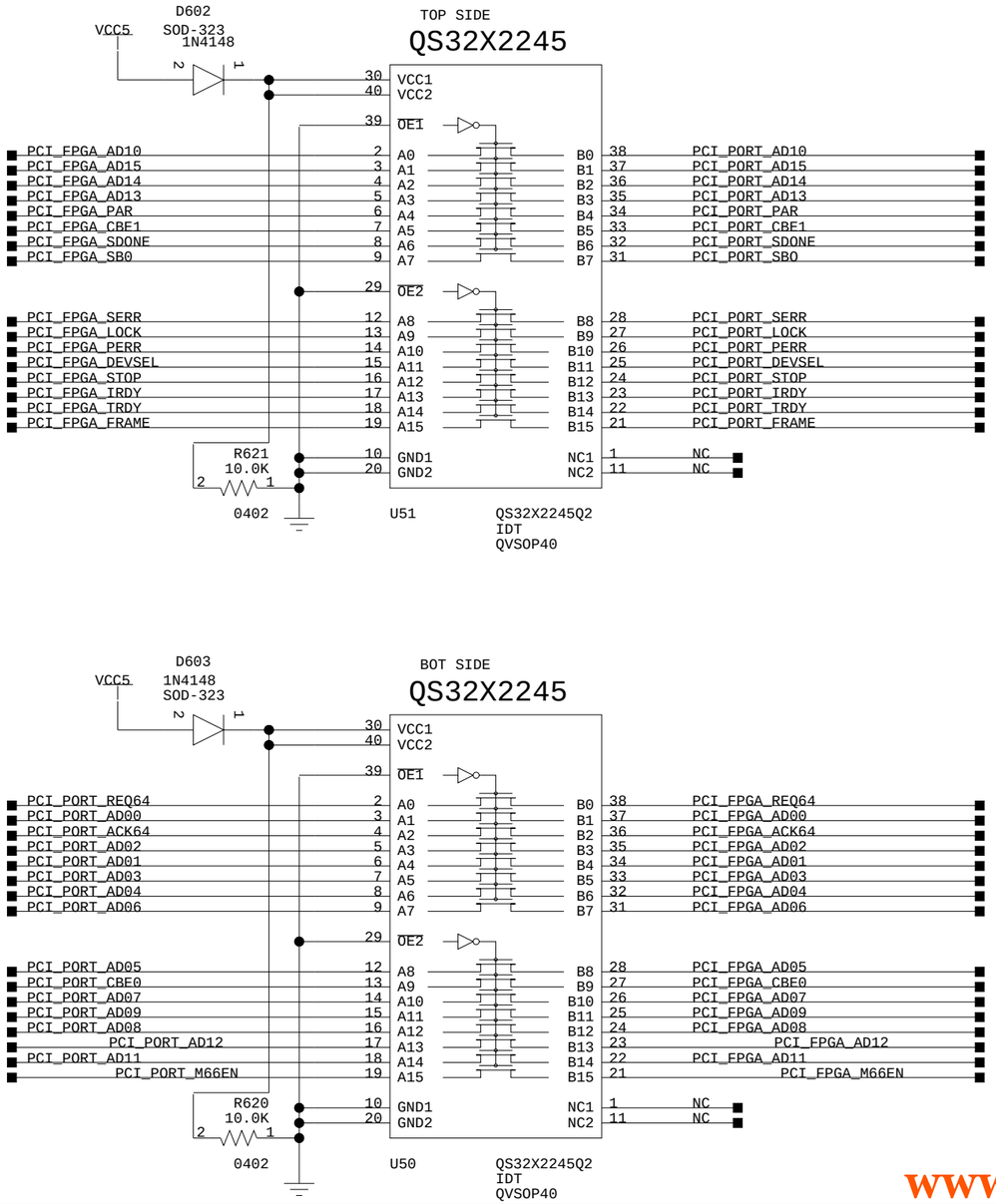
ML300 CPU
Audio Codec PWR Amps

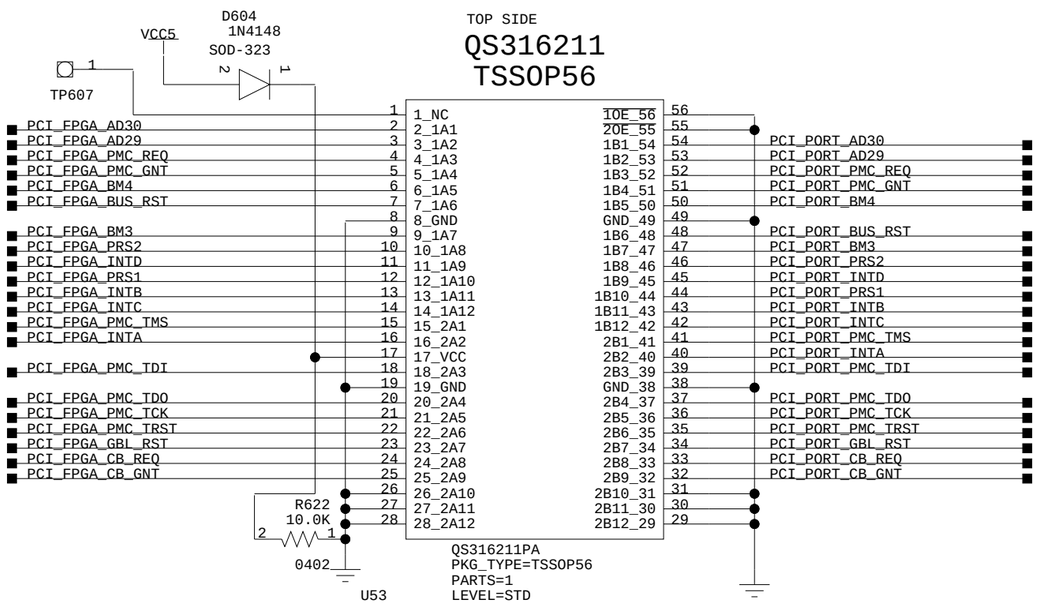
XILINX

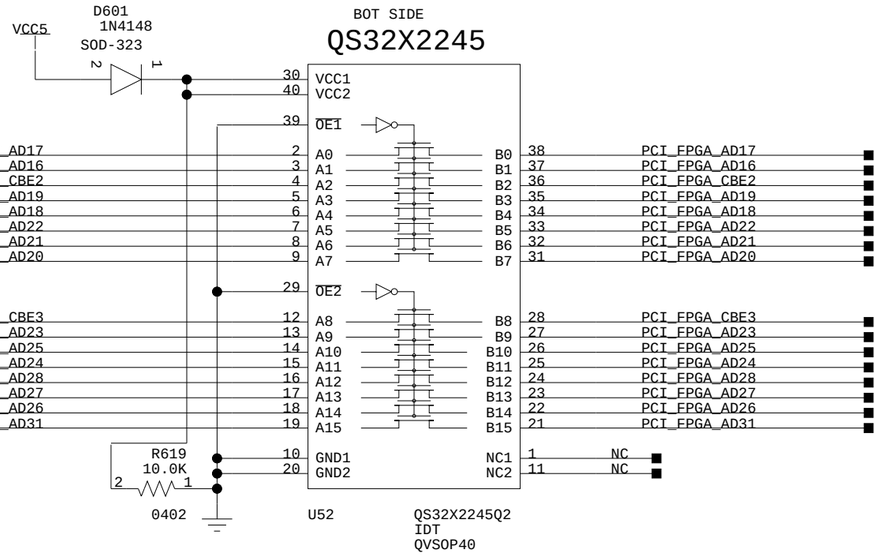
PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
Audio Codec Power Amplifiers

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 46 of 55	Drawn By KD







ML300 CPU
Bank 2/3 (14/15)
PCI Clamps

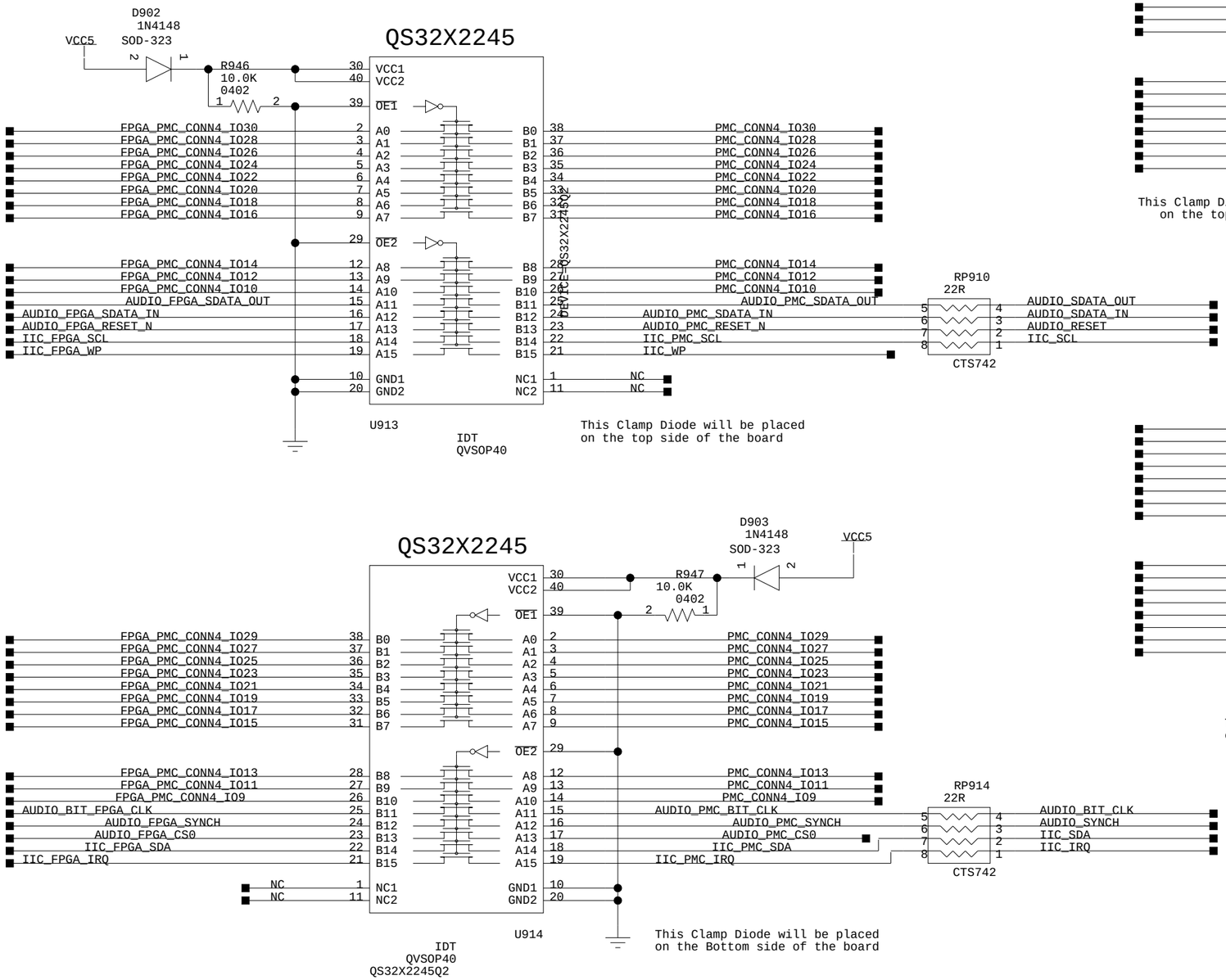
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

PCI Clamp Diodes for 5V Compliance

Date: October 15th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 47 of 55	Drawn By BP/GB



ML300 CPU
Bank 2/3 (14/15)
PMC Clamps

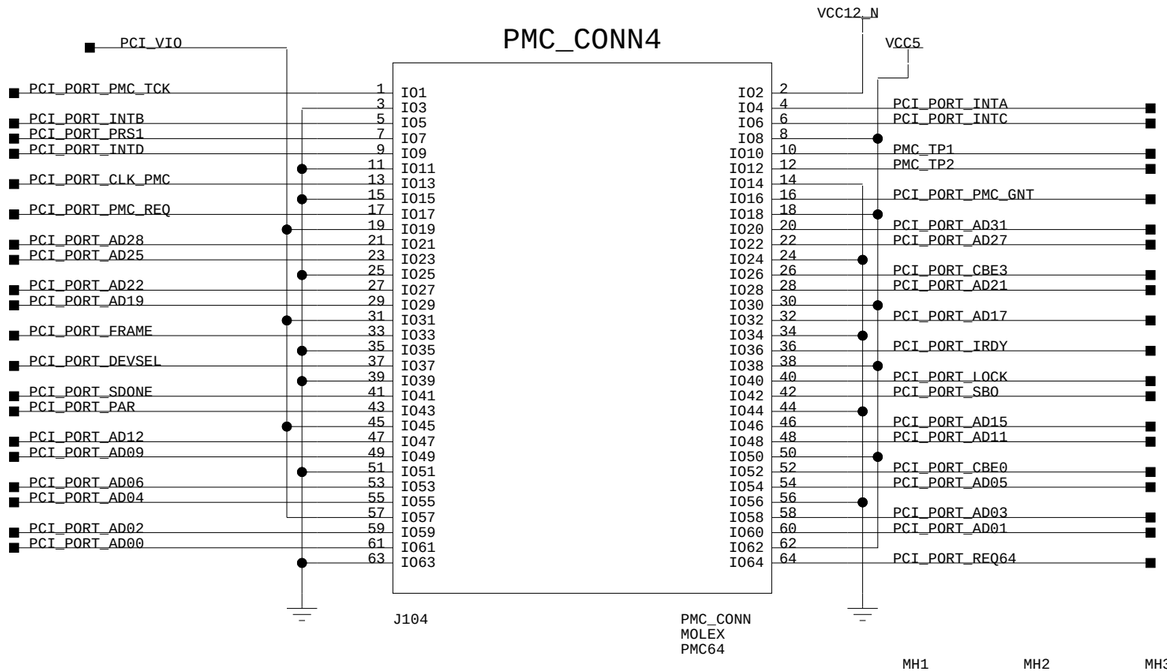
XILINX

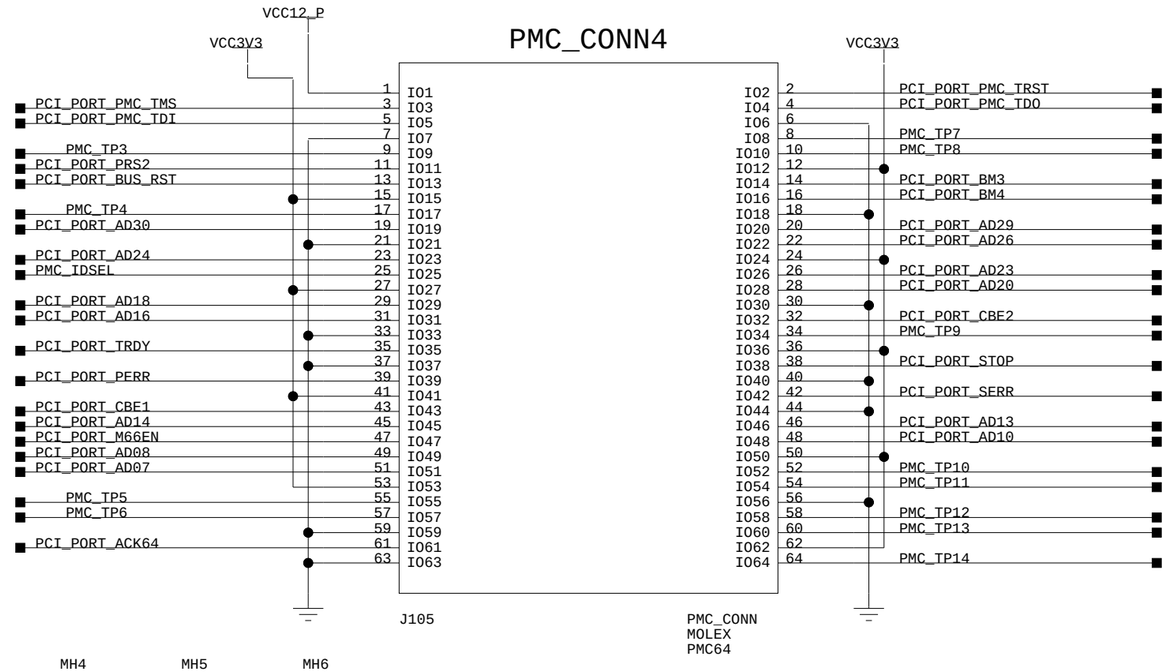
PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

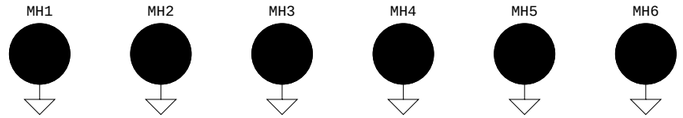
Clamp Diodes for PMC

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 48 of 55	Drawn By BP

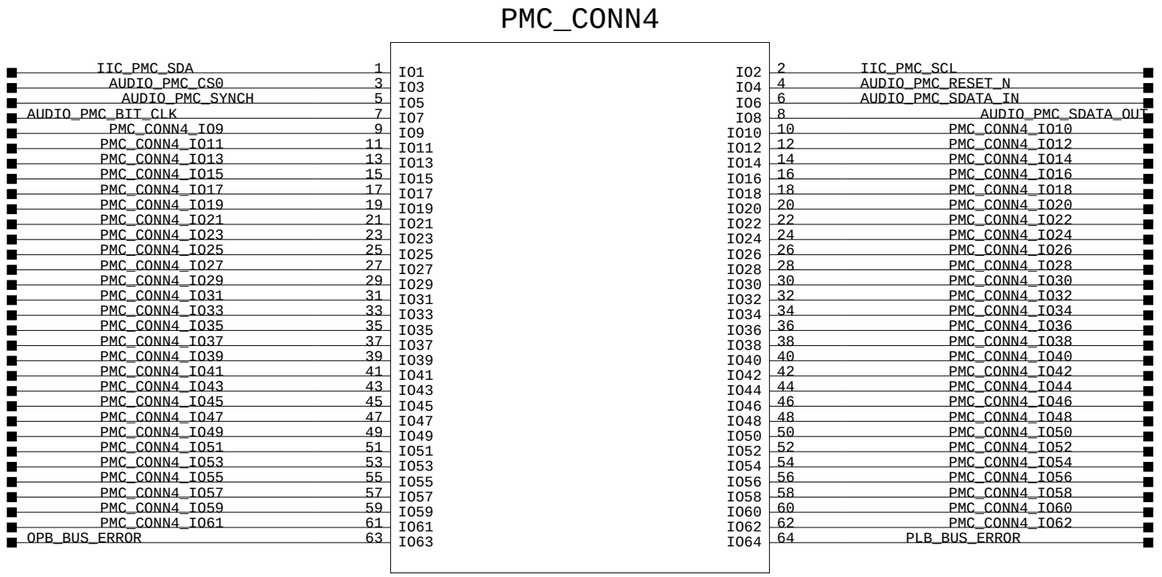




PMC_CONN4_IO61 should be used as a clock if clocking is needed for PMC_CONN4



PMC Mounting Holes



ML300 CPU
Bank 1/2 (13/14)
PMC Connectors

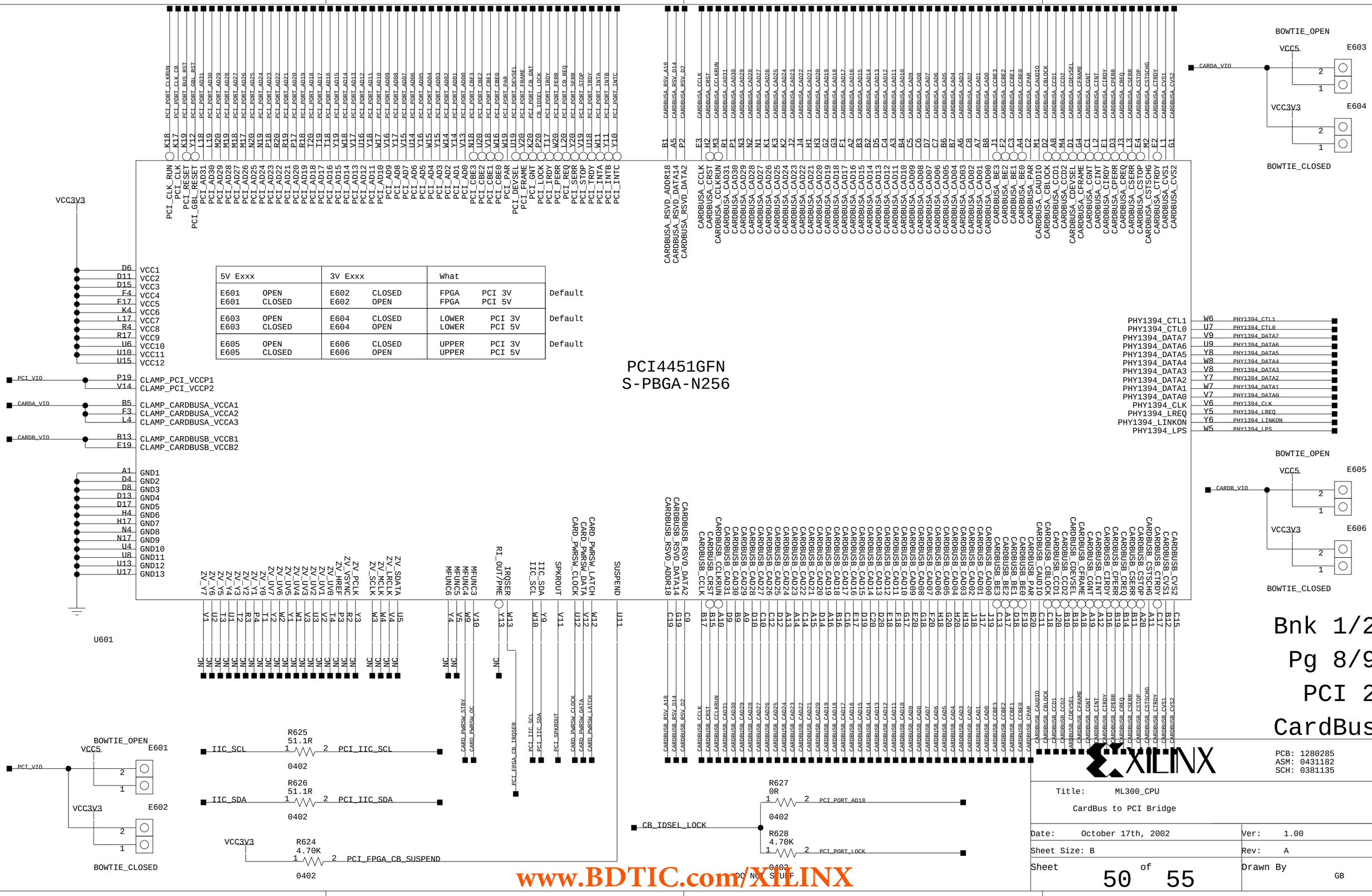
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

PMC Connectors

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 49 of 55	Drawn By BP/GB



CARDBUS_CONN
Upper Slot

P110
PKG_TYPE=FCI71240-340CA

1	GND_CA01	CARDBUSB_CAD0	
2	AD0_CA02	CARDBUSB_CAD1	
3	AD1_CA03	CARDBUSB_CAD2	
4	PAGND1		
5	AD3_CA04	CARDBUSB_CAD3	
6	AD5_CA05	CARDBUSB_CAD5	
7	PAGND2		
8	AD7_CA06	CARDBUSB_CAD7	
9	CAE0#_CA07	CARDBUSB_CCBE0	
10	PAGND3		
11	AD9_CA08	CARDBUSB_CAD9	
12	AD11_CA09	CARDBUSB_CAD11	
13	PAGND4		
14	AD12_CA10	CARDBUSB_CAD12	
15	AD14_CA11	CARDBUSB_CAD14	
16	PAGND5		
17	CAE1#_CA12	CARDBUSB_CCBE1	
18	PAR_CA13	CARDBUSB_CPAR	
19	PAGND6		
20	PERR#_CA14	CARDBUSB_CPERR	
21	GNT#_CA15	CARDBUSB_CGNT	
22	PAGND7		
23	INT#_CA16	CARDBUSB_CINT	
24	VCC_CA17	CARDBUSB_CVCC	
25	PAGND8		
26	PAGND9		
27	VPP1_CA18	CARDBUSB_CVPP	
28	CLK_CA19	CARDBUSB_CCLK	
29	PAGND10		
30	IRDY#_CA20	CARDBUSB_CIRDY	
31	CAE2#_CA21	CARDBUSB_CCBE2	
32	PAGND11		
33	AD18_CA22	CARDBUSB_CAD18	
34	AD20_CA23	CARDBUSB_CAD20	
35	PAGND12		
36	AD21_CA24	CARDBUSB_CAD21	
37	AD22_CA25	CARDBUSB_CAD22	
38	PAGND13		
39	AD23_CA26	CARDBUSB_CAD23	
40	AD24_CA27	CARDBUSB_CAD24	
41	PAGND14		
42	AD25_CA28	CARDBUSB_CAD25	
43	AD26_CA29	CARDBUSB_CAD26	
44	PAGND15		
45	AD27_CA30	CARDBUSB_CAD27	
46	AD29_CA31	CARDBUSB_CAD29	
47	PAGND16		
48	D2_RSRVD_CA32	CARDBUSB_RSV_D2	
49	CLKRUN#_CA33	CARDBUSB_CCLKRUN	
50	GND_CA34		

CARDBUS_CONN
Lower Slot

P110
PKG_TYPE=FCI71240-340CA

101	GND_CB01	CARDBUSA_CAD0	
102	AD0_CB02	CARDBUSA_CAD1	
103	AD1_CB03	CARDBUSA_CAD2	
104	PBGND1		
105	AD3_CB04	CARDBUSA_CAD3	
106	AD5_CB05	CARDBUSA_CAD5	
107	PBGND2		
108	AD7_CB06	CARDBUSA_CAD7	
109	CBE0#_CB07	CARDBUSA_CCBE0	
110	PBGND3		
111	AD9_CB08	CARDBUSA_CAD9	
112	AD11_CB09	CARDBUSA_CAD11	
113	PBGND4		
114	AD12_CB10	CARDBUSA_CAD12	
115	AD14_CB11	CARDBUSA_CAD14	
116	PBGND5		
117	CBE1#_CB12	CARDBUSA_CCBE1	
118	PAR_CB13	CARDBUSA_CPAR	
119	PBGND6		
120	PERR#_CB14	CARDBUSA_CPERR	
121	GNT#_CB15	CARDBUSA_CGNT	
122	PBGND7		
123	INT#_CB16	CARDBUSA_CINT	
124	VCC_CB17	CARDBUSA_CVCC	
125	PBGND8		
126	PBGND9		
127	VPP1_CB18	CARDBUSA_CVPP	
128	CLK_CB19	CARDBUSA_CCLK	
129	PBGND10		
130	IRDY#_CB20	CARDBUSA_CIRDY	
131	CBE2#_CB21	CARDBUSA_CCBE2	
132	PBGND11		
133	AD18_CB22	CARDBUSA_CAD18	
134	AD20_CB23	CARDBUSA_CAD20	
135	PBGND12		
136	AD21_CB24	CARDBUSA_CAD21	
137	AD22_CB25	CARDBUSA_CAD22	
138	PBGND13		
139	AD23_CB26	CARDBUSA_CAD23	
140	AD24_CB27	CARDBUSA_CAD24	
141	PBGND14		
142	AD25_CB28	CARDBUSA_CAD25	
143	AD26_CB29	CARDBUSA_CAD26	
144	PBGND15		
145	AD27_CB30	CARDBUSA_CAD27	
146	AD29_CB31	CARDBUSA_CAD29	
147	PBGND16		
148	D2_RSRVD_CB32	CARDBUSA_RSV_D2	
149	CLKRUN#_CB33	CARDBUSA_CCLKRUN	
150	GND_CB34		
200	SHIELD205		
207	SHIELD207		

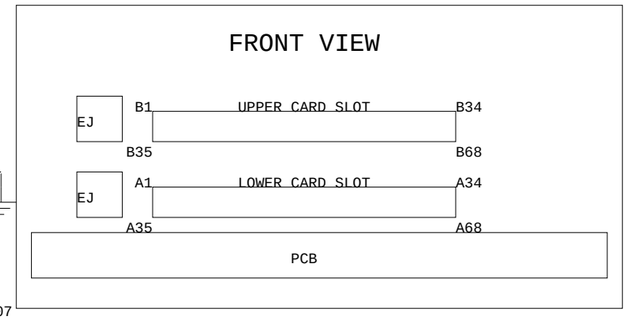
51	CA35_GND	CARDBUSB_CCD0	
52	CA36_CD1#	CARDBUSB_CCD1	
53	CA37_AD2	CARDBUSB_CAD2	
54	PAGND17		
55	CA38_AD4	CARDBUSB_CAD4	
56	CA39_AD6	CARDBUSB_CAD6	
57	PAGND18		
58	CA40_RSRVD_D14	CARDBUSB_RSV_D14	
59	CA41_AD8	CARDBUSB_CAD8	
60	PAGND19		
61	CA42_AD10	CARDBUSB_CAD10	
62	CA43_VS1	CARDBUSB_CVS1	
63	PAGND20		
64	CA44_AD13	CARDBUSB_CAD13	
65	CA45_AD15	CARDBUSB_CAD15	
66	PAGND21		
67	CA46_AD16	CARDBUSB_CAD16	
68	CA47_RSRVD_A18	CARDBUSB_RSV_A18	
69	PAGND22		
70	CA48_BLOCK#	CARDBUSB_CBLOCK	
71	CA49_STOP#	CARDBUSB_CSTOP	
72	PAGND23		
73	CA50_DEVSEL#	CARDBUSB_CDEVSEL	
74	CA51_VCC	CARDBUSB_CVCC	
75	PAGND24		
76	PAGND25		
77	CA52_VPP2	CARDBUSB_CVPP	
78	CA53_TRDY#	CARDBUSB_CTRDY	
79	PAGND26		
80	CA54_FRAME#	CARDBUSB_CFRAME	
81	CA55_AD17	CARDBUSB_CAD17	
82	PAGND27		
83	CA56_AD19	CARDBUSB_CAD19	
84	CA57_VS2	CARDBUSB_CVS2	
85	PAGND28		
86	CA58_RST#	CARDBUSB_CRST	
87	CA59_SERR#	CARDBUSB_CSERR	
88	PAGND29		
89	CA60_REQ#	CARDBUSB_CREQ	
90	CA61_CAE3#	CARDBUSB_CCBE3	
91	PAGND30		
92	CA62_AUDIO	CARDBUSB_CAUDIO	
93	CA63_STSCHG	CARDBUSB_CSTSCHG	
94	PAGND31		
95	CA64_AD28	CARDBUSB_CAD28	
96	CA65_AD30	CARDBUSB_CAD30	
97	PAGND32		
98	CA66_AD31	CARDBUSB_CAD31	
99	CA67_CD2#	CARDBUSB_CCD2	
100	CA68_GND		
205	SHIELD205		
208	SHIELD208		

151	CB35_GND	CARDBUSA_CCD0	
152	CB36_CD1#	CARDBUSA_CCD1	
153	CB37_AD2	CARDBUSA_CAD2	
154	PBGND17		
155	CB38_AD4	CARDBUSA_CAD4	
156	CB39_AD6	CARDBUSA_CAD6	
157	PBGND18		
158	CB40_RSRVD_D14	CARDBUSA_RSV_D14	
159	CB41_AD8	CARDBUSA_CAD8	
160	PBGND19		
161	CB42_AD10	CARDBUSA_CAD10	
162	CB43_VS1	CARDBUSA_CVS1	
163	PBGND20		
164	CB44_AD13	CARDBUSA_CAD13	
165	CB45_AD15	CARDBUSA_CAD15	
166	PBGND21		
167	CB46_AD16	CARDBUSA_CAD16	
168	CB47_RSRVD_A18	CARDBUSA_RSV_A18	
169	PBGND22		
170	CB48_BLOCK#	CARDBUSA_CBLOCK	
171	CB49_STOP#	CARDBUSA_CSTOP	
172	PBGND23		
173	CB50_DEVSEL#	CARDBUSA_CDEVSEL	
174	CB51_VCC	CARDBUSA_CVCC	
175	PBGND24		
176	PBGND25		
177	CB52_VPP2	CARDBUSA_CVPP	
178	CB53_TRDY#	CARDBUSA_CTRDY	
179	PBGND26		
180	CB54_FRAME#	CARDBUSA_CFRAME	
181	CB55_AD17	CARDBUSA_CAD17	
182	PBGND27		
183	CB56_AD19	CARDBUSA_CAD19	
184	CB57_VS2	CARDBUSA_CVS2	
185	PBGND28		
186	CB58_RST#	CARDBUSA_CRST	
187	CB59_SERR#	CARDBUSA_CSERR	
188	PBGND29		
189	CB60_REQ#	CARDBUSA_CREQ	
190	CB61_CBE3#	CARDBUSA_CCBE3	
191	PBGND30		
192	CB62_AUDIO	CARDBUSA_CAUDIO	
193	CB63_STSCHG	CARDBUSA_CSTSCHG	
194	PBGND31		
195	CB64_AD28	CARDBUSA_CAD28	
196	CB65_AD30	CARDBUSA_CAD30	
197	PBGND32		
198	CB66_AD31	CARDBUSA_CAD31	
199	CB67_CD2#	CARDBUSA_CCD2	
200	CB68_GND		
205	SHIELD206		
208	SHIELD208		

CARDBUS_SHIELD

FB601
1000_OHM
IND_BLM21A

CARDBUS_SHIELD



Notes:
1. Power Supply for CardBus found on page 53.

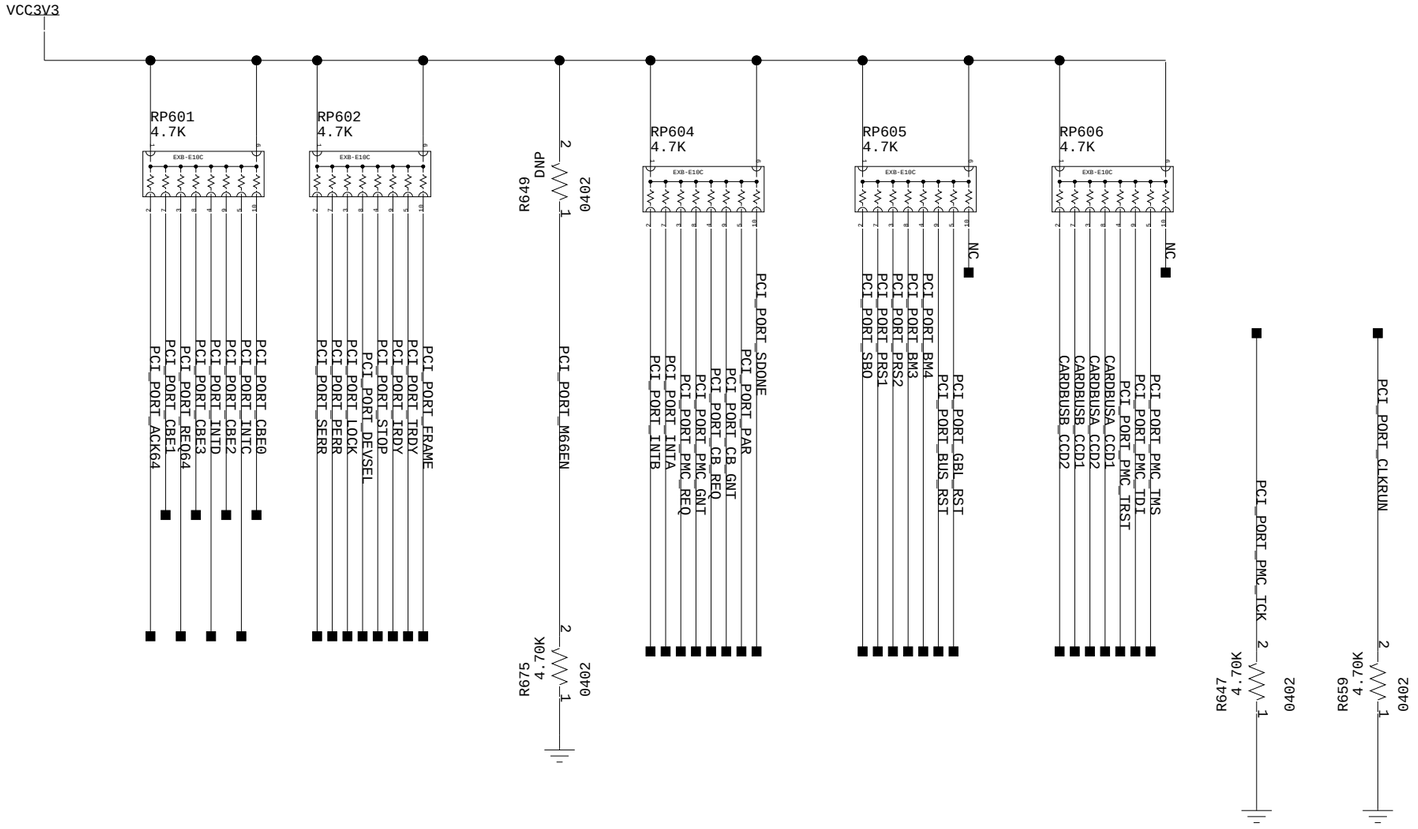
ML300 CPU
PCI Bridge
Cardbus Conn

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
CardBus Connectors

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 51 of 55	Drawn By BP/GB



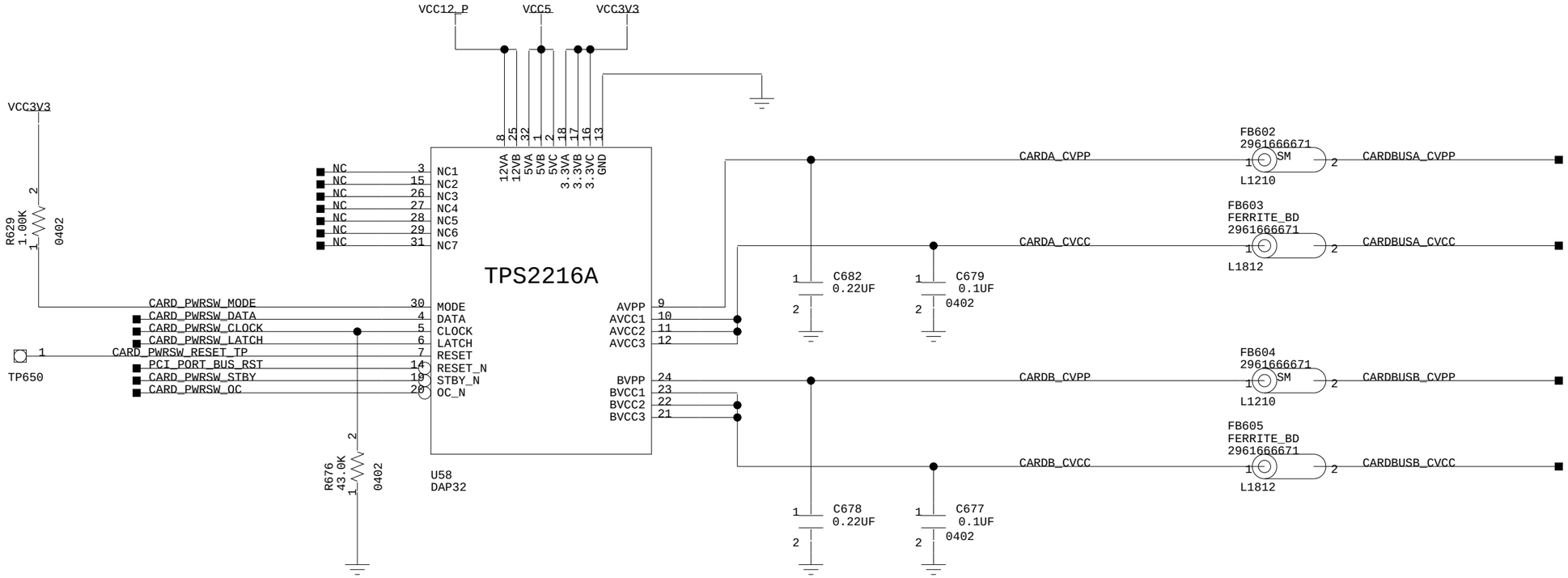
ML300 CPU

PCI Termination

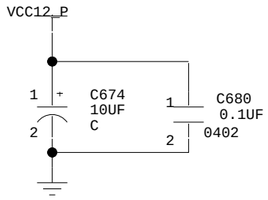
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

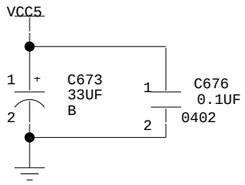
Title: ML300_CPU PCI Termination	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 52 of 56	Drawn By BP



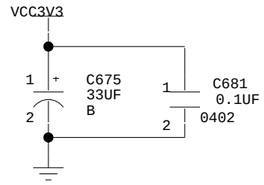
Place Near 12VX of U58



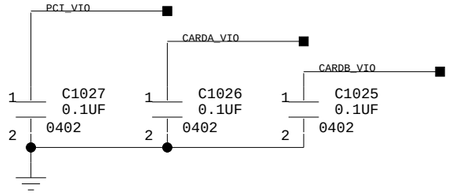
Place Near 5VX of U58



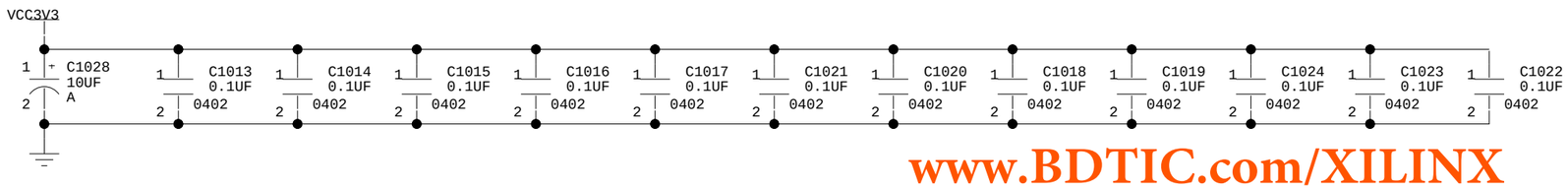
Place Near 3.3VX of U58



Place Near VCCIO PCI pins on U601



Place Near VCC Pins of U601



ML300 CPU
Power Supply

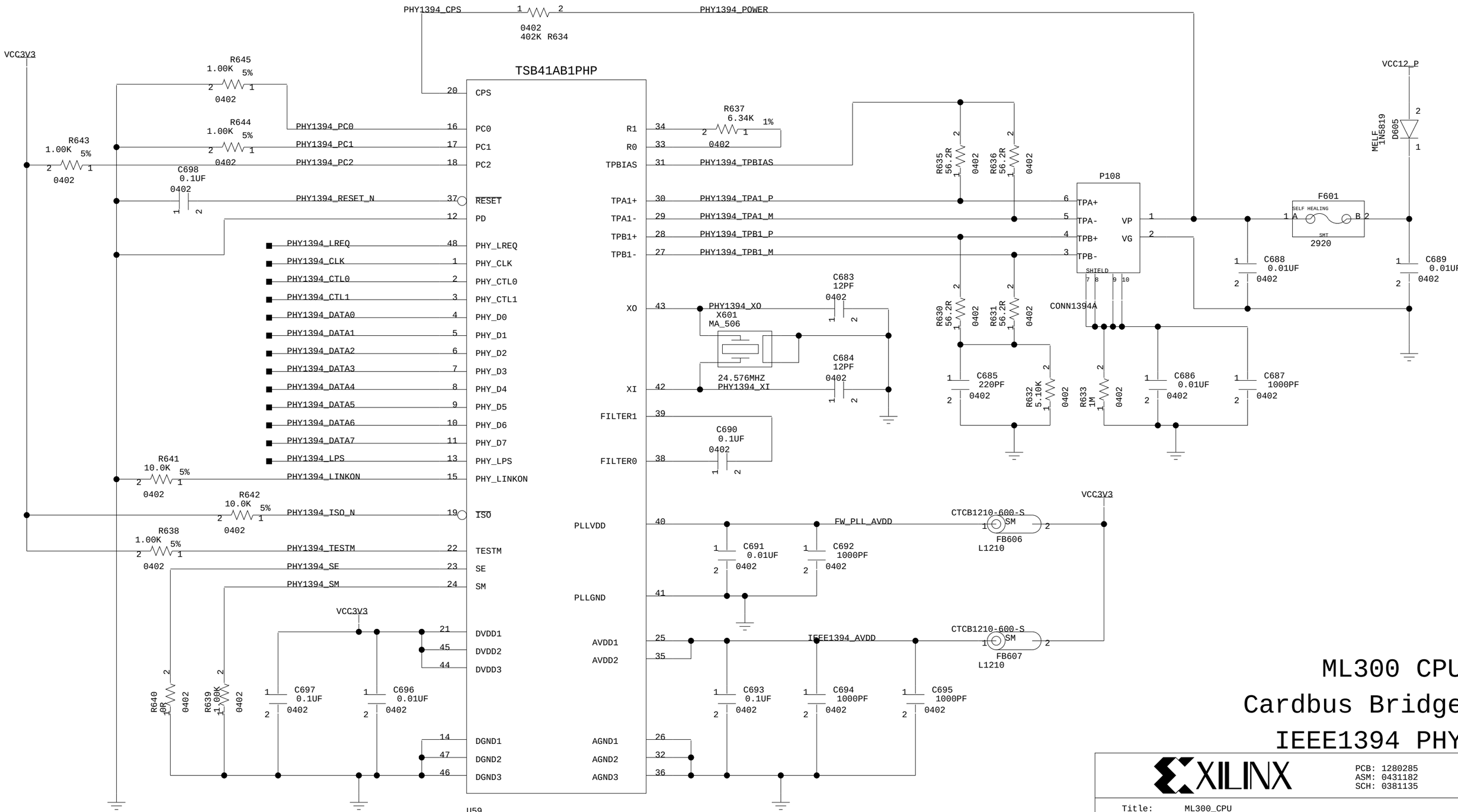
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

CardBus Power Supply

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 53 of 55	Drawn By BP



ML300 CPU
Cardbus Bridge
IEEE1394 PHY

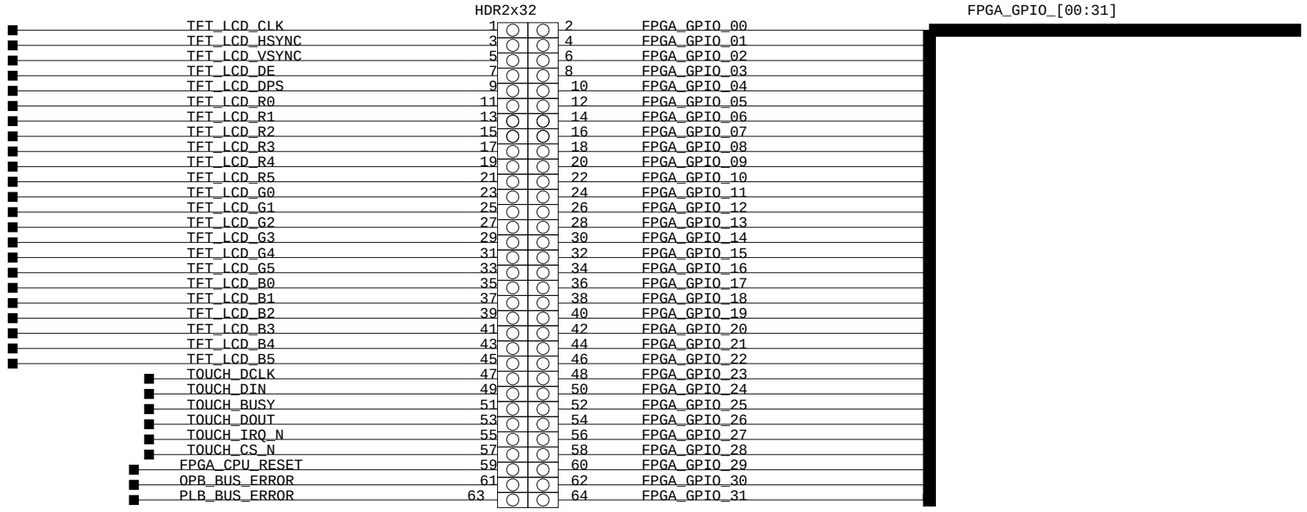
XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

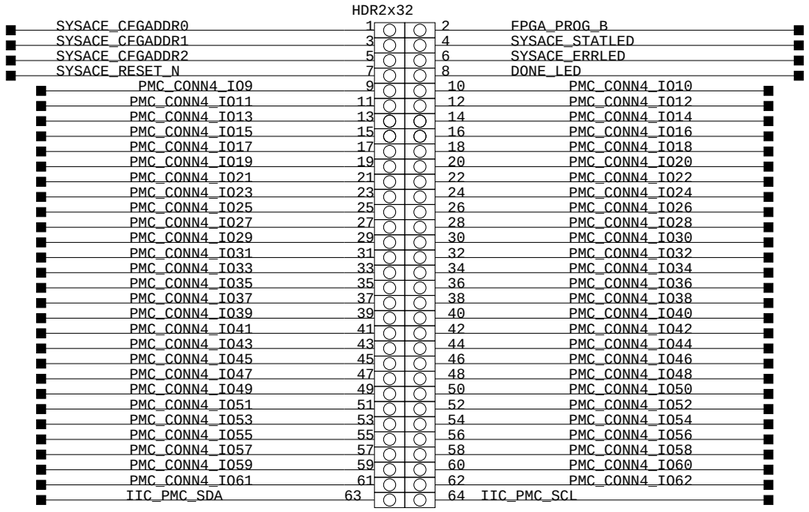
Title: ML300_CPU
IEEE1394 (FireWire) PHY

Date: October 17th, 2002 | Ver: 1.00
Sheet Size: B | Rev: A
Sheet 54 of 55 | Drawn By GB

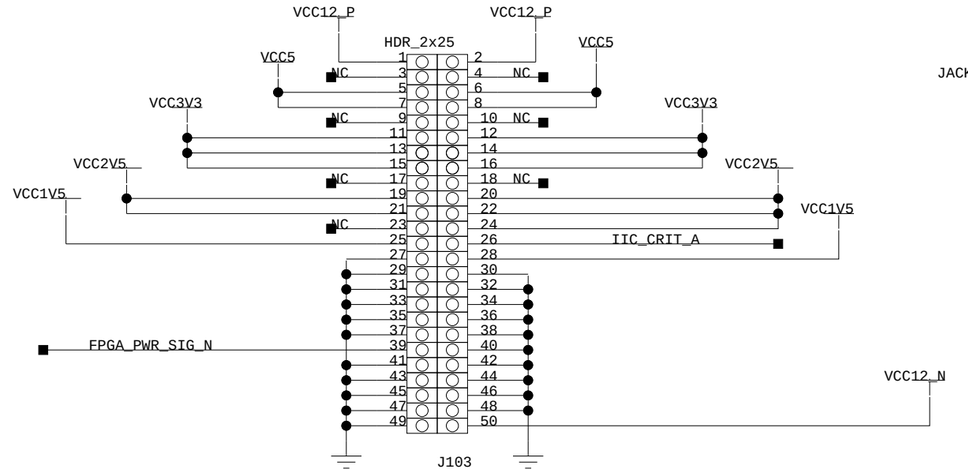
Silkscreen:
"Digital Conn 1"

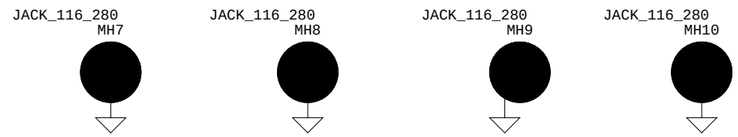


Silkscreen:
"Digital Conn 2"



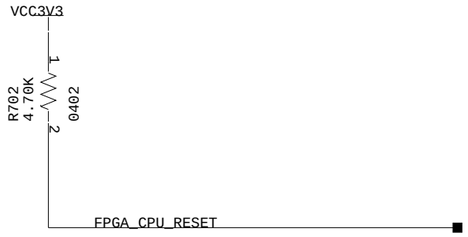
Silkscreen:
"Power Conn"



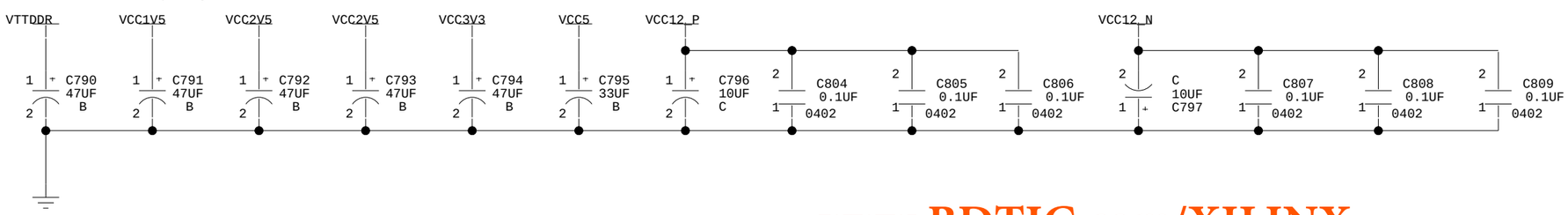


Powerboard Mounting Holes

Fabrication Fiducials
Three per Side



Place Caps adjacent to J702



ML300 CPU
Mezz Connector

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU

Mezzanine Power and I/O Connectors

Date: October 17th, 2002	Ver: 1.00
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Sheet 55 of 55	Drawn By BP

		Net Class Routing Rules			
1	NET_CLASS	DDR_CNTL_FPGA + DDR_CNTL_RES	< 6000 mils	thru resistors	+ ignore tracelength to termination resistor
		Route Order U1 - U15 through (RP362,RP363). Termination Resistor(RP329,RP331) not part of overall length.			
2	NET_CLASS	DDR_CNTL_REG + DDR_CNTL_MEM	< 4500 mils	thru resistors	+ ignore tracelength to termination resistor
		Route Order U15 - U9,U8,U7,U6 through (RP308,RP311). Termination Resistor(RP336) not part of overall length.			
3	NET_CLASS	DDR_ADDR_FPGA + DDR_ADDR_RES	< 6000 mils	thru resistors	+ ignore tracelength to termination resistor
		Route Order U1 - U14 through (RP359,RP360,RP361,RP362). Termination Resistor(RP330,RP331) not part of overall length.			
4	NET_CLASS	DDR_ADDR_REG + DDR_ADDR_MEM	< 4500 mils	thru resistors	+ ignore tracelength to termination resistor
		Route Order U14 - U6,U7,U8,U9 through (RP302,RP303,RP304,RP311). Termination Resistor(RP338,RP339) not part of overall length.			
5	NET_CLASS	DDR_DQS_FPGA + DDR_DQS_RES + DDR_DQS_MEM	< 3300 mils	thru resistors	+ ignore tracelength to termination resistor
		Route Order U1 - U6,U7,U8,U9 through (RP326,RP324,R311-R314). Termination resistor (RP340,RP341,R315-R318) not part of overall length.			
6	NET_CLASS	DDR_DATA_FPGA + DDR_DATA_RES + DDR_DATA_MEM	< 3750 mils	thru resistors	+ ignore tracelength to termination resistor
		Route Order U1 - U6,U7,U8,U9 through (RP315-RP322 and RP347,RP348,RP350,RP351,RP353,RP354,RP356,RP357).			
		Termination resistor (RP349,RP352,RP355,RP358,RP603,RP346,RP344,RP345) not part of overall length.			
7	NET_CLASS	DDR_CLK_FPGA + DDR_CLK_RES	Matched lengths +/- 6 mil		+ ignore tracelength to termination resistor
		Route Order U1 - U16 through (R307, R308). Termination resistor (R302,R303,R309) not part of overall length.			
		DDR_CLK_*** PT 1: Route Order U1.U21 through resistor R308 to U16.13 (ignore tracelength to term R302)			
		DDR_CLK_*** PT 2: Toute Order U1.U21 through resistor R308 back to U1.AC14 (ignore tracelength to R309).			
		DDR_CLK_***_N PT 1: Route Order U1.U22 through resistor R307 to U16.14 (ignore tracelength to term R303).			
		DDR_CLK_***_N PT 2: Route Order U1.U22 through resistor R307 to C366 (ignore tracelength to R310).			
8	NET_CLASS	DDR_CLK_PLL + DDR_CLK_MEM	Matched lengths +/- 60 mils	thru resistors	+ ignore tracelength to term res
		Route Order U16 - U6,U7,U8,U9 through (RP328,RP327,RP325). Term resistor (RP340,RP341,RP330,RP331,RP329) not part of overall length			
9	NET_CLASS	CLK_27MHZ_FPGA + CLK_27MHZ_COMP	Matched length +/- 60 mil	thru resistors	
		Route Order U1 - U601,J104 through (R1007,R108).			
		U1 to U601 through R1007			
		U1 to J104 through R108			
10A	NET_CLASS	ENET_PHY	Matched Length +/- 1000 mil		
10B	NET_CLASS	ENET_PHY_COMP	Tight		Tight
11	NET_CLASS	PS2_1	No Issues		
12	NET_CLASS	PS2_2	No Issues		
13	NET_CLASS	CPU_DEBUG	Matched Length +/- 1250 mil		Tight
		Route Order U1 - P14, P109.			
14	NET_CLASS	CPU_TRACE	Matched Length +/- 50 mil		Tight
15	NET_CLASS	SYSACE_FLASH	Tight		Tight
16	NET_CLASS	SYSACE_MPU	Tight		Tight
17A	NET_CLASS	SYSACE_JTAG_2V5	Tight		Tight
17B	NET_CLASS	SYSACE_JTAG_3V3	Tight		Tight
18	Deleted to remove redundancy				
19	NET_CLASS	TFT_CNTL_FPGA	Tight		These go from the FPGA to a level shifter
20	NET_CLASS	TFT_CNTL_LCD	Tight		These go from level shifter to TFT conn to PWRIO
21	NET_CLASS	TFT_CLR_FPGA	Tight		These go from the FPGA to a level shifter
22	NET_CLASS	TFT_CLR_LCD	Tight		These go from level shifter to TFT conn to PWRIO
23	NET_CLASS	PCI_FPGA_CONN	Tight		These go from the FPGA to clamp diodes
24	NET_CLASS	PCI_PORT_CONN	Tight		These go from clamp diodes to the PMC and PCI4451
		Route Order U50,U51,U52,U53 - J104,J105, U601. Term Res (RP601, RP602, RP604, RP605, RP606 R649, R675, R647, R659) not part of length.			
25	NET_CLASS	CARDBUSA	Tight		these go from the PCI4451 to the Cardbus connectors
26	NET_CLASS	CARDBUSB	Tight		these go from the PCI4451 to the Cardbus connectors
27	NET_CLASS	AUDIO_DIG_FPGA	Tight		these go from the FPGA to the clamp Diodes
28	NET_CLASS	AUDIO_DIG_PMC	Tight		These go from the clamp diodes to conn and res pack
29	NET_CLASS	AUDIO_DIG_COMP	Tight		These go from the resistor pack to the AD1885 comp
30	NET_CLASS	PMC_FPGA_CONN4	Tight		These go from the FPGA to clamp diodes
31	NET_CLASS	PMC_PMC_CONN4	Tight		These go from clamp diodes to PMC4 and PWRIO conn
		Route Order U802,U912,U913,U914 - J106, J102			
32	NET_CLASS	IIC_FPGA	no Issues		These go from the FPGA to clamp diodes
33	NET_CLASS	IIC_PMC	no Issues		These go from clamp diodes to the IIC and conn
34	NET_CLASS	DDR_DM_FPGA + DDR_DM_MEM	< 4500 mils	thru resistors	+ ignore tracelength to termination resistor
		Route Order U1 - U6,U7,U8,U9 through (RP326,RP324). Termination resistor (RP340,RP341) not part of overall length.			

ML300 CPU
Net Classes

XILINX

PCB: 1280285
ASM: 0431182
SCH: 0381135

Title: ML300_CPU
Net Classes

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
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