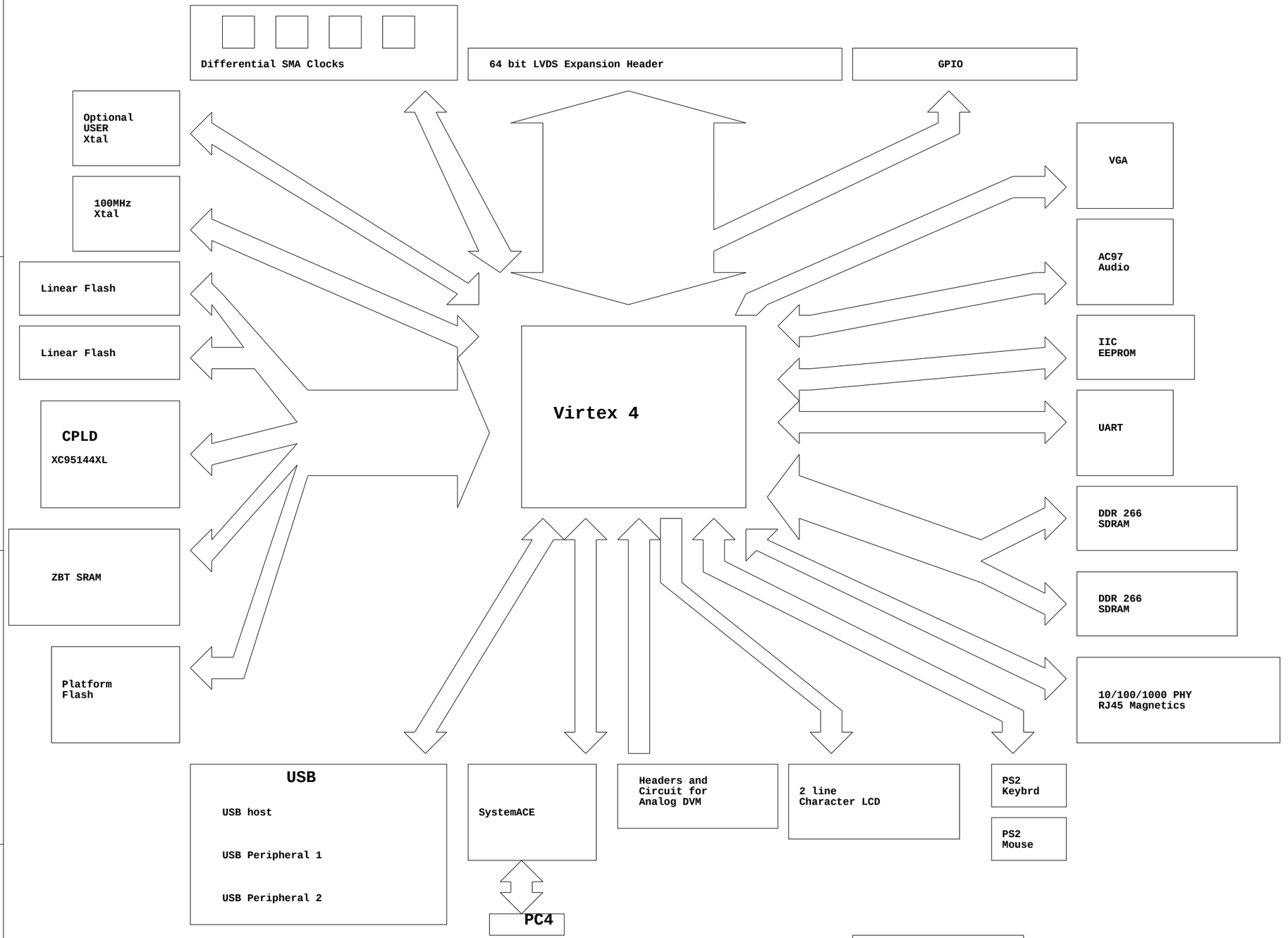
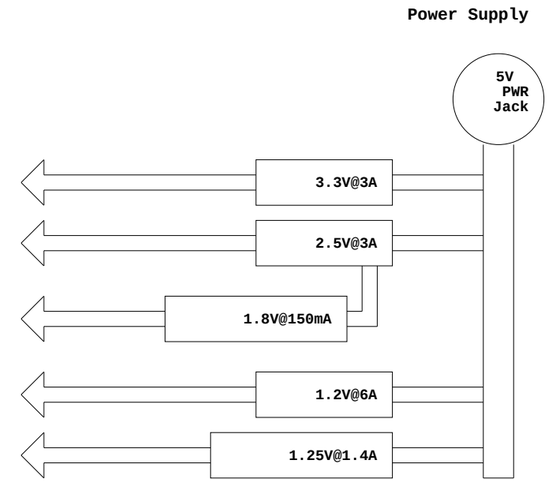
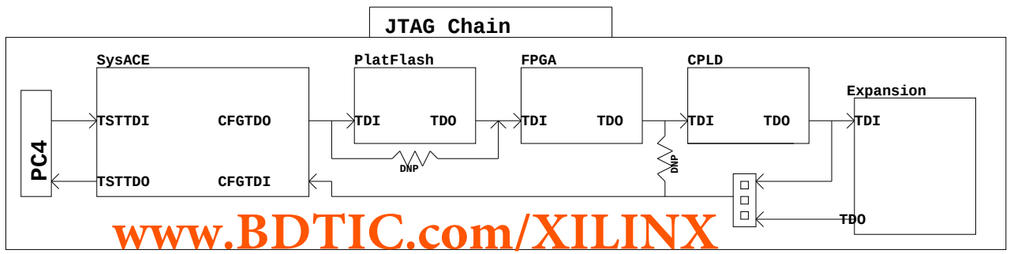




Compatibility and Available IOs

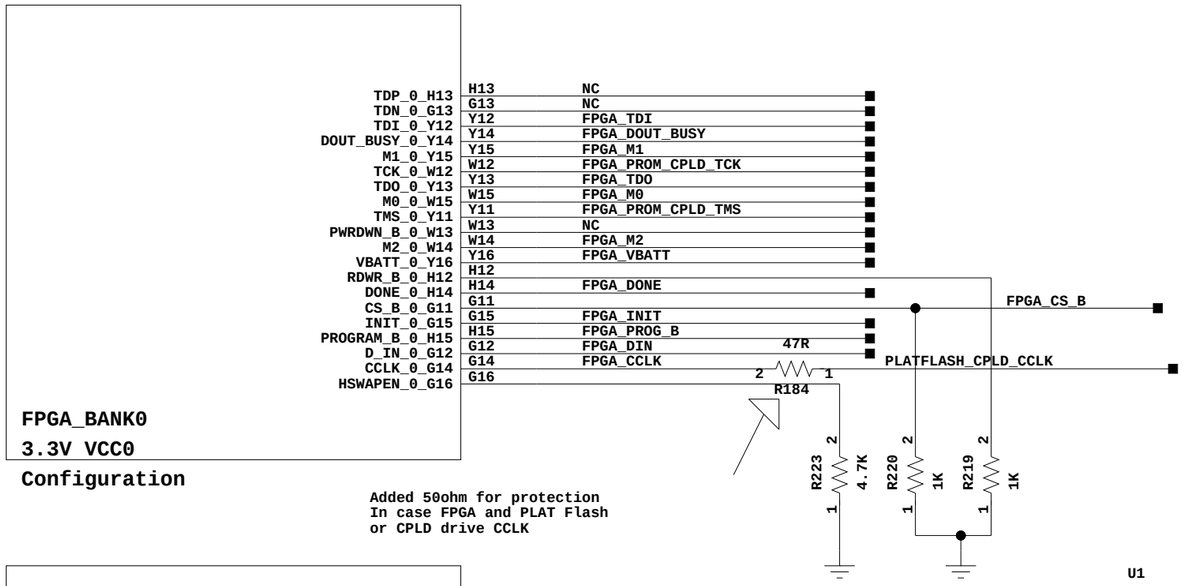
FPGA Device	Banks
LX15, FX12, SX25	8 Banks 320 User IOs
LX25, LX40, LX60 SX35	10 Banks up to 448 User IOs

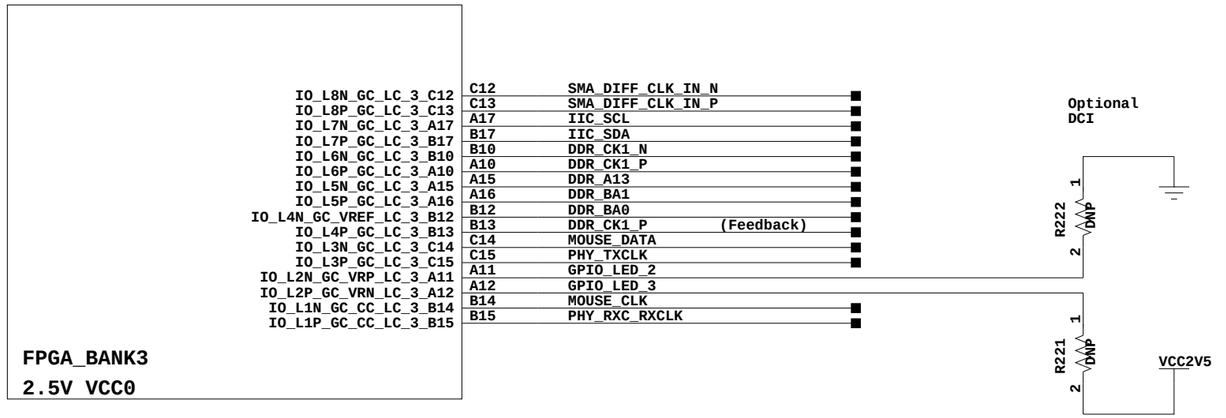


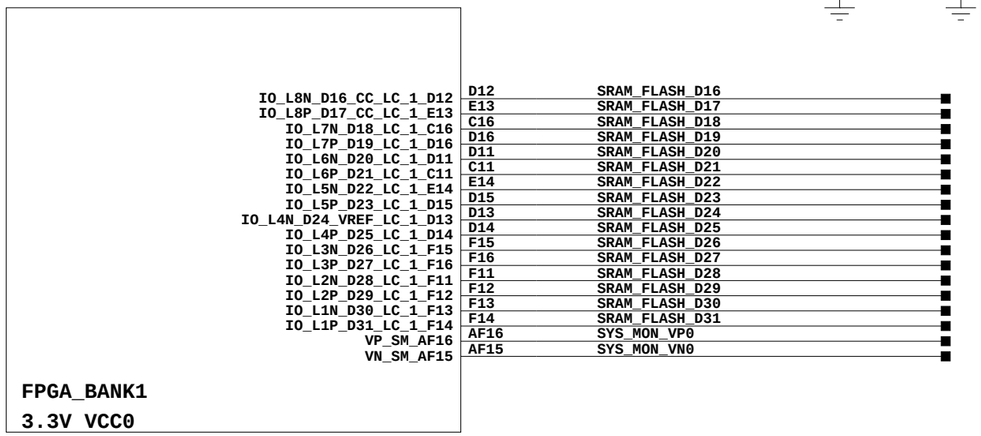
XILINX

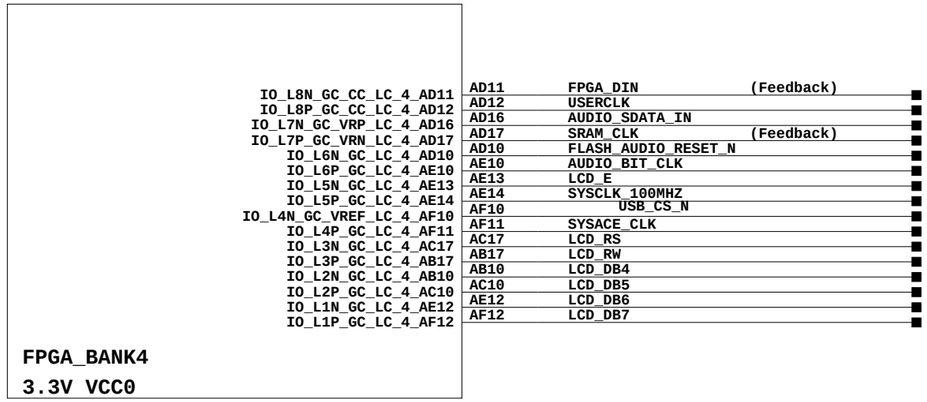
Title: ML401/2/3 Block Diagram

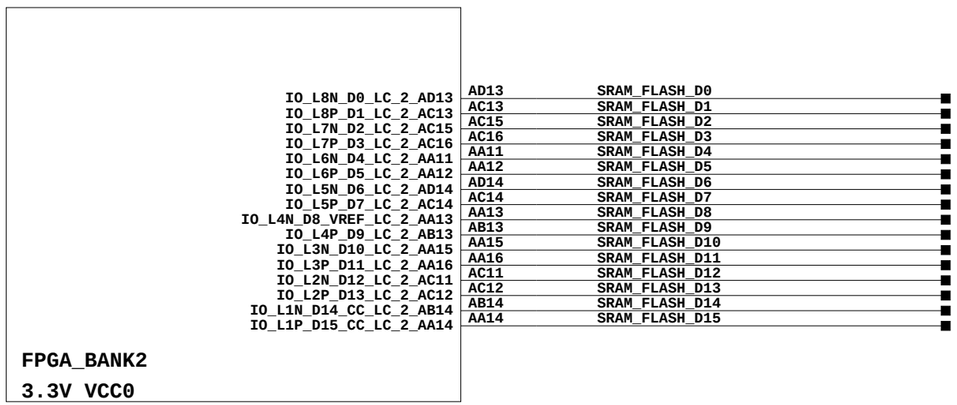
Date: 8/19/2004	Ver: 1.0
Sheet Size: B	Rev: B
Sheet 1 of 24	Drawn By BF







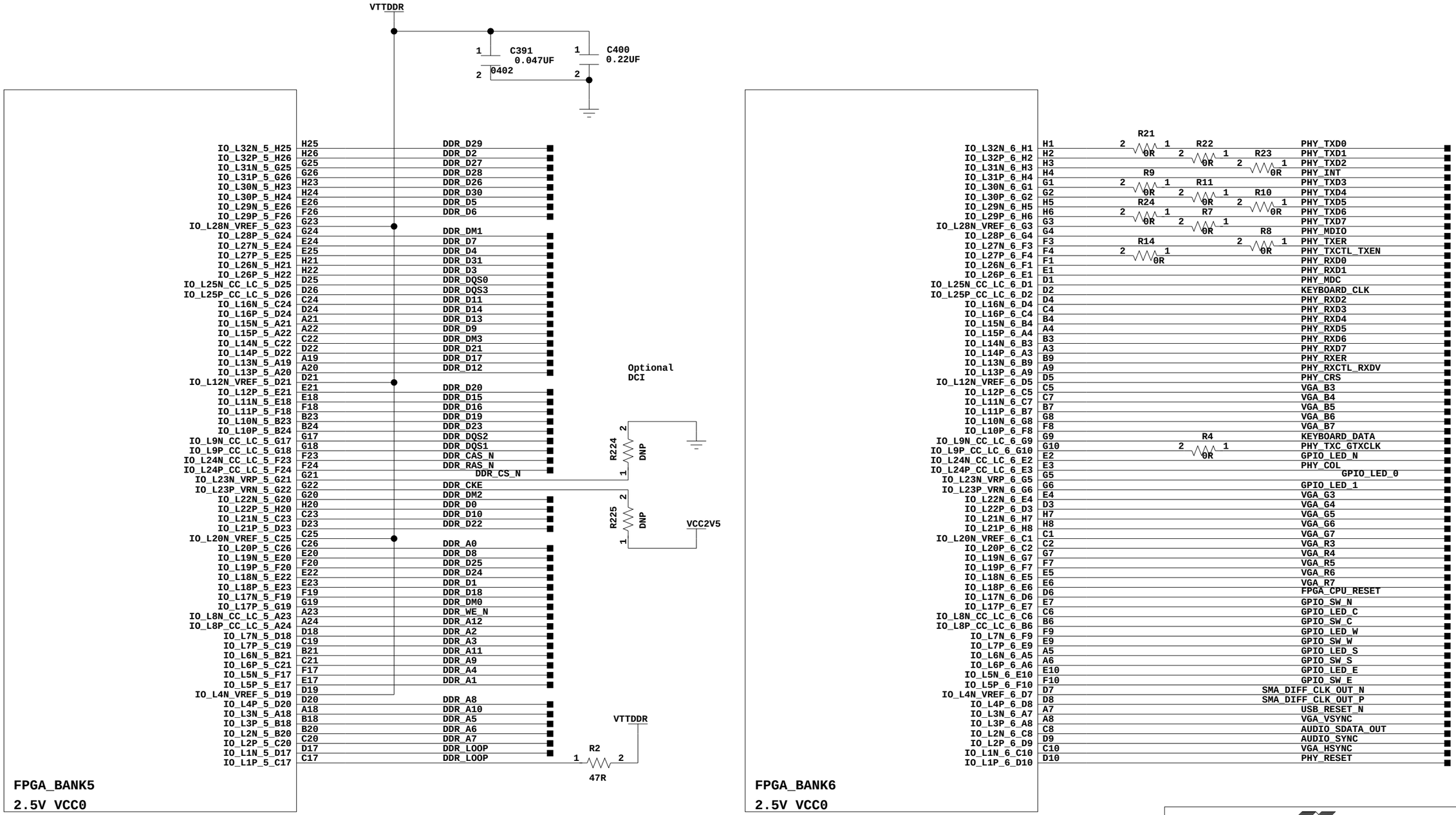




XILINX

Title: FPGA Banks 0,1,2,3,4

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 2 of 24	Drawn By BF



XILINX

Title: FPGA Bank 5, 6

Date:	Ver:
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Sheet 3 of 24	Drawn By BF

IO_L16N_7_AC24	AC24	HDR1_2
IO_L16P_7_AC23	AC23	HDR1_4
IO_L15N_7_AD23	AD23	HDR1_6
IO_L15P_7_AD22	AD22	HDR1_8
IO_L14N_7_AA23	AA23	HDR1_10
IO_L14P_7_AB23	AB23	HDR1_12
IO_L13N_7_AB22	AB22	HDR1_14
IO_L13P_7_AC22	AC22	HDR1_16
IO_L12N_VREF_7_Y23	Y23	HDR2_6
IO_L12P_7_Y22	Y22	HDR2_8
IO_L11N_7_AD26	AD26	HDR1_18
IO_L11P_7_AD25	AD25	HDR1_20
IO_L10N_7_AA26	AA26	HDR1_22
IO_L10P_7_AB26	AB26	HDR1_24
IO_L9N_CC_LC_7_AC26	AC26	HDR1_34
IO_L9P_CC_LC_7_AC25	AC25	HDR1_36
IO_L8N_CC_LC_7_Y24	Y24	HDR1_26
IO_L8P_CC_LC_7_AA24	AA24	HDR1_28
IO_L7N_7_AB25	AB25	HDR1_30
IO_L7P_7_AB24	AB24	HDR1_32
IO_L6N_7_Y26	Y26	HDR1_38
IO_L6P_7_Y25	Y25	HDR1_40
IO_L5N_7_V20	V20	HDR1_42
IO_L5P_7_W20	W20	HDR1_44
IO_L4N_VREF_7_W24	W24	HDR2_10
IO_L4P_7_W23	W23	HDR2_12
IO_L3N_7_W22	W22	HDR1_46
IO_L3P_7_W21	W21	HDR1_48
IO_L2N_7_W26	W26	HDR1_50
IO_L2P_7_W25	W25	HDR1_52
IO_L1N_7_V22	V22	HDR1_54
IO_L1P_7_V21	V21	HDR1_56
IO_L24N_CC_LC_7_AB21	AB21	HDR1_58
IO_L24P_CC_LC_7_AC21	AC21	HDR1_60
IO_L23N_VRP_7_AD20	AD20	HDR2_14
IO_L23P_VRN_7_AE20	AE20	HDR2_16
IO_L22N_7_AE24	AE24	HDR1_62
IO_L22P_7_AF24	AF24	HDR1_64
IO_L21N_7_Y18	Y18	HDR2_2
IO_L21P_7_AA18	AA18	HDR2_4
IO_L20N_VREF_7_Y21	Y21	HDR2_18
IO_L20P_7_Y20	Y20	HDR2_20
IO_L19N_7_AE23	AE23	HDR2_22
IO_L19P_7_AF23	AF23	HDR2_24
IO_L18N_7_W19	W19	HDR2_26
IO_L18P_7_Y19	Y19	HDR2_28
IO_L17N_7_AF20	AF20	HDR2_30
IO_L17P_7_AF19	AF19	HDR2_32
IO_L32N_SM7_7_AD21	AD21	HDR2_34_SYS_MON_VN7
IO_L32P_SM7_7_AE21	AE21	HDR2_36_SYS_MON_VP7
IO_L31N_SM6_7_AE18	AE18	HDR2_38_SYS_MON_VN6
IO_L31P_SM6_7_AF18	AF18	HDR2_40_SYS_MON_VP6
IO_L30N_SM5_7_AF22	AF22	HDR2_42_SYS_MON_VN5
IO_L30P_SM5_7_AF21	AF21	HDR2_44_SYS_MON_VP5
IO_L29N_SM4_7_AB18	AB18	HDR2_46_SYS_MON_VN4
IO_L29P_SM4_7_AC18	AC18	HDR2_48_SYS_MON_VP4
IO_L28N_VREF_7_AC20	AC20	HDR2_50
IO_L28P_7_AB20	AB20	HDR2_52
IO_L27N_SM3_7_AA17	AA17	HDR2_54_SYS_MON_VN3
IO_L27P_SM3_7_Y17	Y17	HDR2_56_SYS_MON_VP3
IO_L26N_SM2_7_AA20	AA20	HDR2_58_SYS_MON_VN2
IO_L26P_SM2_7_AA19	AA19	HDR2_60_SYS_MON_VP2
IO_L25N_CC_SM1_LC_7_AC19	AC19	HDR2_62_SYS_MON_VN1
IO_L25P_CC_SM1_LC_7_AD19	AD19	HDR2_64_SYS_MON_VP1

R289 2 DNP 1

R290 2 DNP 1 VCCO_7

FPGA_BANK7

3.3V or 2.5V VCC0

U1

IO_L16N_8_AD1	AD1	SRAM_FLASH_A7
IO_L16P_8_AD2	AD2	SRAM_FLASH_A8
IO_L15N_8_AE3	AE3	SRAM_FLASH_A9
IO_L15P_8_AF3	AF3	SRAM_FLASH_A10
IO_L14N_8_AC1	AC1	SRAM_FLASH_A5
IO_L14P_8_AC2	AC2	SRAM_FLASH_A6
IO_L13N_8_AB5	AB5	SRAM_FLASH_A19
IO_L13P_8_AC5	AC5	SRAM_FLASH_A20
IO_L12N_VREF_8_AB2	AB2	SRAM_FLASH_A4
IO_L12P_8_AB3	AB3	SRAM_FLASH_A16
IO_L11N_8_AB4	AB4	SRAM_FLASH_A17
IO_L11P_8_AC4	AC4	SRAM_FLASH_A18
IO_L10N_8_AA1	AA1	SRAM_FLASH_A2
IO_L10P_8_AB1	AB1	SRAM_FLASH_A3
IO_L9N_CC_LC_8_Y5	Y5	SRAM_BW1
IO_L9P_CC_LC_8_Y6	Y6	SRAM_BW0
IO_L8N_CC_LC_8_Y3	Y3	SRAM_BW3
IO_L8P_CC_LC_8_Y4	Y4	SRAM_BW2
IO_L7N_8_AA3	AA3	SRAM_FLASH_A14
IO_L7P_8_AA4	AA4	SRAM_FLASH_A15
IO_L6N_8_Y1	Y1	SRAM_FLASH_A0
IO_L6P_8_Y2	Y2	SRAM_FLASH_A1
IO_L5N_8_W5	W5	SRAM_FLASH_A13
IO_L5P_8_W6	W6	SRAM_FLASH_A12
IO_L4N_VREF_8_W3	W3	SRAM_FLASH_A11
IO_L4P_8_W4	W4	SRAM_ADV_LD_N
IO_L3N_8_V7	V7	SRAM_CE1_N
IO_L3P_8_W7	W7	FLASH_CE2
IO_L2N_8_V5	V5	USB_INT
IO_L2P_8_V6	V6	BUS_ERROR_1
IO_L1N_8_W1	W1	UART_SOUT
IO_L1P_8_W2	W2	UART_SIN
IO_L24N_CC_LC_8_AB6	AB6	SRAM_FLASH_WE_N
IO_L24P_CC_LC_8_AC6	AC6	SRAM_FLASH_OE_N
IO_L23N_VRP_8_AD7	AD7	
IO_L23P_VRN_8_AE7	AE7	
IO_L22N_8_AD4	AD4	SYSACE_MPIRQ
IO_L22P_8_AD5	AD5	SYSACE_MPCE
IO_L21N_8_Y9	Y9	SYSACE_MPA06
IO_L21P_8_AA9	AA9	SYSACE_MPA05
IO_L20N_VREF_8_Y7	Y7	SYSACE_MPA04
IO_L20P_8_AA7	AA7	SYSACE_USB_D15
IO_L19N_8_AF5	AF5	SYSACE_USB_D14
IO_L19P_8_AF6	AF6	SYSACE_USB_D13
IO_L18N_8_AC3	AC3	SYSACE_USB_D12
IO_L18P_8_AD3	AD3	SYSACE_USB_D11
IO_L17N_8_AE4	AE4	SYSACE_USB_D10
IO_L17P_8_AF4	AF4	SYSACE_USB_D9
IO_L32N_8_AC8	AC8	SYSACE_USB_D8
IO_L32P_8_AD8	AD8	SYSACE_USB_D7
IO_L31N_8_AE9	AE9	SYSACE_USB_D6
IO_L31P_8_AF9	AF9	SYSACE_USB_D5
IO_L30N_8_AD6	AD6	SYSACE_USB_D4
IO_L30P_8_AE6	AE6	SYSACE_USB_D3
IO_L29N_8_AB9	AB9	SYSACE_USB_D2
IO_L29P_8_AC9	AC9	SYSACE_USB_D1
IO_L28N_VREF_8_AB7	AB7	SYSACE_USB_D0
IO_L28P_8_AC7	AC7	SYSACE_MPA03
IO_L27N_8_AA10	AA10	SYSACE_A2_USB_A1
IO_L27P_8_Y10	Y10	SYSACE_A1_USB_A0
IO_L26N_8_Y8	Y8	SYSACE_MPWE_USB_WR_N
IO_L26P_8_AA8	AA8	SYSACE_MPOE_USB_RD_N
IO_L25N_CC_LC_8_AF7	AF7	SRAM_CLK
IO_L25P_CC_LC_8_AF8	AF8	VGA_CLK

FPGA_CCLK (Feedback)

R228 2 DNP 1

R165 2 49.9R 1

R166 2 49.9R 1 VCC3V3

Enable DCI

FPGA_BANK8

3.3V VCC0

U1

XILINX

Title: FPGA Bank 7, 8

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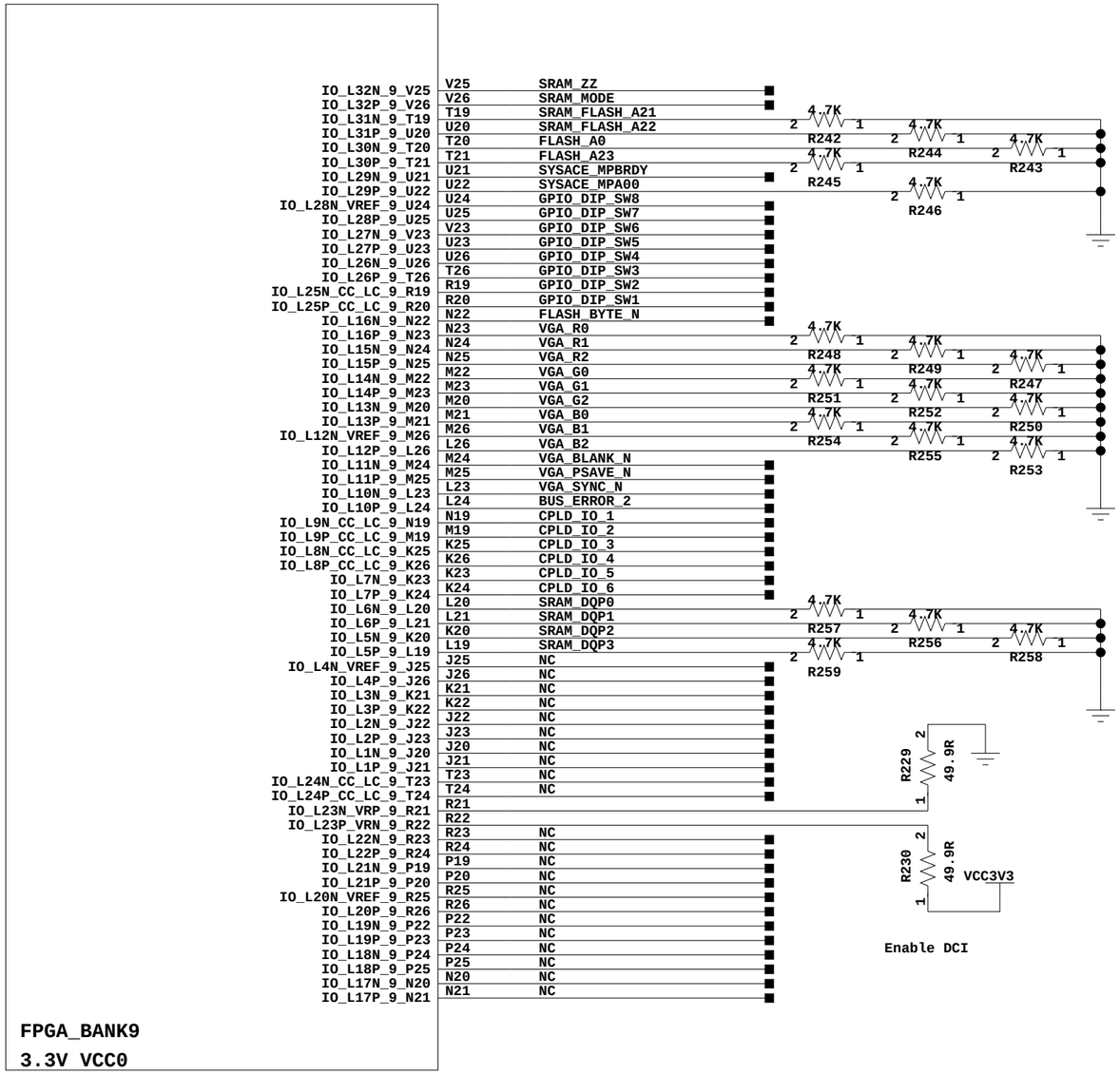

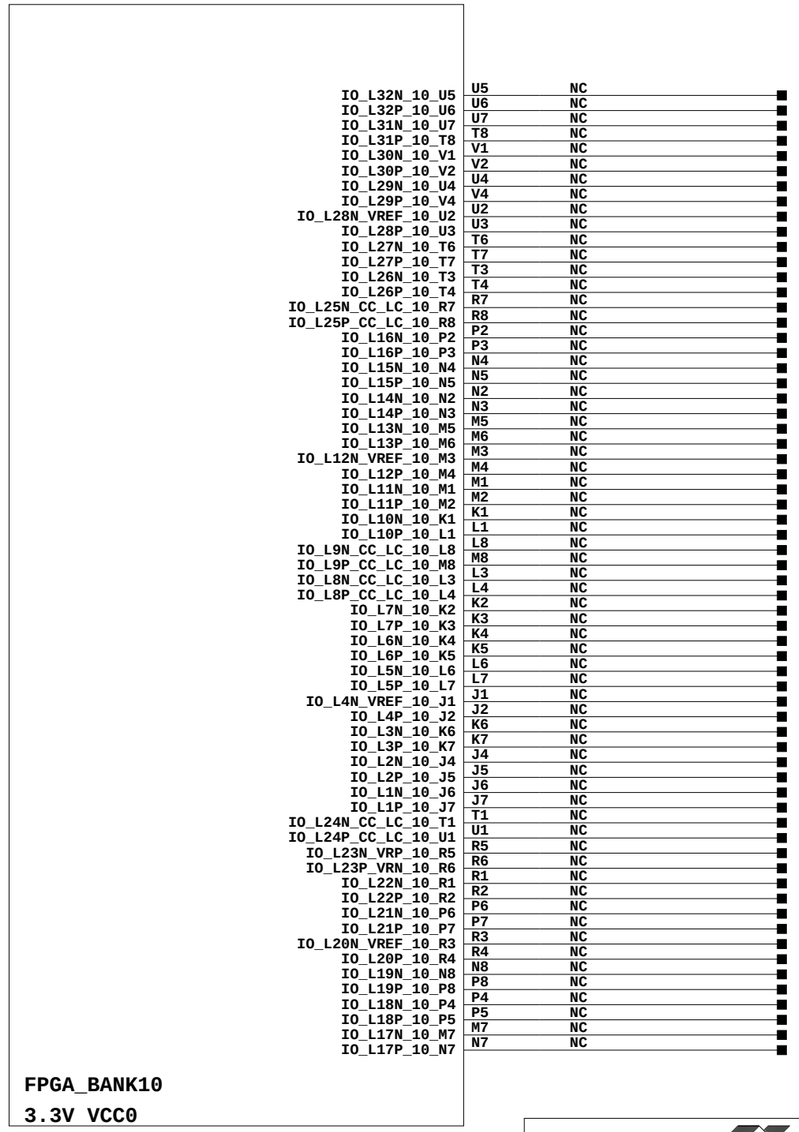

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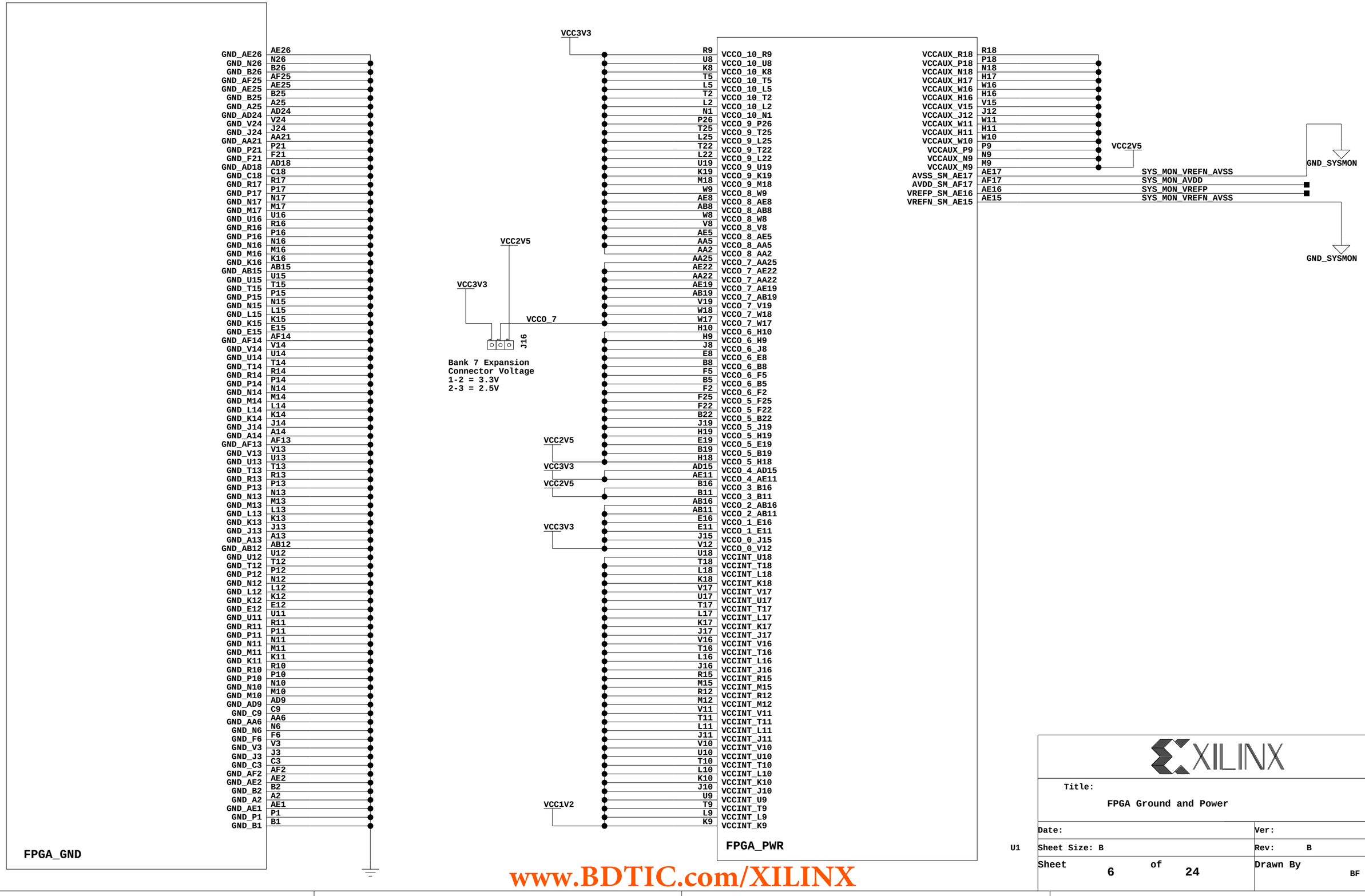
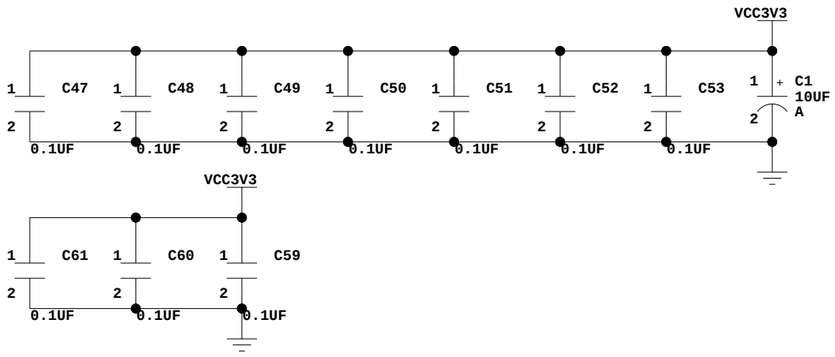
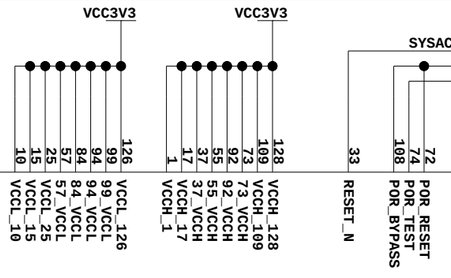
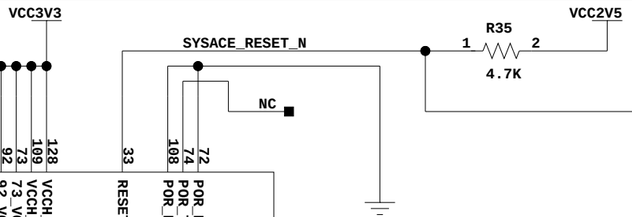
Title: FPGA Bank 9, 10

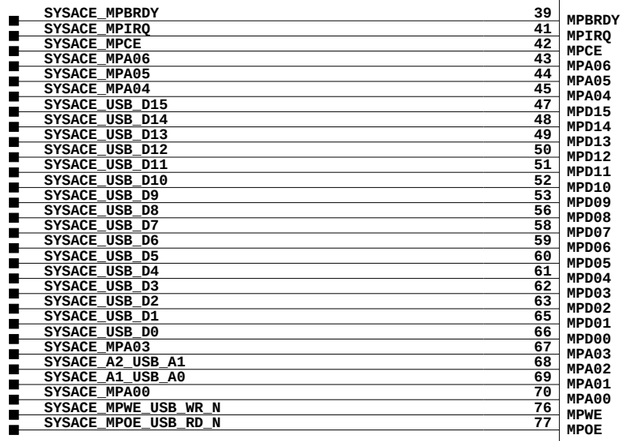
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 5 of 24	Drawn By BF











SYSTEMACE TQFP144 (DIE DOWN)

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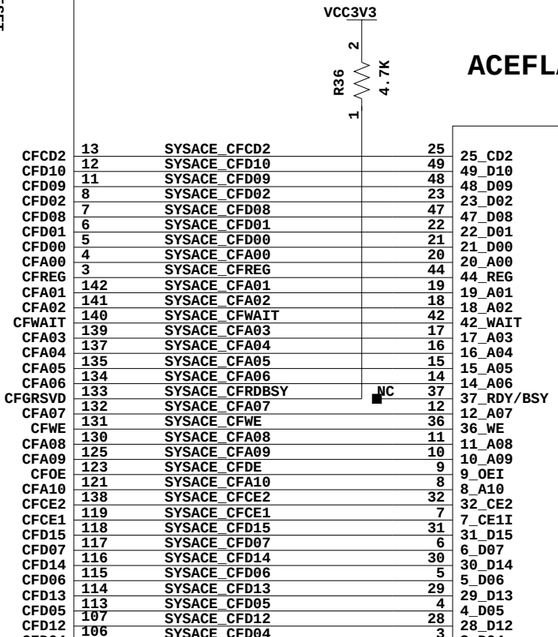
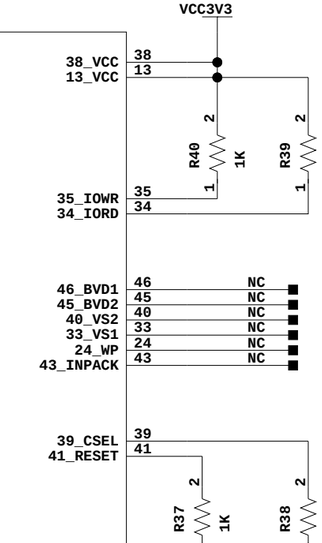
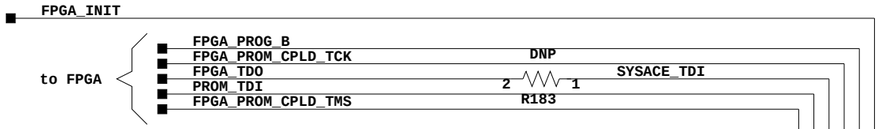
PKG_TYPE=TQ144
PARTS=1
LEVEL=STD

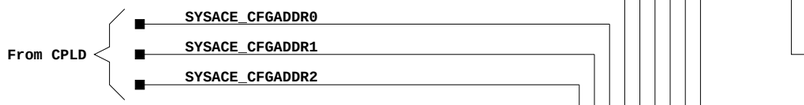
U2

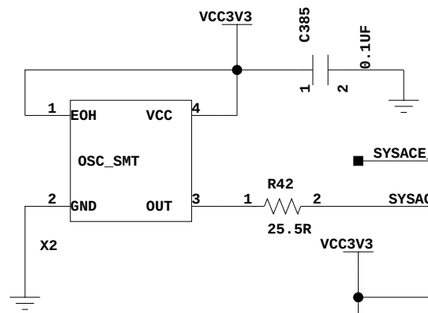


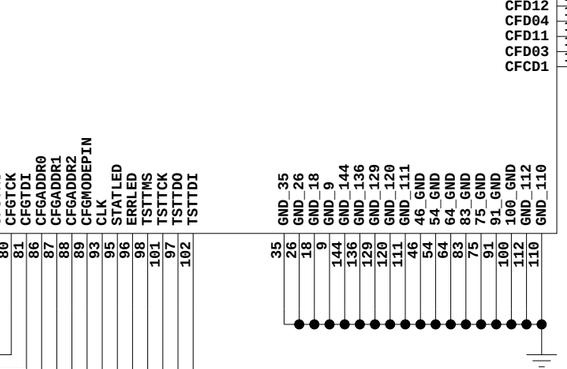
ACEFLASH

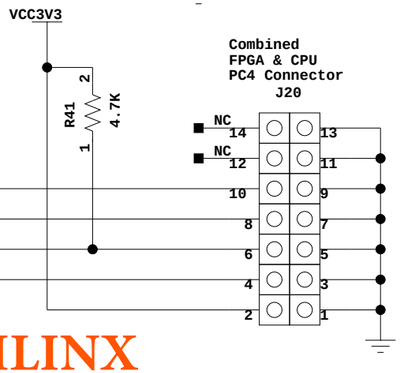


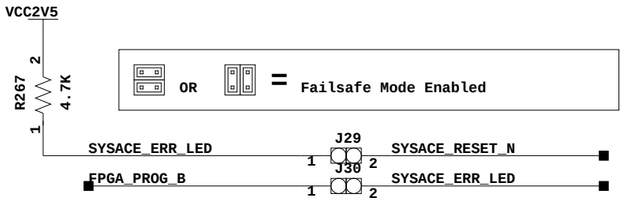












SysACE Failsafe Mode Jumpers

XILINX

Title: System ACE

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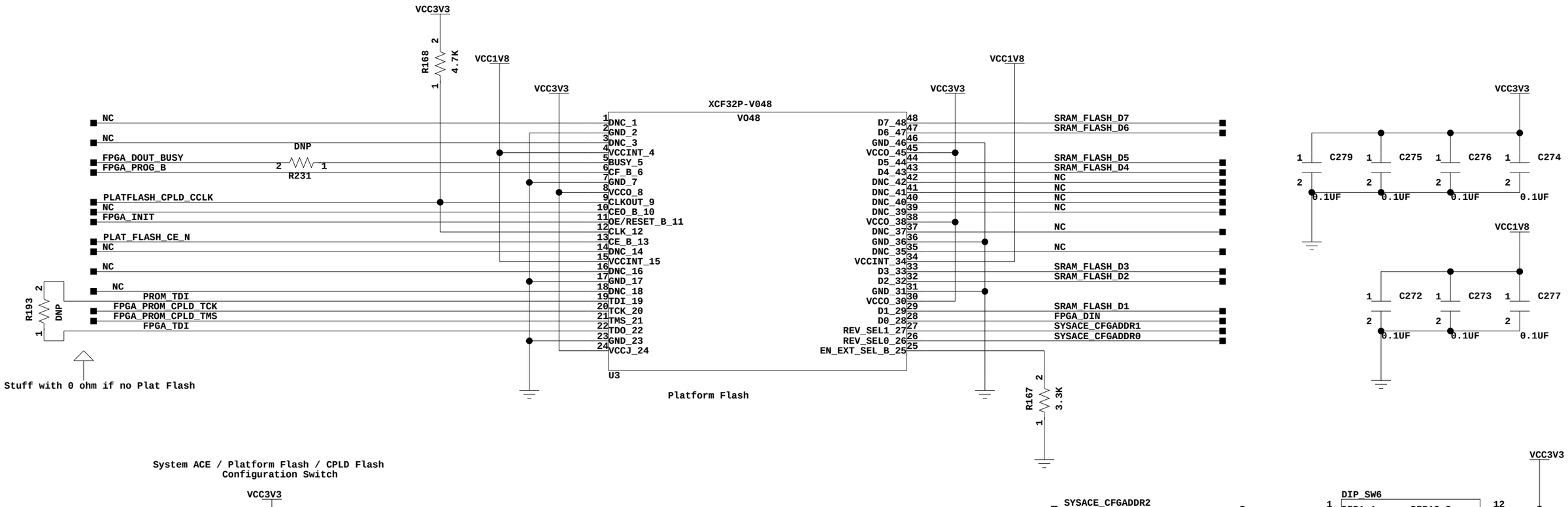
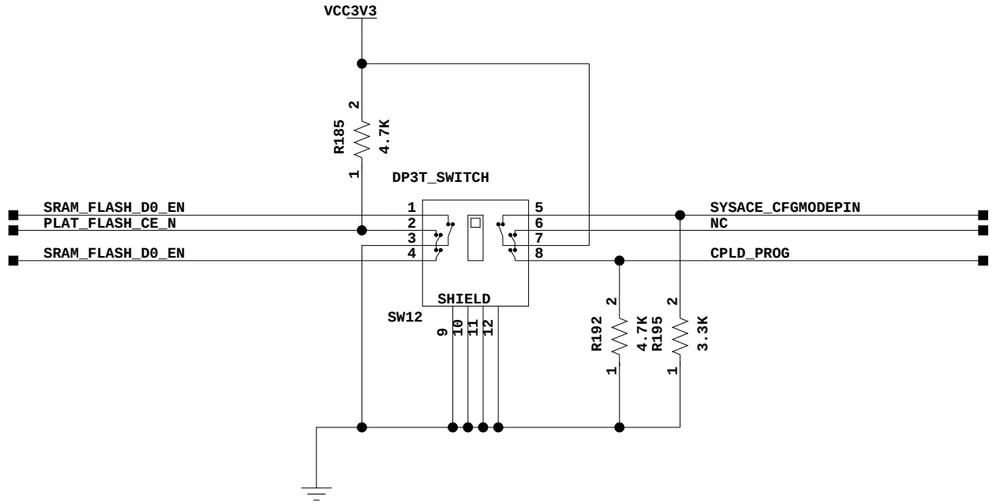
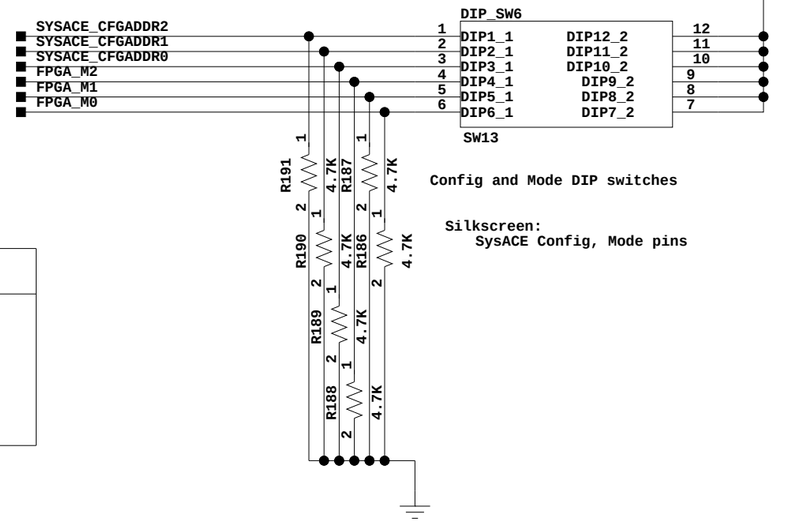


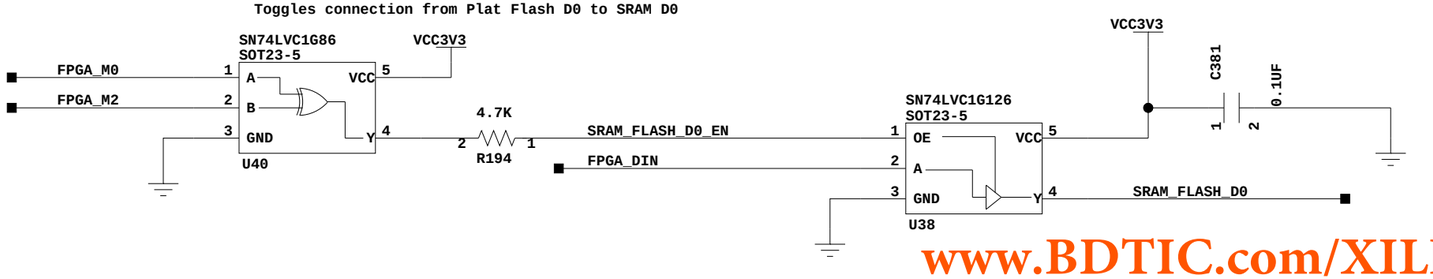
System ACE / Platform Flash / CPLD Flash Configuration Switch



m0	m2	Cfg Switch	D0/DIN Short
0	0	SysACE/CPLD	OPEN
0	1	SysACE/CPLD	OPEN
1	0	SysACE/CPLD	OPEN
1	1	SysACE/CPLD	OPEN
0	0	Plat FLASH	OPEN
0	1	Plat FLASH	SHORT
1	0	Plat FLASH	SHORT
1	1	Plat FLASH	OPEN



Toggles connection from Plat Flash D0 to SRAM D0



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Title: Platform Flash

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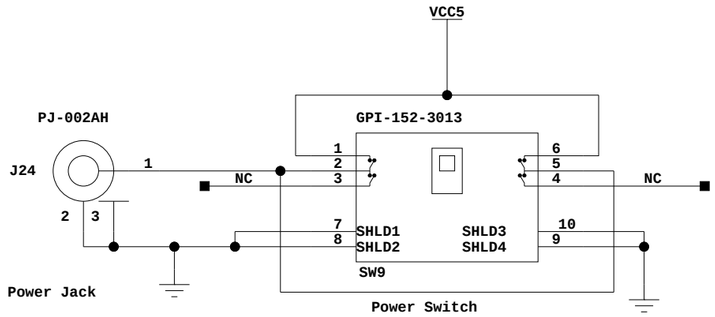
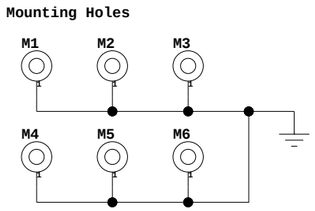
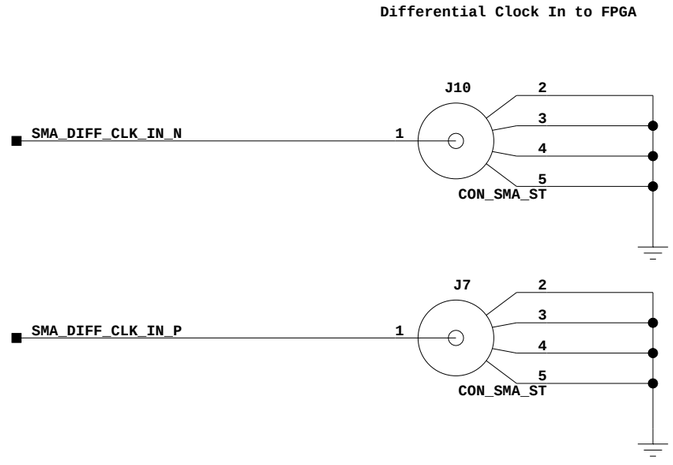
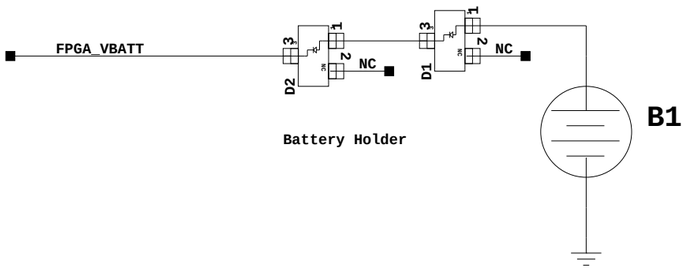
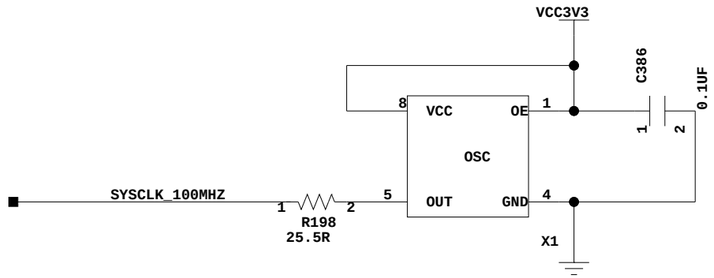
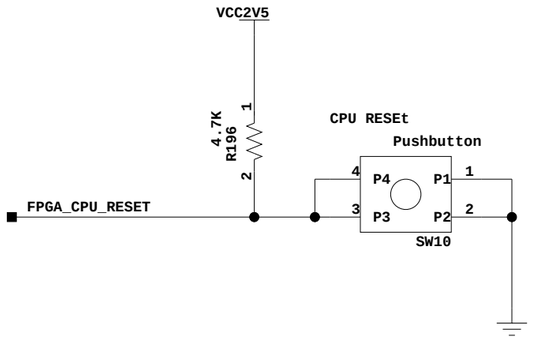








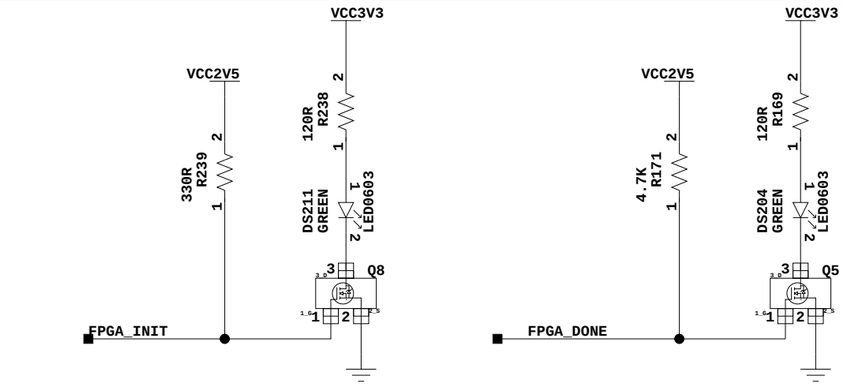


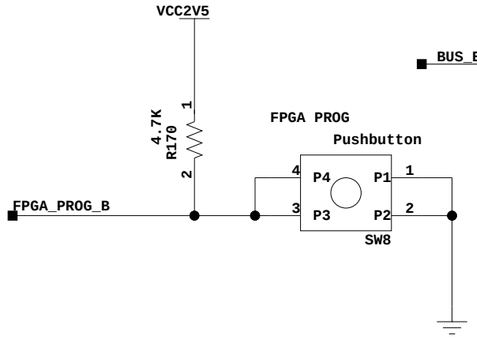


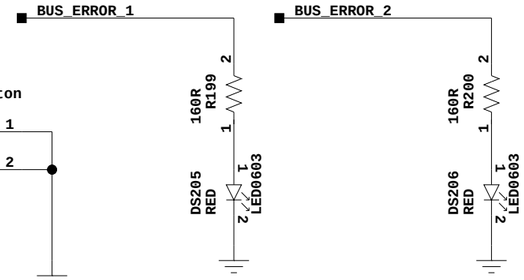
XILINX

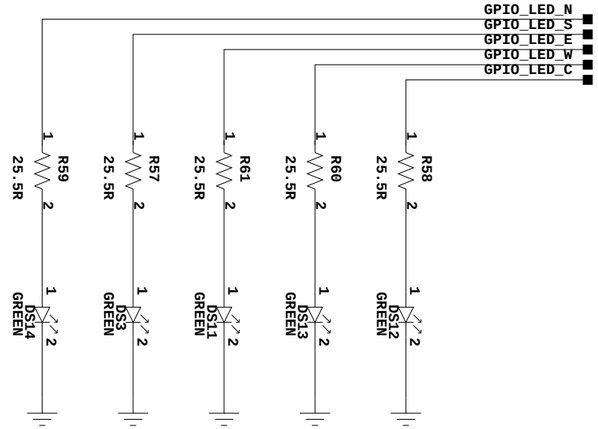
Title:
SMA Connectors, Power Switch, Battery, Oscillators, Reset

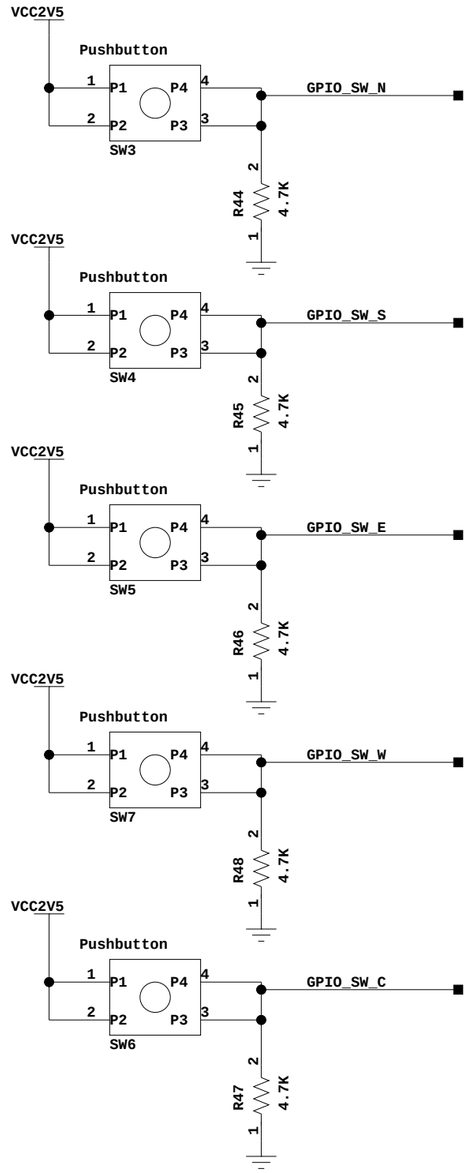
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 9 of 24	Drawn By BF

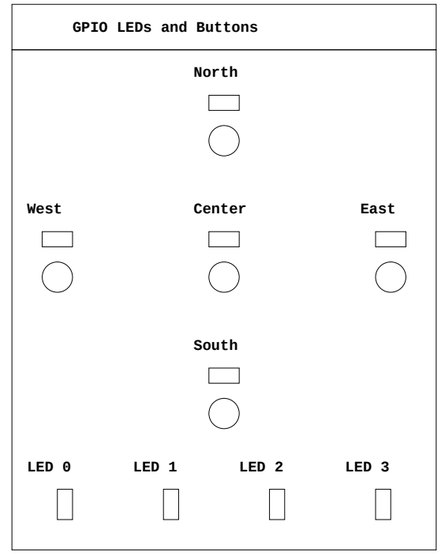


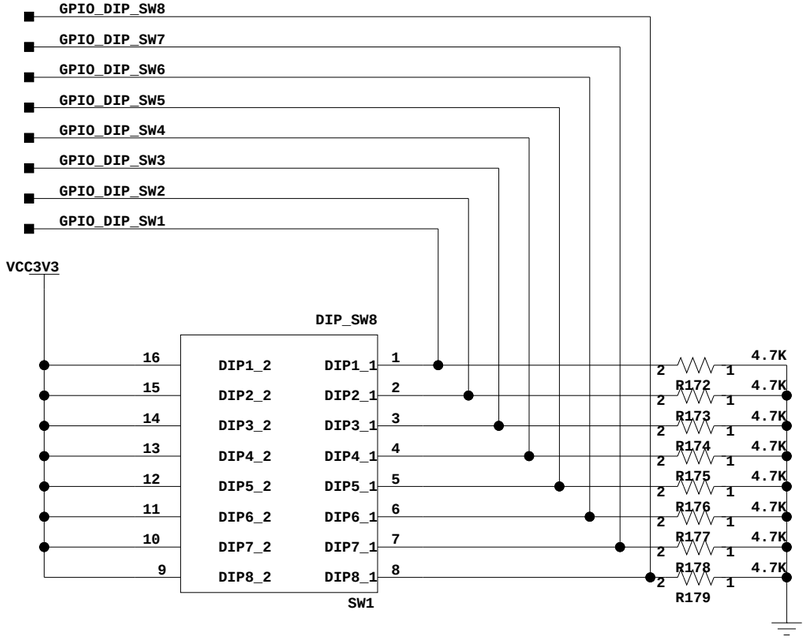


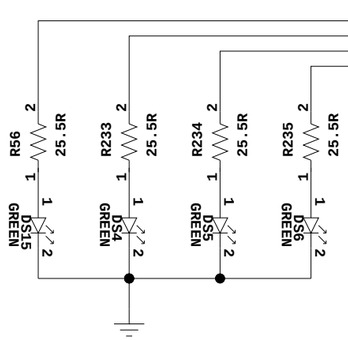


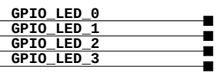








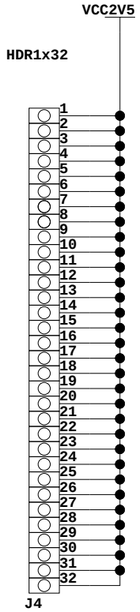


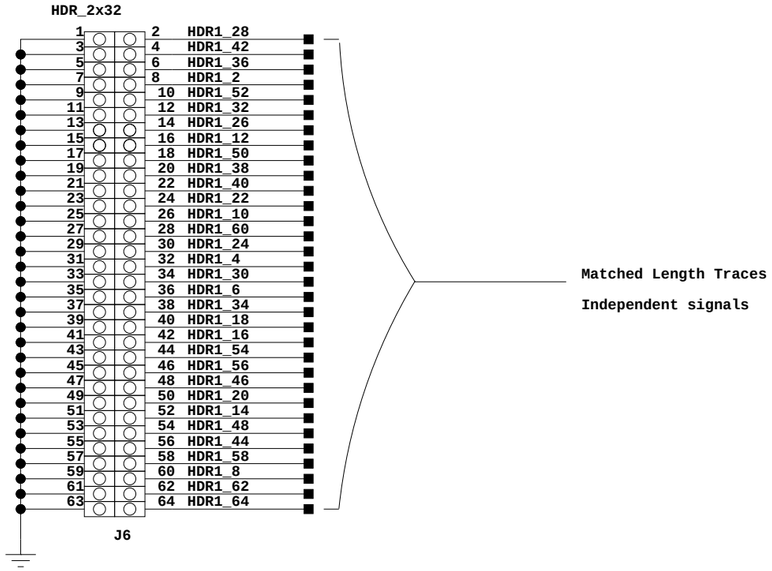


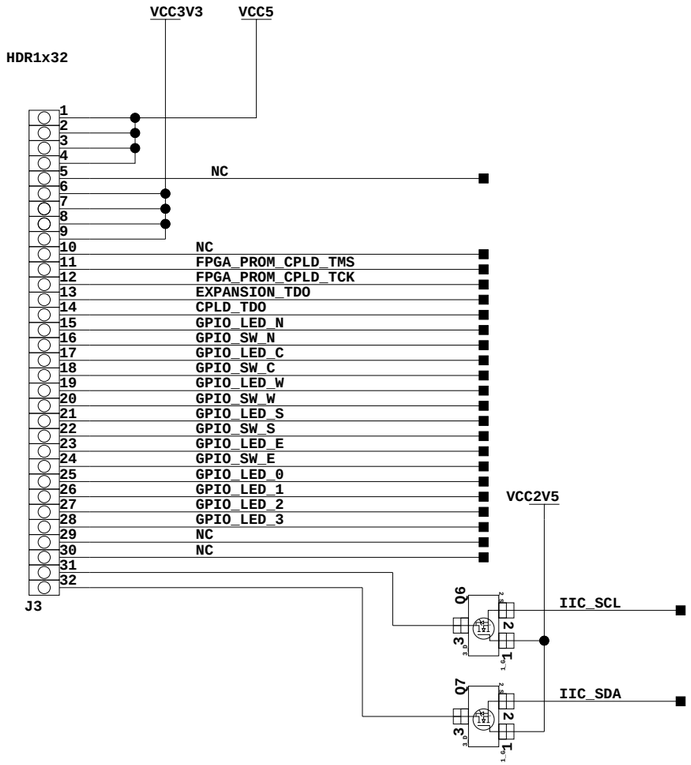
XILINX

Title: Buttons, LEDs, Switches

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 10 of 24	Drawn By BF



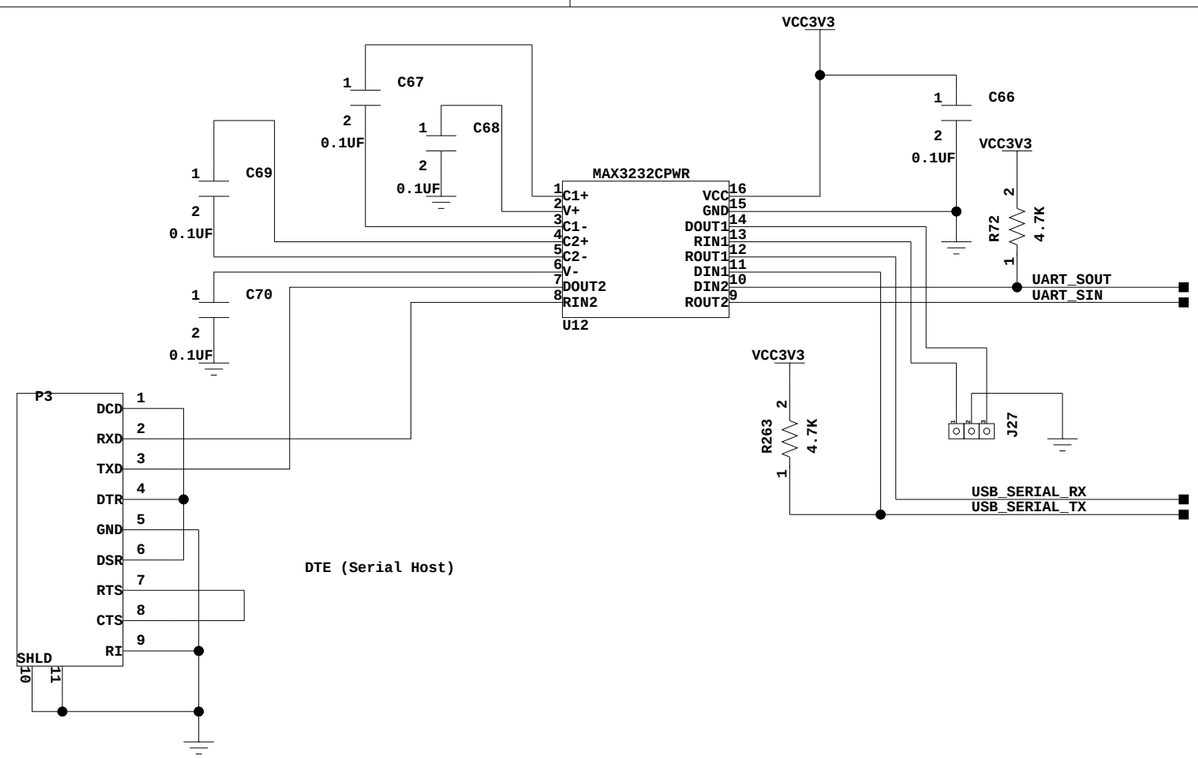


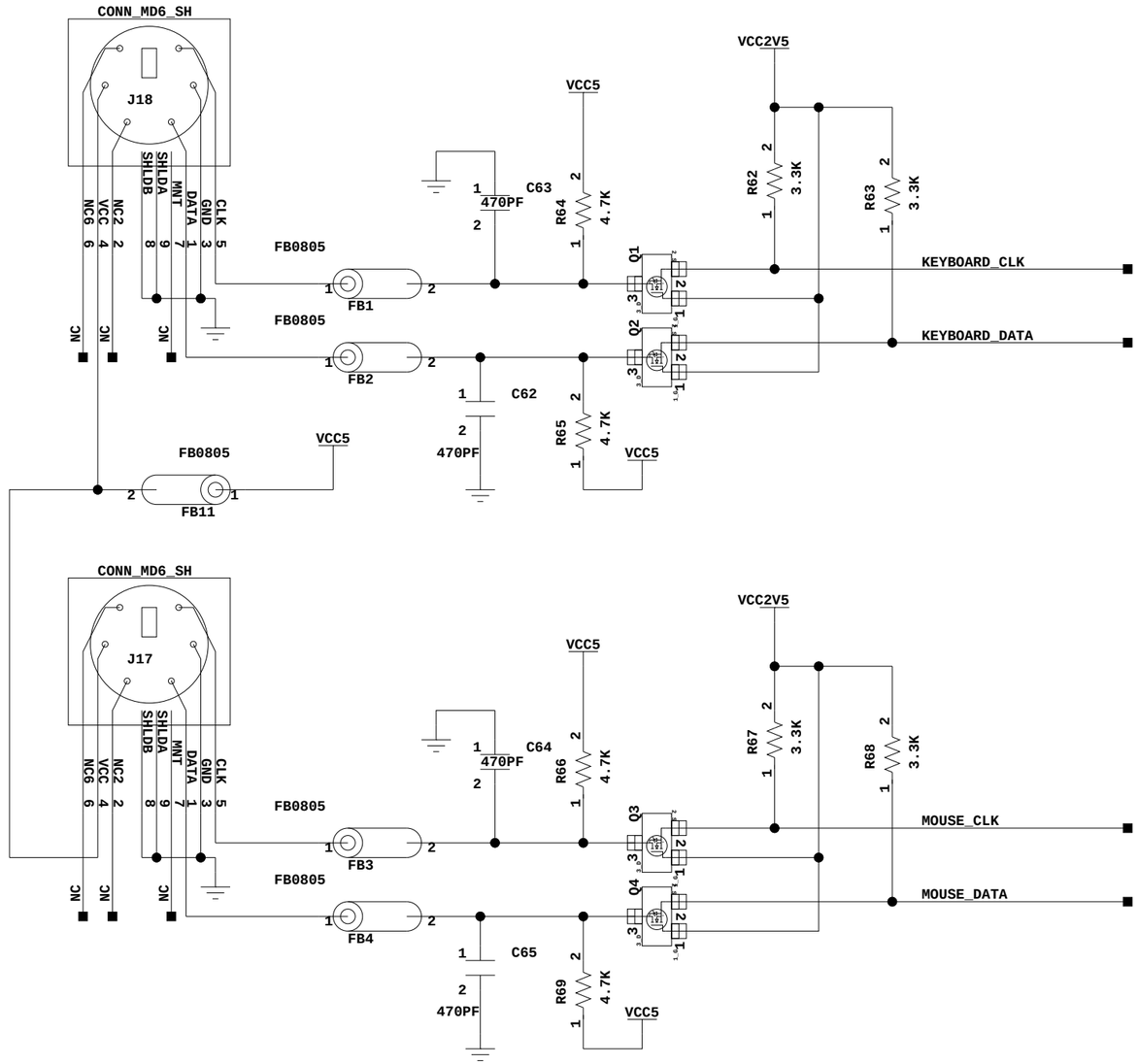


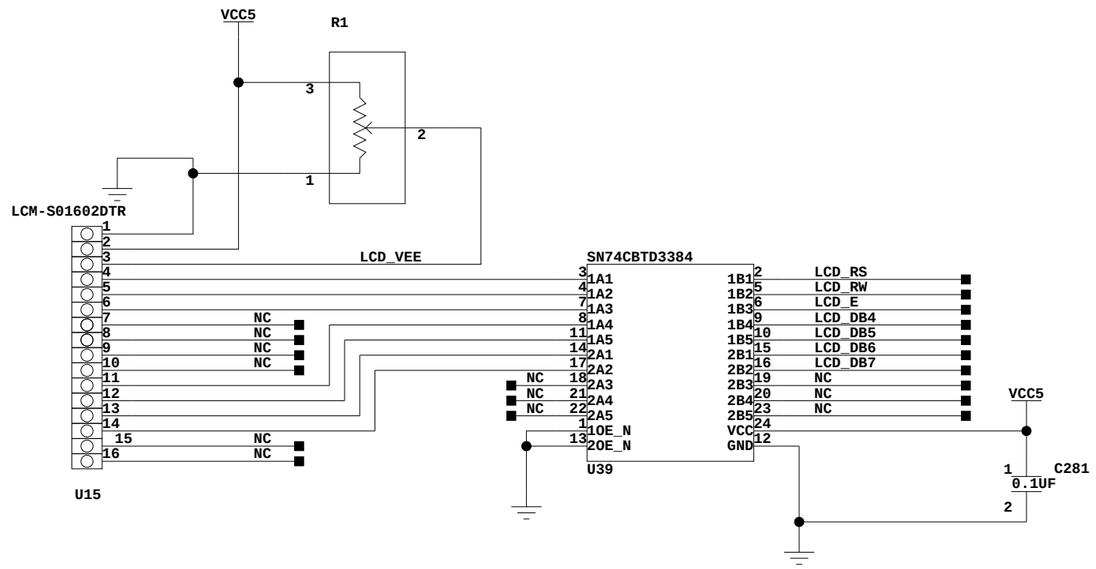
XILINX

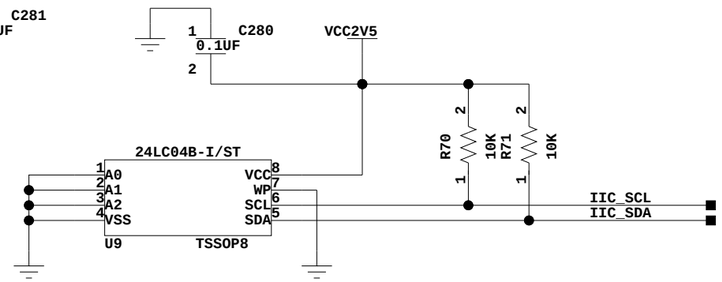
Title: Expansion Headers

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 11 of 24	Drawn By BF









XILINX

Title: LCD, PS2, UART, IIC EEPROM

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 12 of 24	Drawn By BF

Matched Length Nets

DDR_A3
DDR_A2
DDR_A1
DDR_A0
DDR_A10
DDR_BA1
DDR_BA0
DDR_CS_N

DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_DM2
DDR_A13
DDR_DQS2
DDR_D23
DDR_D22

DDR_D20
DDR_D19
DDR_D18
DDR_D17
DDR_D16

DDR_DM3

DDR_DQS3
DDR_D24
DDR_D25
DDR_D26
DDR_D27
DDR_D28
DDR_D29
DDR_D30

DDR_A7
DDR_A6
DDR_A5
DDR_A4
DDR_A12
DDR_A11
DDR_A9
DDR_A8

DDR_DM1
DDR_CK1_N
DDR_CK1_P
DDR_CKE
DDR_D10
DDR_D9
DDR_D8
DDR_DQS1

DDR_D14
DDR_D13
DDR_D12
DDR_D11
DDR_D7
DDR_DQS0
DDR_DM0
DDR_D15

DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D31
DDR_D0
DDR_D1
DDR_D2
DDR_D21

VTTDDR
VCC2V5

RP1 47R
RP2 47R
RP3 47R
RP4 47R
RP5 47R
RP6 47R
RP7 47R
RP8 K?
RP9
RP10 K?
RP11
RP12 K?
RP13
RP14 K?
RP15
RP16 K?
R73 47R

NC
NC

C424 0.1UF
C82 0.1UF
C41 100UF
C300 100UF
C423 0.1UF
C81 0.1UF
C40 100UF
C301 100UF
C422 0.1UF
C80 0.1UF
C39 100UF
C302 100UF
C421 0.1UF
C71 0.1UF
C38 100UF

C408 0.1UF
C407 0.1UF

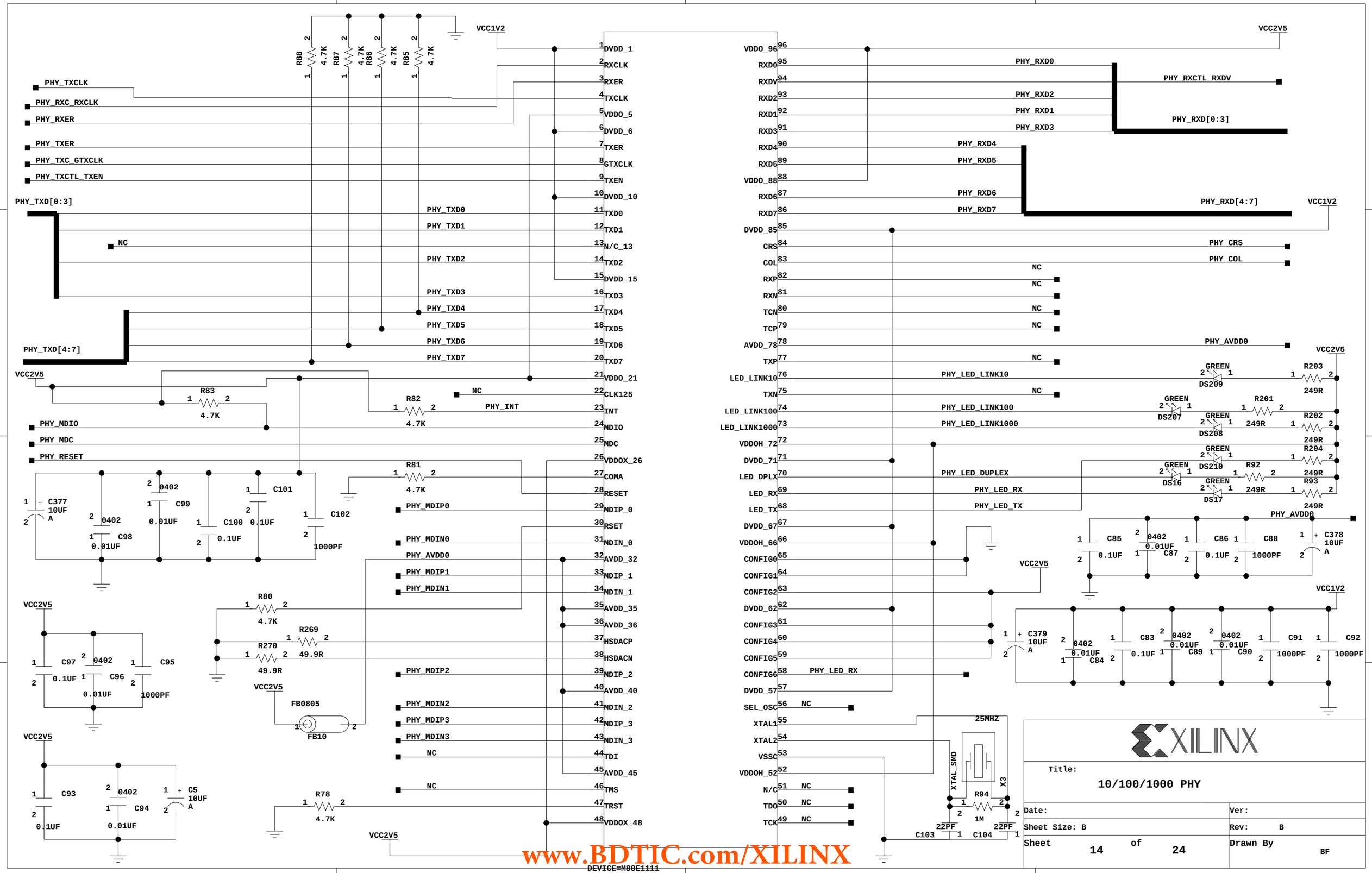
U4 64Mx16x4 DDR SDRAM HYB25D256160BT-7F TSOP66
U5 64Mx16x4 DDR SDRAM HYB25D256160BT-7F TSOP66

C72 0.1UF
C73 0.1UF
C74 0.1UF
C75 0.1UF
C76 0.1UF
C77 0.1UF
C78 0.1UF
C79 0.1UF

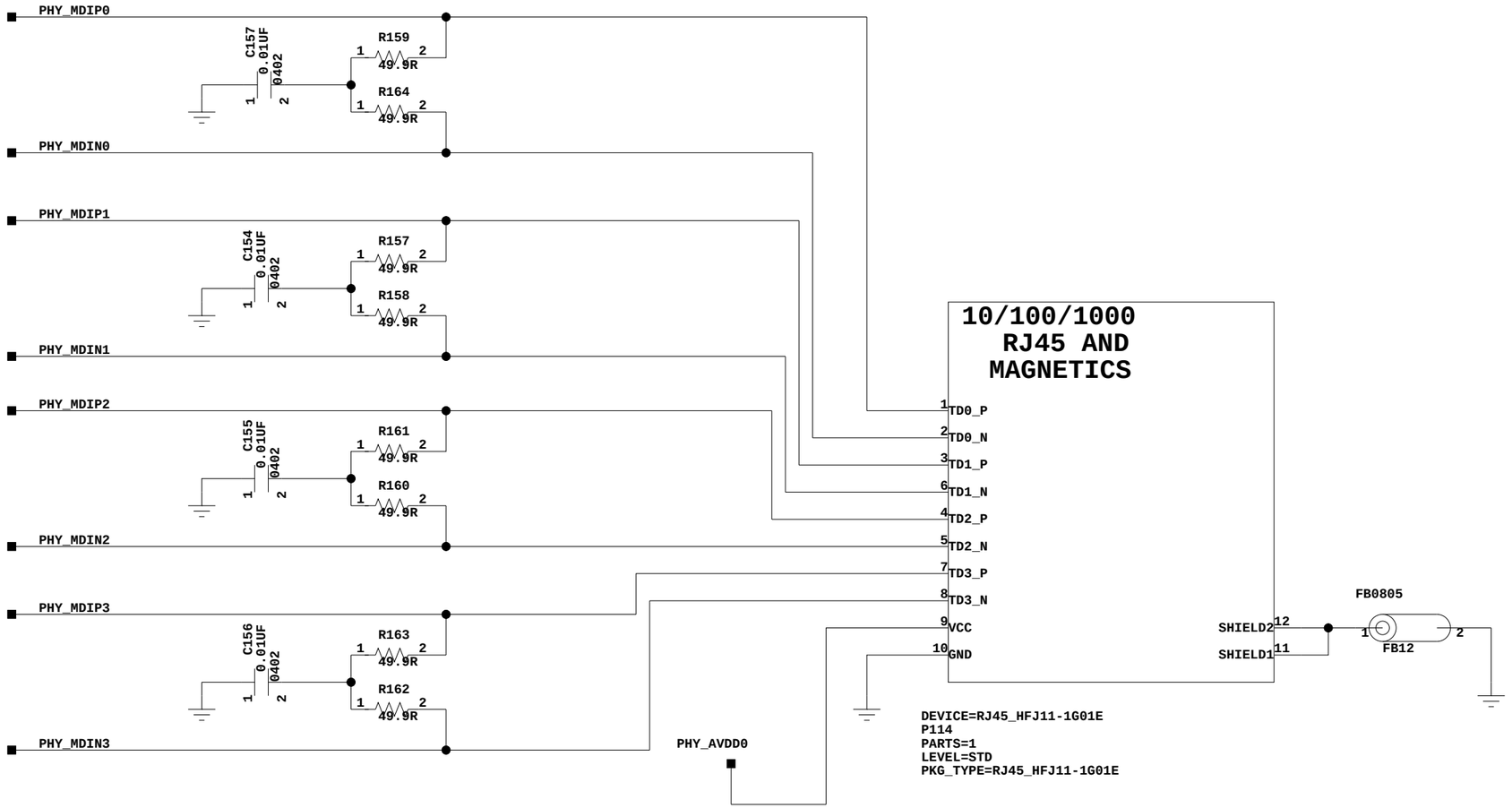
XILINX

Title: DDR Memory

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 13 of 24	Drawn By BF



Pin to Constant Mapping	
Pin	Bit[2:0]
VCC2V5	111
PHY_LED_LINK10	110
PHY_LED_LINK100	101
PHY_LED_LINK1000	100
PHY_LED_DUPLEX	011
PHY_LED_RX	010
PHY_LED_TX	001
GND	000

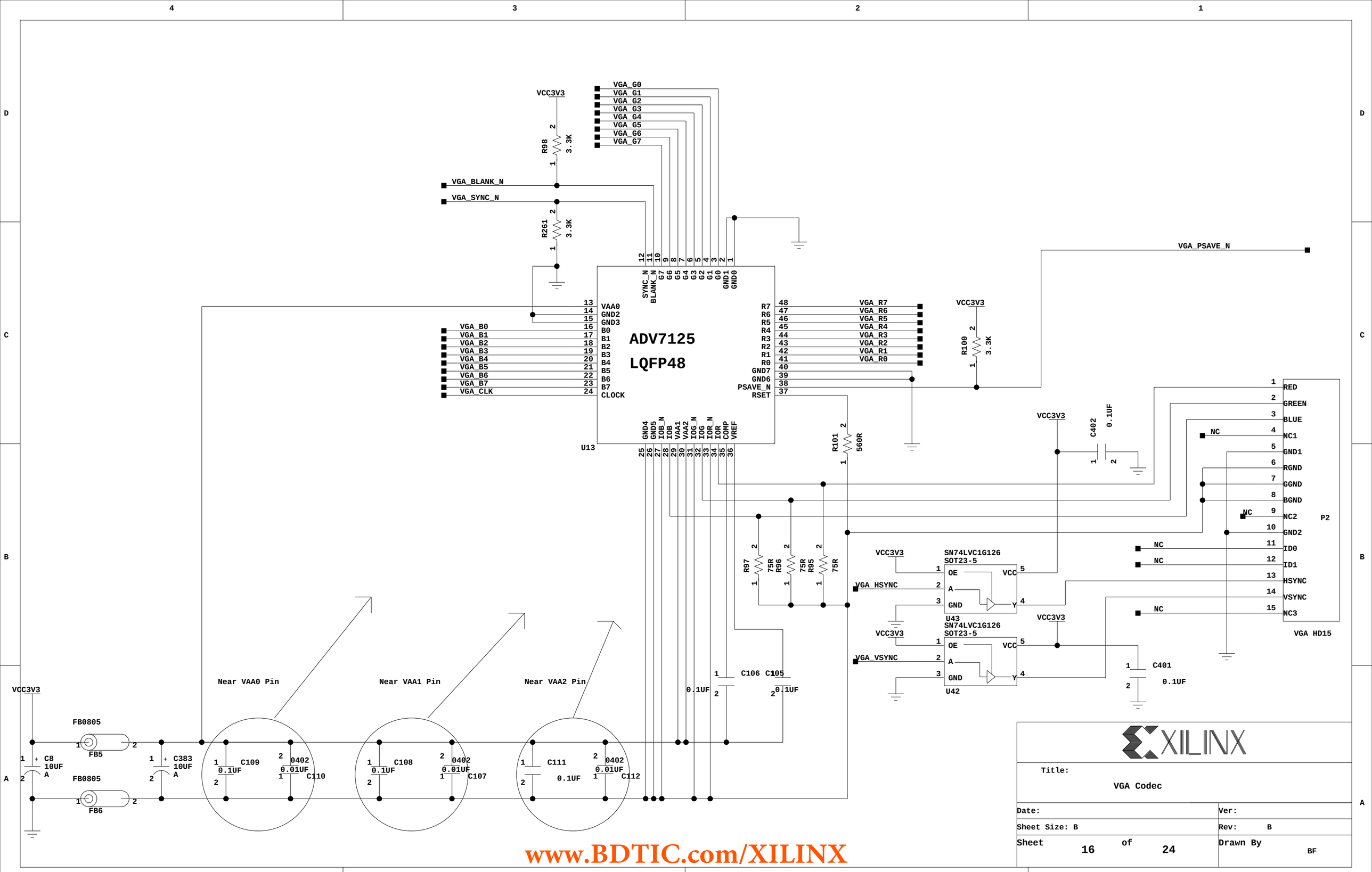


Pin	Bit[2]	Bit[1]	Bit[0]		
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddress "00000". Do not advertise the PAUSE bit
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg enabled, advertise all capabilities; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CONFIG3	ANEG[0]	ENA_XC	DIS_125	111	
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	111	
CONFIG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW Interrupt. 50Ohm SERDES option.

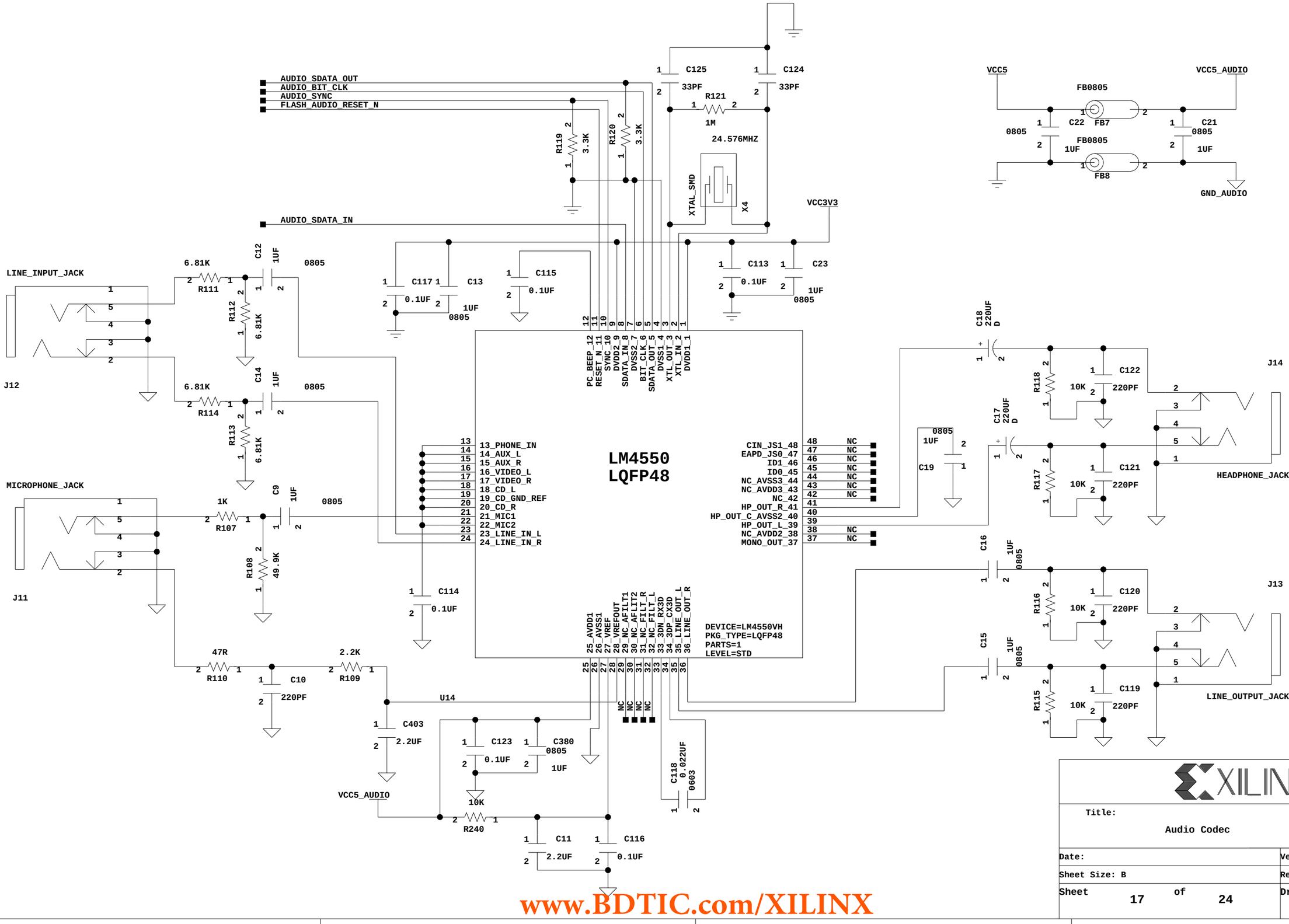
XILINX

Title:
RJ45 Connector and PHY Decoupling

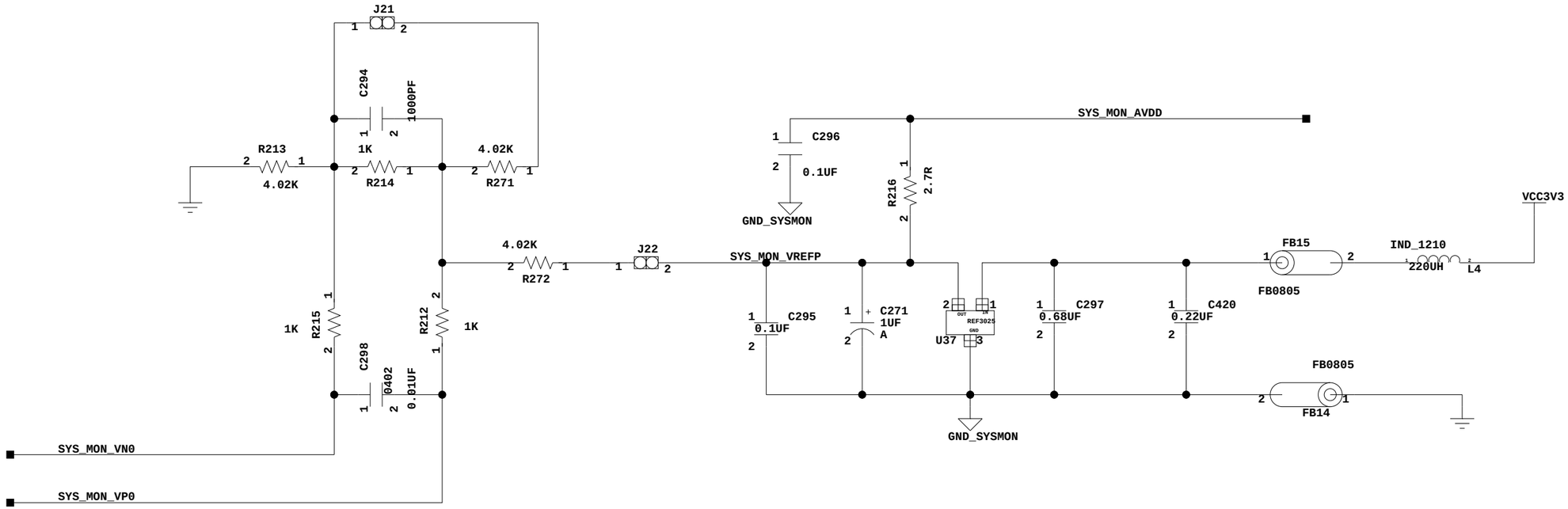
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 15 of 24	Drawn By BF



Title: VGA Codec	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 16 of 24	Drawn By BF



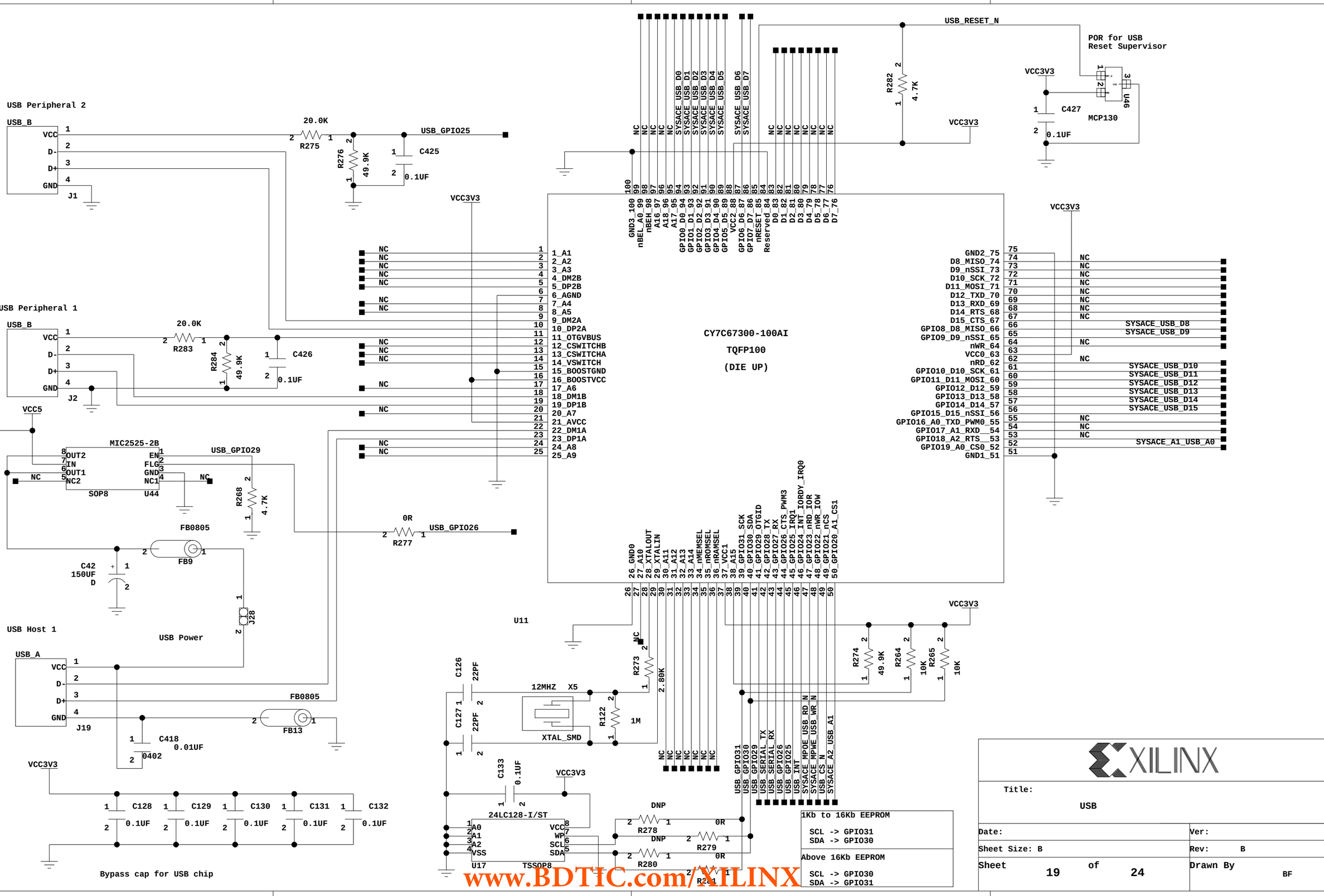
Title: Audio Codec	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 17 of 24	Drawn By BF

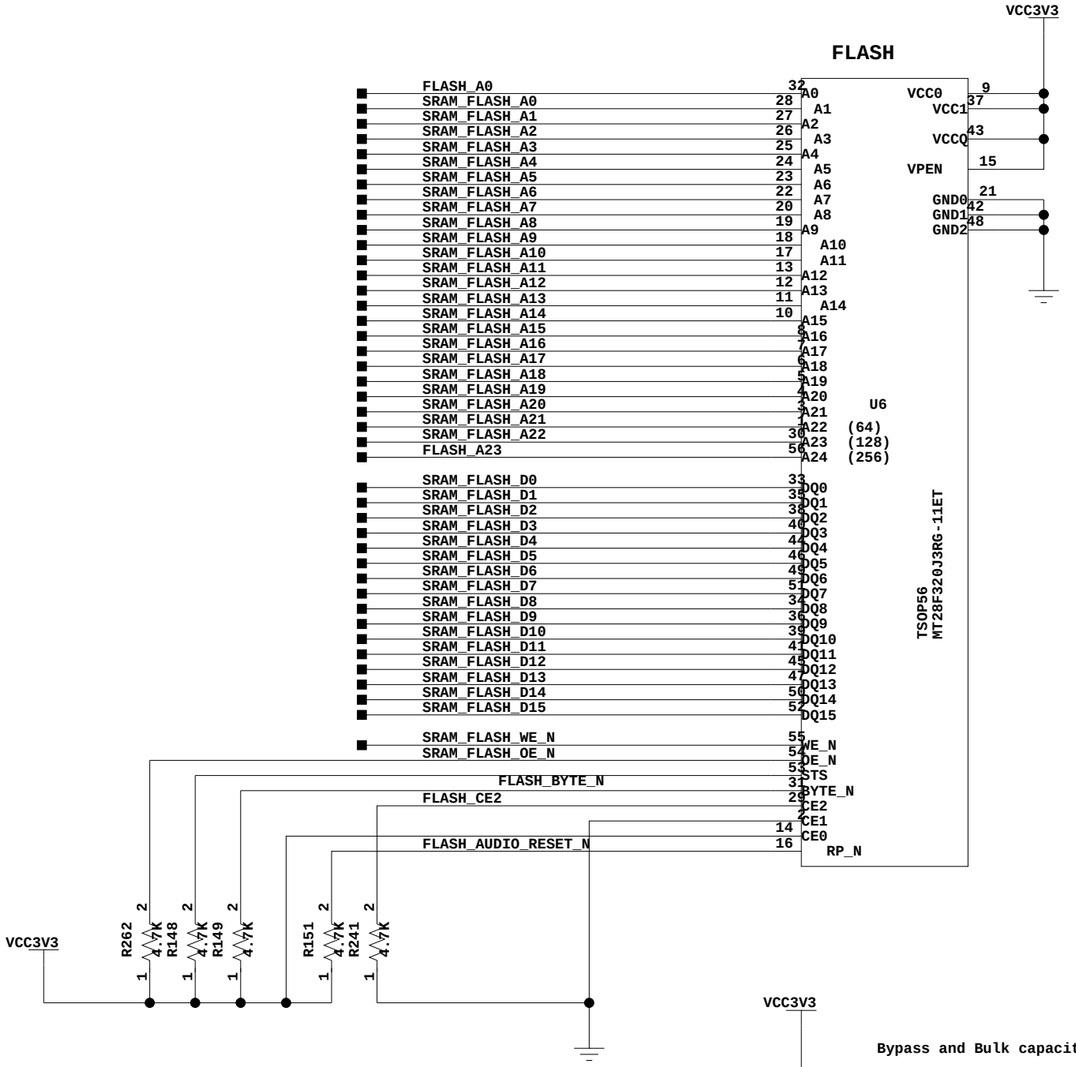


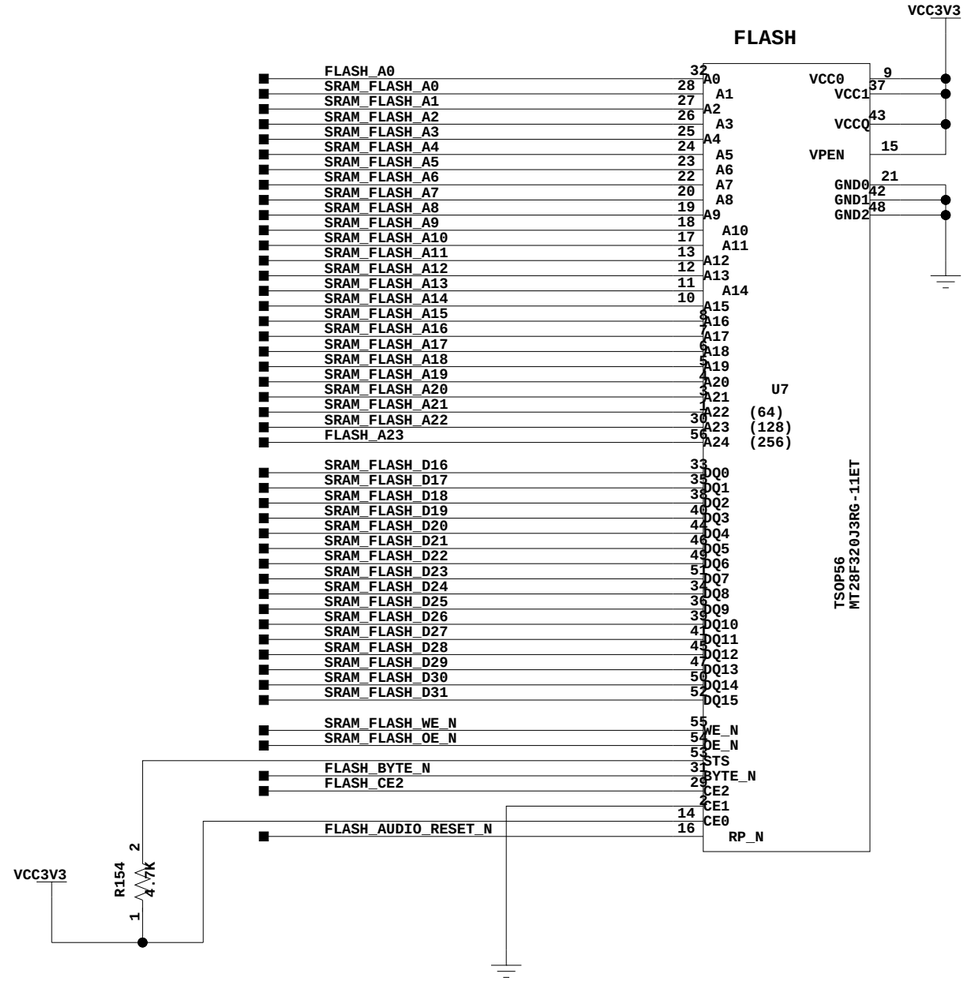
XILINX

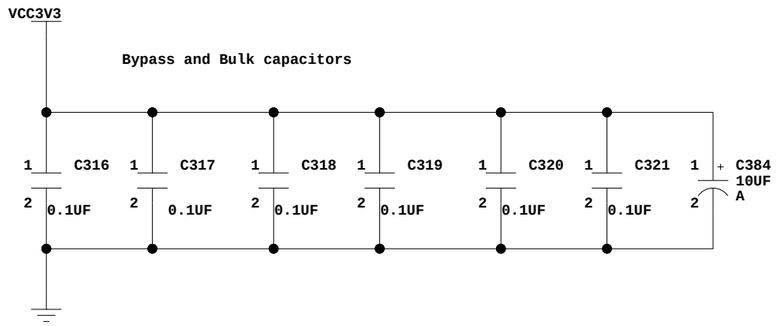
Title: System Monitor DVM Circuit

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 18 of 24	Drawn By BF









XILINX

Title: Flash Memory

Date:	Ver:
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The burst order mode of the SRAM is set to "Linear" by default

VCC3V3

R210 4.7K
R209 4.7K
R208 4.7K
R211 4.7K

SRAM_CE1_N
SRAM_MODE
SRAM_ZZ
SRAM_BW1
SRAM_BW0
SRAM_BW3
SRAM_BW2
SRAM_ADV_LD_N
SRAM_FLASH_OE_N
SRAM_FLASH_WE_N
SRAM_CLK

SRAM_FLASH_A0
SRAM_FLASH_A1
SRAM_FLASH_A2
SRAM_FLASH_A3
SRAM_FLASH_A4
SRAM_FLASH_A5
SRAM_FLASH_A6
SRAM_FLASH_A7
SRAM_FLASH_A8
SRAM_FLASH_A9
SRAM_FLASH_A10
SRAM_FLASH_A11
SRAM_FLASH_A12
SRAM_FLASH_A13
SRAM_FLASH_A14
SRAM_FLASH_A15
SRAM_FLASH_A16
SRAM_FLASH_A17
SRAM_FLASH_A18
SRAM_FLASH_A19
SRAM_FLASH_A20
SRAM_FLASH_A21
SRAM_FLASH_A22

SRAM_DQP2
SRAM_FLASH_D31_RES
SRAM_FLASH_D30_RES
SRAM_FLASH_D29_RES
SRAM_FLASH_D28_RES
SRAM_FLASH_D27_RES
SRAM_FLASH_D26_RES
SRAM_FLASH_D25_RES
SRAM_FLASH_D24_RES
SRAM_FLASH_D23_RES
SRAM_FLASH_D22_RES
SRAM_FLASH_D21_RES
SRAM_FLASH_D20_RES
SRAM_FLASH_D19_RES
SRAM_FLASH_D18_RES
SRAM_FLASH_D17_RES
SRAM_FLASH_D16_RES
SRAM_DQP3
SRAM_DQP0
SRAM_FLASH_D15_RES
SRAM_FLASH_D14_RES
SRAM_FLASH_D13_RES
SRAM_FLASH_D12_RES
SRAM_FLASH_D11_RES
SRAM_FLASH_D10_RES
SRAM_FLASH_D9_RES
SRAM_FLASH_D8_RES
SRAM_FLASH_D7_RES
SRAM_FLASH_D6_RES
SRAM_FLASH_D5_RES
SRAM_FLASH_D4_RES
SRAM_FLASH_D3_RES
SRAM_FLASH_D2_RES
SRAM_FLASH_D1_RES
SRAM_FLASH_D0_RES
SRAM_DQP1

R287 47R
R288 47R
R286 47R
R285 47R

U41 CY7C1354B TQFP100

87	87_CEN_N	NC_66	66 NC
92	92_CE3_N	NC_16	16 NC
97	97_CE2	NC_14	14 NC
98	98_CE1_N	VSS_90	90
31	MODE_31	VSS_76	76
64	ZZ_64	VSS_71	71
93	93_BWA_N	VSS_67	67
94	94_BWB_N	VSS_60	60
95	95_BWC_N	VSS_55	55
96	96_BWD_N	VSS_40	40
85	85_ADV/LD_N	VSS_26	26
86	86_OE_N	VSS_21	21
88	88_WE_N	VSS_17	17
89	89_CLK	VSS_10	10
		VSS_5	5
37	37_A0	VDD_91	91
36	36_A1	VDDQ_77	77
35	35_A	VDDQ_70	70
34	34_A	VDD_65	65
33	33_A	VDDQ_61	61
32	32_A	VDDQ_54	54
44	44_A	VDD_41	41
45	45_A	VDDQ_27	27
46	46_A	VDDQ_20	20
47	47_A	VDDQ_15	15
48	48_A	VDDQ_11	11
49	49_A	VDDQ_4	4
50	50_A		
81	81_A		
82	82_A		
83	83_A		
99	99_A		
100	100_A		
84	84_E18		
43	43_E36		
42	42_E72		
39	39_E144		
38	38_E288		
1	1_DQPC		
2	2_DQC		
3	3_DQC		
6	6_DQC		
7	7_DQC		
8	8_DQC		
9	9_DQC		
12	12_DQC		
13	13_DQC		
18	18_DQD		
19	19_DQD		
22	22_DQD		
23	23_DQD		
24	24_DQD		
25	25_DQD		
28	28_DQD		
29	DQD_29		
30	DQPD_30		
51	DQPA_51		
52	DQA_52		
53	DQA_53		
56	DQA_56		
57	DQA_57		
58	DQA_58		
59	DQA_59		
62	DQA_62		
63	DQA_63		
68	DQB_68		
69	DQB_69		
72	DQB_72		
73	DQB_73		
74	DQB_74		
75	DQB_75		
78	DQB_78		
79	DQB_79		
80	DQPB_80		

RP24 47R
RP23 47R
RP22 47R
RP21 47R
RP17 K?
RP18 K?
RP19 K?
RP20 K?

VCC3V3

C282 0.1UF
C283 0.1UF
C284 0.1UF
C285 0.1UF
C286 0.1UF
C287 0.1UF
C288 0.1UF
C289 0.1UF
C269 10UF A

XILINX

Title: ZBT SRAM

Date:
Ver:
Sheet Size: B
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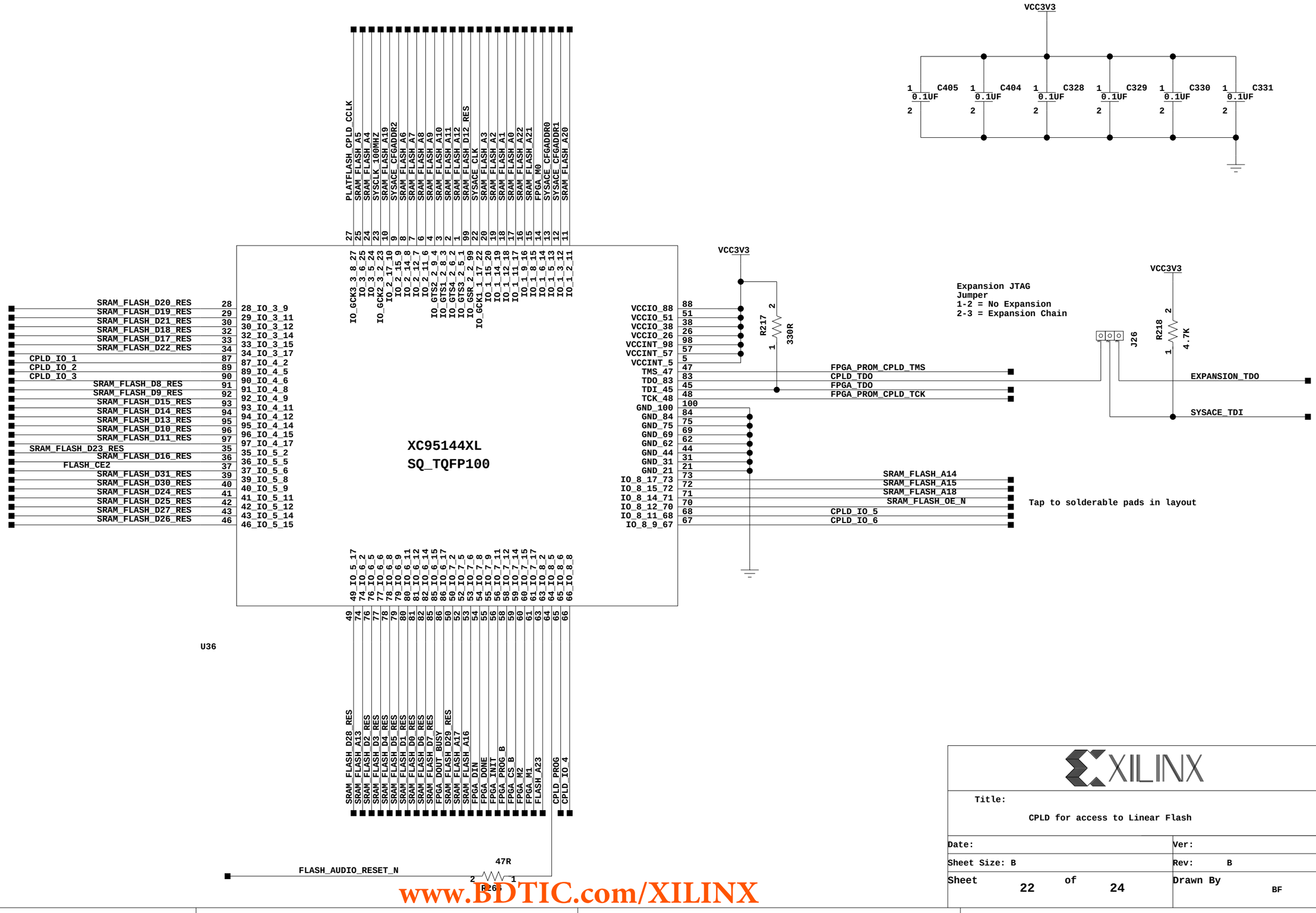
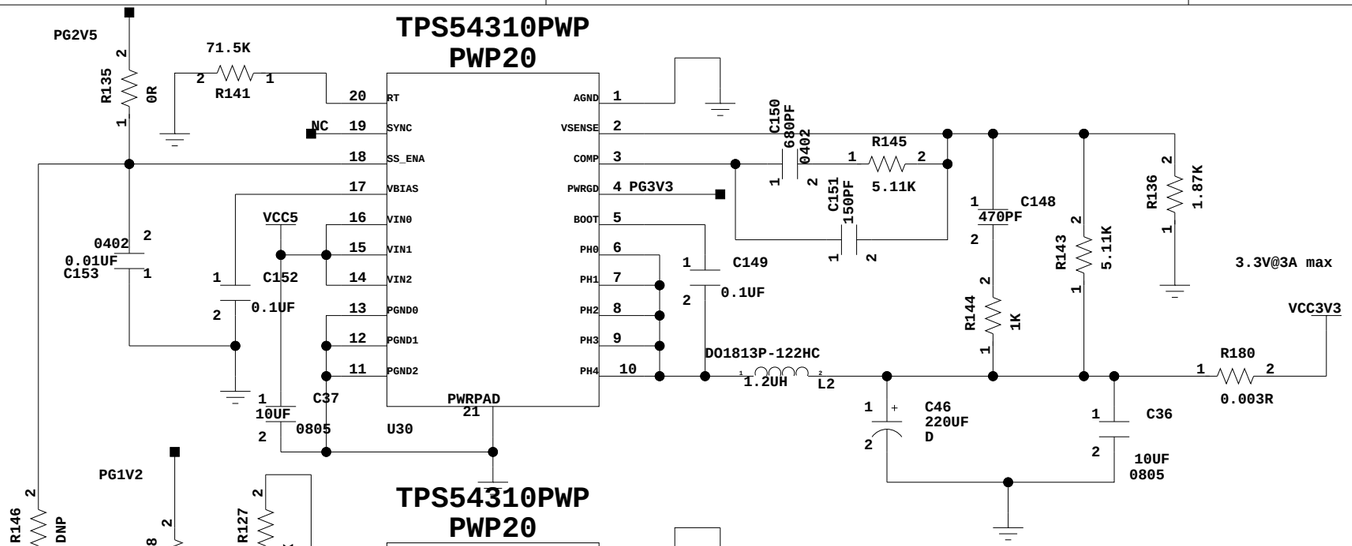
Sheet 21 of 24
Drawn By BF

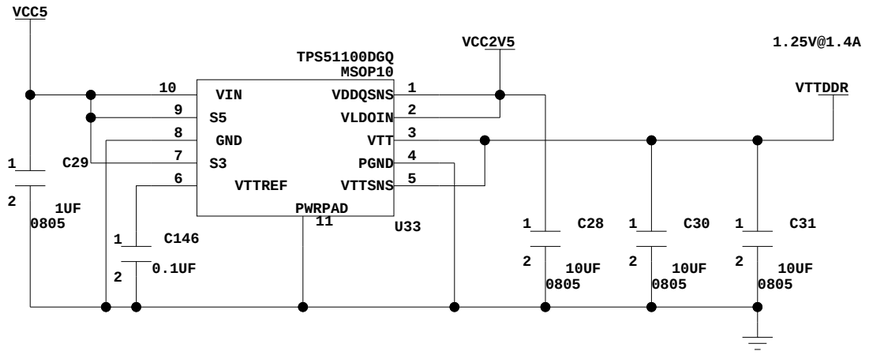


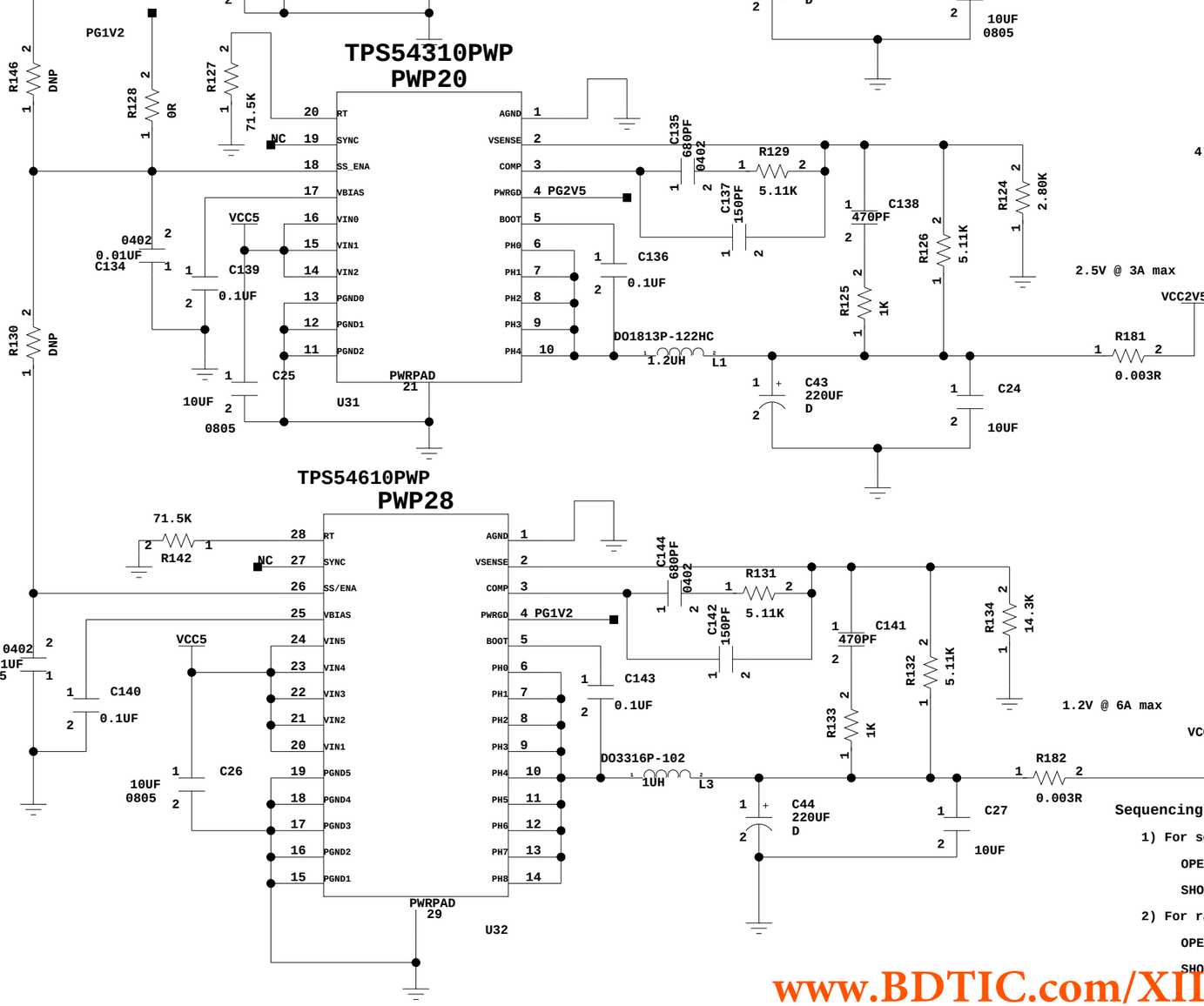
XILINX

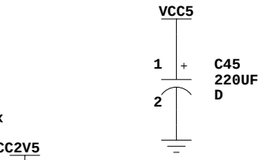
Title: CPLD for access to Linear Flash

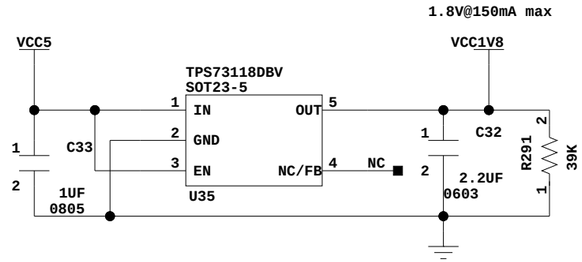
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 22 of 24	Drawn By BF

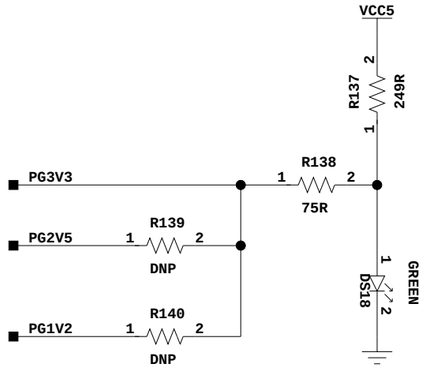












Sequencing Options:

1) For sequential startup :
   OPEN R130, R146, R139 & R140
   SHORT R128 & R135
2) For ratiometric startup :
   OPEN R128 & R135
   SHORT R130, R146, R139 & R140

XILINX

Title: Power Supply

Date:	Ver:
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3.3V VCCO

VCC3V3

C259 0.047UF 0402 · C238 0.047UF 0402 · C239 0.047UF 0402 · C240 0.047UF 0402 · C241 0.047UF 0402 · C245 0.047UF 0402 · C246 0.047UF 0402 · C247 0.047UF 0402 · C248 0.047UF 0402 · C252 0.047UF 0402 · C267 0.047UF 0402 · C261 0.047UF 0402 · C265 0.047UF 0402 · C414 0.047UF 0402

VCC3V3

C260 0.22UF · C262 0.22UF · C268 0.22UF · C266 0.22UF · C249 0.22UF · C258 0.22UF · C250 0.22UF

VCC3V3

C333 0.68UF · C335 0.68UF · C332 0.68UF

VCC3V3

C357 2.2UF · C351 2.2UF

VCC3V3

C376 330UF D

2.5V VCCO and VCCAUX

VCC2V5

C220 0.047UF 0402 · C219 0.047UF 0402 · C218 0.047UF 0402 · C217 0.047UF 0402 · C224 0.047UF 0402 · C225 0.047UF 0402 · C226 0.047UF 0402 · C227 0.047UF 0402 · C263 0.047UF 0402 · C210 0.047UF 0402 · C211 0.047UF 0402 · C212 0.047UF 0402 · C213 0.047UF 0402 · C214 0.047UF 0402 · C215 0.047UF 0402 · C216 0.047UF 0402

VCC2V5

C413 0.047UF 0402 · C412 0.047UF 0402

VCC2V5

C223 0.22UF · C222 0.22UF · C221 0.22UF · C228 0.22UF · C229 0.22UF · C230 0.22UF · C206 0.22UF · C207 0.22UF · C208 0.22UF

VCC2V5

C334 0.68UF · C338 0.68UF · C339 0.68UF · C348 0.68UF

VCC2V5

C355 2.2UF · C356 2.2UF · C352 2.2UF · C373 330UF D · C370 330UF D

1.2V VCCINT

VCC1V2

C178 0.047UF 0402 · C179 0.047UF 0402 · C180 0.047UF 0402 · C181 0.047UF 0402 · C182 0.047UF 0402 · C183 0.047UF 0402 · C184 0.047UF 0402 · C185 0.047UF 0402 · C410 0.047UF 0402

C186 0.047UF 0402 · C187 0.047UF 0402 · C188 0.047UF 0402 · C189 0.047UF 0402 · C190 0.047UF 0402 · C191 0.047UF 0402 · C192 0.047UF 0402 · C193 0.047UF 0402 · C411 0.047UF 0402

C194 0.22UF · C195 0.22UF · C196 0.22UF · C197 0.22UF · C198 0.22UF

C199 0.22UF · C200 0.22UF · C201 0.22UF

C343 0.68UF · C344 0.68UF · C345 0.68UF · C346 0.68UF

C361 2.2UF · C362 2.2UF · C417 2.2UF

C371 330UF D

Place these near Bank 7 VCCO

VCCO_7

C231 0.047UF 0402 · C232 0.047UF 0402 · C233 0.047UF 0402 · C234 0.047UF 0402 · C236 0.22UF · C237 0.22UF · C337 0.68UF · C358 2.2UF · C409 330UF D

XILINX

Title: FPGA Decoupling

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 24 of 24	Drawn By BF