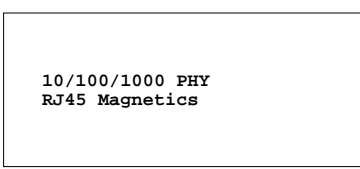
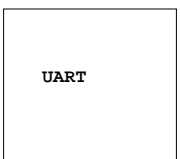
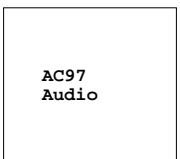
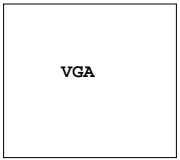
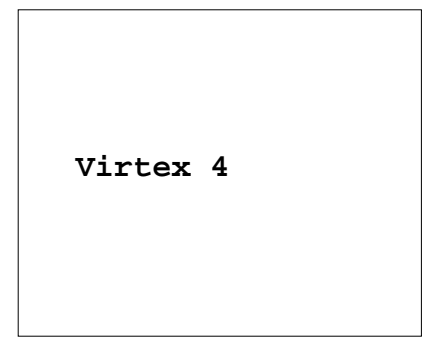
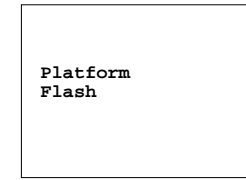
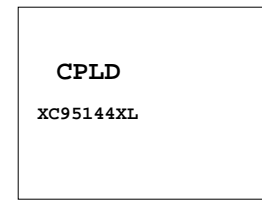
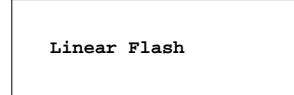
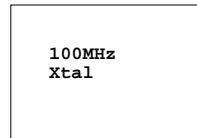
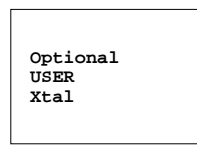
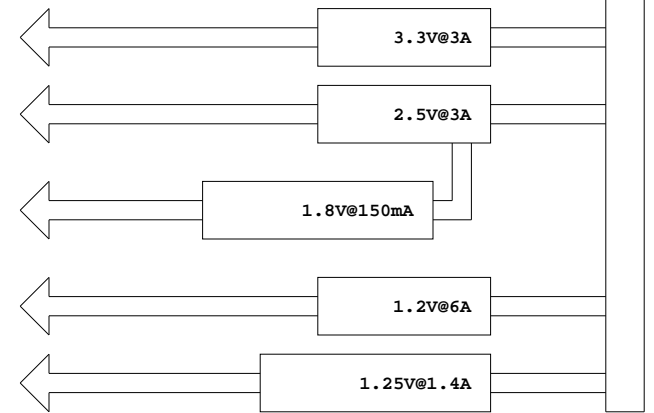
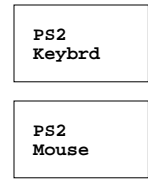
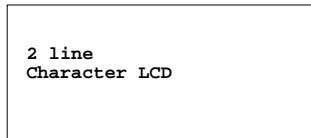
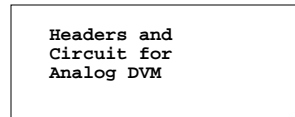
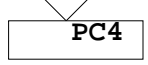
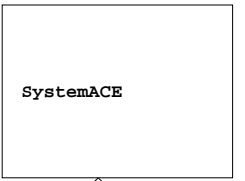
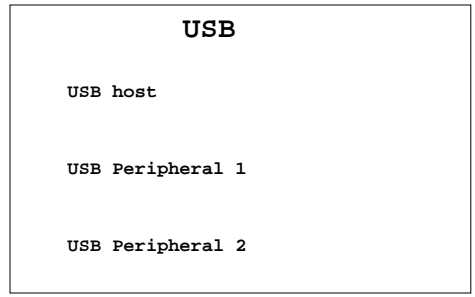


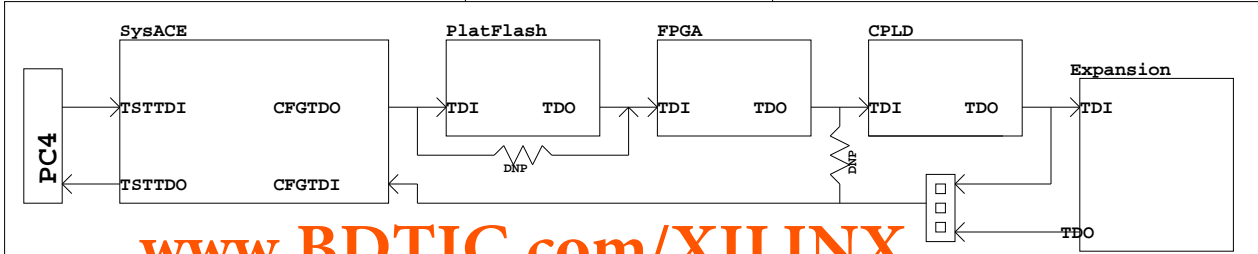
Power Supply



Compatibility and Available IOs	
FPGA Device	Banks
LX15, FX12, SX25	8 Banks 320 User IOs
LX25, LX40, LX60 SX35	10 Banks up to 448 User IOs



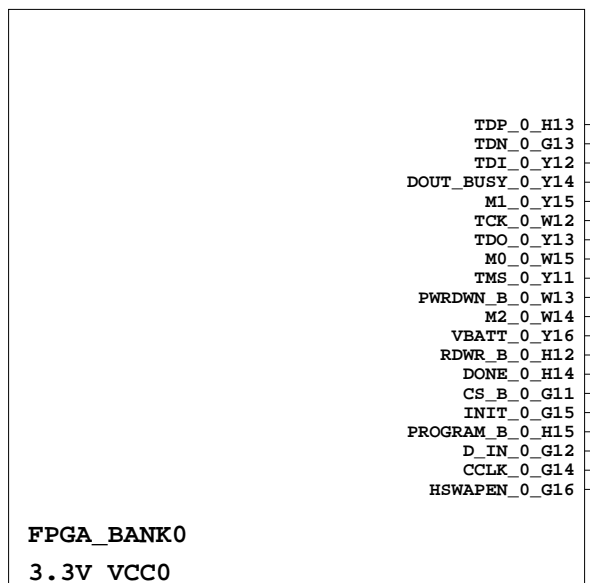
JTAG Chain



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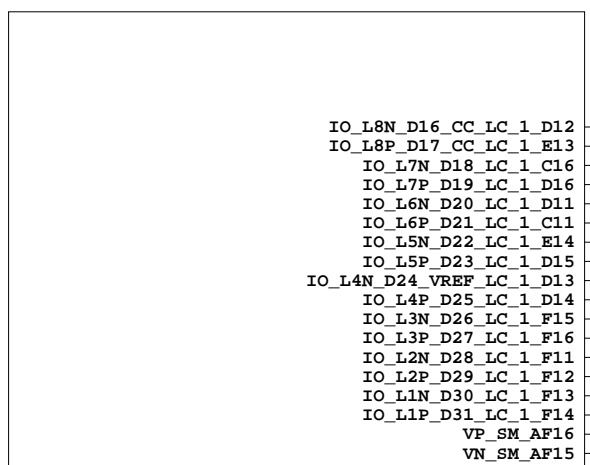
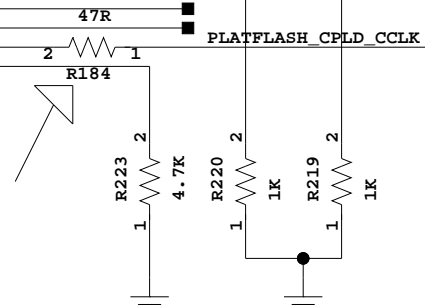


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Date: 8/19/2004	Ver: 1.0
Sheet Size: B	Rev: B
Sheet 1 of 24	Drawn By BF

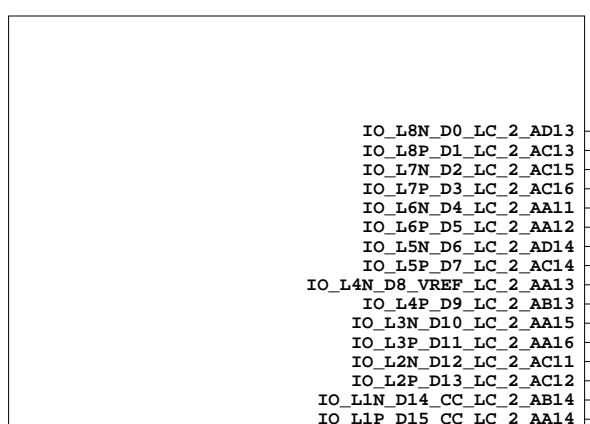


Configuration

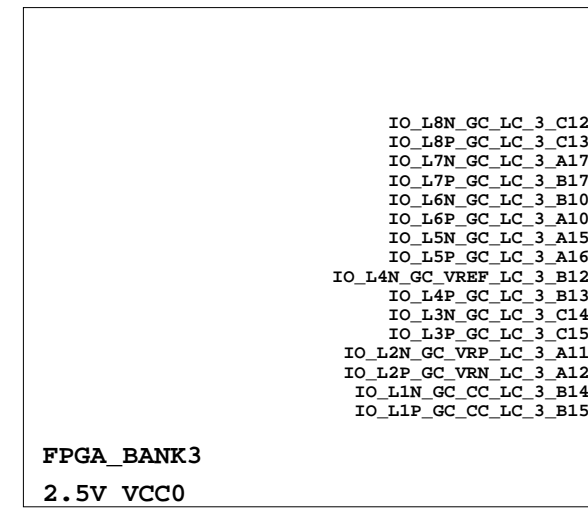
Added 50ohm for protection
In case FPGA and PLAT Flash
or CPLD drive CCLK



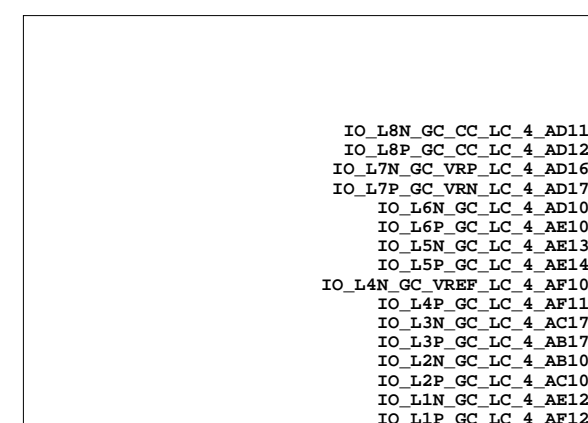
Configuration



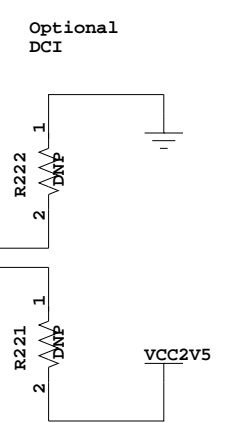
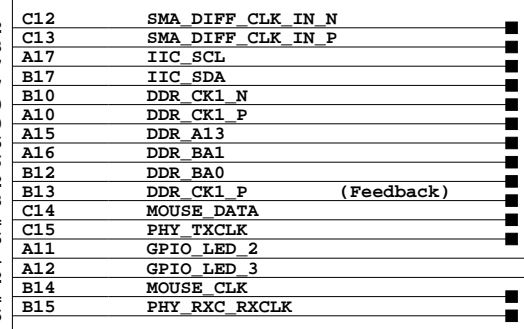
Configuration



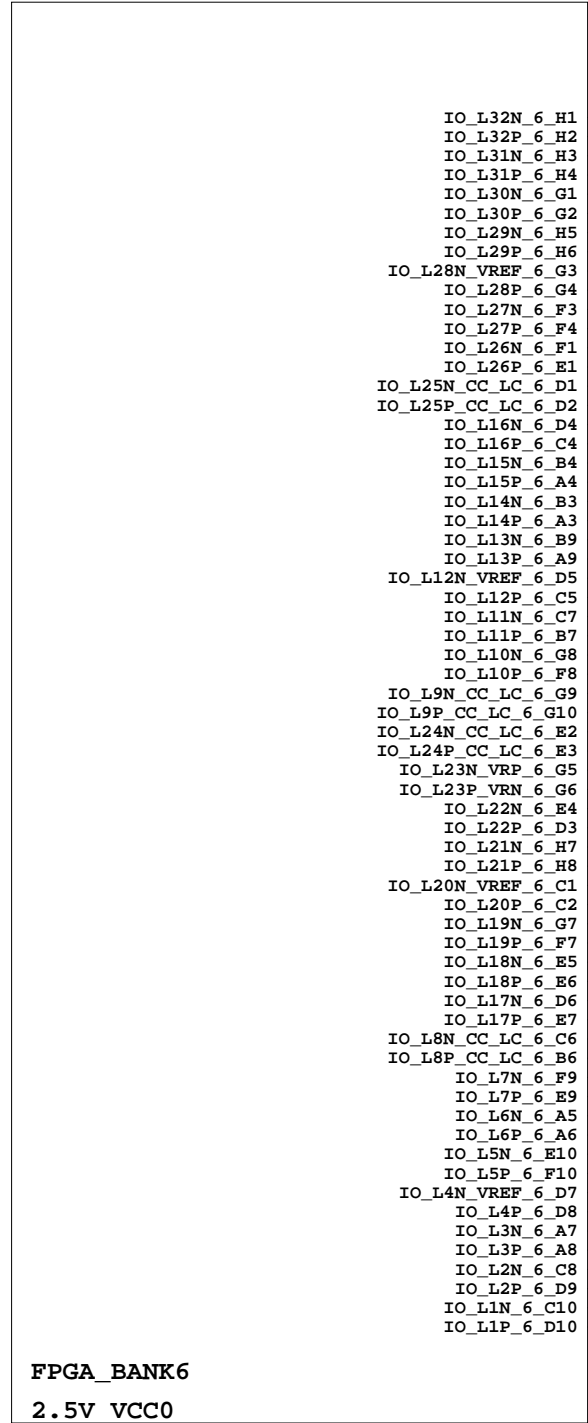
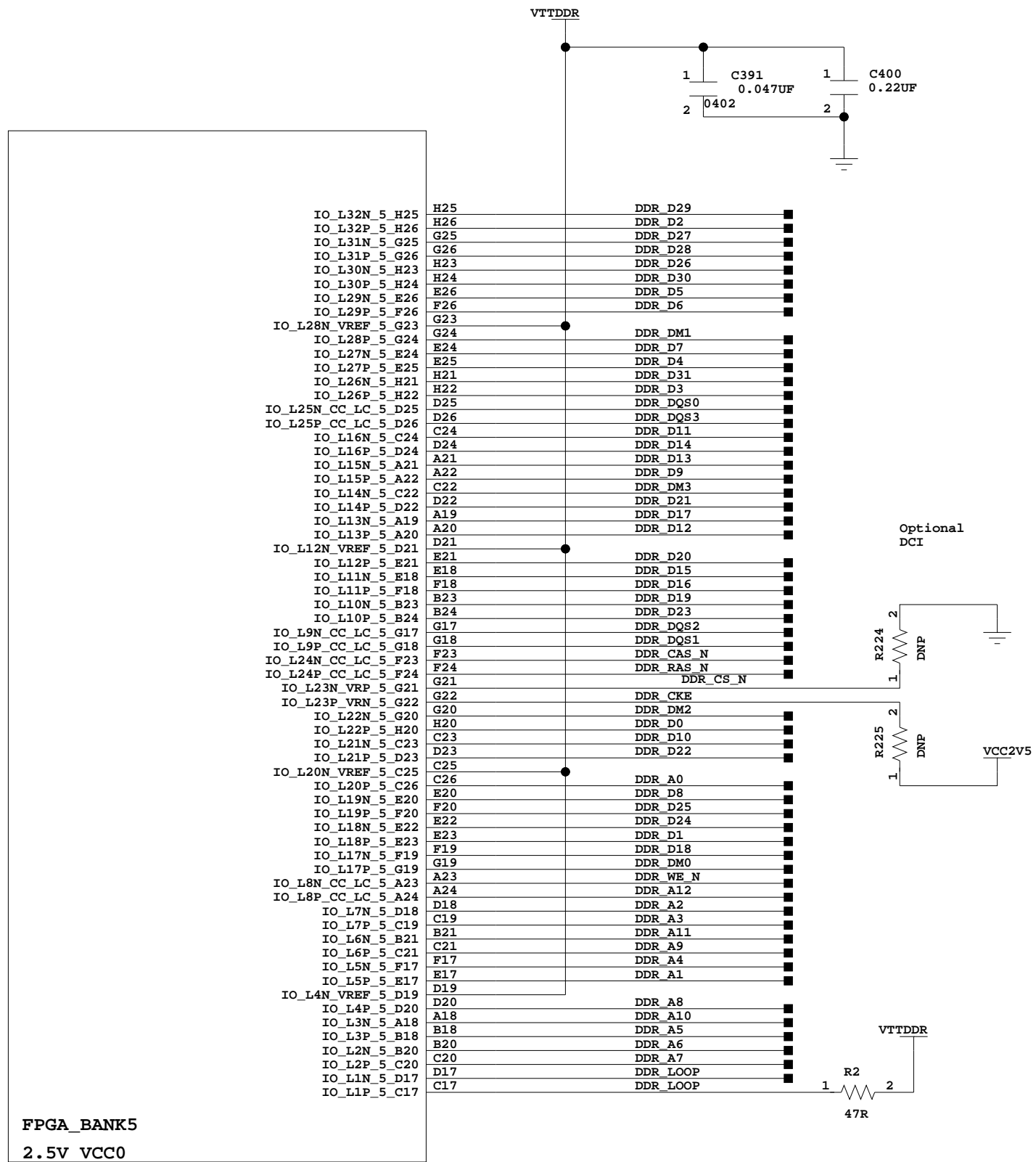
Configuration



Configuration



Title: FPGA Banks 0,1,2,3,4	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 2 of 24	Drawn By BF



Title:
FPGA Bank 5, 6

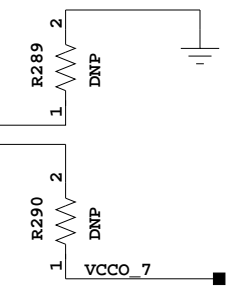
Date: _____ **Ver:** _____

Sheet Size: B **Rev:** B

Sheet 3 **of** 24 **Drawn By** BF

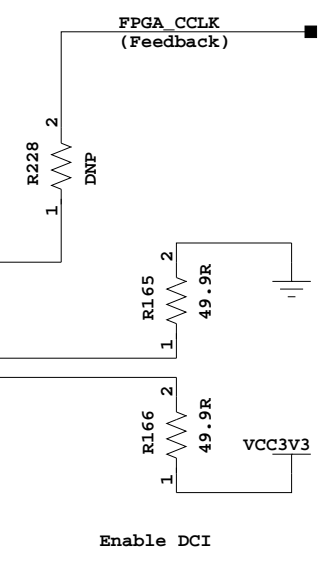
IO_L16N_7_AC24	AC24	HDR1_2
IO_L16P_7_AC23	AC23	HDR1_4
IO_L15N_7_AD23	AD23	HDR1_6
IO_L15P_7_AD22	AD22	HDR1_8
IO_L14N_7_AA23	AA23	HDR1_10
IO_L14P_7_AB23	AB23	HDR1_12
IO_L13N_7_AB22	AB22	HDR1_14
IO_L13P_7_AC22	AC22	HDR1_16
IO_L12N_VREF_7_Y23	Y23	HDR2_6
IO_L12P_7_Y22	Y22	HDR2_8
IO_L11N_7_AD26	AD26	HDR1_18
IO_L11P_7_AD25	AD25	HDR1_20
IO_L10N_7_AA26	AA26	HDR1_22
IO_L10P_7_AB26	AB26	HDR1_24
IO_L9N_CC_LC_7_AC26	AC26	HDR1_34
IO_L9P_CC_LC_7_AC25	AC25	HDR1_36
IO_L8N_CC_LC_7_Y24	Y24	HDR1_26
IO_L8P_CC_LC_7_AA24	AA24	HDR1_28
IO_L7N_7_AB25	AB25	HDR1_30
IO_L7P_7_AB24	AB24	HDR1_32
IO_L6N_7_Y26	Y26	HDR1_38
IO_L6P_7_Y25	Y25	HDR1_40
IO_L5N_7_V20	V20	HDR1_42
IO_L5P_7_W20	W20	HDR1_44
IO_L4N_VREF_7_W24	W24	HDR2_10
IO_L4P_7_W23	W23	HDR2_12
IO_L3N_7_W22	W22	HDR1_46
IO_L3P_7_W21	W21	HDR1_48
IO_L2N_7_W26	W26	HDR1_50
IO_L2P_7_W25	W25	HDR1_52
IO_L1N_7_V22	V22	HDR1_54
IO_L1P_7_V21	V21	HDR1_56
IO_L24N_CC_LC_7_AB21	AB21	HDR1_58
IO_L24P_CC_LC_7_AC21	AC21	HDR1_60
IO_L23N_VRP_7_AD20	AD20	HDR2_14
IO_L23P_VRN_7_AE20	AE20	HDR2_16
IO_L22N_7_AE24	AE24	HDR1_62
IO_L22P_7_AF24	AF24	HDR1_64
IO_L21N_7_Y18	Y18	HDR2_2
IO_L21P_7_AA18	AA18	HDR2_4
IO_L20N_VREF_7_Y21	Y21	HDR2_18
IO_L20P_7_Y20	Y20	HDR2_20
IO_L19N_7_AE23	AE23	HDR2_22
IO_L19P_7_AF23	AF23	HDR2_24
IO_L18N_7_W19	W19	HDR2_26
IO_L18P_7_Y19	Y19	HDR2_28
IO_L17N_7_AF20	AF20	HDR2_30
IO_L17P_7_AF19	AF19	HDR2_32
IO_L32N_SM7_7_AD21	AD21	HDR2_34 SYS MON VN7
IO_L32P_SM7_7_AE21	AE21	HDR2_36 SYS MON VP7
IO_L31N_SM6_7_AE18	AE18	HDR2_38 SYS MON VN6
IO_L31P_SM6_7_AF18	AF18	HDR2_40 SYS MON VP6
IO_L30N_SM5_7_AF22	AF22	HDR2_42 SYS MON VN5
IO_L30P_SM5_7_AF21	AF21	HDR2_44 SYS MON VP5
IO_L29N_SM4_7_AB18	AB18	HDR2_46 SYS MON VN4
IO_L29P_SM4_7_AC18	AC18	HDR2_48 SYS MON VP4
IO_L28N_VREF_7_AC20	AC20	HDR2_50
IO_L28P_7_AB20	AB20	HDR2_52
IO_L27N_SM3_7_AA17	AA17	HDR2_54 SYS MON VN3
IO_L27P_SM3_7_Y17	Y17	HDR2_56 SYS MON VP3
IO_L26N_SM2_7_AA20	AA20	HDR2_58 SYS MON VN2
IO_L26P_SM2_7_AA19	AA19	HDR2_60 SYS MON VP2
IO_L25N_CC_SM1_LC_7_AC19	AC19	HDR2_62 SYS MON VN1
IO_L25P_CC_SM1_LC_7_AD19	AD19	HDR2_64 SYS MON VP1

FPGA_BANK7
3.3V or 2.5V VCC0

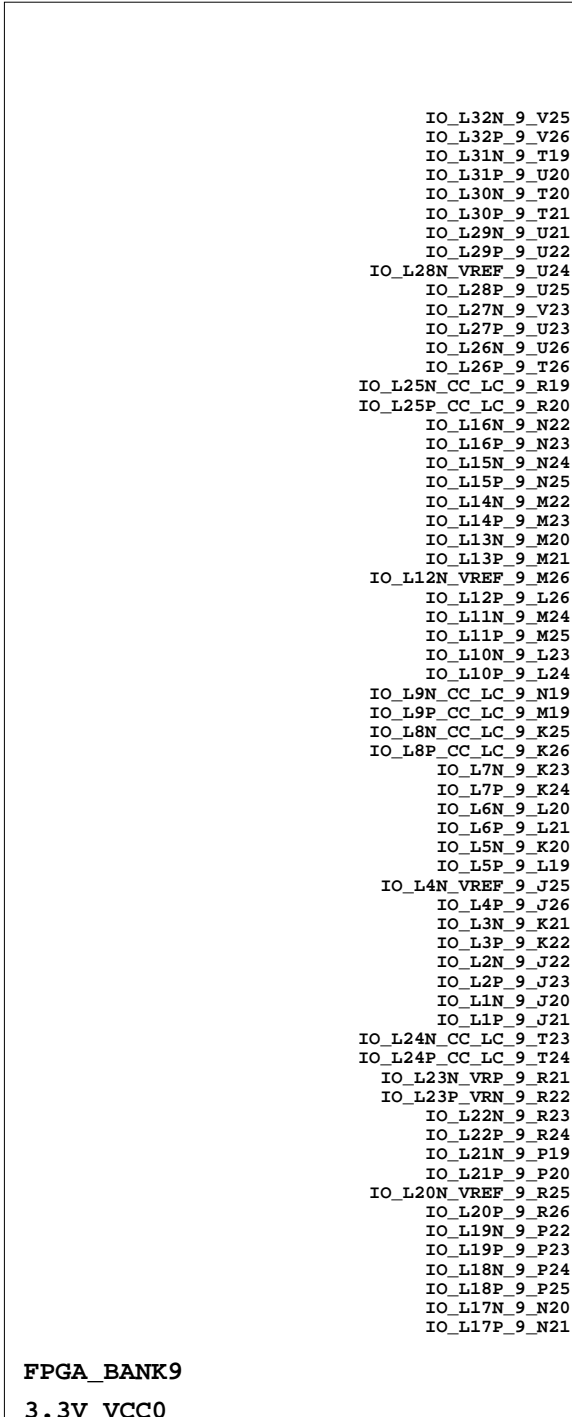


IO_L16N_8_AD1	AD1	SRAM FLASH A7
IO_L16P_8_AD2	AD2	SRAM FLASH A8
IO_L15N_8_AE3	AE3	SRAM FLASH A9
IO_L15P_8_AF3	AF3	SRAM FLASH A10
IO_L14N_8_AC1	AC1	SRAM FLASH A5
IO_L14P_8_AC2	AC2	SRAM FLASH A6
IO_L13N_8_AB5	AB5	SRAM FLASH A19
IO_L13P_8_AC5	AC5	SRAM FLASH A20
IO_L12N_VREF_8_AB2	AB2	SRAM FLASH A4
IO_L12P_8_AB3	AB3	SRAM FLASH A16
IO_L11N_8_AB4	AB4	SRAM FLASH A17
IO_L11P_8_AC4	AC4	SRAM FLASH A18
IO_L10N_8_AA1	AA1	SRAM FLASH A2
IO_L10P_8_AB1	AB1	SRAM FLASH A3
IO_L9N_CC_LC_8_Y5	Y5	SRAM BW1
IO_L9P_CC_LC_8_Y6	Y6	SRAM BW0
IO_L8N_CC_LC_8_Y3	Y3	SRAM BW3
IO_L8P_CC_LC_8_Y4	Y4	SRAM BW2
IO_L7N_8_AA3	AA3	SRAM FLASH A14
IO_L7P_8_AA4	AA4	SRAM FLASH A15
IO_L6N_8_Y1	Y1	SRAM FLASH A0
IO_L6P_8_Y2	Y2	SRAM FLASH A1
IO_L5N_8_W5	W5	SRAM FLASH A13
IO_L5P_8_W6	W6	SRAM FLASH A12
IO_L4N_VREF_8_W3	W3	SRAM FLASH A11
IO_L4P_8_W4	W4	SRAM ADV LD N
IO_L3N_8_V7	V7	SRAM CE1 N
IO_L3P_8_W7	W7	FLASH CE2
IO_L2N_8_V5	V5	USB INT
IO_L2P_8_V6	V6	BUS ERROR 1
IO_L1N_8_W1	W1	UART SOUT
IO_L1P_8_W2	W2	UART SIN
IO_L24N_CC_LC_8_AB6	AB6	SRAM FLASH WE N
IO_L24P_CC_LC_8_AC6	AC6	SRAM FLASH OE N
IO_L23N_VRP_8_AD7	AD7	
IO_L23P_VRN_8_AE7	AE7	
IO_L22N_8_AD4	AD4	SYSACE MPIRQ
IO_L22P_8_AD5	AD5	SYSACE MPCE
IO_L21N_8_Y9	Y9	SYSACE MPA06
IO_L21P_8_AA9	AA9	SYSACE MPA05
IO_L20N_VREF_8_Y7	Y7	SYSACE MPA04
IO_L20P_8_AA7	AA7	SYSACE USB D15
IO_L19N_8_AF5	AF5	SYSACE USB D14
IO_L19P_8_AF6	AF6	SYSACE USB D13
IO_L18N_8_AC3	AC3	SYSACE USB D12
IO_L18P_8_AD3	AD3	SYSACE USB D11
IO_L17N_8_AE4	AE4	SYSACE USB D10
IO_L17P_8_AF4	AF4	SYSACE USB D9
IO_L32N_8_AC8	AC8	SYSACE USB D8
IO_L32P_8_AD8	AD8	SYSACE USB D7
IO_L31N_8_AE9	AE9	SYSACE USB D6
IO_L31P_8_AF9	AF9	SYSACE USB D5
IO_L30N_8_AD6	AD6	SYSACE USB D4
IO_L30P_8_AE6	AE6	SYSACE USB D3
IO_L29N_8_AB9	AB9	SYSACE USB D2
IO_L29P_8_AC9	AC9	SYSACE USB D1
IO_L28N_VREF_8_AB7	AB7	SYSACE USB D0
IO_L28P_8_AC7	AC7	SYSACE MPA03
IO_L27N_8_AA10	AA10	SYSACE A2 USB A1
IO_L27P_8_Y10	Y10	SYSACE A1 USB A0
IO_L26N_8_Y8	Y8	SYSACE MPWE USB WR N
IO_L26P_8_AA8	AA8	SYSACE MPOE USB RD N
IO_L25N_CC_LC_8_AF7	AF7	SRAM CLK
IO_L25P_CC_LC_8_AF8	AF8	VGA CLK

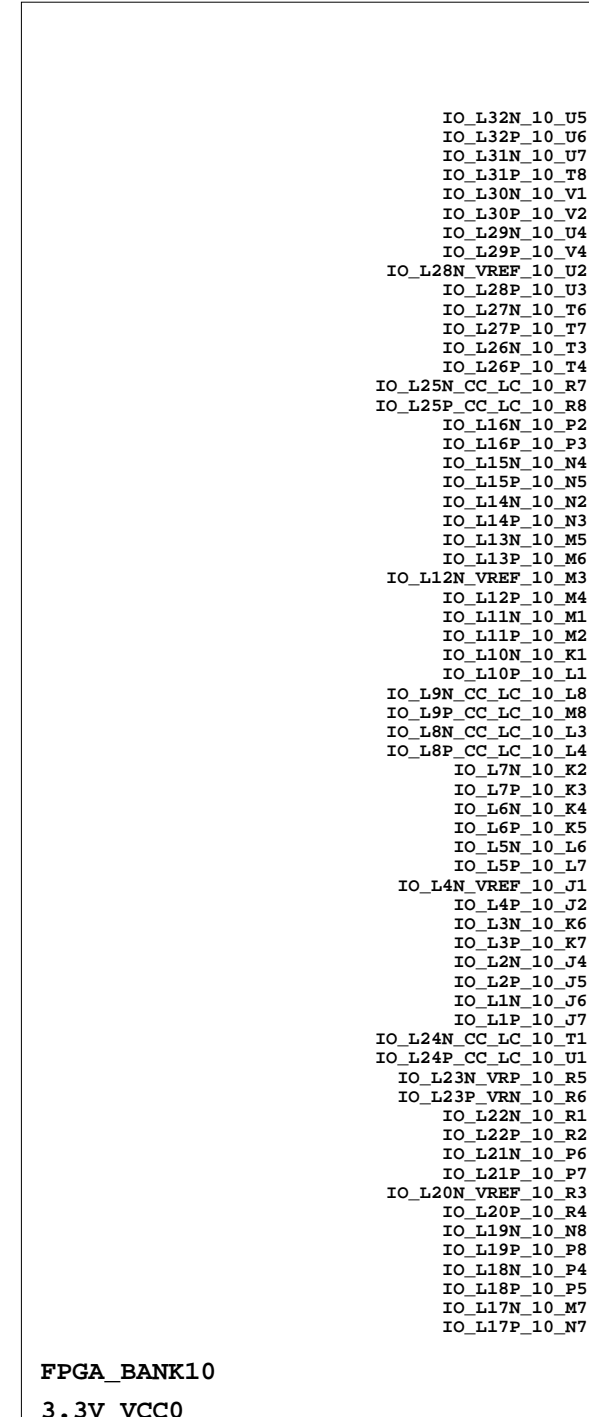
FPGA_BANK8
3.3V VCC0



Title:	
FPGA Bank 7, 8	
Date:	Ver:
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V25	SRAM ZZ
V26	SRAM MODE
T19	SRAM FLASH A21
U20	SRAM FLASH A22
T20	FLASH A0
T21	FLASH A23
U21	SYSACE MPBRDY
U22	SYSACE MPA00
U24	GPIO DIP SW8
U25	GPIO DIP SW7
V23	GPIO DIP SW6
U23	GPIO DIP SW5
U26	GPIO DIP SW4
T26	GPIO DIP SW3
R19	GPIO DIP SW2
R20	GPIO DIP SW1
N22	FLASH BYTE N
N23	VGA R0
N24	VGA R1
N25	VGA R2
M22	VGA G0
M23	VGA G1
M20	VGA G2
M21	VGA B0
M26	VGA B1
L26	VGA B2
M24	VGA BLANK N
M25	VGA PSAVE N
L23	VGA SYNC N
L24	BUS ERROR 2
N19	CPLD IO 1
M19	CPLD IO 2
K25	CPLD IO 3
K26	CPLD IO 4
K23	CPLD IO 5
K24	CPLD IO 6
L20	SRAM DQP0
L21	SRAM DQP1
K20	SRAM DQP2
L19	SRAM DQP3
J25	NC
J26	NC
K21	NC
K22	NC
J22	NC
J23	NC
J20	NC
J21	NC
T23	NC
T24	NC
R21	NC
R22	NC
R23	NC
R24	NC
P19	NC
P20	NC
R25	NC
R26	NC
P22	NC
P23	NC
P24	NC
P25	NC
N20	NC
N21	NC

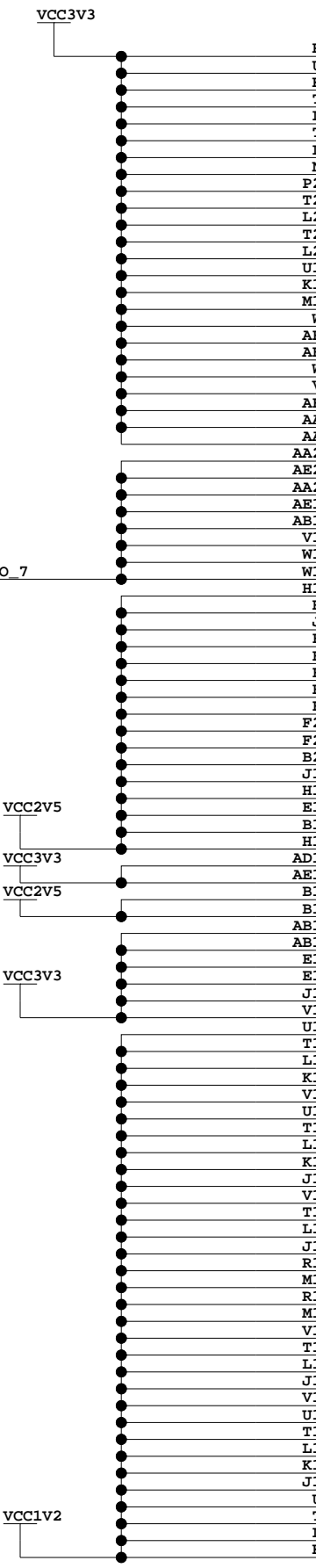
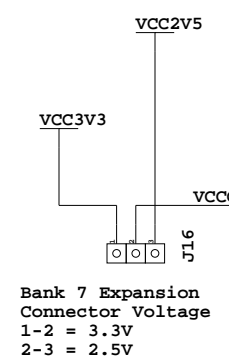
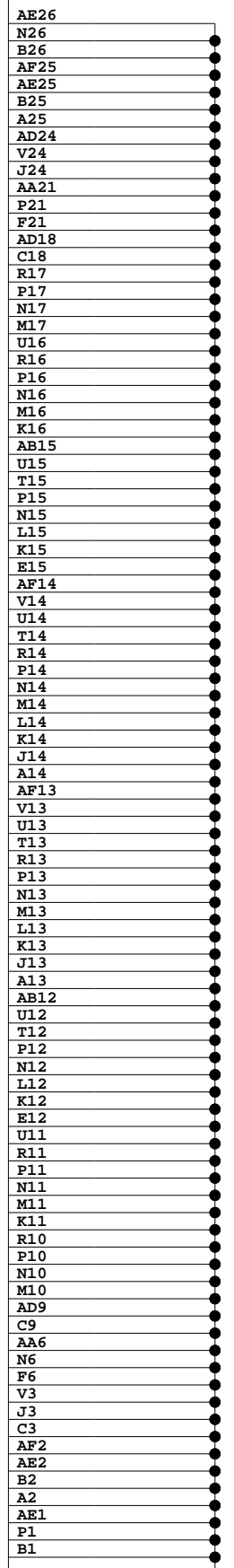


U5	NC
U6	NC
U7	NC
T8	NC
T8	NC
V1	NC
V2	NC
U4	NC
V4	NC
U2	NC
U3	NC
T6	NC
T7	NC
T7	NC
T3	NC
T4	NC
R7	NC
R8	NC
P2	NC
P2	NC
P3	NC
N4	NC
N4	NC
N5	NC
N2	NC
N3	NC
M5	NC
M6	NC
M3	NC
M4	NC
M1	NC
M2	NC
K1	NC
L1	NC
L1	NC
L8	NC
M8	NC
L3	NC
L3	NC
L4	NC
K2	NC
K3	NC
K4	NC
K5	NC
L6	NC
L7	NC
L7	NC
J1	NC
J2	NC
K6	NC
K7	NC
J4	NC
J5	NC
J6	NC
J7	NC
T1	NC
U1	NC
R5	NC
R6	NC
R1	NC
R2	NC
P6	NC
P7	NC
R3	NC
R4	NC
N8	NC
P8	NC
P4	NC
P5	NC
M7	NC
N7	NC



Title: FPGA Bank 9, 10	
Date:	Ver:
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GND_AE26
GND_N26
GND_B26
GND_AF25
GND_AE25
GND_B25
GND_A25
GND_AD24
GND_V24
GND_J24
GND_AA21
GND_F21
GND_P21
GND_AD18
GND_C18
GND_R17
GND_P17
GND_N17
GND_M17
GND_U16
GND_R16
GND_P16
GND_N16
GND_M16
GND_K16
GND_AB15
GND_U15
GND_T15
GND_P15
GND_N15
GND_L15
GND_K15
GND_E15
GND_AF14
GND_V14
GND_U14
GND_T14
GND_R14
GND_P14
GND_N14
GND_M14
GND_L14
GND_K14
GND_J14
GND_A14
GND_AF13
GND_V13
GND_U13
GND_T13
GND_R13
GND_P13
GND_N13
GND_M13
GND_L13
GND_K13
GND_J13
GND_A13
GND_AB12
GND_U12
GND_T12
GND_P12
GND_N12
GND_L12
GND_K12
GND_E12
GND_U11
GND_R11
GND_P11
GND_N11
GND_M11
GND_K11
GND_R10
GND_P10
GND_N10
GND_M10
GND_AD9
GND_C9
GND_AA6
GND_N6
GND_F6
GND_V3
GND_J3
GND_C3
GND_AF2
GND_AE2
GND_B2
GND_A2
GND_AE1
GND_P1
GND_B1



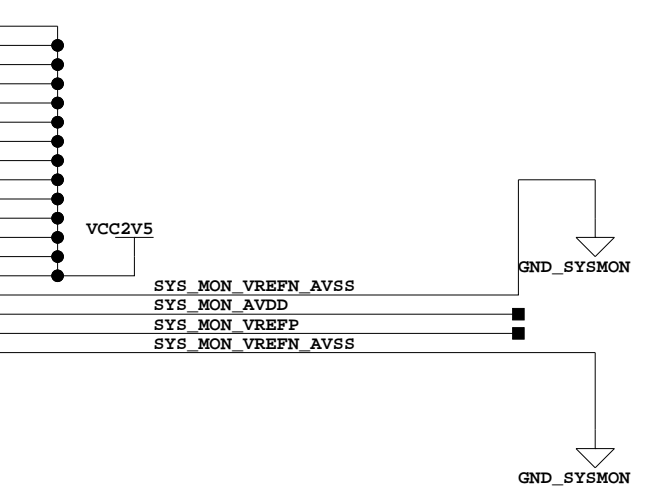
R9
U8
K8
T5
L5
T2
L2
N1
P26
T25
L25
T22
L22
U19
K19
M18
W9
AE8
AB8
W8
V8
AE5
AA5
AA2
AA25
AE22
AA22
AE19
AB19
V19
W18
W17
H10
H9
J8
E8
B8
F5
B5
F2
F25
F22
B22
J19
H19
E19
B19
H18
AD15
AE11
B16
B11
AB16
AB11
E16
E11
J15
V12
U18
T18
L18
K18
V17
U17
T17
L17
K17
J17
V16
T16
L16
J16
R15
M15
R12
M12
V11
T11
L11
J11
V10
U10
T10
L10
K10
J10
U9
T9
L9
K9

VCCO_10_R9
VCCO_10_U8
VCCO_10_K8
VCCO_10_T5
VCCO_10_L5
VCCO_10_T2
VCCO_10_L2
VCCO_10_N1
VCCO_9_P26
VCCO_9_T25
VCCO_9_L25
VCCO_9_T22
VCCO_9_L22
VCCO_9_U19
VCCO_9_K19
VCCO_9_M18
VCCO_8_W9
VCCO_8_AE8
VCCO_8_AB8
VCCO_8_W8
VCCO_8_V8
VCCO_8_AE5
VCCO_8_AA5
VCCO_8_AA2
VCCO_7_AA25
VCCO_7_AE22
VCCO_7_AA22
VCCO_7_AE19
VCCO_7_AB19
VCCO_7_V19
VCCO_7_W18
VCCO_7_W17
VCCO_6_H10
VCCO_6_H9
VCCO_6_J8
VCCO_6_E8
VCCO_6_B8
VCCO_6_F5
VCCO_6_B5
VCCO_6_F2
VCCO_5_F25
VCCO_5_F22
VCCO_5_B22
VCCO_5_J19
VCCO_5_H19
VCCO_5_E19
VCCO_5_B19
VCCO_5_H18
VCCO_4_AD15
VCCO_4_AE11
VCCO_3_B16
VCCO_3_B11
VCCO_2_AB16
VCCO_2_AB11
VCCO_1_E16
VCCO_1_E11
VCCO_0_J15
VCCO_0_V12

VCCO_U18
VCCO_T18
VCCO_L18
VCCO_K18
VCCO_V17
VCCO_U17
VCCO_T17
VCCO_L17
VCCO_K17
VCCO_J17
VCCO_V16
VCCO_T16
VCCO_L16
VCCO_J16
VCCO_R15
VCCO_M15
VCCO_R12
VCCO_M12
VCCO_V11
VCCO_T11
VCCO_L11
VCCO_J11
VCCO_V10
VCCO_U10
VCCO_T10
VCCO_L10
VCCO_K10
VCCO_J10
VCCO_U9
VCCO_T9
VCCO_L9
VCCO_K9

VCCAUX_R18
VCCAUX_P18
VCCAUX_N18
VCCAUX_H17
VCCAUX_W16
VCCAUX_H16
VCCAUX_V15
VCCAUX_J12
VCCAUX_W11
VCCAUX_H11
VCCAUX_W10
VCCAUX_P9
VCCAUX_N9
VCCAUX_M9
AVSS_SM_AE17
AVDD_SM_AF17
VREFP_SM_AE16
VREFN_SM_AE15

R18
P18
N18
H17
W16
H16
V15
J12
W11
H11
W10
P9
N9
M9
AE17
AF17
AE16
AE15

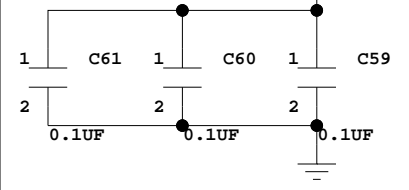
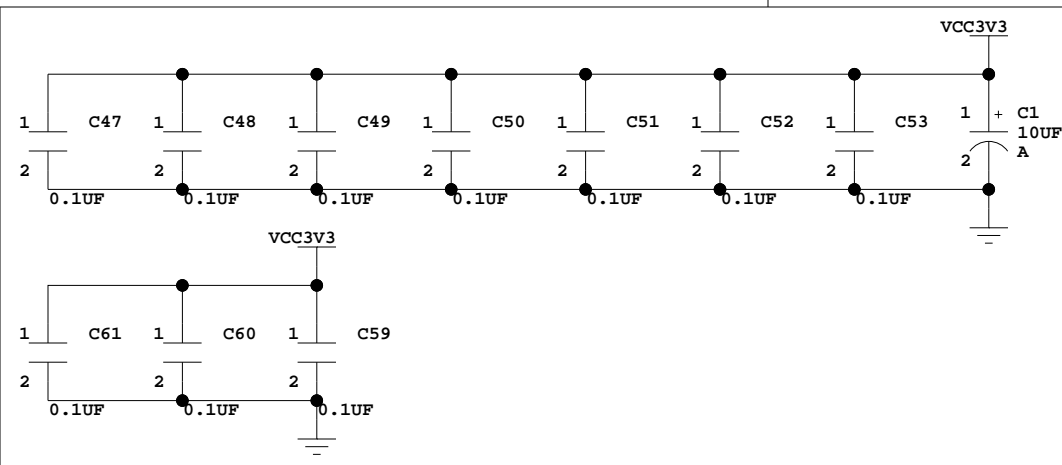


FPGA_GND

FPGA_PWR



Title: FPGA Ground and Power	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 6 of 24	Drawn By BF

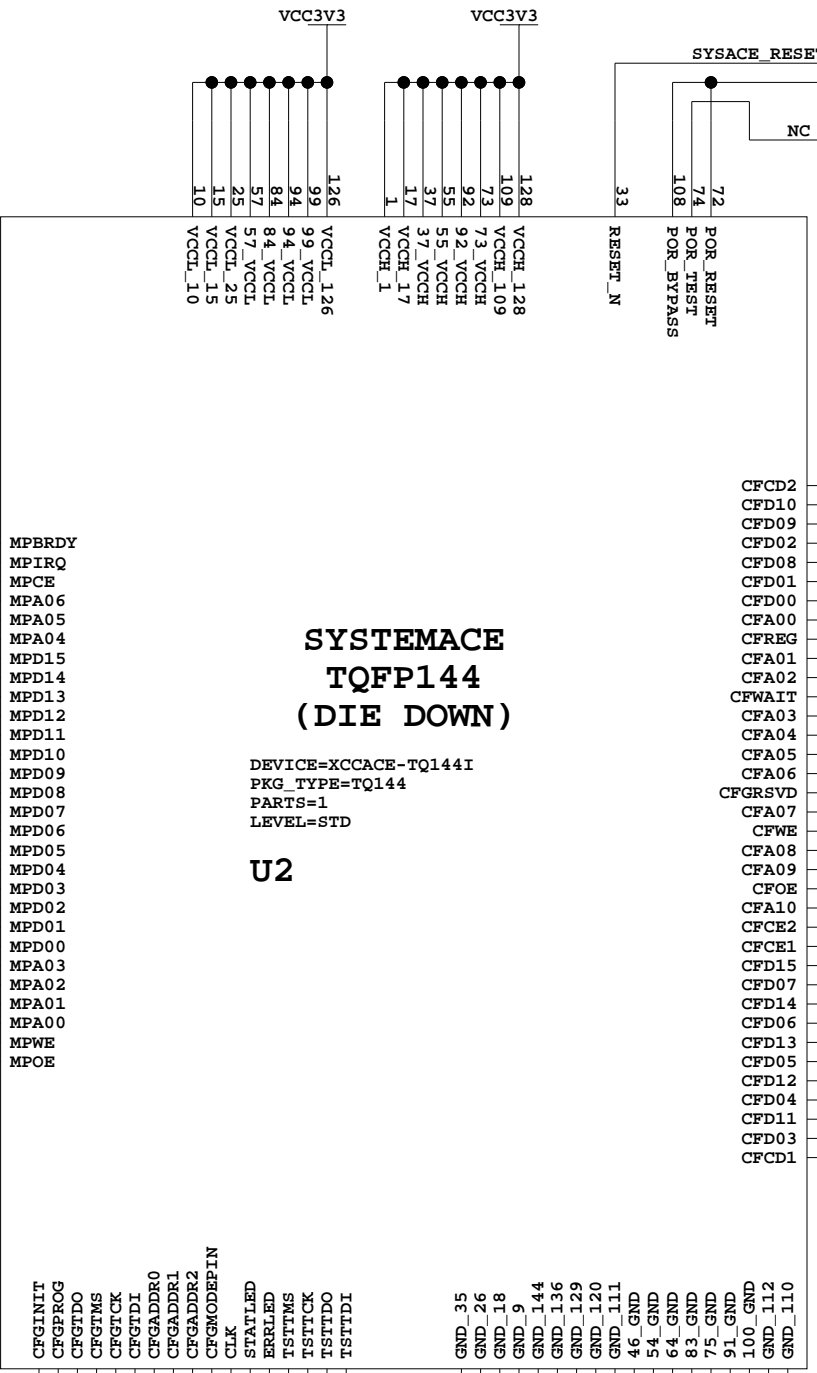


■	SYSACE MPBRDY	39	MPBRDY
■	SYSACE MPIRQ	41	MPIRQ
■	SYSACE MPCE	42	MPCE
■	SYSACE MPA06	43	MPA06
■	SYSACE MPA05	44	MPA05
■	SYSACE MPA04	45	MPA04
■	SYSACE USB D15	47	MPD15
■	SYSACE USB D14	48	MPD14
■	SYSACE USB D13	49	MPD13
■	SYSACE USB D12	50	MPD12
■	SYSACE USB D11	51	MPD11
■	SYSACE USB D10	52	MPD10
■	SYSACE USB D9	53	MPD09
■	SYSACE USB D8	56	MPD08
■	SYSACE USB D7	58	MPD07
■	SYSACE USB D6	59	MPD06
■	SYSACE USB D5	60	MPD05
■	SYSACE USB D4	61	MPD04
■	SYSACE USB D3	62	MPD03
■	SYSACE USB D2	63	MPD02
■	SYSACE USB D1	65	MPD01
■	SYSACE USB D0	66	MPD00
■	SYSACE MPA03	67	MPA03
■	SYSACE A2 USB A1	68	MPA02
■	SYSACE A1 USB A0	69	MPA01
■	SYSACE MPA00	70	MPA00
■	SYSACE MPWE USB WR_N	76	MPWE
■	SYSACE MPOE USB RD_N	77	MPOE

**SYSTEMACE
TQFP144
(DIE DOWN)**

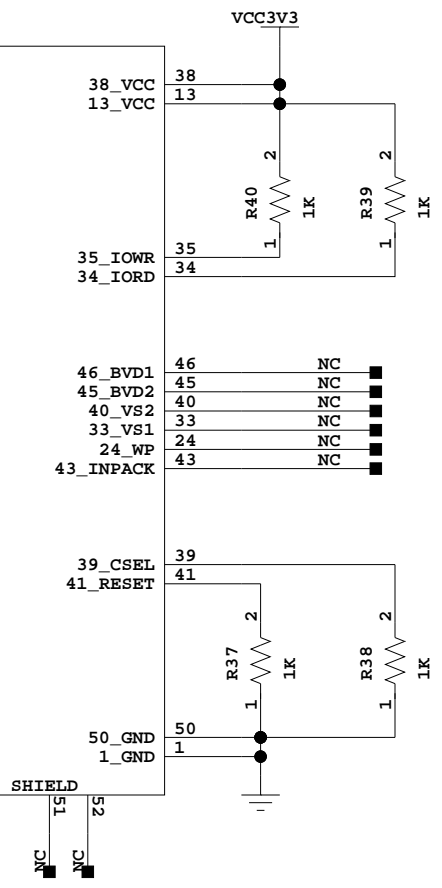
DEVICE=XCCACE-TQ144I
PKG_TYPE=TQ144
PARTS=1
LEVEL=STD

U2

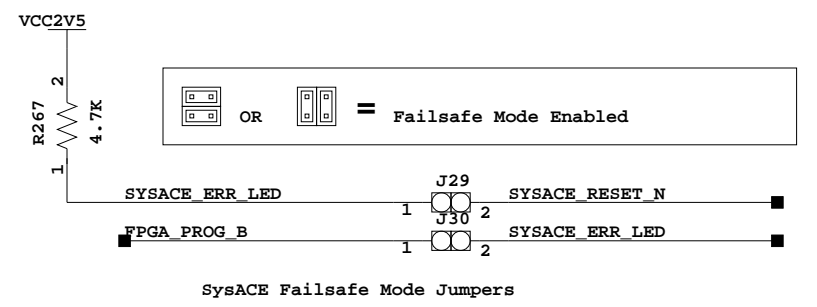
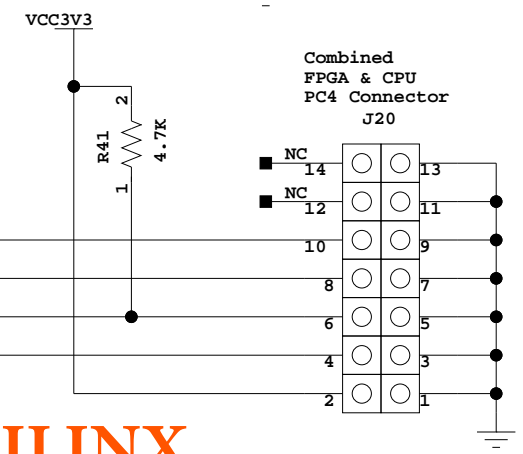
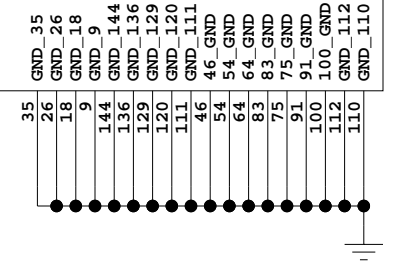
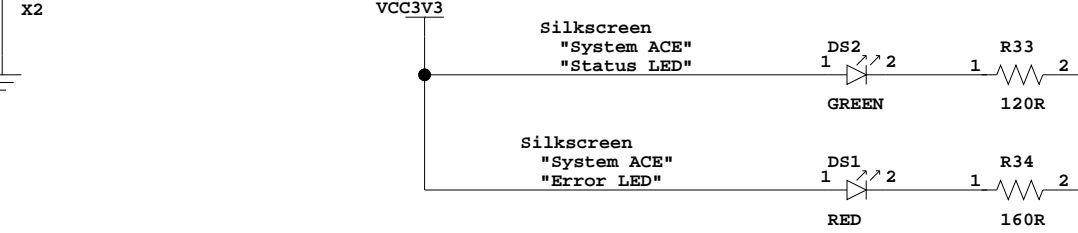
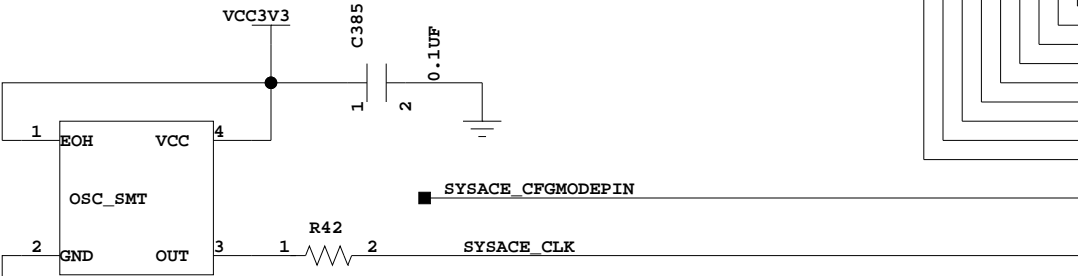
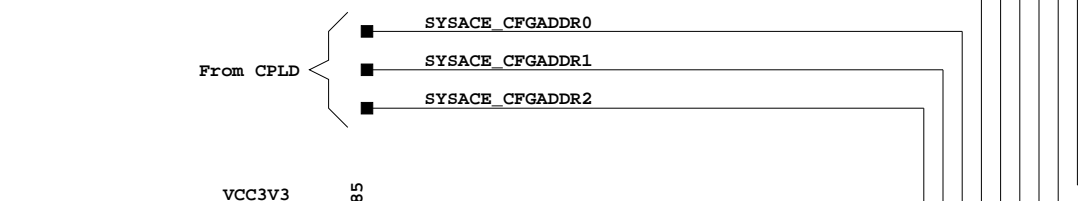
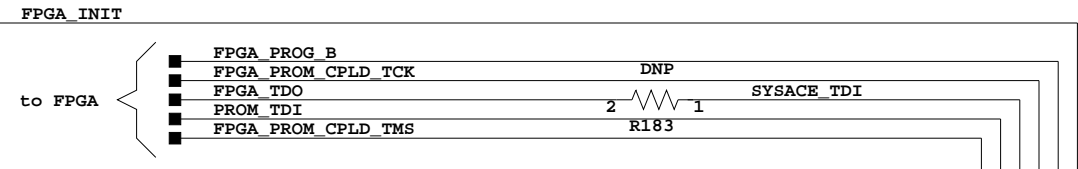


CFCD2	13	SYSACE CFCD2	25	25_CD2
CFD10	12	SYSACE CFD10	49	49_D10
CFD09	11	SYSACE CFD09	48	48_D09
CFD02	8	SYSACE CFD02	23	23_D02
CFD08	7	SYSACE CFD08	47	47_D08
CFD01	6	SYSACE CFD01	22	22_D01
CFD00	5	SYSACE CFD00	21	21_D00
CFA00	4	SYSACE CFA00	20	20_A00
CFREG	3	SYSACE CFREG	44	44_REG
CFA01	142	SYSACE CFA01	19	19_A01
CFA02	141	SYSACE CFA02	18	18_A02
CFWAIT	140	SYSACE CFWAIT	42	42_WAIT
CFA03	139	SYSACE CFA03	17	17_A03
CFA04	137	SYSACE CFA04	16	16_A04
CFA05	135	SYSACE CFA05	15	15_A05
CFA06	134	SYSACE CFA06	14	14_A06
CFGRSVD	133	SYSACE CFRDBSY	37	37_RDY/BSY
CFA07	132	SYSACE CFA07	12	12_A07
CFWE	131	SYSACE CFWE	36	36_WE
CFA08	130	SYSACE CFA08	11	11_A08
CFA09	125	SYSACE CFA09	10	10_A09
CFOE	123	SYSACE CFDE	9	9_OEI
CFA10	121	SYSACE CFA10	8	8_A10
CFCE2	138	SYSACE CFCE2	32	32_CE2
CFCE1	119	SYSACE CFCE1	7	7_CE1I
CFD15	118	SYSACE CFD15	31	31_D15
CFD07	117	SYSACE CFD07	6	6_D07
CFD14	116	SYSACE CFD14	30	30_D14
CFD06	115	SYSACE CFD06	5	5_D06
CFD13	114	SYSACE CFD13	29	29_D13
CFD05	113	SYSACE CFD05	4	4_D05
CFD12	107	SYSACE CFD12	28	28_D12
CFD04	106	SYSACE CFD04	3	3_D04
CFD11	105	SYSACE CFD11	27	27_D11
CFD03	104	SYSACE CFD03	2	2_D03
CFCD1	103	SYSACE CFCD1	26	26_CD1

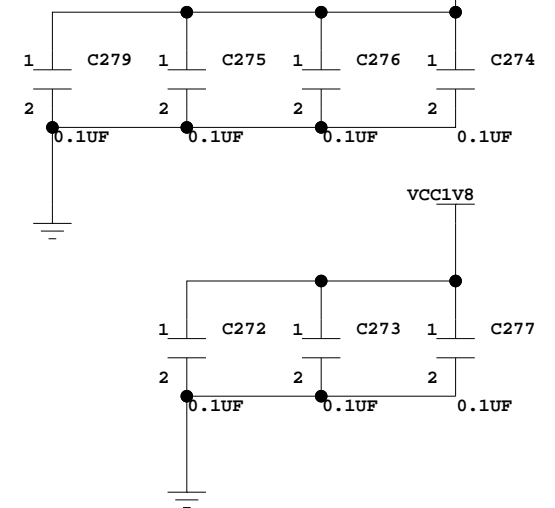
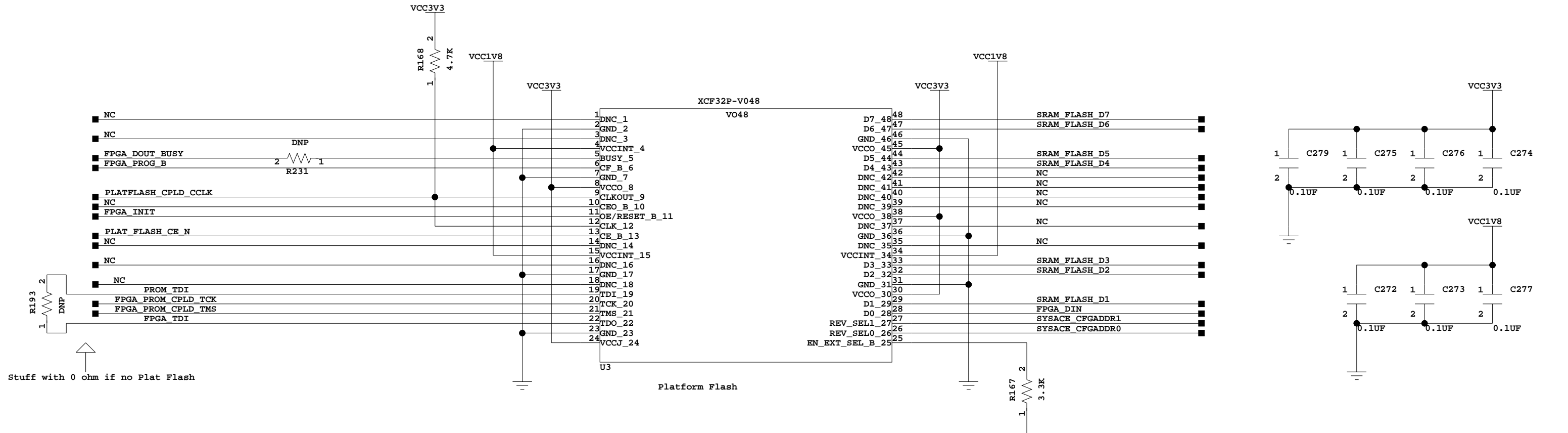
ACEFLASH



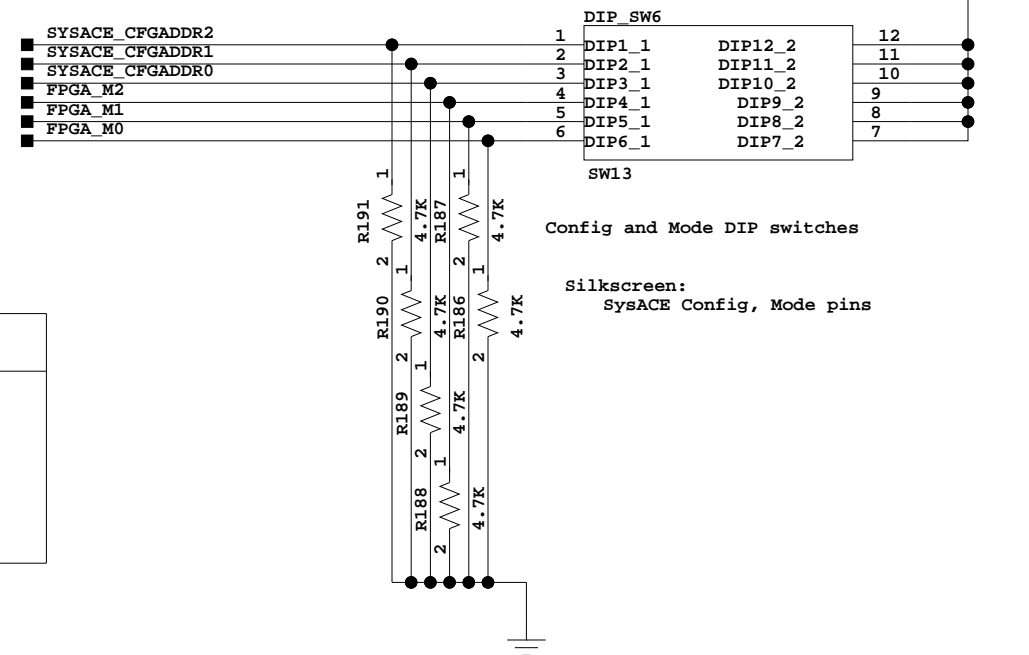
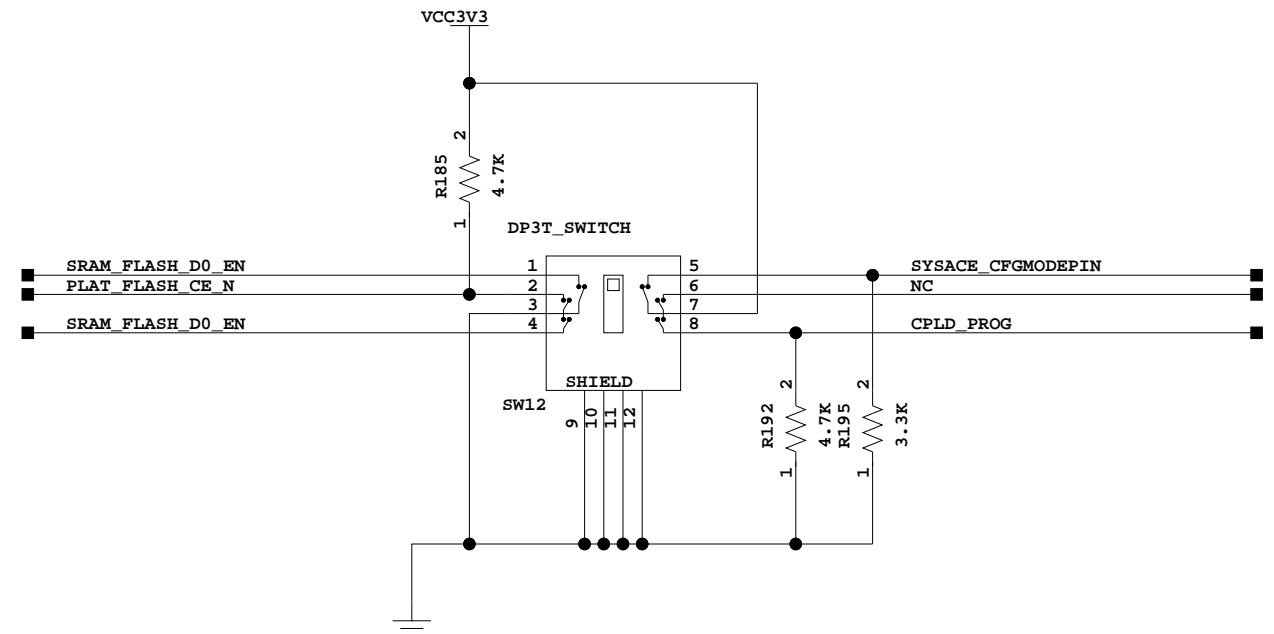
P113



Title:		System ACE	
Date:		Ver:	
Sheet Size:	B	Rev:	B
Sheet	7 of 24	Drawn By	BF

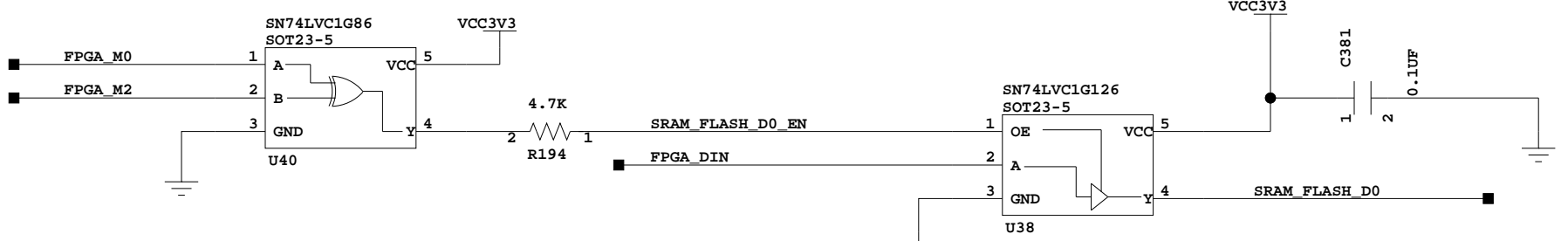



System ACE / Platform Flash / CPLD Flash Configuration Switch



m0	m2	Cfg Switch	D0/DIN Short
0	0	SysACE/CPLD	OPEN
0	1	SysACE/CPLD	OPEN
1	0	SysACE/CPLD	OPEN
1	1	SysACE/CPLD	OPEN
0	0	Plat FLASH	OPEN
0	1	Plat FLASH	SHORT
1	0	Plat FLASH	SHORT
1	1	Plat FLASH	OPEN

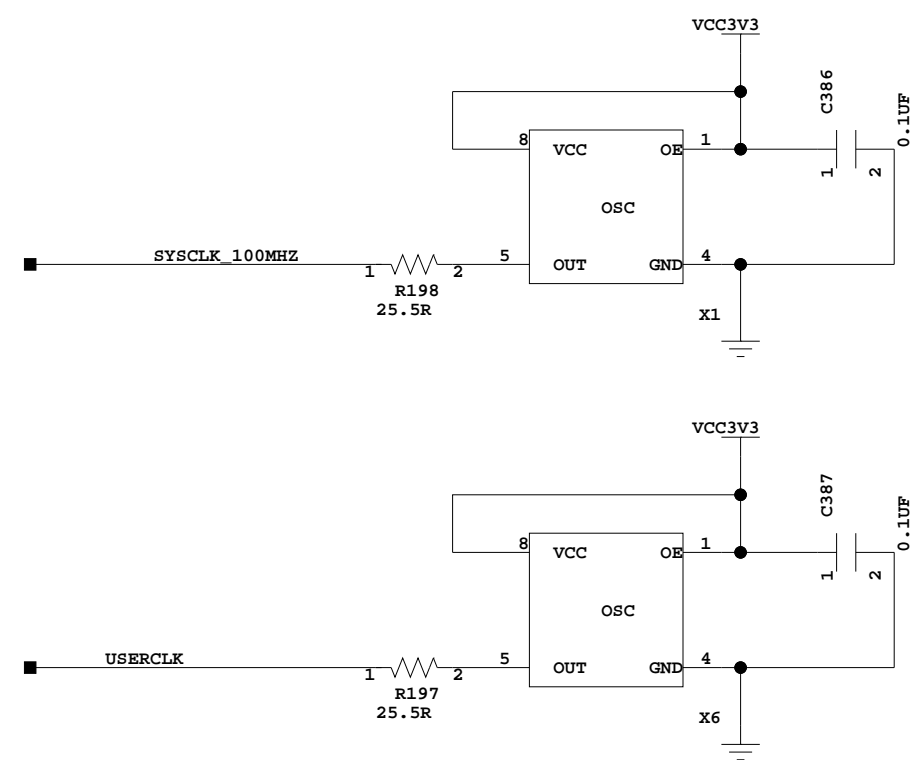
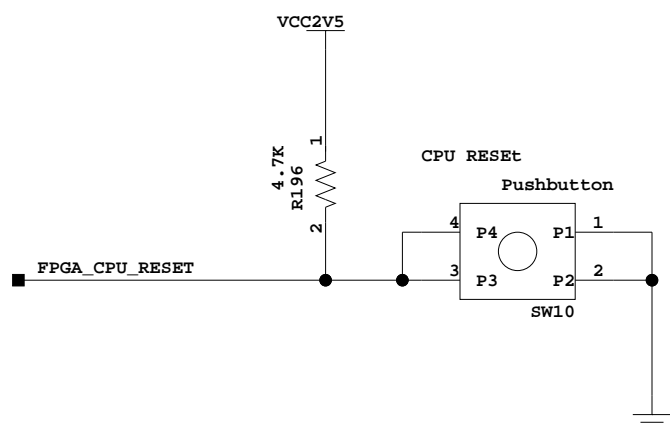
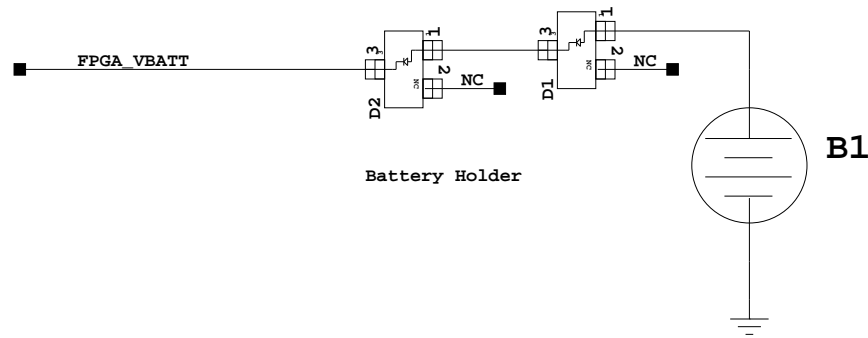
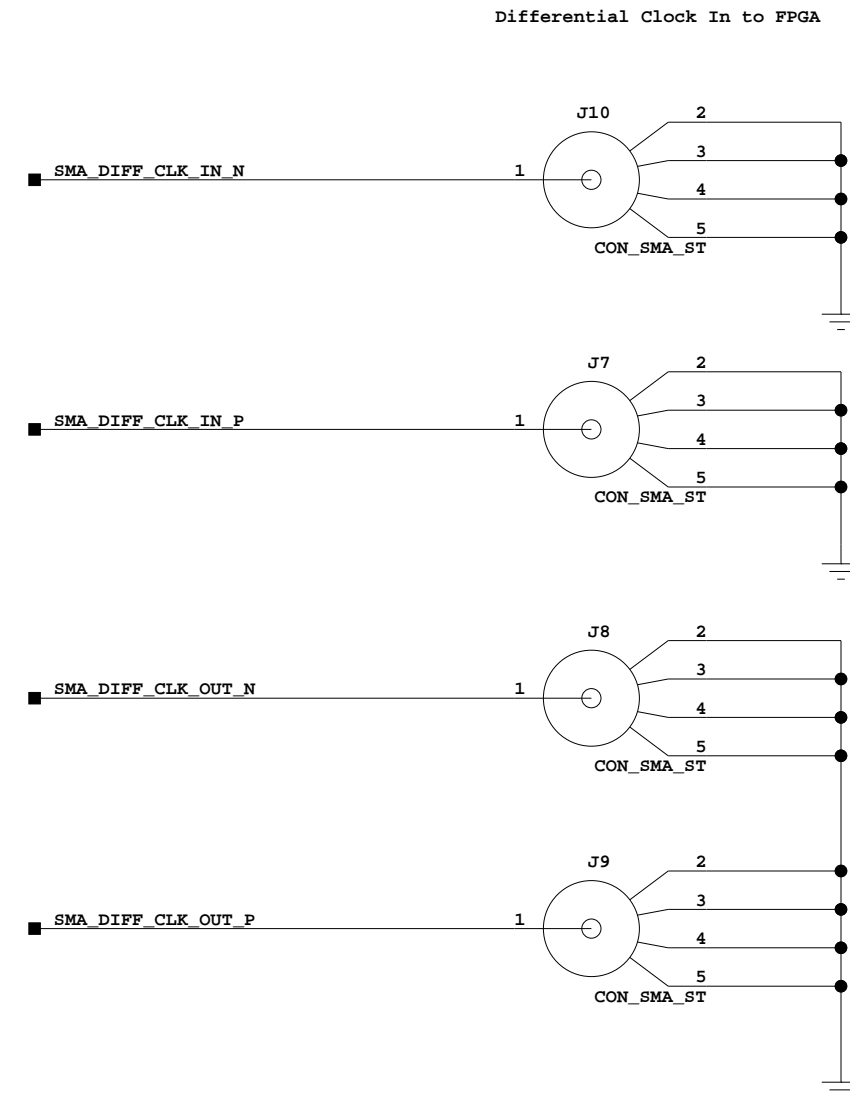
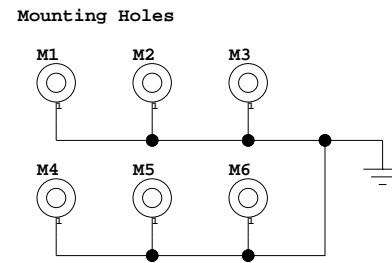
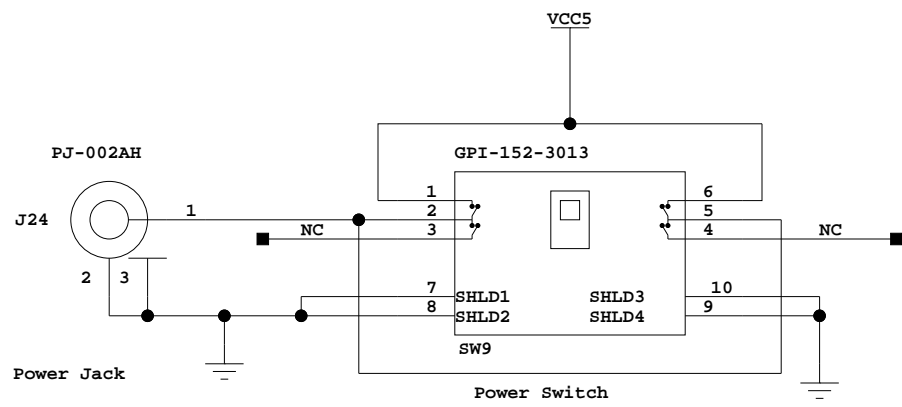
Toggles connection from Plat Flash D0 to SRAM D0





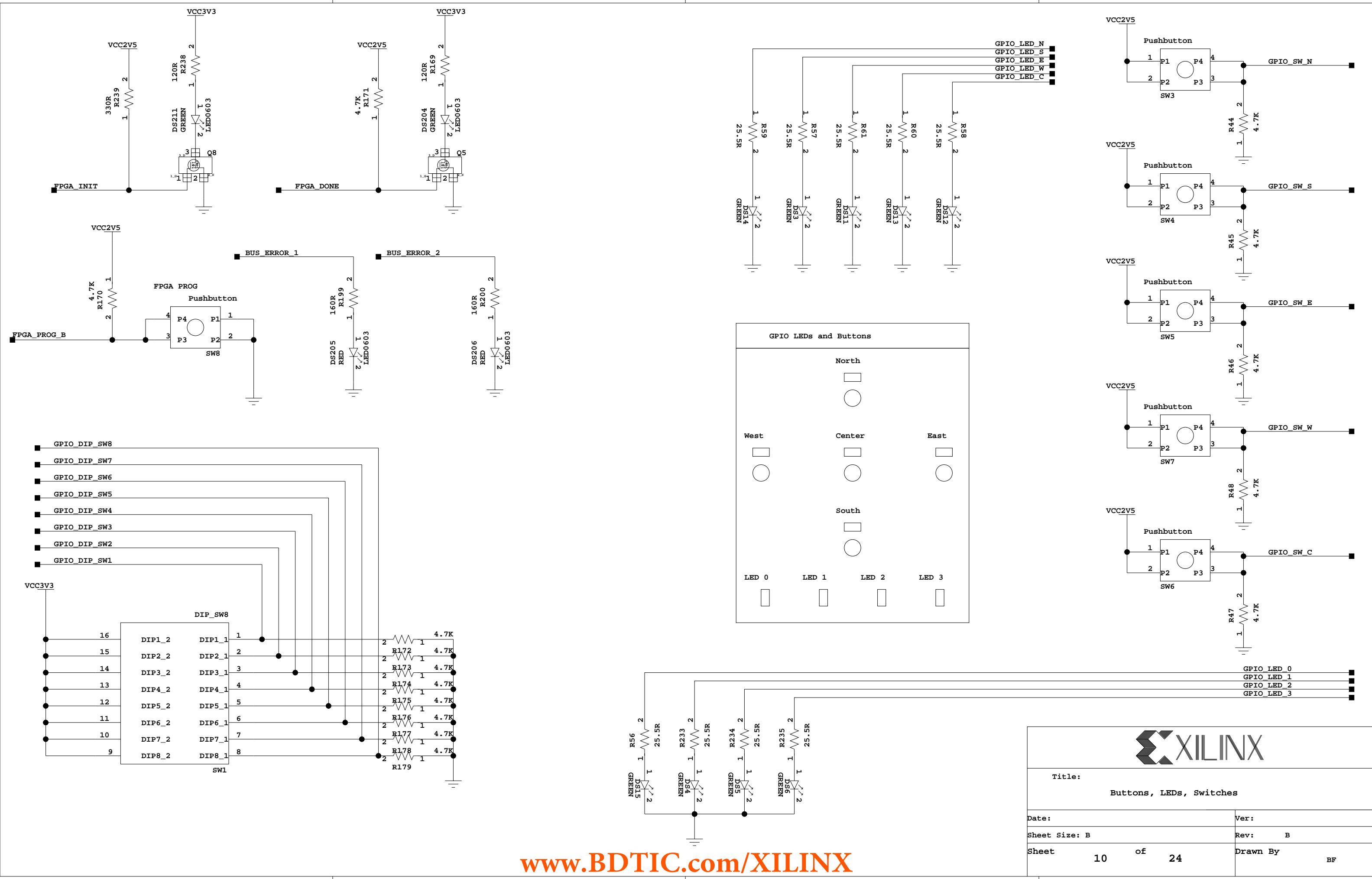
Title: Platform Flash

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 8 of 24	Drawn By BF



Differential Clock Out from FPGA

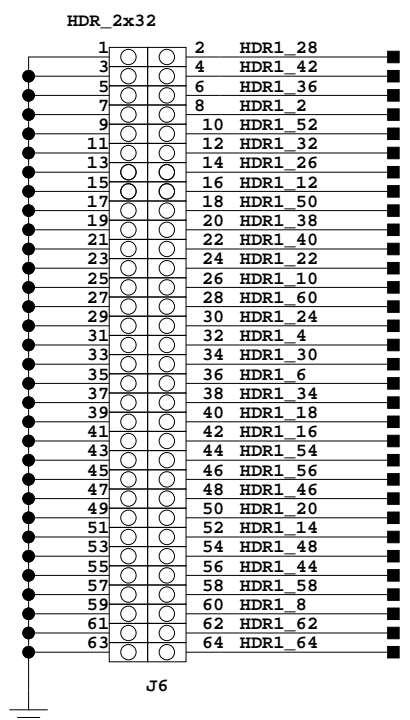
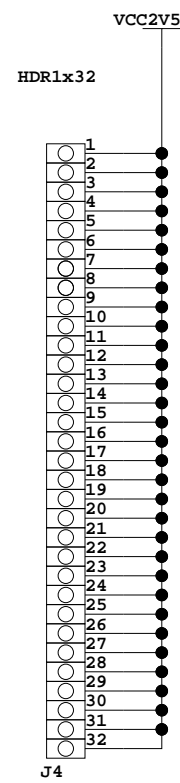
Title: SMA Connectors, Power Switch, Battery, Oscillators, Reset	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 9 of 24	Drawn By BF



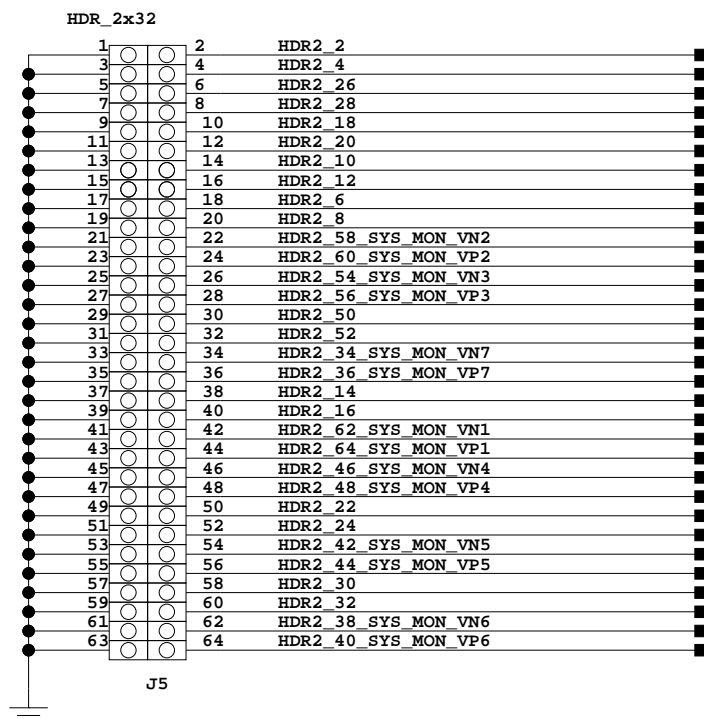
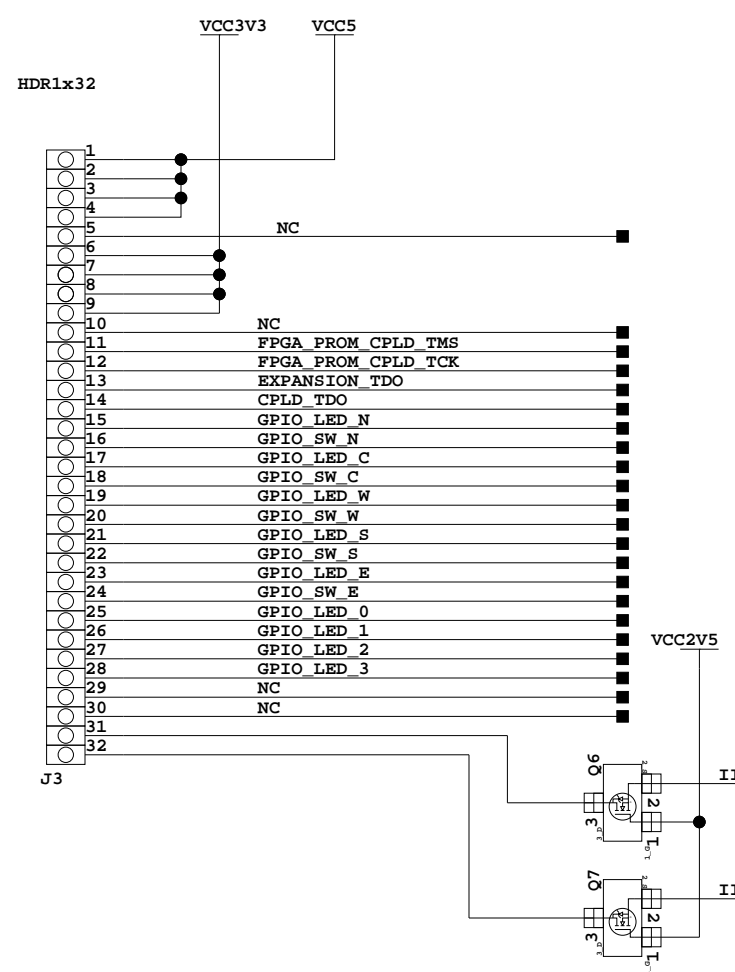
XILINX

Title: Buttons, LEDs, Switches

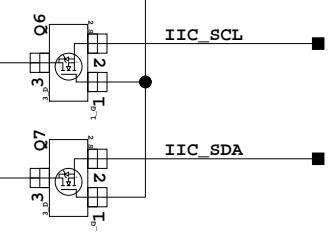
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 10 of 24	Drawn By BF



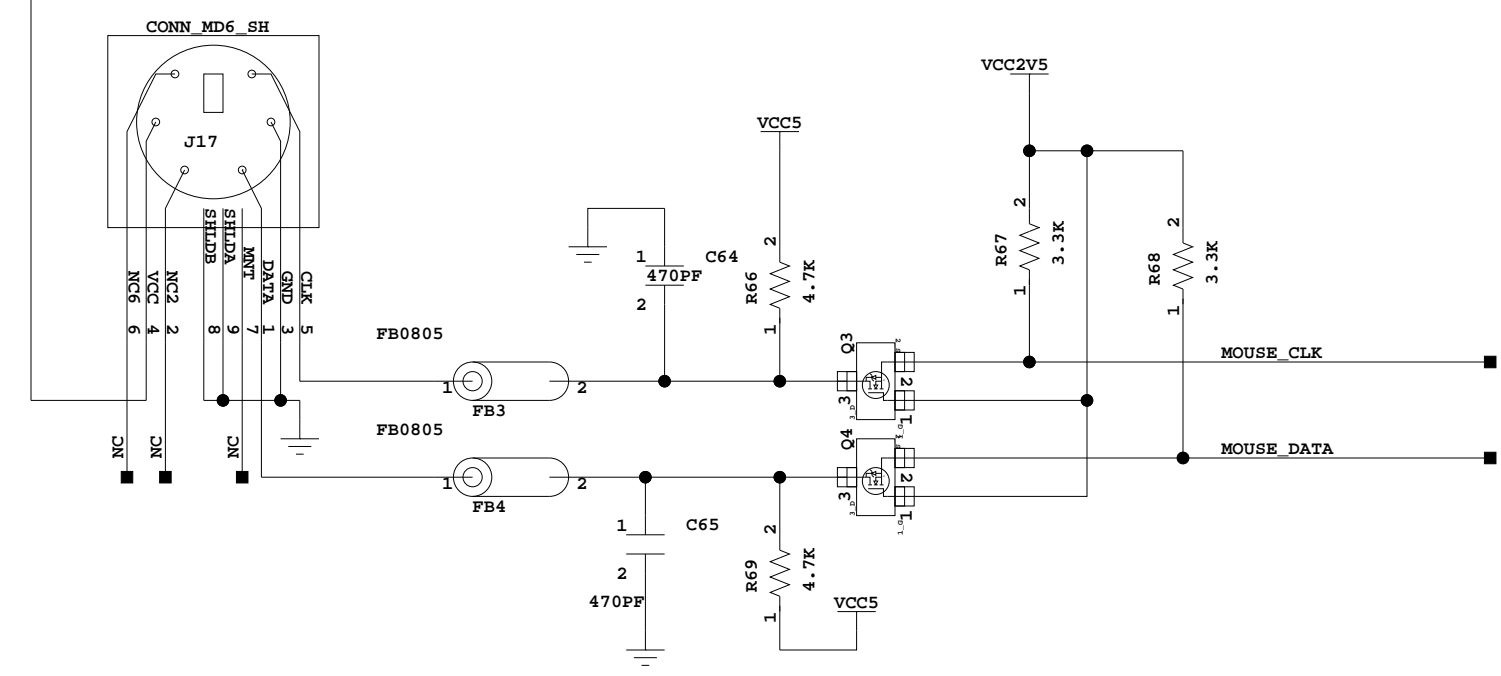
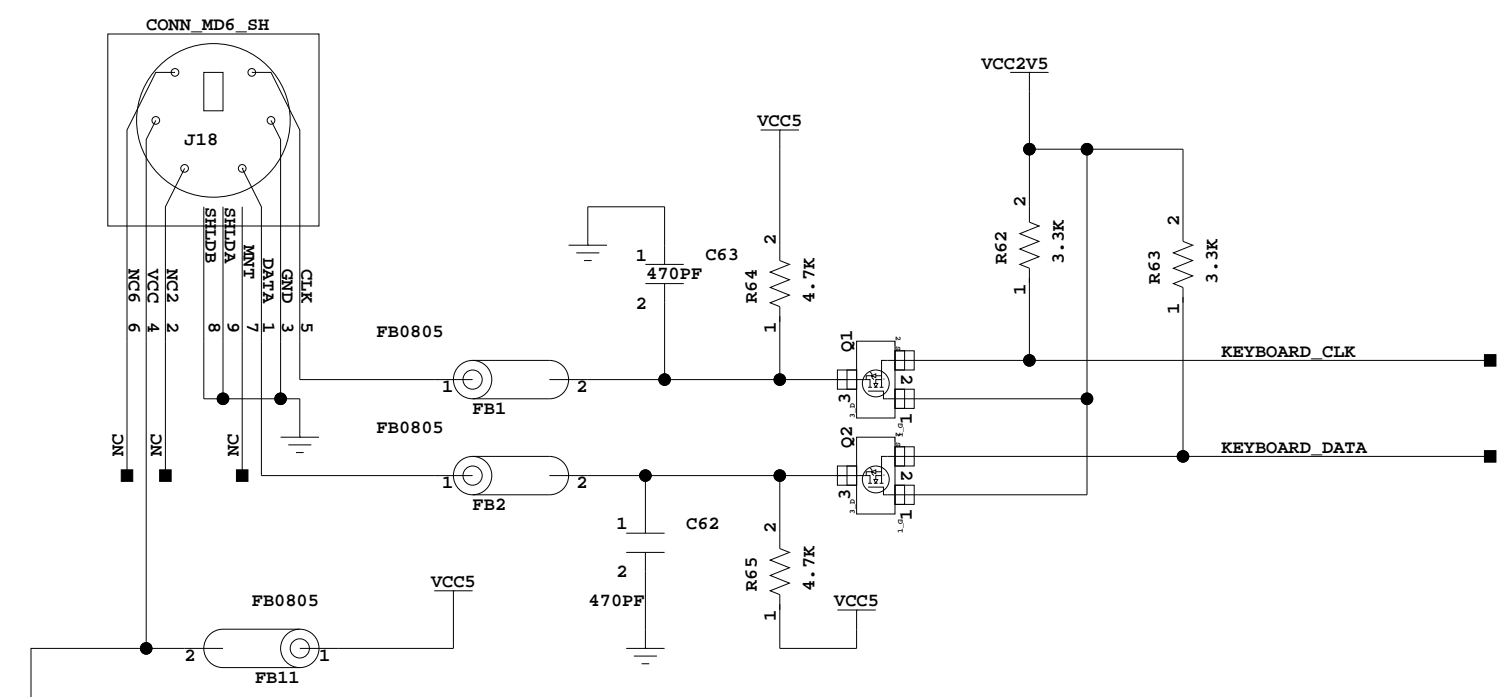
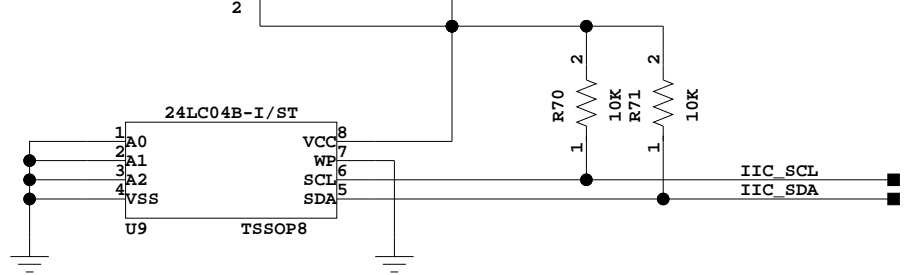
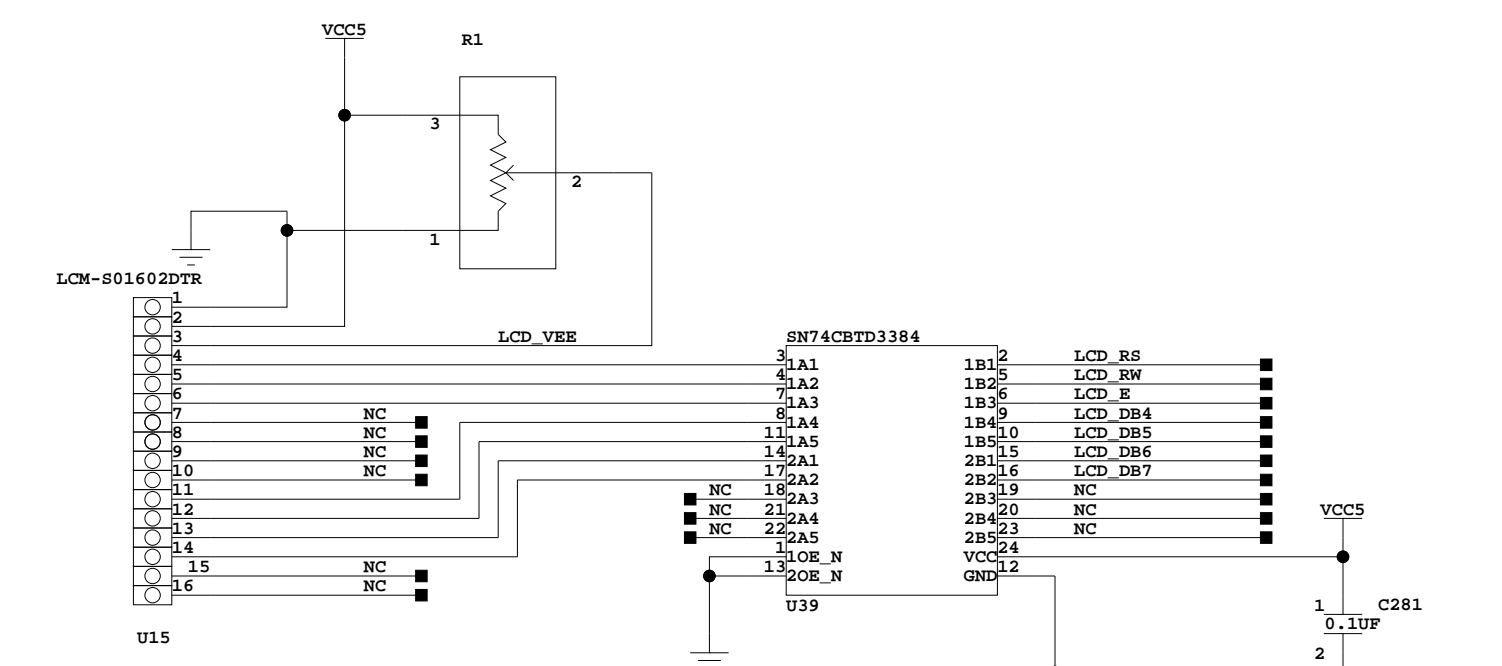
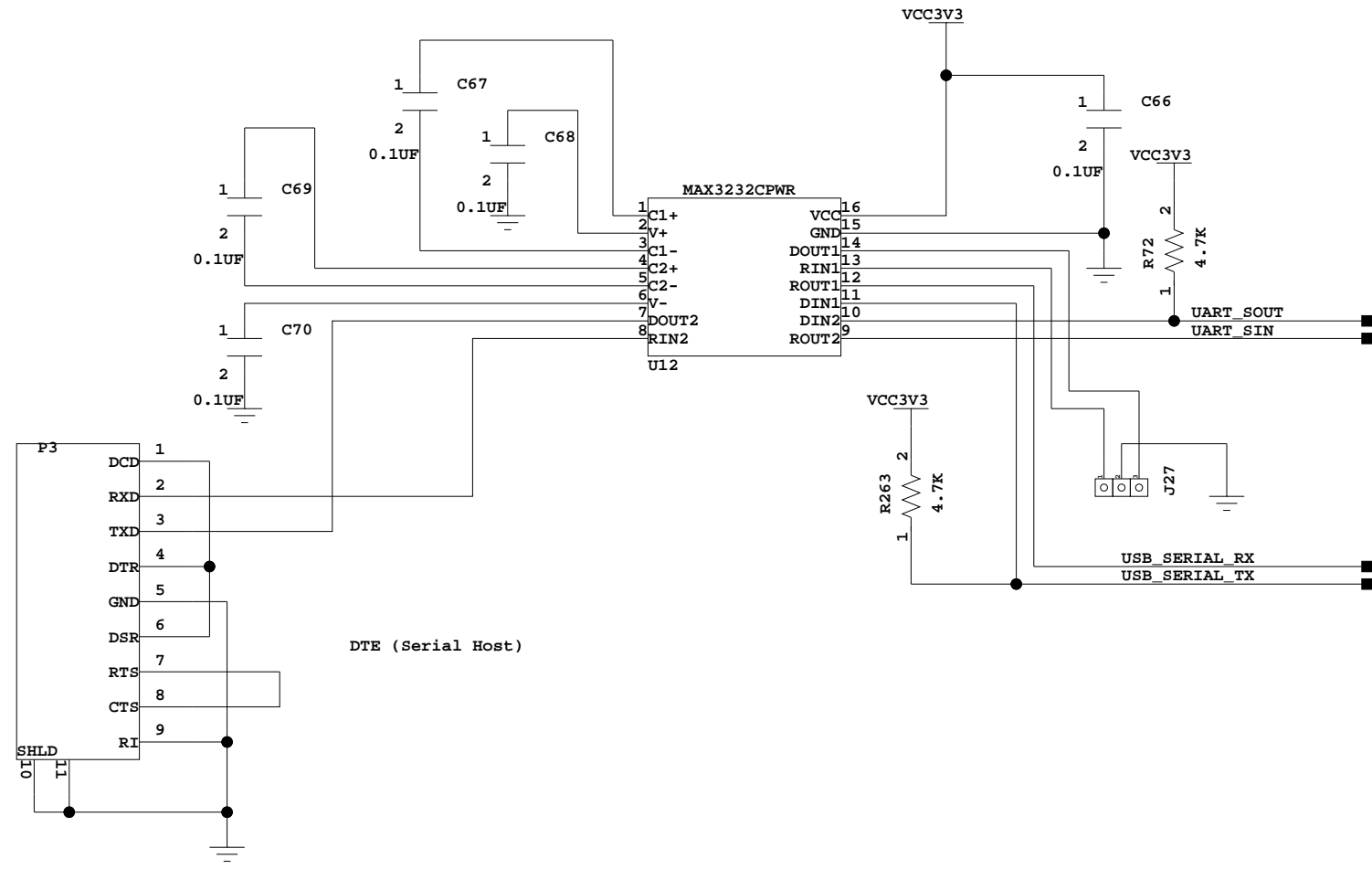
Matched Length Traces
Independent signals



Matched Length Traces
Differential Pairs

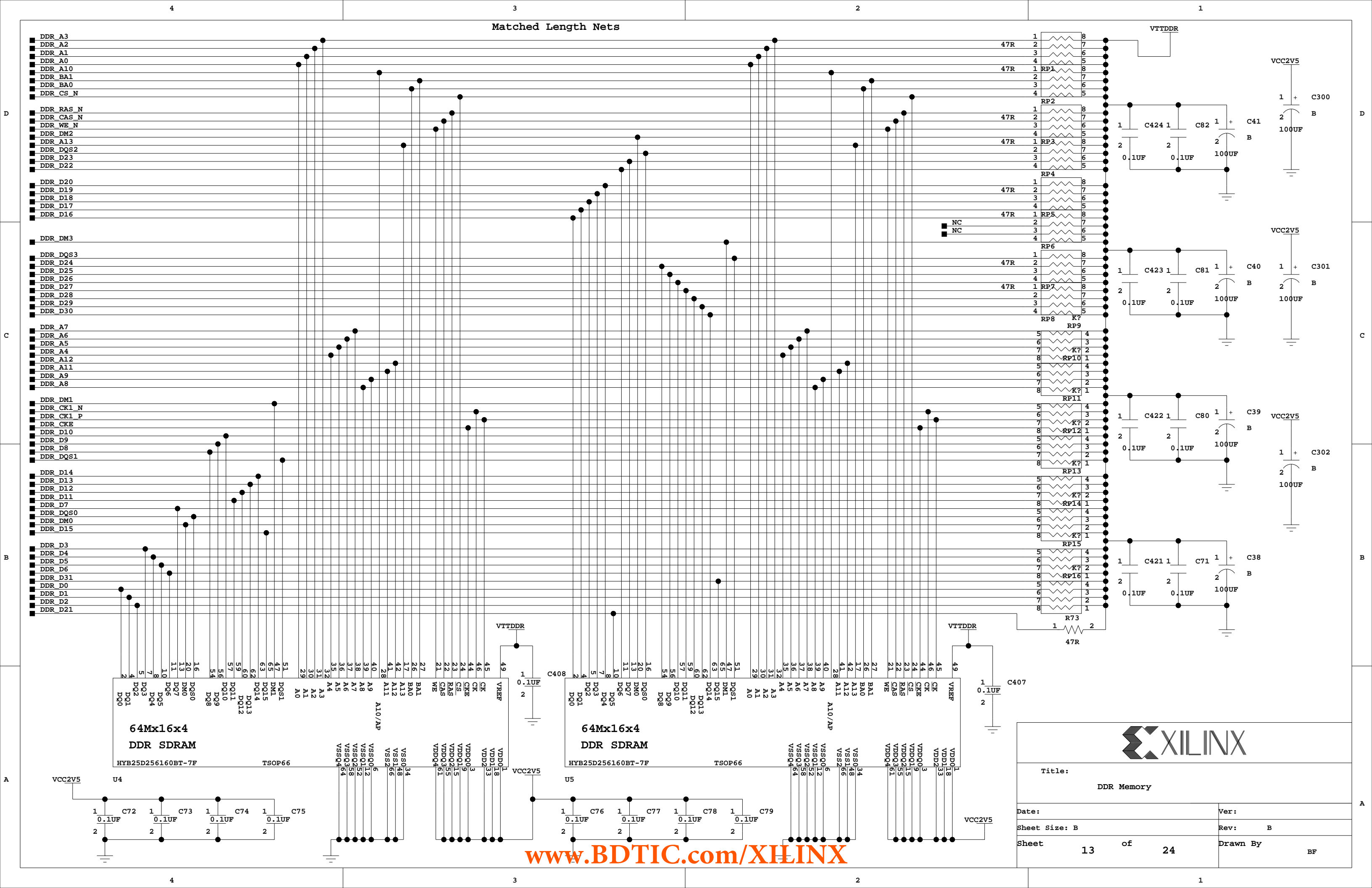


Title:	
Expansion Headers	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 11 of 24	Drawn By BF

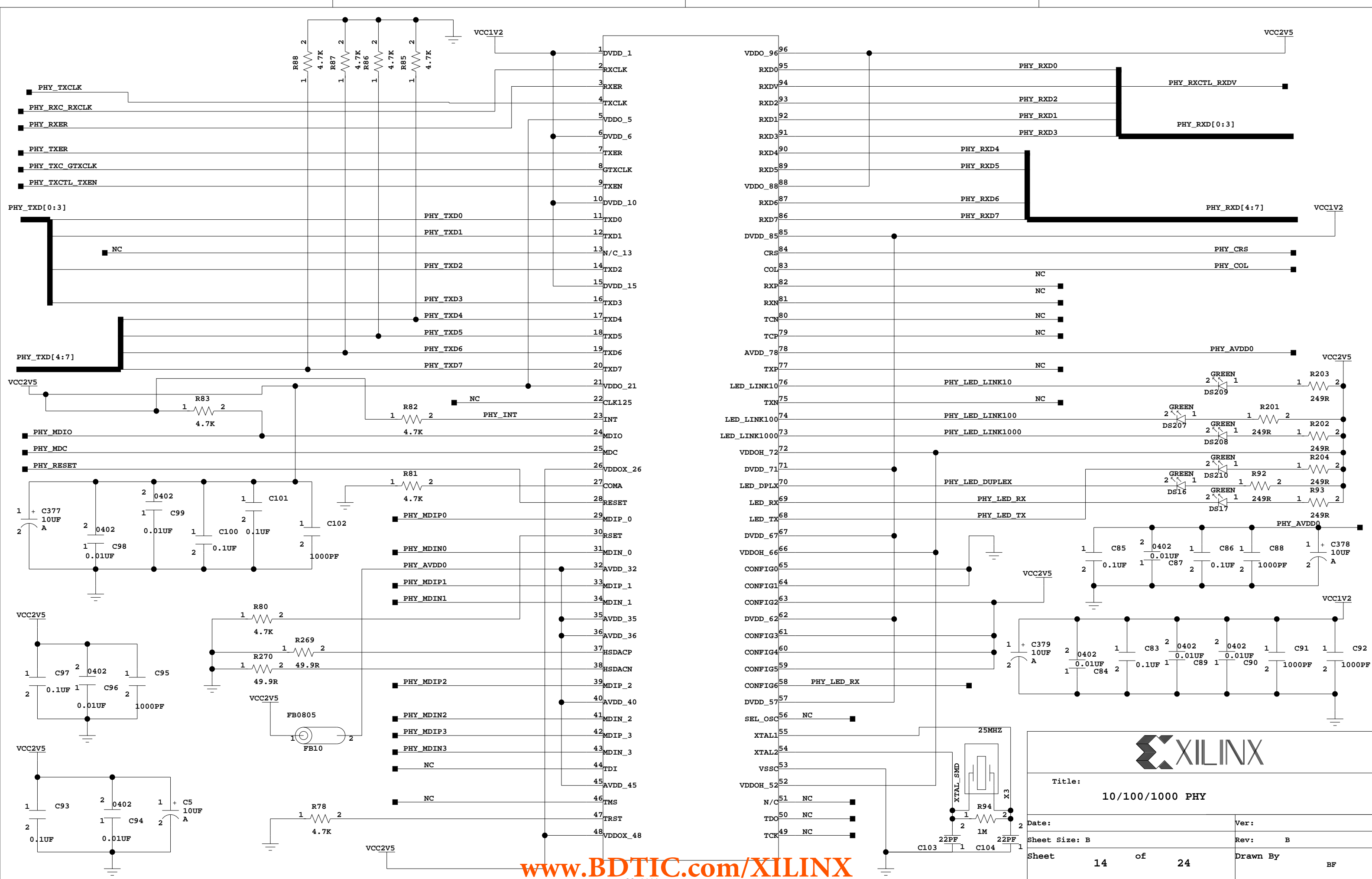


Title: LCD, PS2, UART, IIC EEPROM	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 12 of 24	Drawn By BF

Matched Length Nets



Title: DDR Memory	
Date:	Ver:
Sheet Size: B	Rev: B
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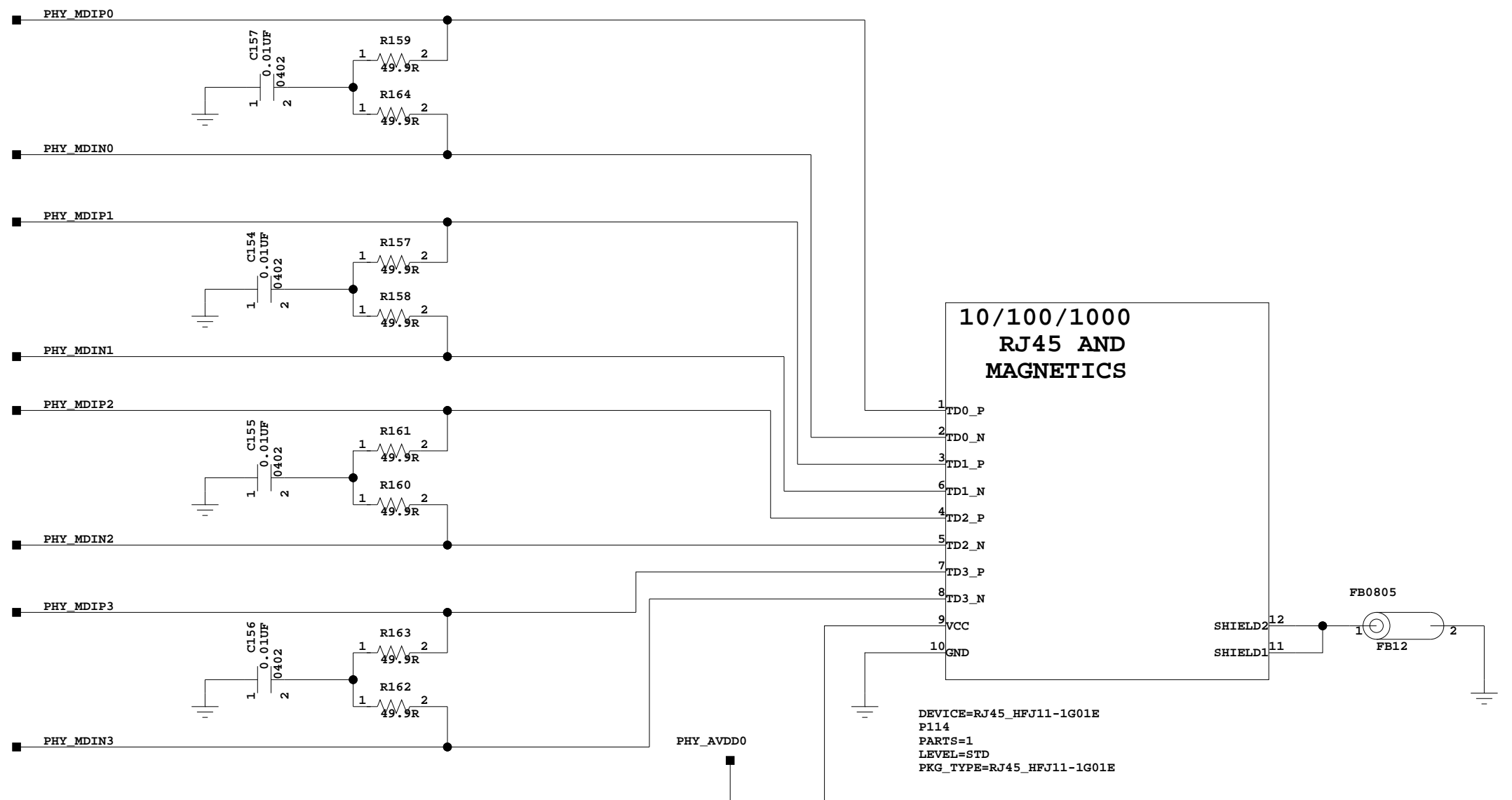
XILINX

Title: 10/100/1000 PHY

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 14 of 24	Drawn By BF

DEVICE=M88E1111
U45
PARTS=1

Pin to Constant Mapping	
Pin	Bit[2:0]
VCC2V5	111
PHY_LED_LINK10	110
PHY_LED_LINK100	101
PHY_LED_LINK1000	100
PHY_LED_DUPLEX	011
PHY_LED_RX	010
PHY_LED_TX	001
GND	000

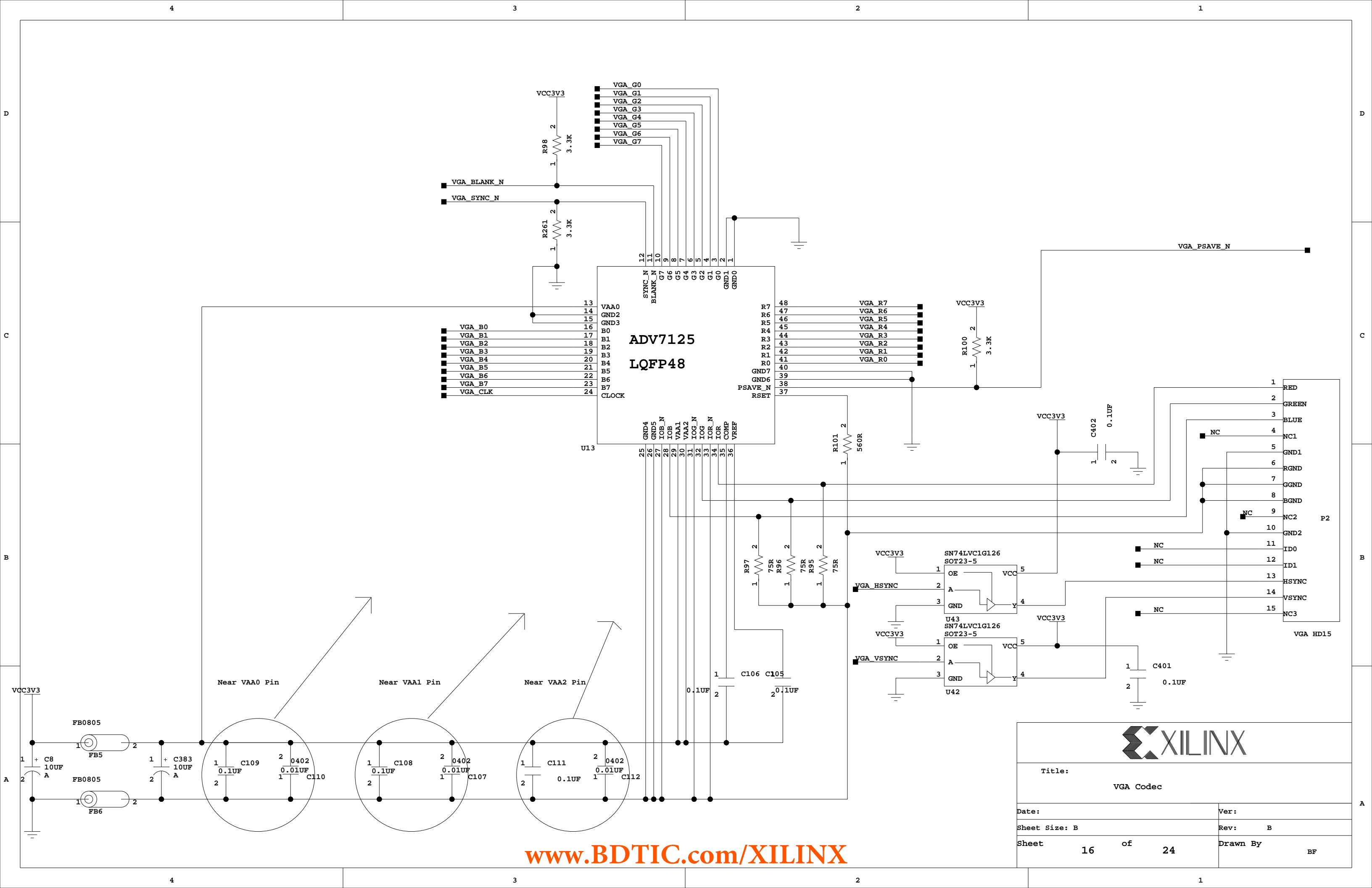


DEVICE=RJ45_HFJ11-1G01E
 P114
 PARTS=1
 LEVEL=STD
 PKG_TYPE=RJ45_HFJ11-1G01E

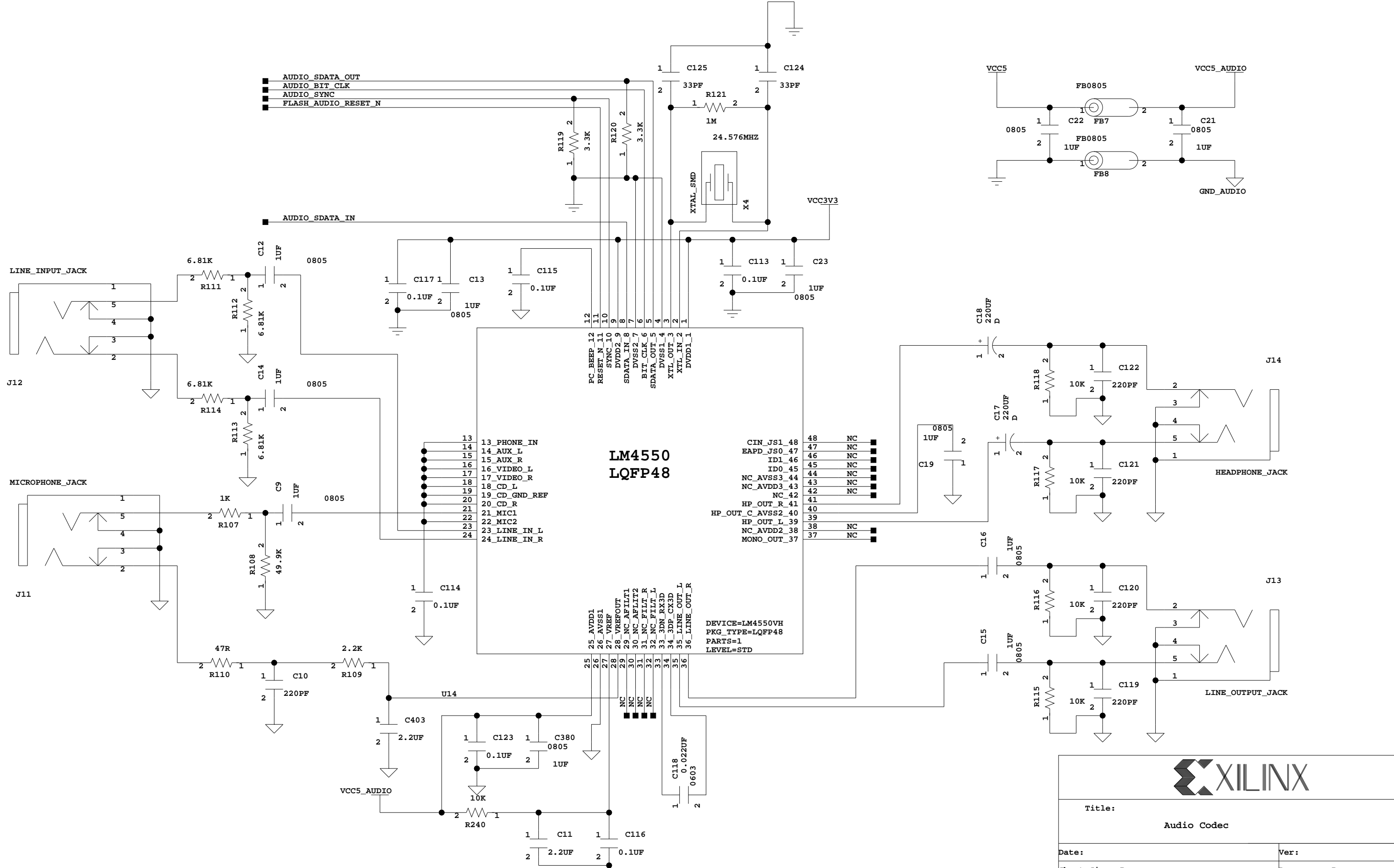
Pin	Bit[2]	Bit[1]	Bit[0]		
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddress "00000". Do not advertise the PAUSE bit
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg enabled, advertise all capabilities; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CONFIG3	ANEG[0]	ENA_XC	DIS_125	111	
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. sleep mode disabled.
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	111	
CONFIG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW Interrupt. 50ohm SERDES option.



Title: RJ45 Connector and PHY Decoupling	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 15 of 24	Drawn By BF



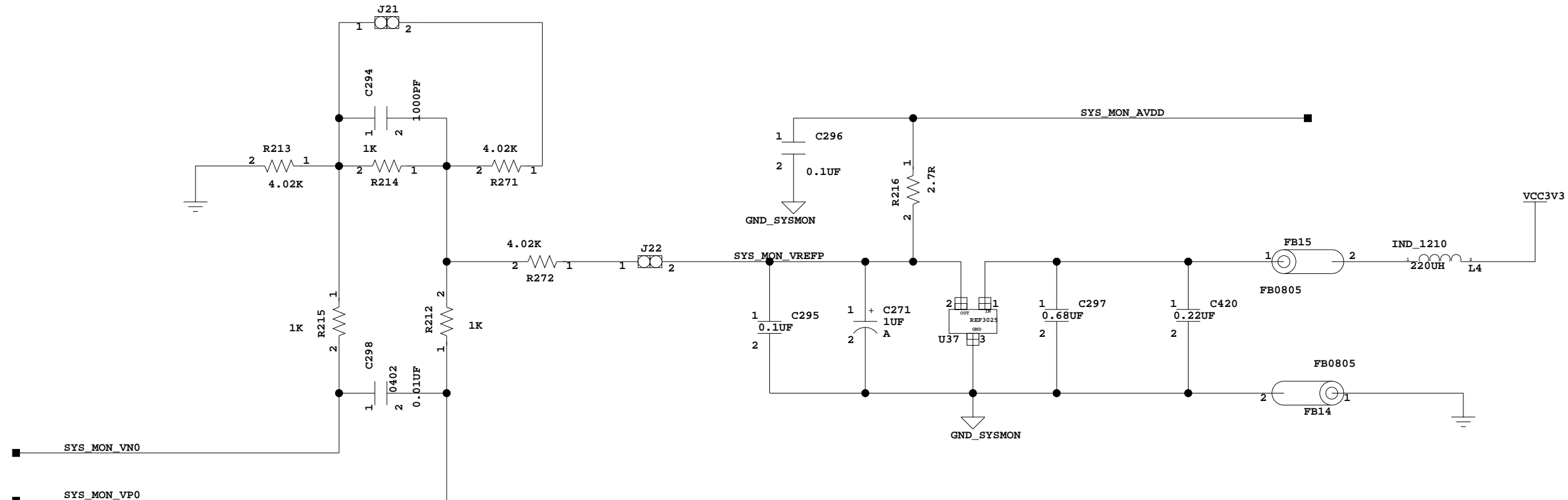
Title:		VGA Codec	
Date:		Ver:	
Sheet Size:	B	Rev:	B
Sheet	16	of	24
		Drawn By	BF



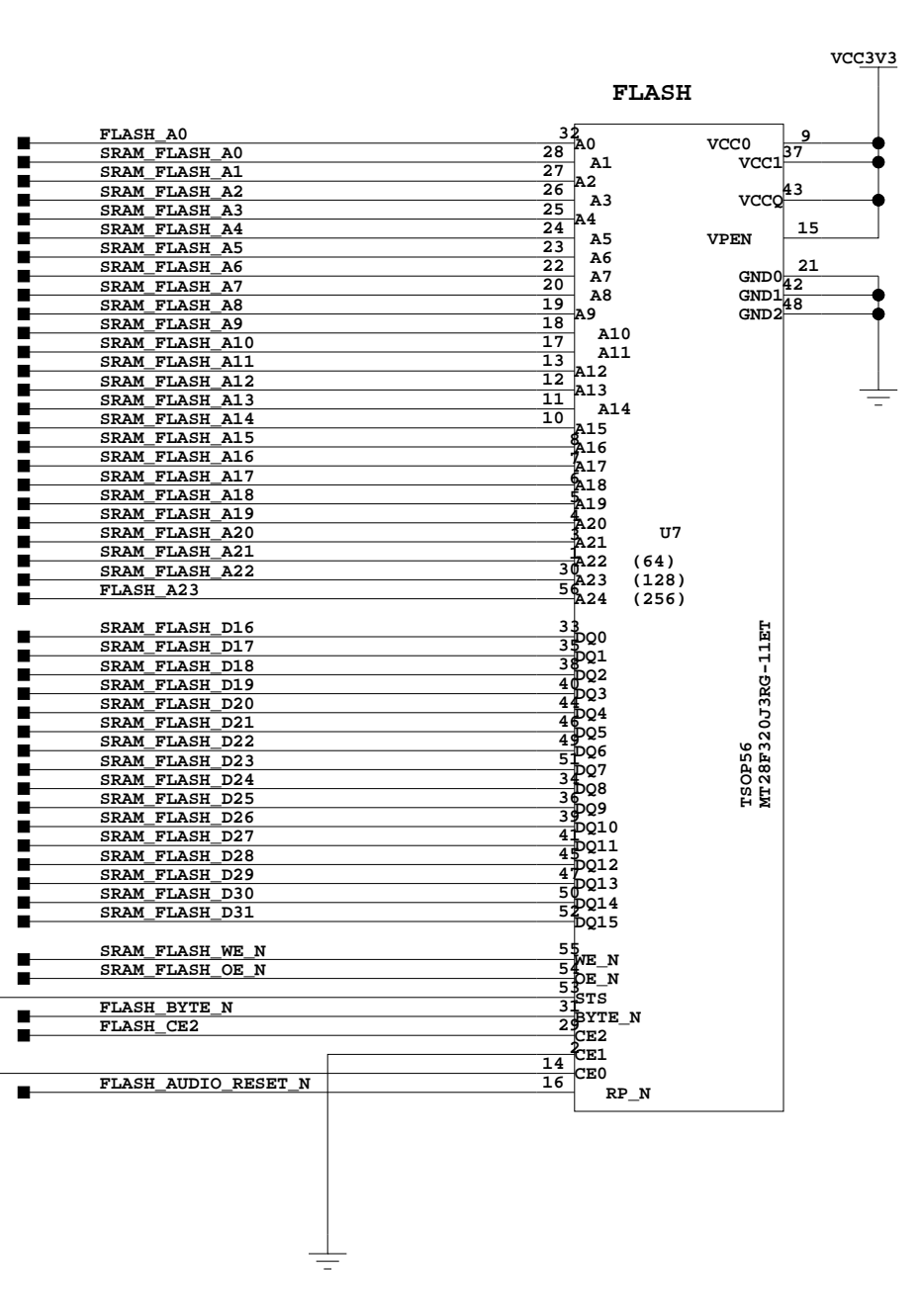
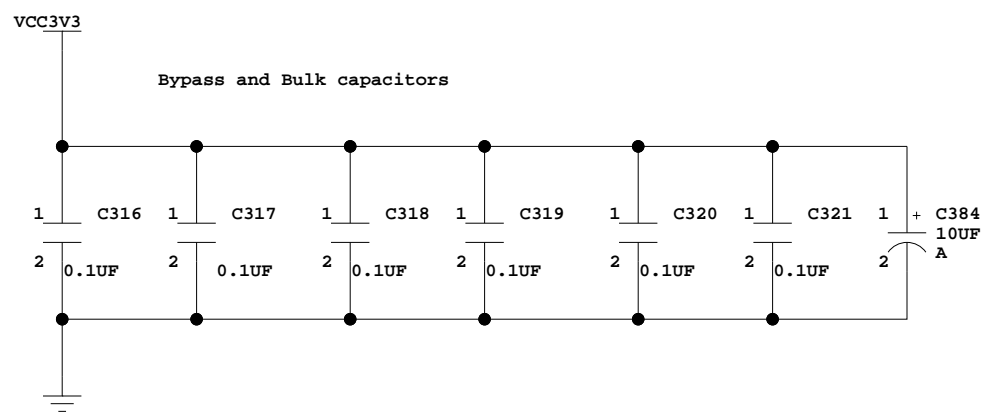
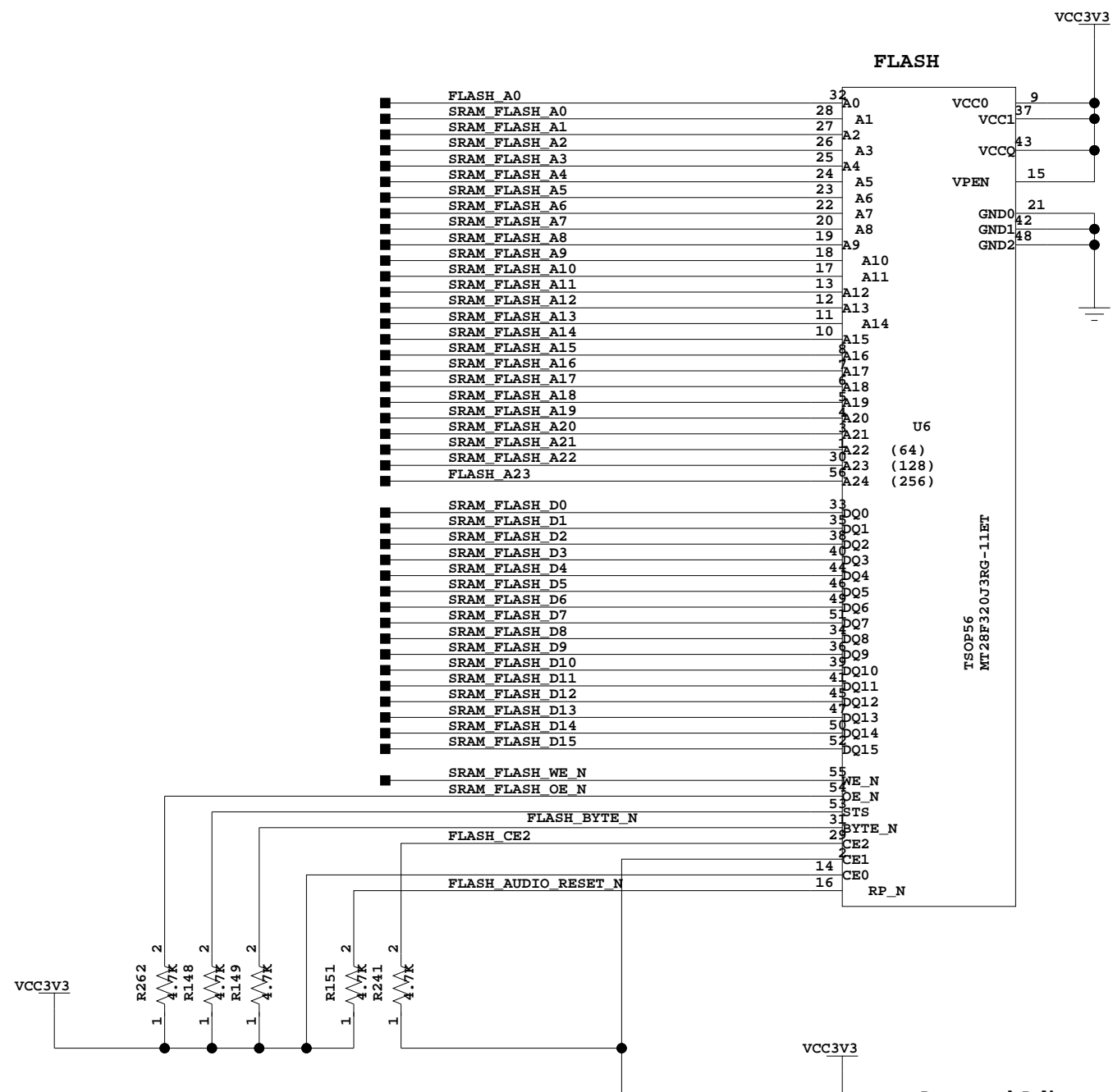
XILINX


Title:
Audio Codec

Date:	Ver:
Sheet Size: B	Rev: B
Sheet 17 of 24	Drawn By BF



Title: System Monitor DVM Circuit	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 18 of 24	Drawn By BF

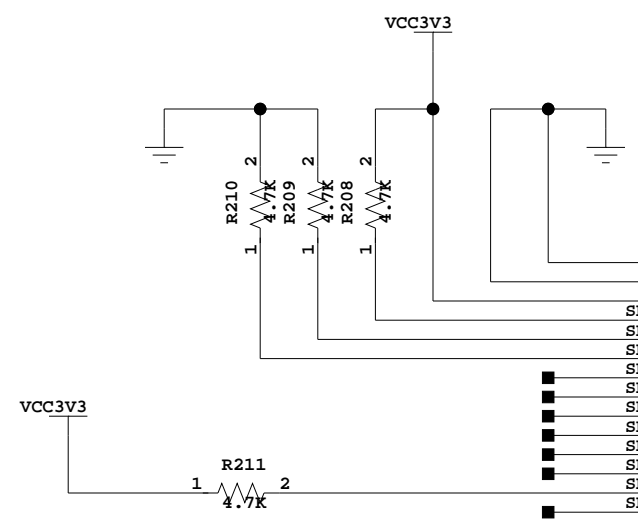




XILINX

Title:	
Flash Memory	
Date:	Ver:
Sheet Size: B	Rev: B
Sheet 20 of 24	Drawn By BF

The burst order mode of the SRAM is set to "Linear" by default



87	87 CEN_N	92	92 CE3_N
97	97 CE2	98	98 CE1_N
31	SRAM MODE	64	MODE_ZZ
93	SRAM BW1	94	SRAM BW0
95	SRAM BW3	96	SRAM BW2
85	SRAM ADV_LD_N	86	SRAM_FLASH_OE_N
88	SRAM_FLASH_WE_N	89	SRAM_CLK
37	SRAM_FLASH_A0	36	SRAM_FLASH_A1
35	SRAM_FLASH_A2	34	SRAM_FLASH_A3
33	SRAM_FLASH_A4	32	SRAM_FLASH_A5
44	SRAM_FLASH_A6	45	SRAM_FLASH_A7
46	SRAM_FLASH_A8	47	SRAM_FLASH_A9
48	SRAM_FLASH_A10	49	SRAM_FLASH_A11
50	SRAM_FLASH_A12	81	SRAM_FLASH_A13
82	SRAM_FLASH_A14	83	SRAM_FLASH_A15
99	SRAM_FLASH_A16	100	SRAM_FLASH_A17
84	SRAM_FLASH_A18	43	SRAM_FLASH_A19
42	SRAM_FLASH_A20	39	SRAM_FLASH_A21
38	SRAM_FLASH_A22		

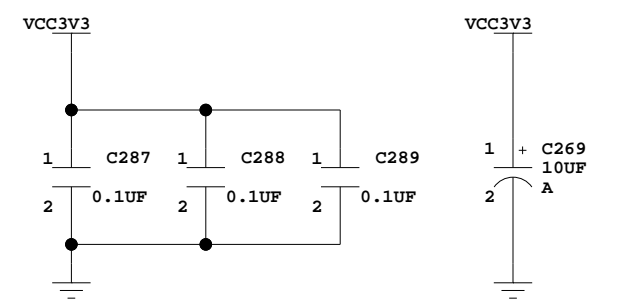
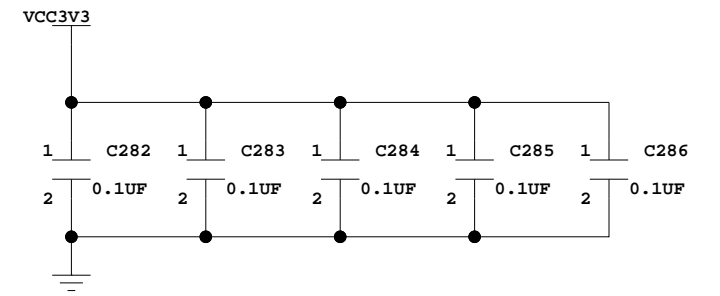
66	NC	16	NC
14	NC	14	NC
90	VSS_90	76	VSS_76
71	VSS_71	67	VSS_67
60	VSS_60	55	VSS_55
40	VSS_40	26	VSS_26
21	VSS_21	17	VSS_17
10	VSS_10	5	VSS_5
91	VDD_91	77	VDDQ_77
70	VDDQ_70	65	VDDQ_65
61	VDDQ_61	54	VDDQ_54
41	VDDQ_41	27	VDDQ_27
20	VDDQ_20	15	VDDQ_15
11	VDDQ_11	4	VDDQ_4

RP24	SRAM_FLASH_D23 RES	4	SRAM_FLASH_D22 RES	3	SRAM_FLASH_D21 RES	2	SRAM_FLASH_D20 RES	1	SRAM_FLASH_D19 RES	4	SRAM_FLASH_D18 RES	3	SRAM_FLASH_D17 RES	2	SRAM_FLASH_D16 RES	1	SRAM_FLASH_D31 RES	4	SRAM_FLASH_D30 RES	3	SRAM_FLASH_D29 RES	2	SRAM_FLASH_D28 RES	1	SRAM_FLASH_D27 RES	4	SRAM_FLASH_D26 RES	3	SRAM_FLASH_D25 RES	2	SRAM_FLASH_D24 RES	1
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K?	SRAM_FLASH_D7 RES	4	SRAM_FLASH_D6 RES	3	SRAM_FLASH_D5 RES	2	SRAM_FLASH_D4 RES	1	SRAM_FLASH_D3 RES	4	SRAM_FLASH_D2 RES	3	SRAM_FLASH_D1 RES	2	SRAM_FLASH_D0 RES	1	SRAM_FLASH_D15 RES	4	SRAM_FLASH_D14 RES	3	SRAM_FLASH_D13 RES	2	SRAM_FLASH_D12 RES	1	SRAM_FLASH_D11 RES	4	SRAM_FLASH_D10 RES	3	SRAM_FLASH_D9 RES	2	SRAM_FLASH_D8 RES	1
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R287	1	2	1	1	DQPC	2	DQC	3	DQC	6	DQC	7	DQC	8	DQC	9	DQC	12	DQC	13	DQC	18	DQD	19	DQD	22	DQD	23	DQD	24	DQD	25	DQD	28	DQD	29	DQD	30	DQP3	51	DQP0	52	DQA	53	DQA	56	DQA	57	DQA	58	DQA	59	DQA	62	DQA	63	DQA	68	DQB	69	DQB	72	DQB	73	DQB	74	DQB	75	DQB	78	DQB	79	DQB	80	DQP1
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CY7C1354B TQFP100



Title:		ZBT SRAM	
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SRAM_FLASH_D20_RES	28	28	IO_3_9
SRAM_FLASH_D19_RES	29	29	IO_3_11
SRAM_FLASH_D21_RES	30	30	IO_3_12
SRAM_FLASH_D18_RES	32	32	IO_3_14
SRAM_FLASH_D17_RES	33	33	IO_3_15
SRAM_FLASH_D22_RES	34	34	IO_3_17
CPLD_IO_1	87	87	IO_4_2
CPLD_IO_2	89	89	IO_4_5
CPLD_IO_3	90	90	IO_4_6
SRAM_FLASH_D8_RES	91	91	IO_4_8
SRAM_FLASH_D9_RES	92	92	IO_4_9
SRAM_FLASH_D15_RES	93	93	IO_4_11
SRAM_FLASH_D14_RES	94	94	IO_4_12
SRAM_FLASH_D13_RES	95	95	IO_4_14
SRAM_FLASH_D10_RES	96	96	IO_4_15
SRAM_FLASH_D11_RES	97	97	IO_4_17
SRAM_FLASH_D23_RES	35	35	IO_5_2
SRAM_FLASH_D16_RES	36	36	IO_5_5
FLASH_CE2	37	37	IO_5_6
SRAM_FLASH_D31_RES	39	39	IO_5_8
SRAM_FLASH_D30_RES	40	40	IO_5_9
SRAM_FLASH_D24_RES	41	41	IO_5_11
SRAM_FLASH_D25_RES	42	42	IO_5_12
SRAM_FLASH_D27_RES	43	43	IO_5_14
SRAM_FLASH_D26_RES	46	46	IO_5_15

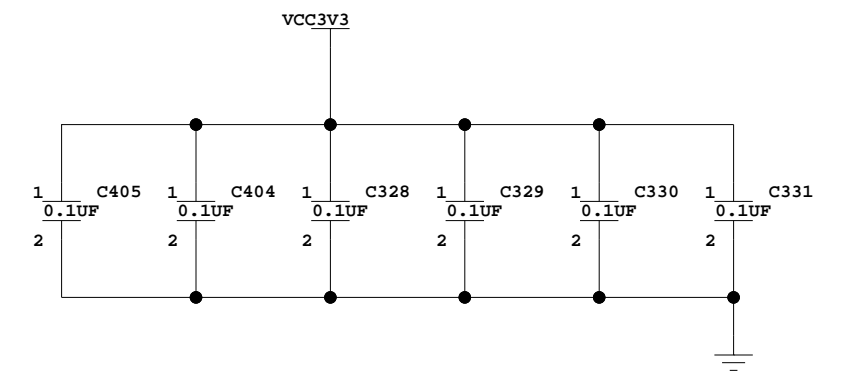
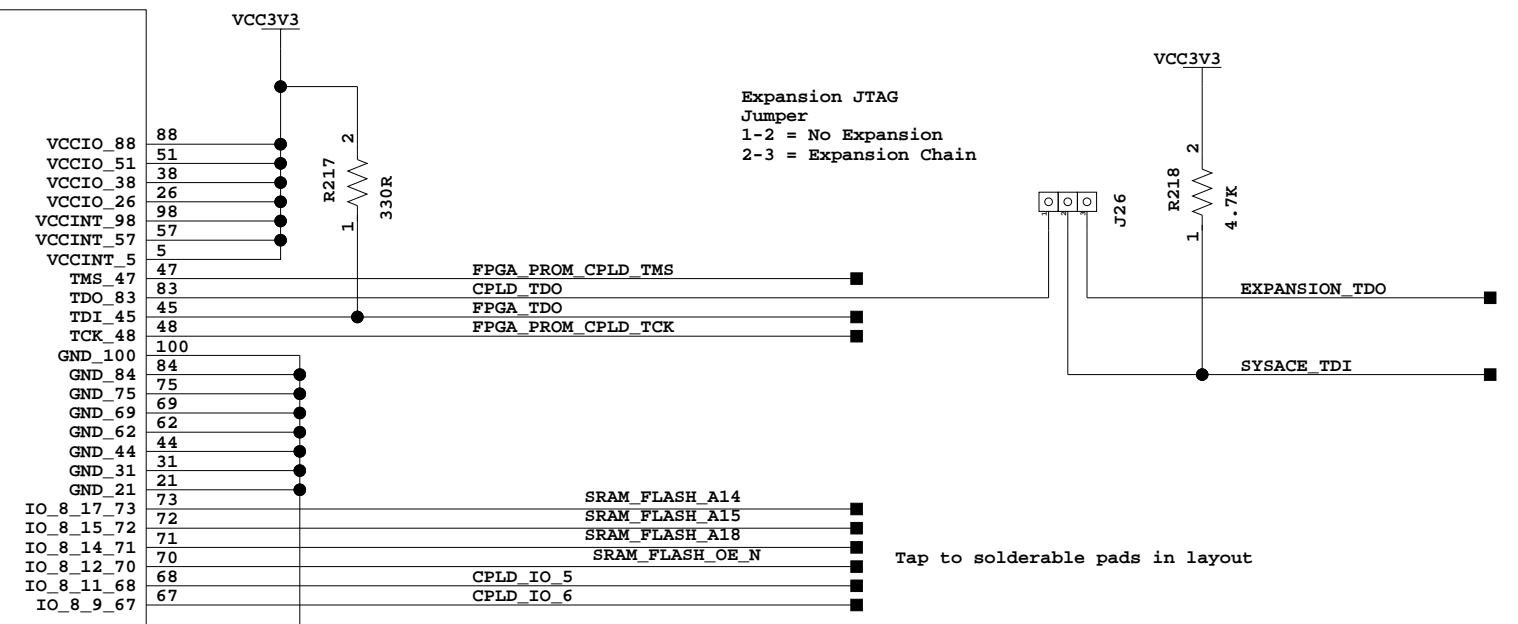
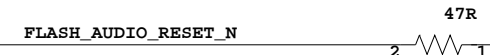
PLATFLASH_CPLD_CCLK	27
SRAM_FLASH_A5	25
SRAM_FLASH_A4	24
SYSCLK_100MHZ	23
SRAM_FLASH_A19	10
SYSPACE_CFGADDR2	9
SRAM_FLASH_A6	8
SRAM_FLASH_A7	7
SRAM_FLASH_A8	6
SRAM_FLASH_A9	4
SRAM_FLASH_A10	3
SRAM_FLASH_A11	2
SRAM_FLASH_A12	1
SRAM_FLASH_D12_RES	99
SYSPACE_CLK	22
SRAM_FLASH_A3	20
SRAM_FLASH_A2	19
SRAM_FLASH_A1	18
SRAM_FLASH_A0	17
SRAM_FLASH_A21	16
FPGA_M0	15
FPGA_M1	14
SYSPACE_CFGADDR0	13
SYSPACE_CFGADDR1	12
SRAM_FLASH_A20	11

IO_GCK3_3_8_27	27
IO_3_6_25	25
IO_3_5_24	24
IO_GCK2_3_2_23	23
IO_2_17_10	10
IO_2_15_9	9
IO_2_14_8	8
IO_2_12_7	7
IO_2_11_6	6
IO_GTS2_2_9_4	4
IO_GTS1_2_8_3	3
IO_GTS4_2_6_2	2
IO_GTS3_2_5_1	1
IO_GSR_2_2_99	99
IO_GCK1_1_17_22	22
IO_1_15_20	20
IO_1_14_19	19
IO_1_12_18	18
IO_1_11_17	17
IO_1_9_16	16
IO_1_8_15	15
IO_1_6_14	14
IO_1_5_13	13
IO_1_3_12	12
IO_1_2_11	11

XC95144XL
SQ_TQFP100

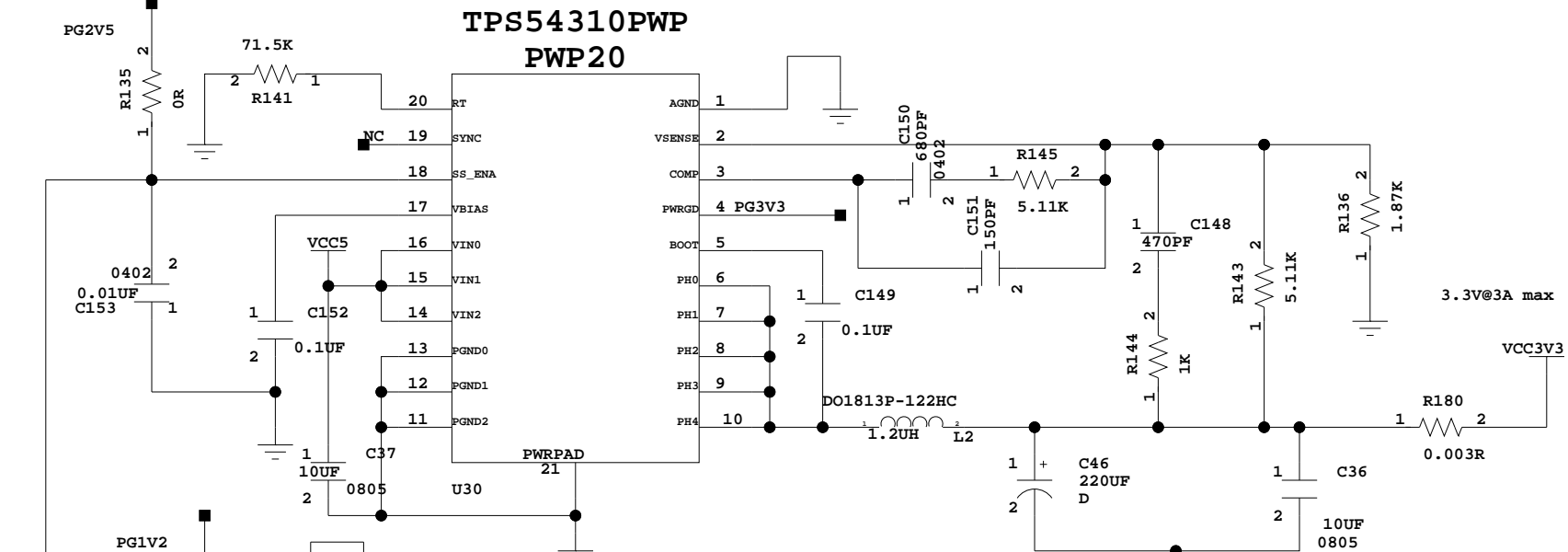
SRAM_FLASH_D28_RES	49	IO_5_17
SRAM_FLASH_A13	74	IO_6_2
SRAM_FLASH_D2_RES	76	IO_6_5
SRAM_FLASH_D3_RES	77	IO_6_6
SRAM_FLASH_D4_RES	78	IO_6_8
SRAM_FLASH_D5_RES	79	IO_6_9
SRAM_FLASH_D1_RES	80	IO_6_11
SRAM_FLASH_D0_RES	81	IO_6_12
SRAM_FLASH_D6_RES	82	IO_6_14
SRAM_FLASH_D7_RES	85	IO_6_15
FPGA_DOUT_BUSY	86	IO_6_17
SRAM_FLASH_D29_RES	50	IO_7_2
SRAM_FLASH_A17	52	IO_7_5
SRAM_FLASH_A16	53	IO_7_6
FPGA_DIN	54	IO_7_8
FPGA_DONE	55	IO_7_9
FPGA_INIT	56	IO_7_11
FPGA_PROG_B	58	IO_7_12
FPGA_CS_B	59	IO_7_14
FPGA_M2	60	IO_7_15
FPGA_M1	61	IO_7_17
FLASH_A23	63	IO_8_2
FPGA_M0	64	IO_8_5
CPLD_PROG	65	IO_8_6
CPLD_IO_4	66	IO_8_8

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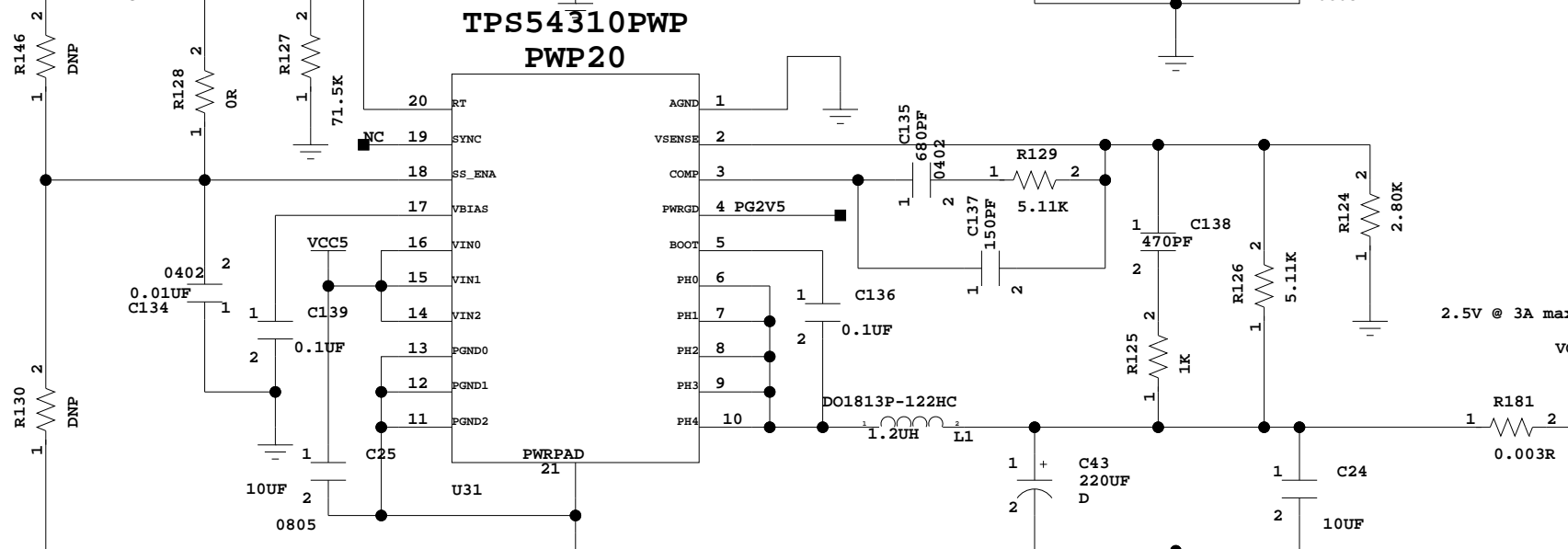


Title:	
CPLD for access to Linear Flash	
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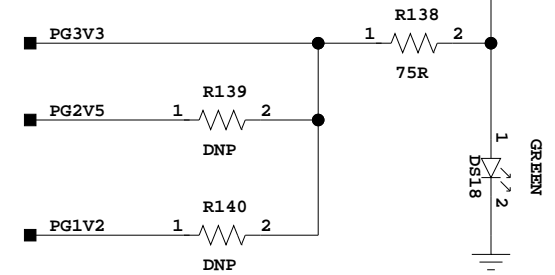
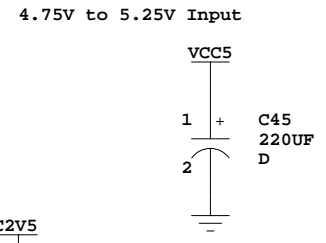
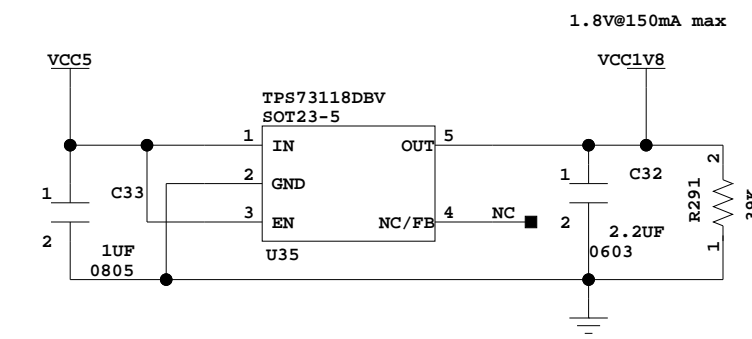
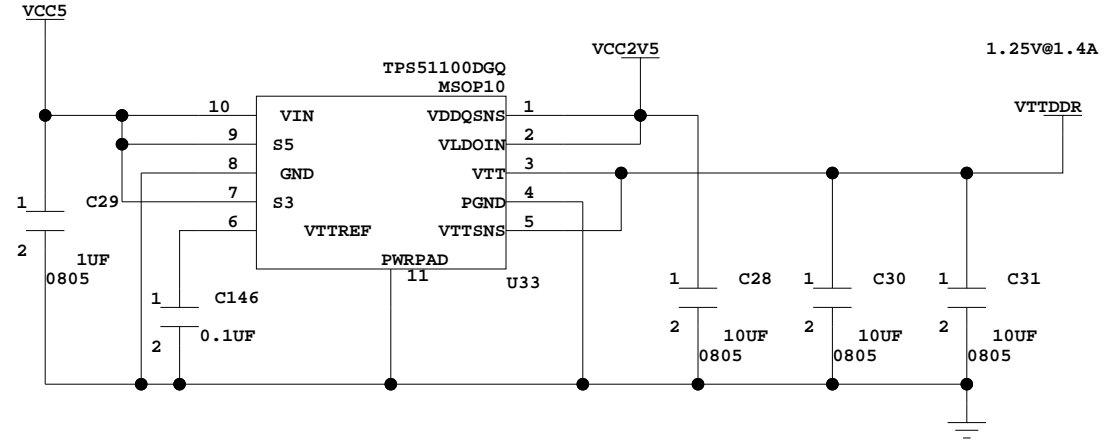
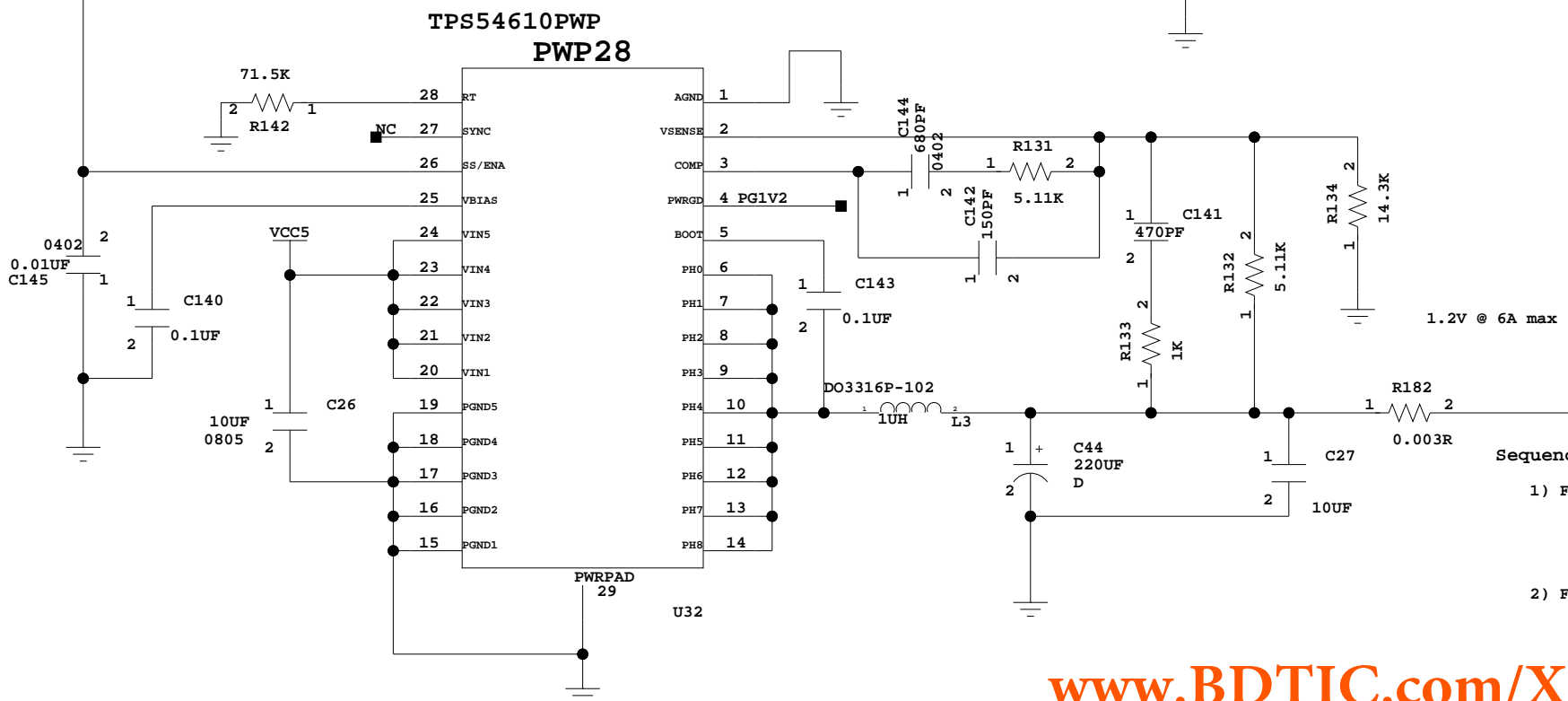
**TPS54310PWP
PWP20**



**TPS54310PWP
PWP20**



**TPS54610PWP
PWP28**

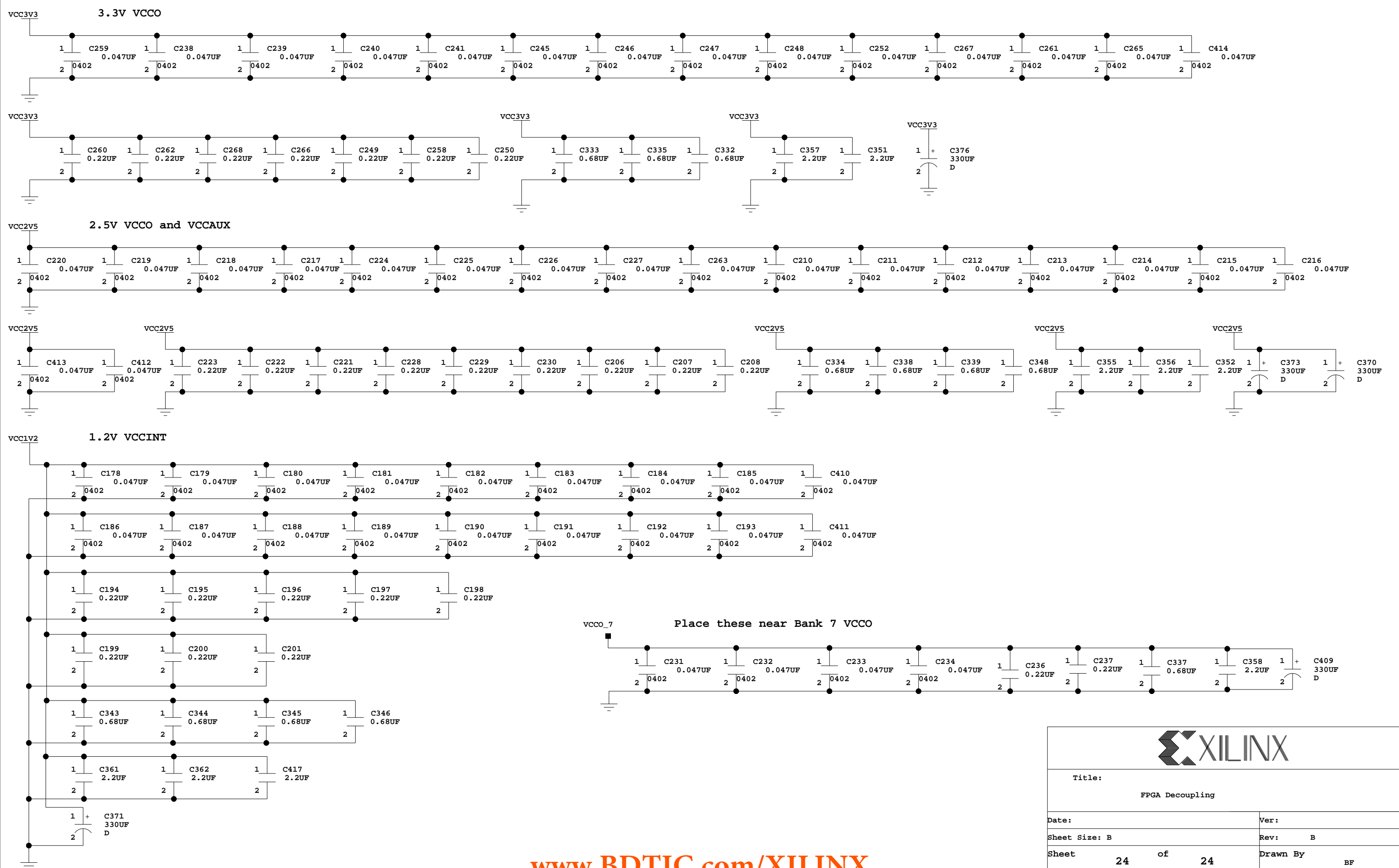


Sequencing Options:

- 1) For sequential startup :
OPEN R130, R146, R139 & R140
SHORT R128 & R135
- 2) For ratiometric startup :
OPEN R128 & R135
SHORT R130, R146, R139 & R140



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Title:	
FPGA Decoupling	
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