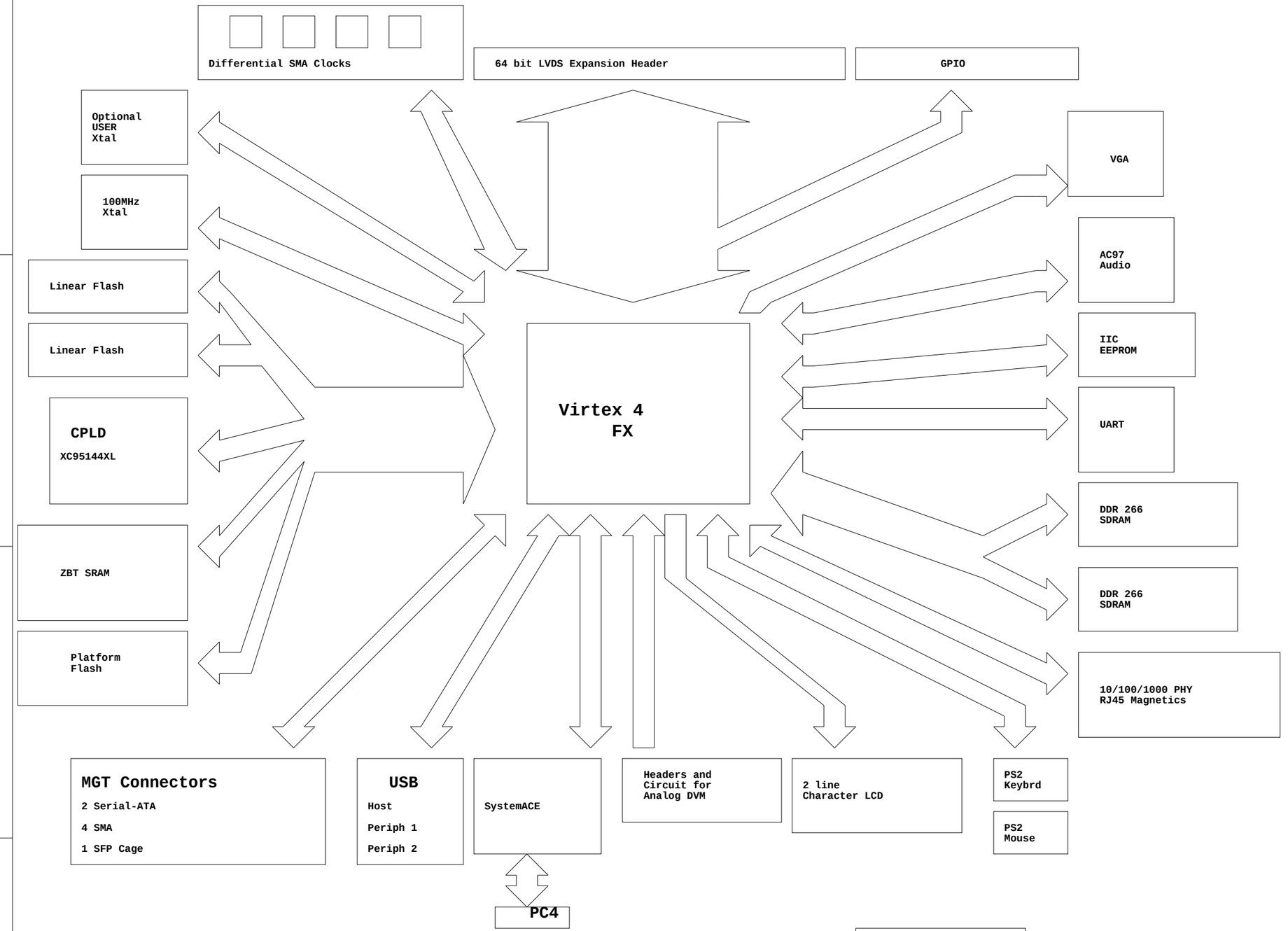
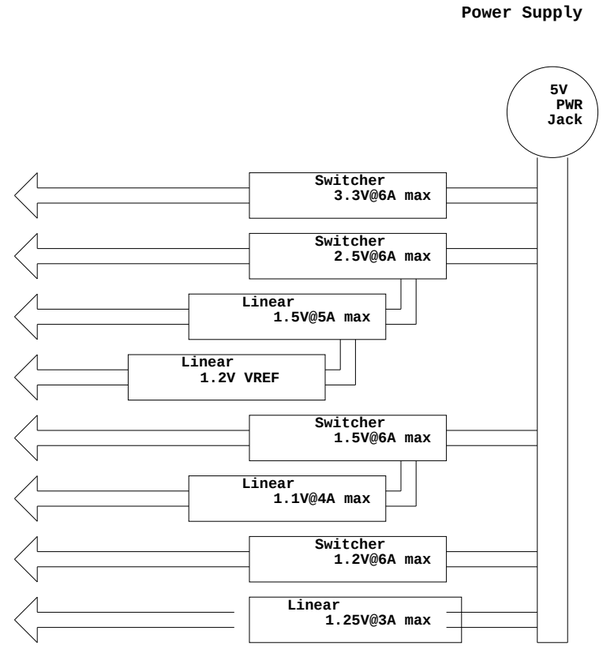
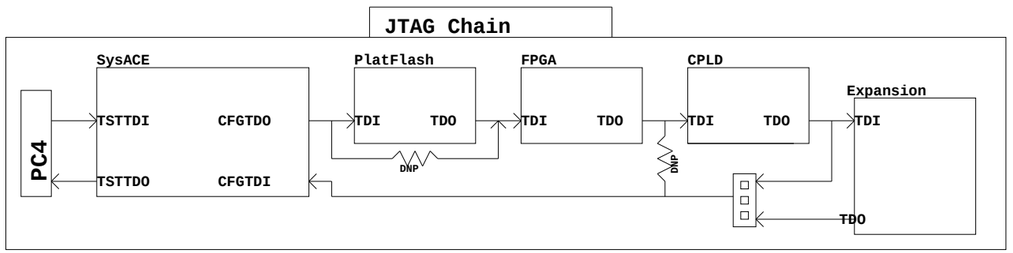




Compatibility and Available IOs	
FPGA Device	Banks
FX20	8 Banks 320 User IOs
FX40, FX60	10 Banks 352 User IOs



03

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
ML405 Block Diagram
0381199

Date: 12-11-2007_19:38	Ver: C
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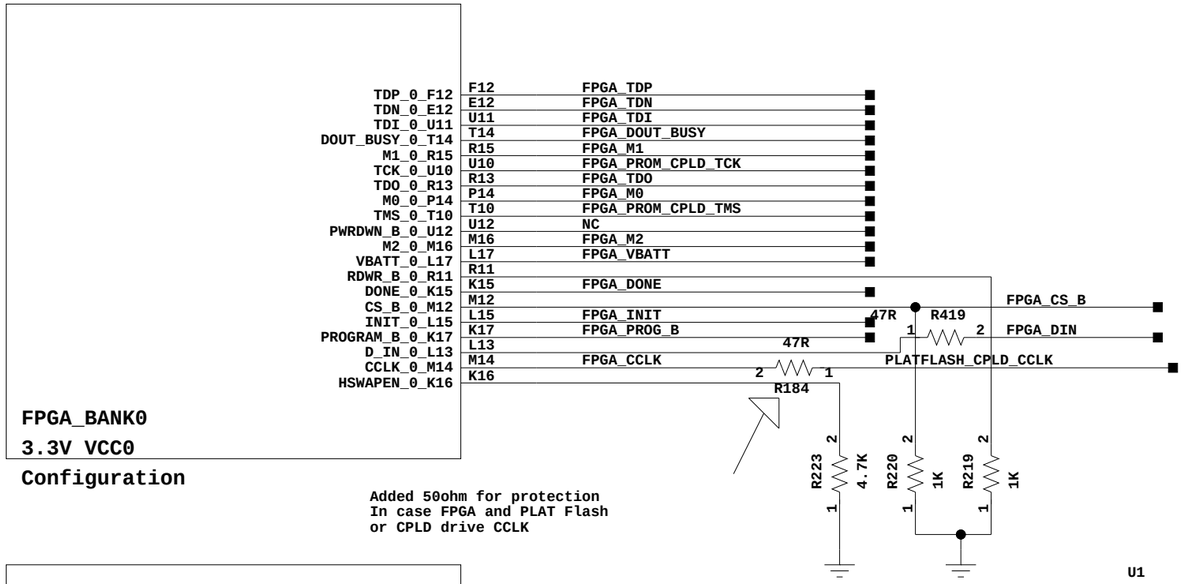

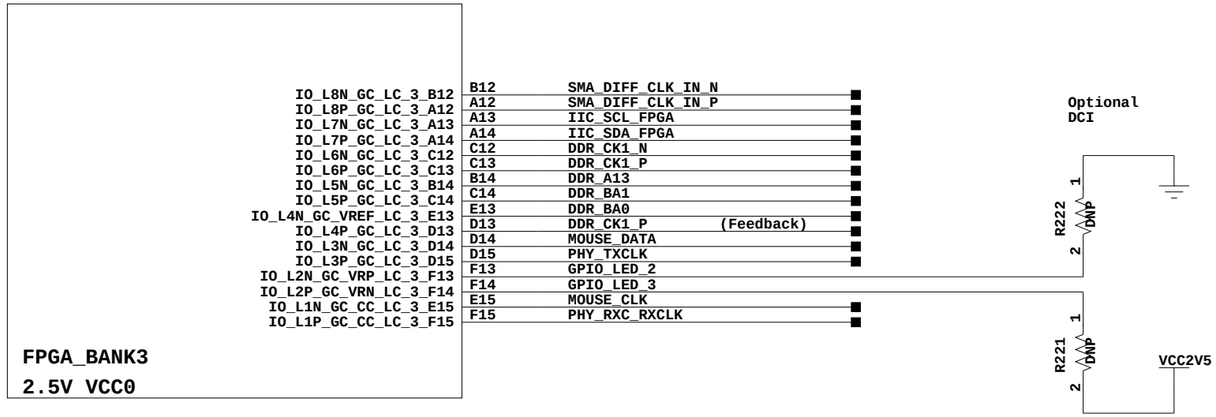

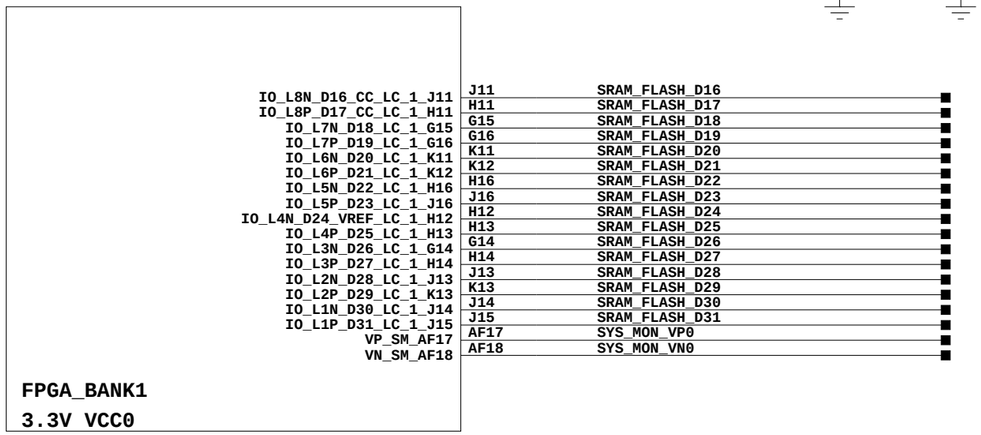

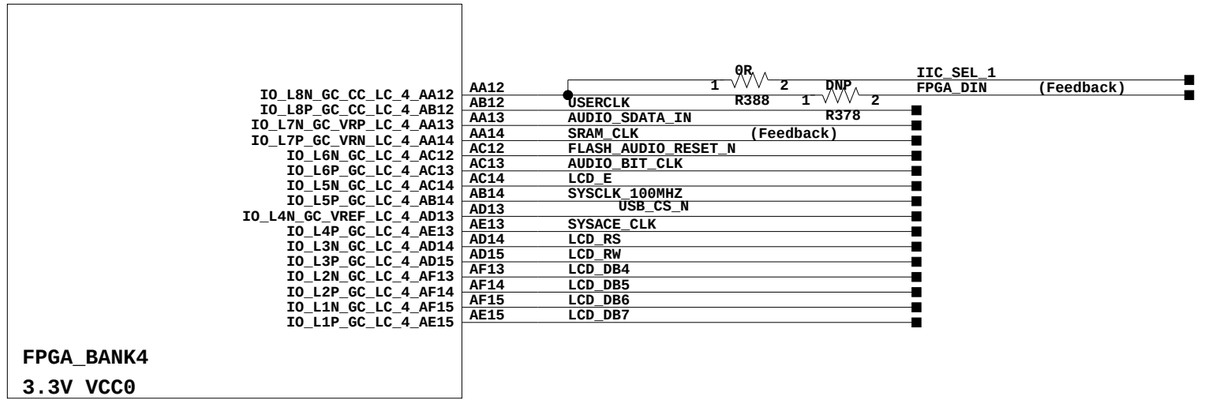

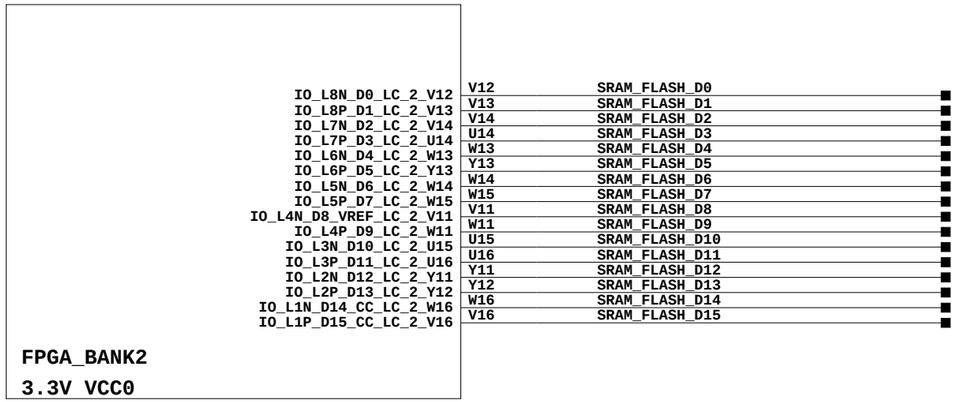

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
FPGA Banks 0,1,2,3,4

0381199

Date:	12-11-2007_19:38	Ver:	C
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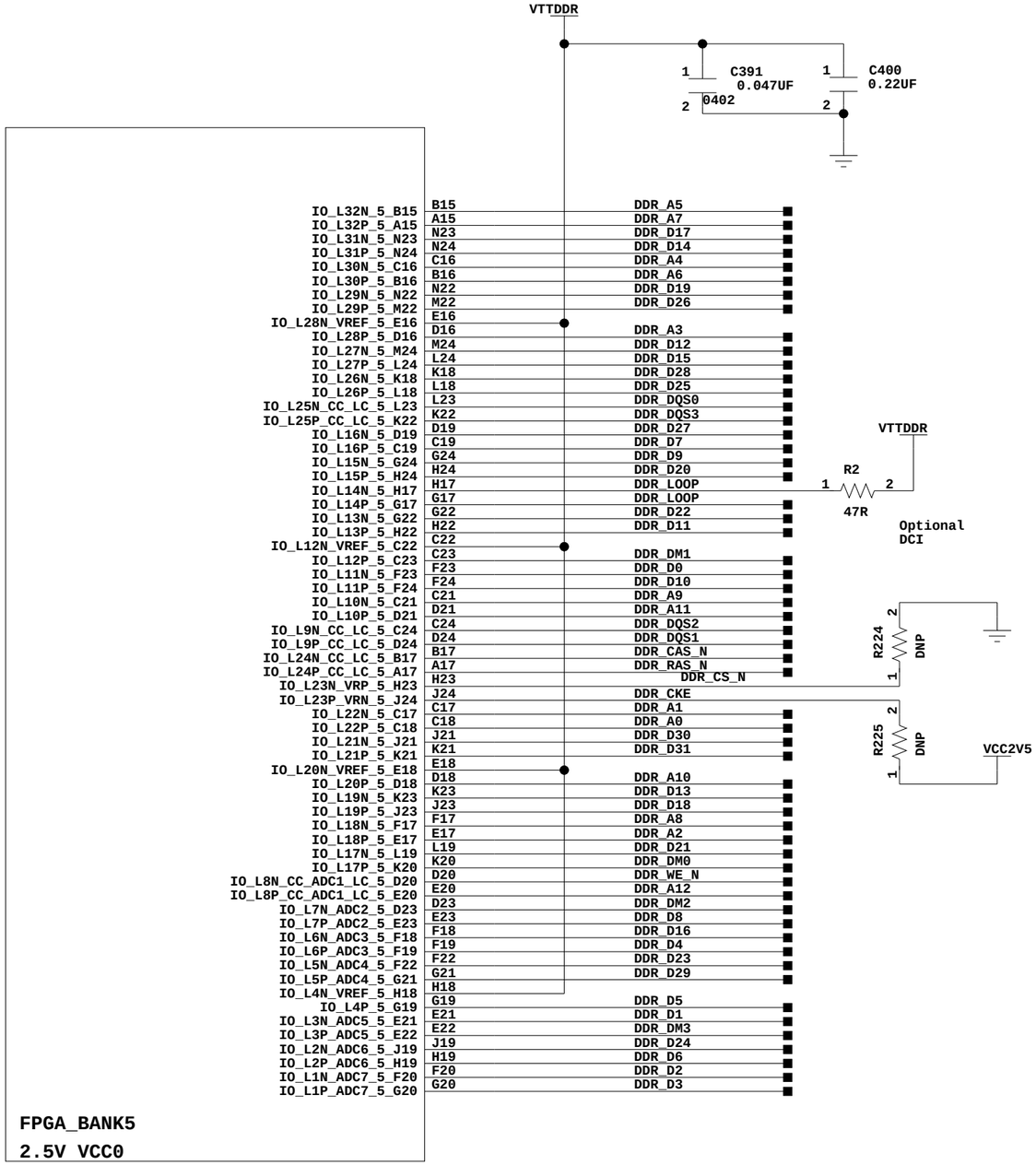

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
FPGA Bank 5, 6

0381199

Date: 12-11-2007_19:38	Ver: C
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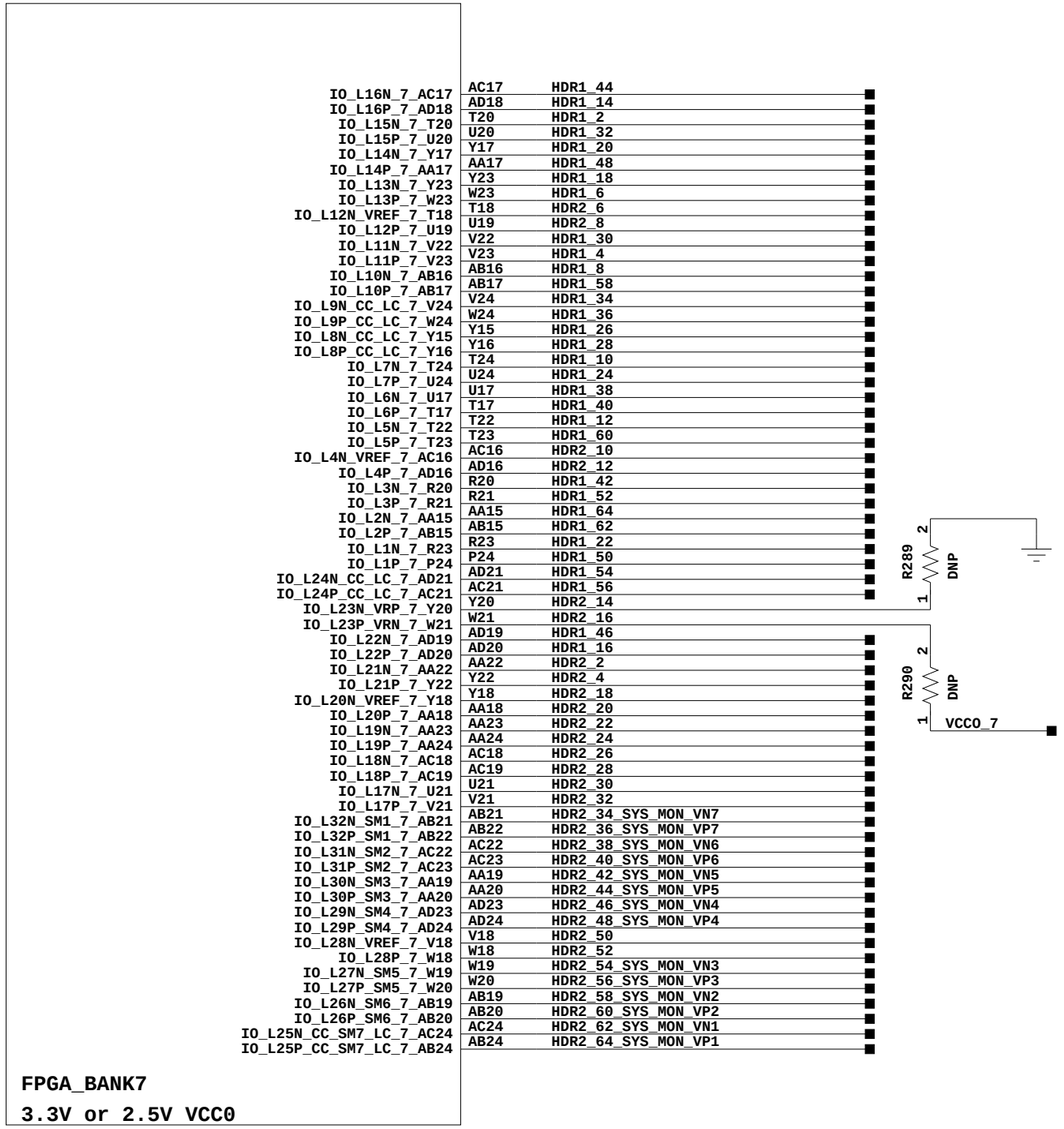

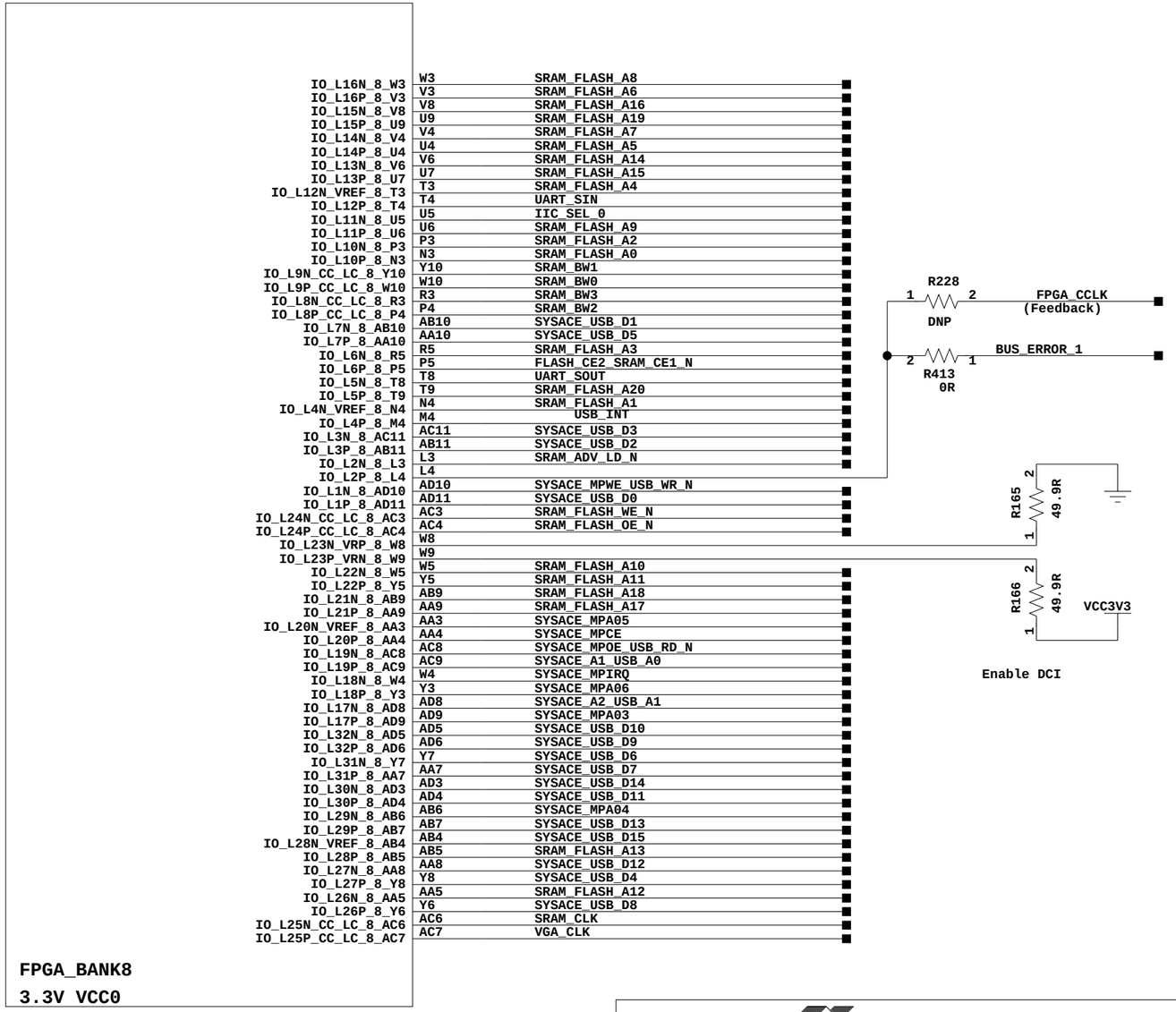

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
FPGA Bank 7, 8
0381199

Date:	12-11-2007_19:38	Ver:	C
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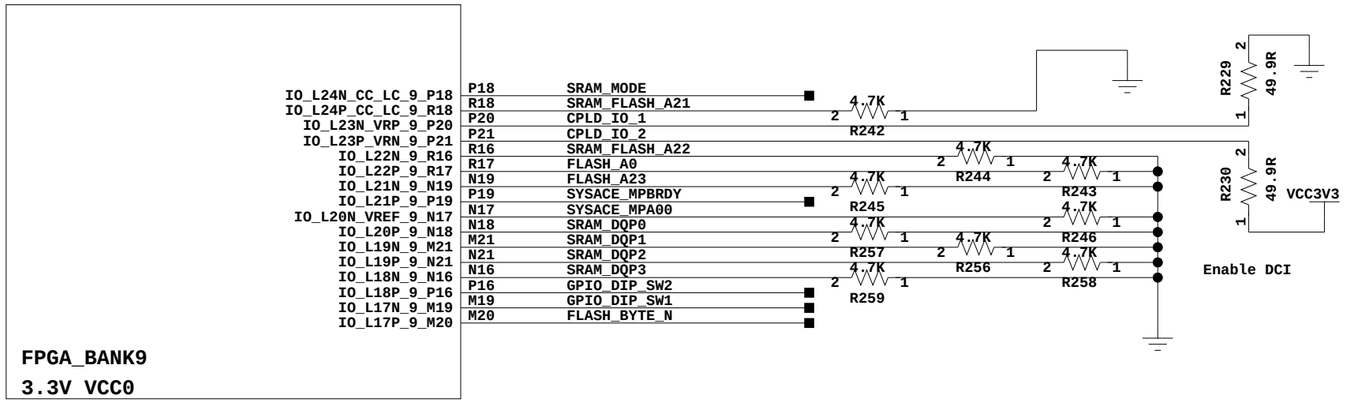

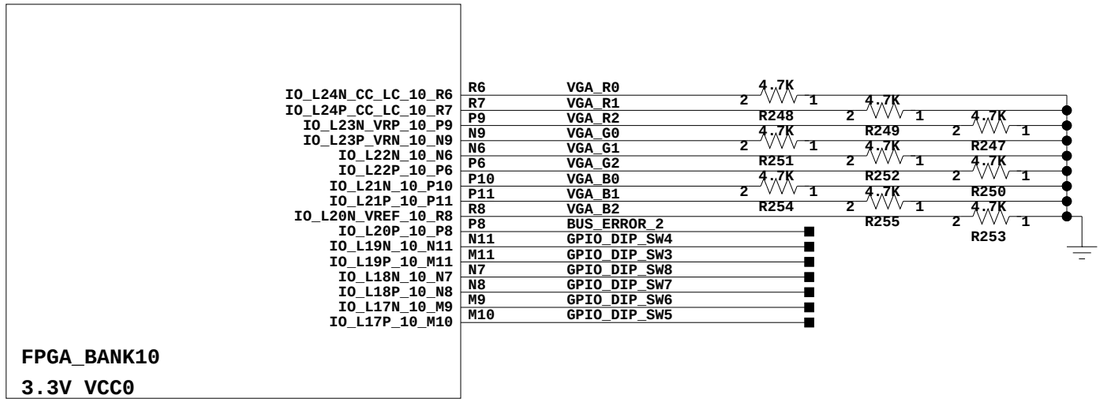

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
FPGA Bank 9, 10
0381199

Date:	12-11-2007_19:38	Ver:	C
Sheet Size: B		Rev:	03
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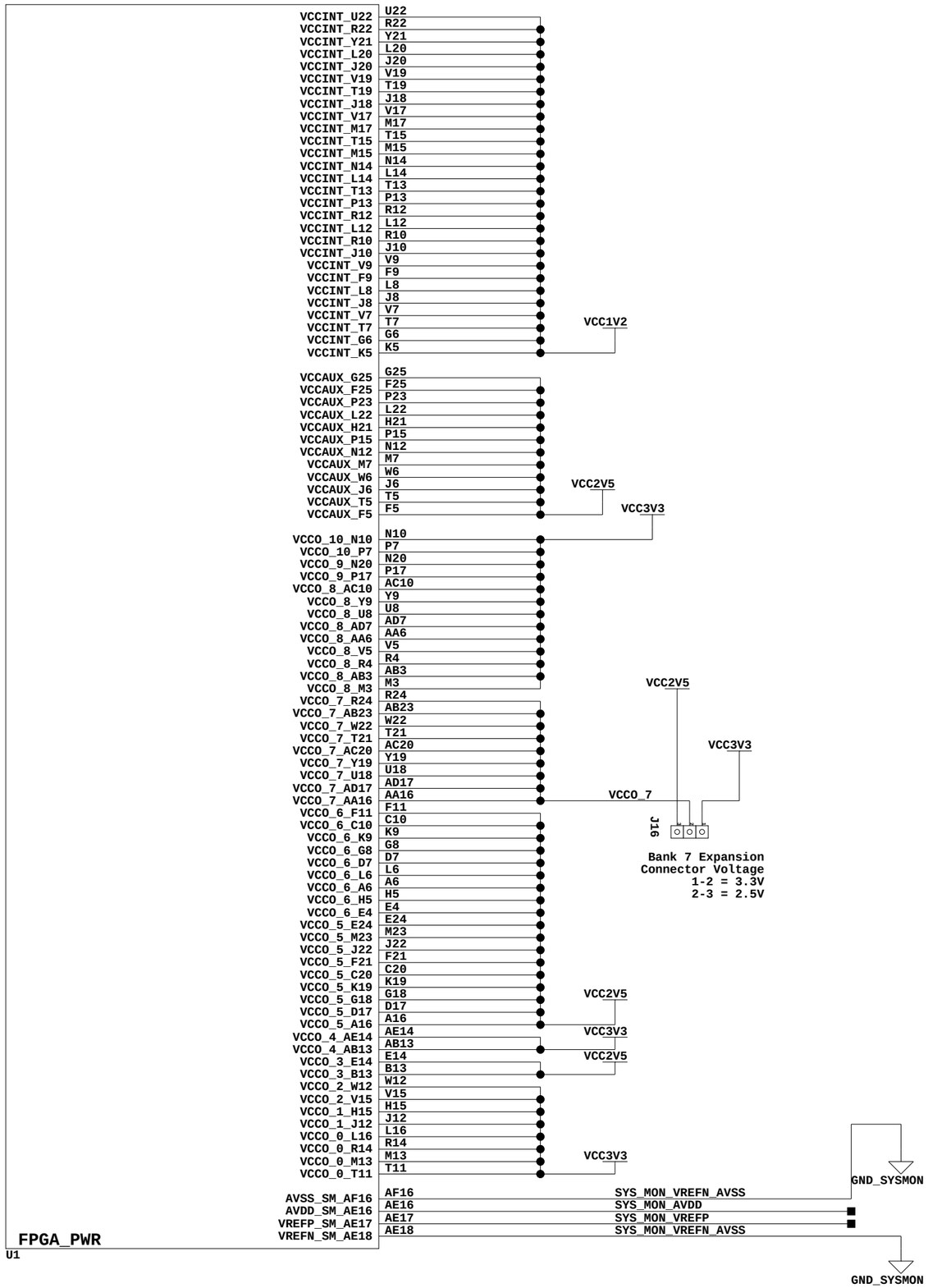

Title:
SCHEM, ML405 EVAL PLATFORM
FPGA Ground and Power

0381199

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ACEFLASH

SYSTEMACE TQFP144 (DIE DOWN)

DEVICE=XCCACE-TQ144I
PKG_TYPE=TQ144
PARTS=1
LEVEL=STD

U2

P113

SysACE Failsafe Mode Jumpers

Combined FPGA & CPU PC4 Connector J20

"SYSACE RESET" Pushbutton SW2

Title:	SCHEM, ML405 EVAL PLATFORM System ACE 0381199
Date:	12-11-2007_19:38
Ver:	C
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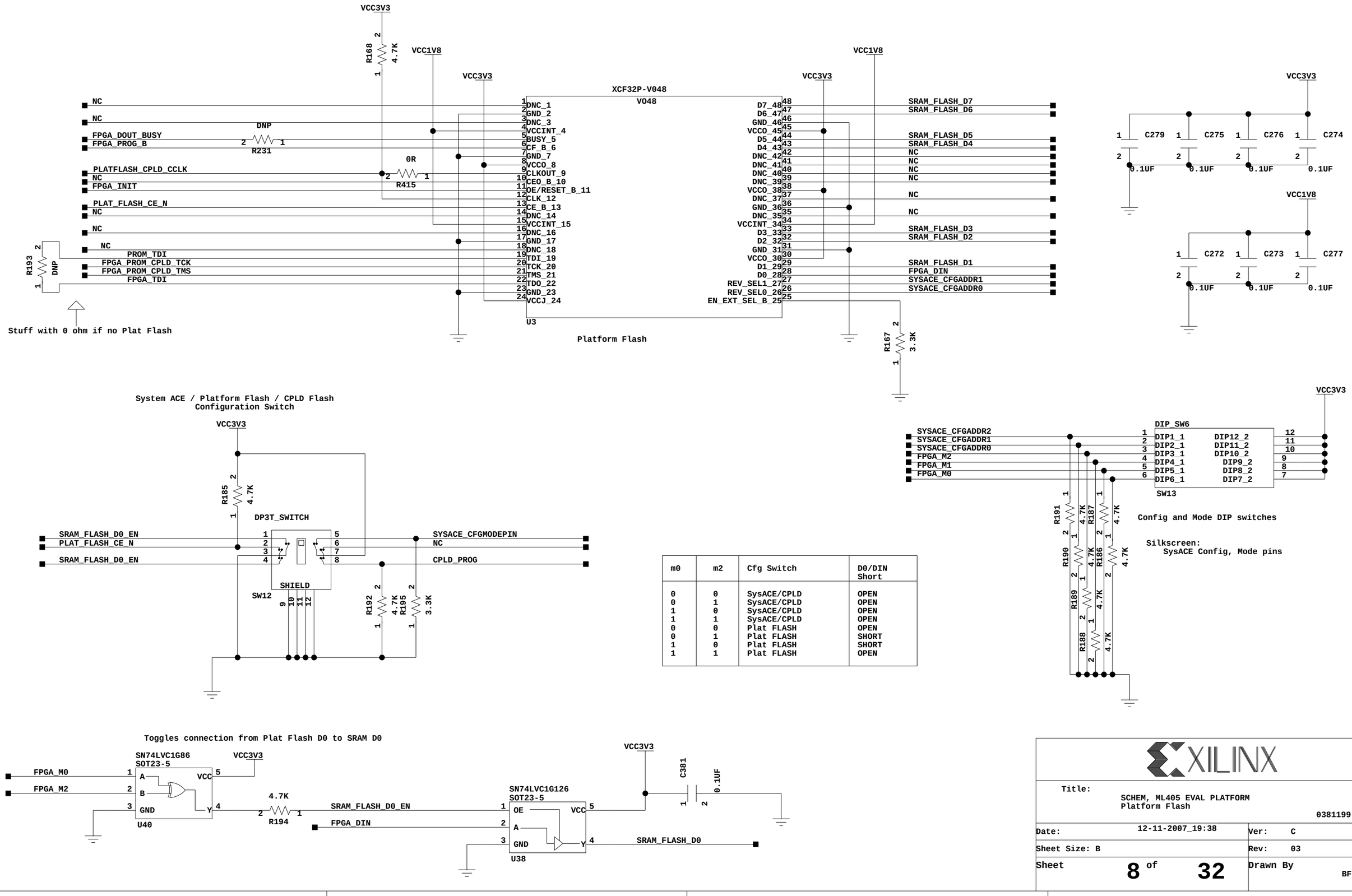
VCC3V3
R168 2 4.7K 1
VCC1V8
VCC3V3
XCF32P-V048
VO48
NC
NC
FPGA_DOUT_BUSY
FPGA_PROG_B
DNP
R231
PLATFLASH_CPLD_CCLK
NC
FPGA_INIT
0R
R415
PLAT_FLASH_CE_N
NC
NC
NC
PROM_TDI
FPGA_PROM_CPLD_TCK
FPGA_PROM_CPLD_TMS
FPGA_TDI
R193 DNP
Stuff with 0 ohm if no Plat Flash
DNC_1
GND_2
DNC_3
VCCINT_4
BUSY_5
CF_B_6
GND_7
VCCO_8
CLKOUT_9
CEO_B_10
OE/RESET_B_11
CLK_12
CE_B_13
DNC_14
VCCINT_15
DNC_16
GND_17
DNC_18
TDI_19
TCK_20
TMS_21
TDO_22
GND_23
VCCJ_24
U3
D7_48
D6_47
GND_46
VCCO_45
D5_44
D4_43
DNC_42
DNC_41
DNC_40
DNC_39
VCCO_38
DNC_37
GND_36
DNC_35
VCCINT_34
D3_33
D2_32
GND_31
VCCO_30
D1_29
D0_28
REV_SEL1_27
REV_SEL0_26
EN_EXT_SEL_B_25
SRAM_FLASH_D7
SRAM_FLASH_D6
SRAM_FLASH_D5
SRAM_FLASH_D4
NC
NC
NC
NC
NC
SRAM_FLASH_D3
SRAM_FLASH_D2
SRAM_FLASH_D1
FPGA_DIN
SYSACE_CFGADDR1
SYSACE_CFGADDR0
R167 2 3.3K 1
Platform Flash
VCC3V3
C279 C275 C276 C274
0.1UF
VCC1V8
C272 C273 C277
0.1UF
System ACE / Platform Flash / CPLD Flash
Configuration Switch
VCC3V3
R185 2 4.7K 1
DP3T_SWITCH
SRAM_FLASH_D0_EN
PLAT_FLASH_CE_N
SRAM_FLASH_D0_EN
SYSACE_CFGMODEPIN
NC
CPLD_PROG
SHIELD
SW12
R192 2 4.7K 1
R195 2 3.3K 1
SYSACE_CFGADDR2
SYSACE_CFGADDR1
SYSACE_CFGADDR0
FPGA_M2
FPGA_M1
FPGA_M0
DIP_SW6
DIP1_1
DIP2_1
DIP3_1
DIP4_1
DIP5_1
DIP6_1
DIP12_2
DIP11_2
DIP10_2
DIP9_2
DIP8_2
DIP7_2
SW13
R191 R187 R190 R186 R189 R188 4.7K
Config and Mode DIP switches
Silkscreen:
SysACE Config, Mode pins
m0 | m2 | Cfg Switch | D0/DIN Short
0 | 0 | SysACE/CPLD | OPEN
0 | 1 | SysACE/CPLD | OPEN
1 | 0 | SysACE/CPLD | OPEN
1 | 1 | SysACE/CPLD | OPEN
0 | 0 | Plat FLASH | OPEN
0 | 1 | Plat FLASH | SHORT
1 | 0 | Plat FLASH | SHORT
1 | 1 | Plat FLASH | OPEN
Toggles connection from Plat Flash D0 to SRAM D0
SN74LVC1G86
SOT23-5
U40
FPGA_M0
FPGA_M2
4.7K
R194
SRAM_FLASH_D0_EN
SN74LVC1G126
SOT23-5
U38
FPGA_DIN
C381 0.1UF
SRAM_FLASH_D0
XILINX
Title:
SCHEM, ML405 EVAL PLATFORM
Platform Flash
0381199
Date: 12-11-2007_19:38
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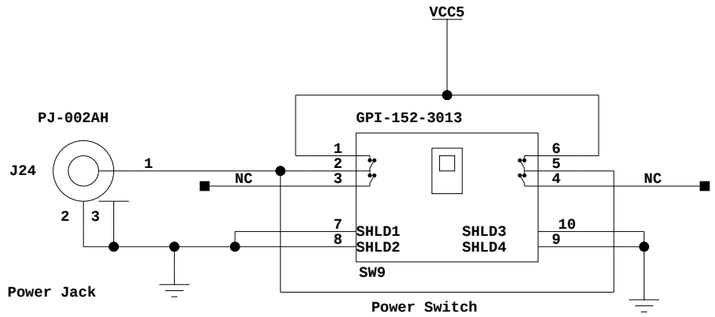

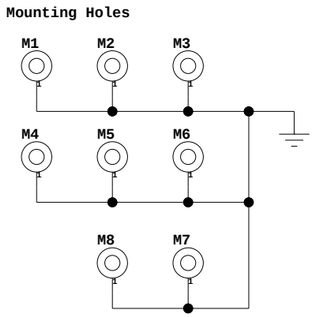

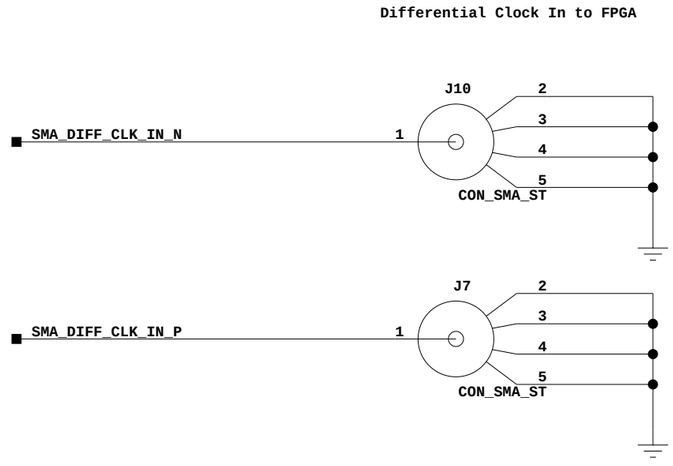

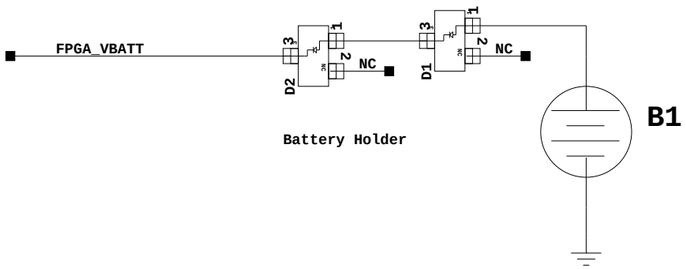

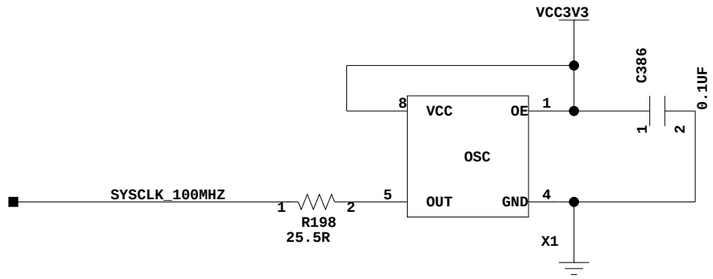

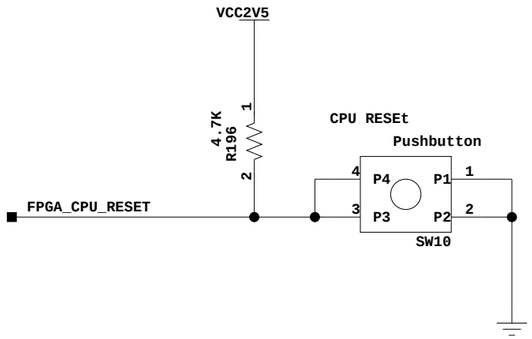

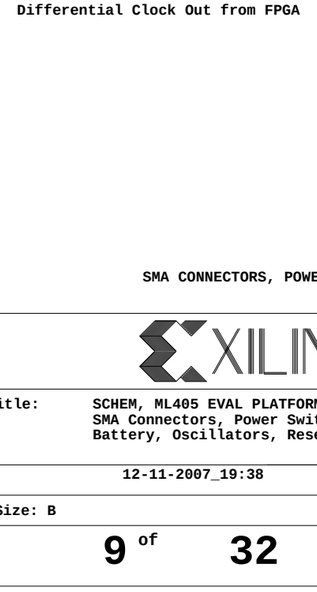

SMA CONNECTORS, POWER SWITCH,

XILINX

Title:	SCHEM, ML405 EVAL PLATFORM SMA Connectors, Power Switch, Battery, Oscillators, Reset	0381199	
Date:	12-11-2007_19:38	Ver:	C
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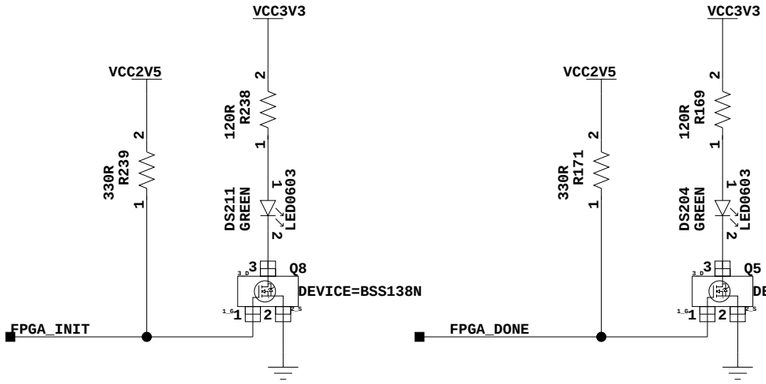

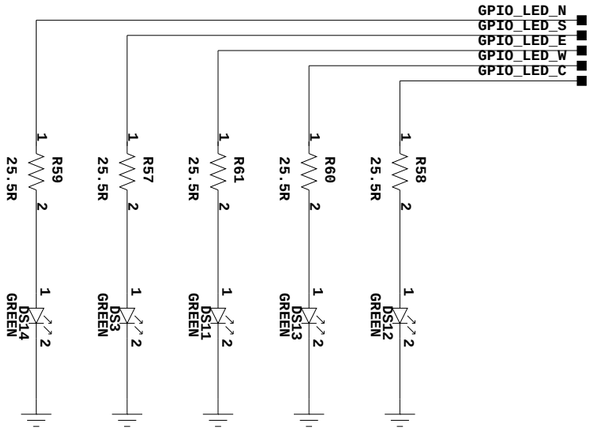

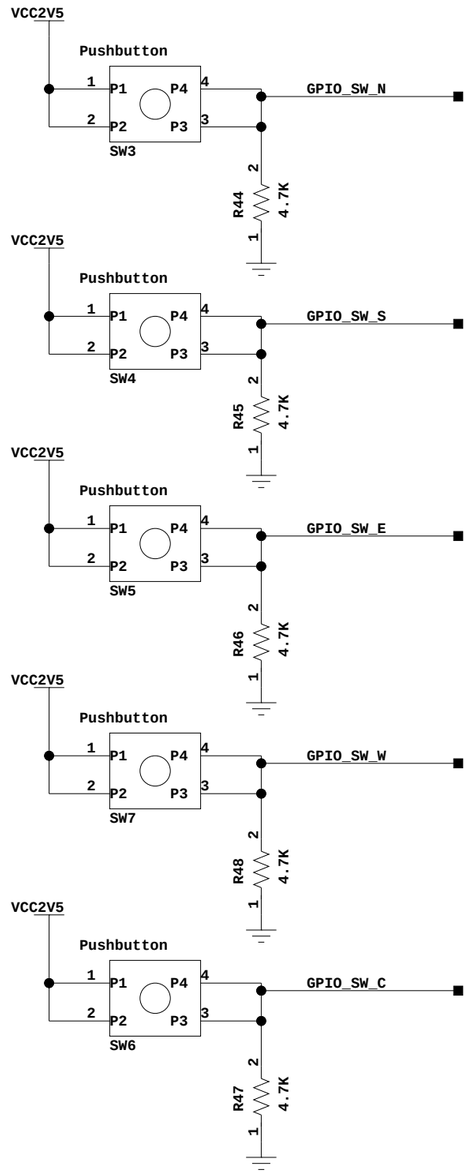

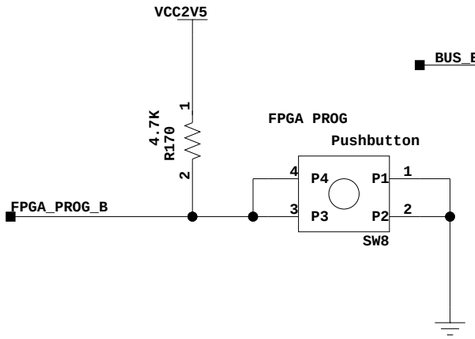

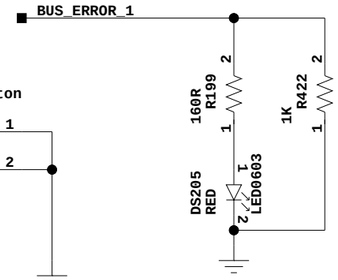

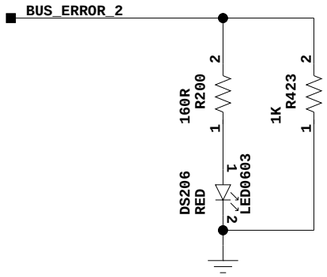

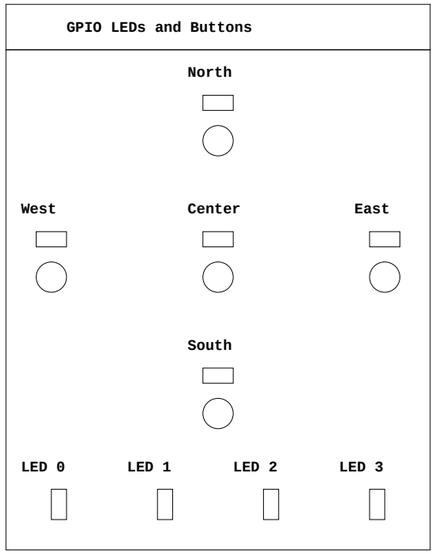

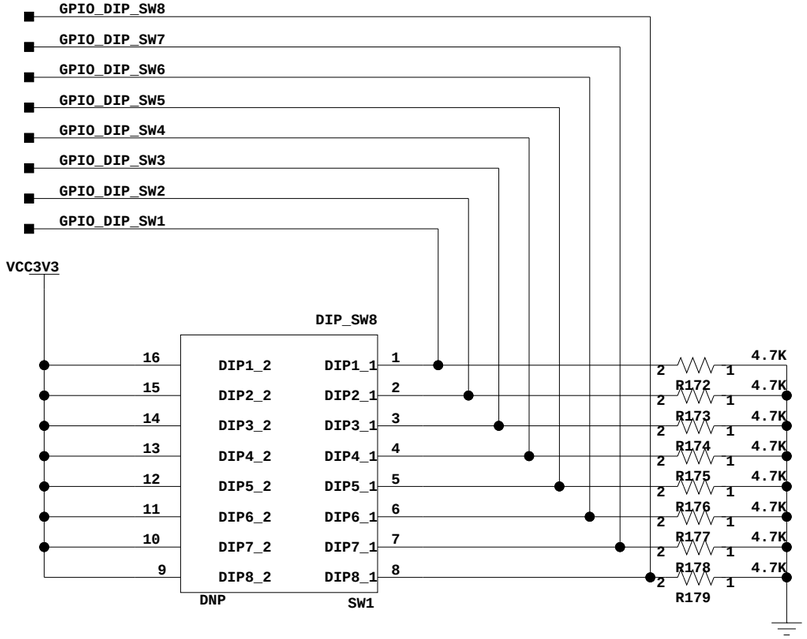

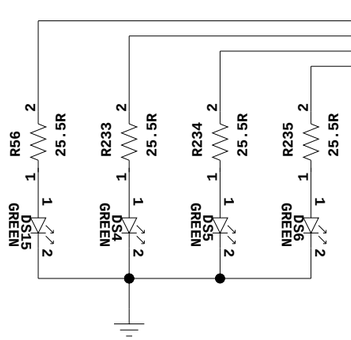

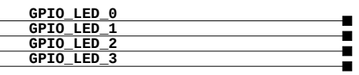

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
Buttons, LEDs, Switches

0381199

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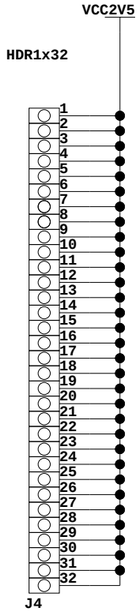

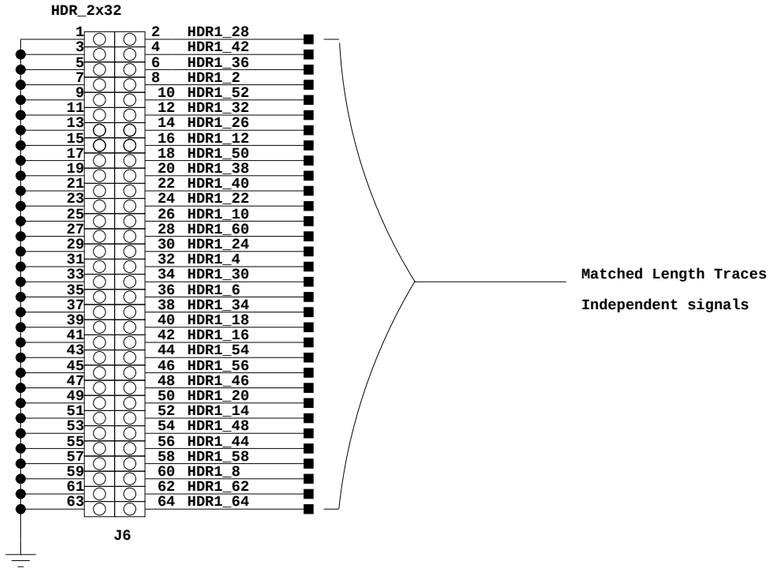

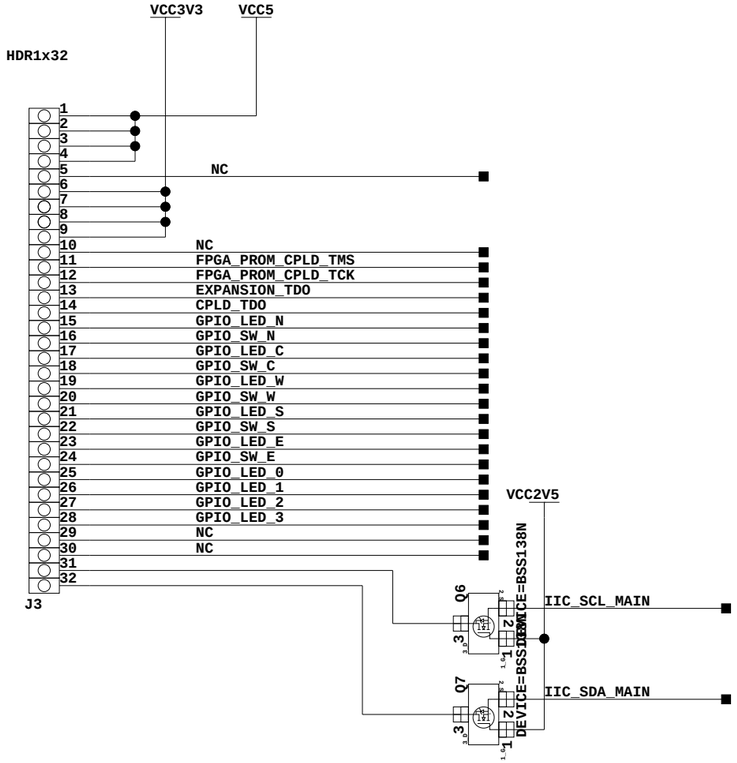

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
Expansion Headers

0381199

Date:	12-11-2007_19:38	Ver:	C
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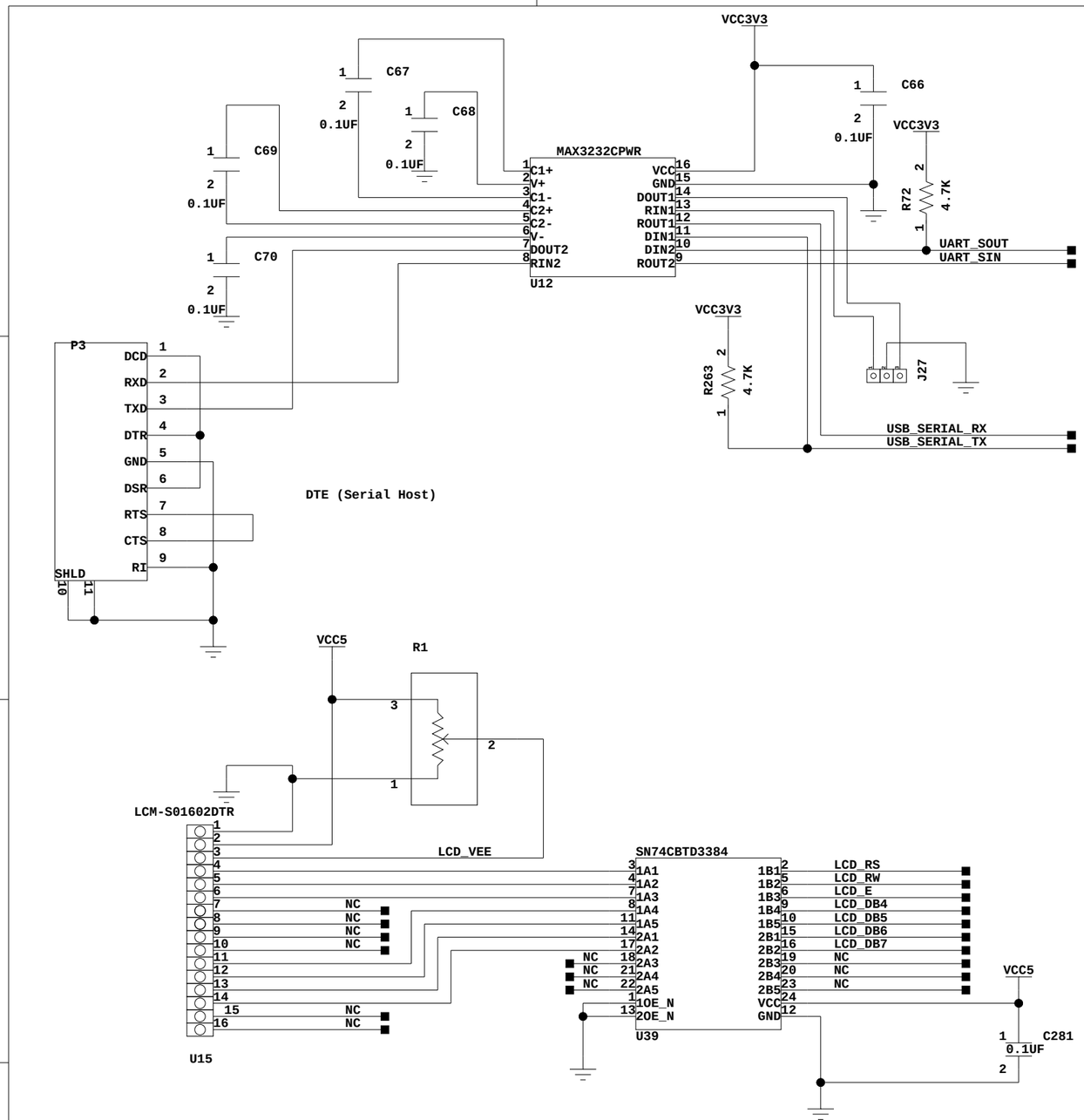

Title:	SCHEM, ML405 EVAL PLATFORM LCD, PS2, UART, IIC EEPROM
	0381199
Date:	12-11-2007_19:56
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Matched Length Nets

DDR_A3
DDR_A2
DDR_A1
DDR_A0
DDR_A10
DDR_BA1
DDR_BA0
DDR_CS_N

DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_DM2
DDR_A13
DDR_DQS2
DDR_D23
DDR_D22

DDR_D20
DDR_D19
DDR_D18
DDR_D17
DDR_D16

DDR_DM3

DDR_DQS3
DDR_D24
DDR_D25
DDR_D26
DDR_D27
DDR_D28
DDR_D29
DDR_D30

DDR_A7
DDR_A6
DDR_A5
DDR_A4
DDR_A12
DDR_A11
DDR_A9
DDR_A8

DDR_DM1
DDR_CK1_N
DDR_CK1_P
DDR_CKE
DDR_D10
DDR_D9
DDR_D8
DDR_DQS1

DDR_D14
DDR_D13
DDR_D12
DDR_D11
DDR_D7
DDR_DQS0
DDR_DM0
DDR_D15

DDR_D3
DDR_D4
DDR_D5
DDR_D6
DDR_D31
DDR_D0
DDR_D1
DDR_D2
DDR_D21

VTTDDR
VCC2V5

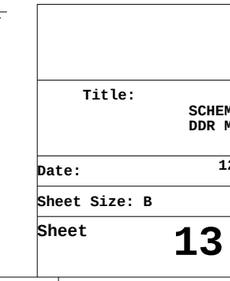
RP1 47R
RP2 47R
RP3 47R
RP4 47R
RP5 47R
RP6 47R
RP7 47R
RP8 47R
RP9 47R
RP10 47R
RP11 47R
RP12 47R
RP13 47R
RP14 47R
RP15 47R
RP16 47R
R73 47R

NC
NC

C424 0.1UF
C82 0.1UF
C41 100UF
C300 100UF
C423 0.1UF
C81 0.1UF
C40 100UF
C301 100UF
C422 0.1UF
C80 0.1UF
C39 100UF
C302 100UF
C421 0.1UF
C71 0.1UF
C38 100UF
C408 0.1UF
C407 0.1UF
C72 0.1UF
C73 0.1UF
C74 0.1UF
C75 0.1UF
C76 0.1UF
C77 0.1UF
C78 0.1UF
C79 0.1UF

U4
U5

64Mx16x4
DDR SDRAM
HYB25D256160BT-7F
TSOP66



Title:
SCHEM, ML405 EVAL PLATFORM
DDR Memory

0381199

Date: 12-11-2007_19:56	Ver: C
Sheet Size: B	Rev: 03
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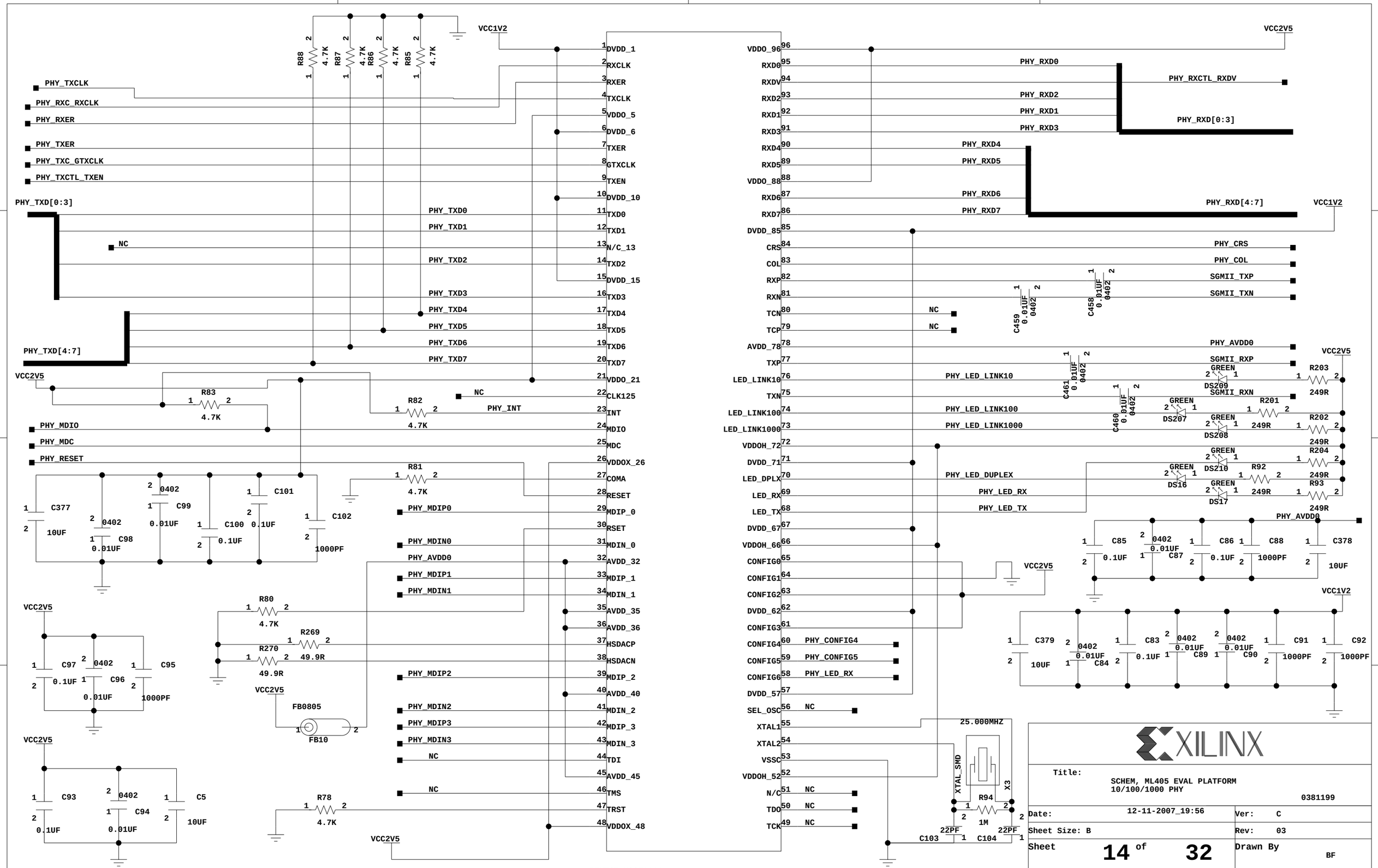
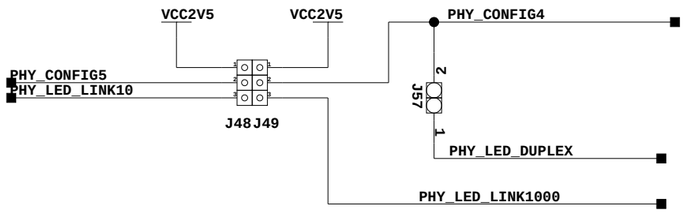
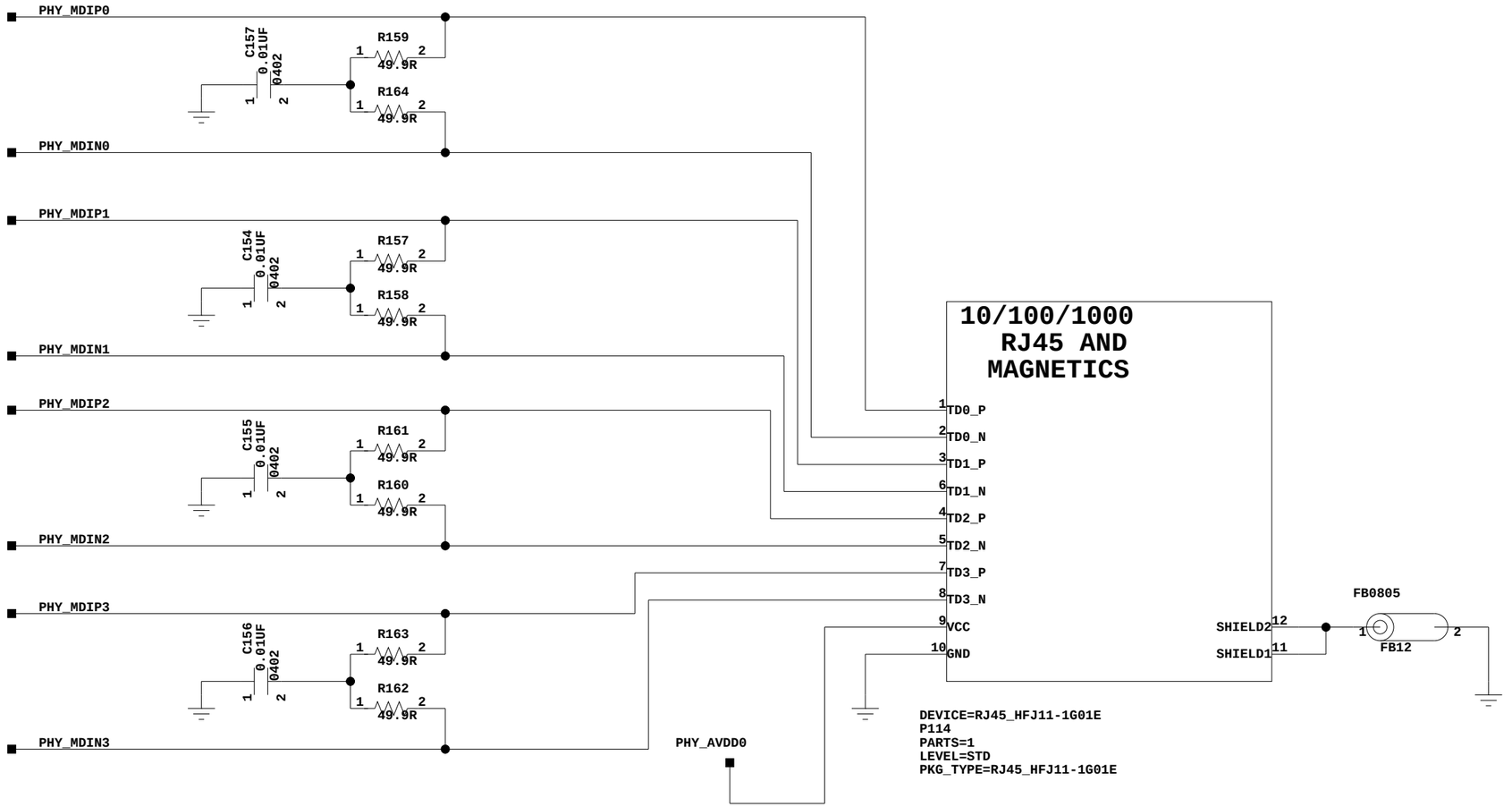

VCC1V2
VCC2V5
R88 4.7K
R87 4.7K
R86 4.7K
R85 4.7K
PHY_TXCLK
PHY_RXC_RXCLK
PHY_RXER
PHY_TXER
PHY_TXC_GTXCLK
PHY_TXCTL_TXEN
PHY_TXD[0:3]
PHY_TXD[4:7]
NC
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_MDIO
PHY_MDC
PHY_RESET
PHY_INT
R83 4.7K
R82 4.7K
C377 10UF
C98 0.01UF
C99 0.01UF
C100 0.1UF
C101 0.1UF
C102 1000PF
C97 0.1UF
C96 0.01UF
C95 1000PF
C93 0.1UF
C94 0.01UF
C5 10UF
R81 4.7K
R80 4.7K
R269
R270 49.9R
49.9R
FB0805
FB10
R78 4.7K
PHY_MDIP0
PHY_MDIN0
PHY_AVDD0
PHY_MDIP1
PHY_MDIN1
PHY_MDIP2
PHY_MDIN2
PHY_MDIP3
PHY_MDIN3
DVDD_1
RXCLK
RXER
TXCLK
VDDO_5
DVDD_6
TXER
GTXCLK
TXEN
DVDD_10
TXD0
TXD1
N/C_13
TXD2
DVDD_15
TXD3
TXD4
TXD5
TXD6
TXD7
VDDO_21
CLK125
INT
MDIO
MDC
VDDOX_26
COMA
RESET
MDIP_0
RSET
MDIN_0
AVDD_32
MDIP_1
MDIN_1
AVDD_35
AVDD_36
HSDACP
HSDACN
MDIP_2
AVDD_40
MDIN_2
MDIP_3
MDIN_3
TDI
AVDD_45
TMS
TRST
VDDOX_48
VDDO_96
RXD0
RXDV
RXD2
RXD1
RXD3
RXD4
RXD5
VDDO_88
RXD6
RXD7
DVDD_85
CRS
COL
RXP
RXN
TCN
TCP
AVDD_78
TXP
LED_LINK10
TXN
LED_LINK100
LED_LINK1000
VDDOH_72
DVDD_71
LED_DPLX
LED_RX
LED_TX
DVDD_67
VDDOH_66
CONFIG0
CONFIG1
CONFIG2
DVDD_62
CONFIG3
CONFIG4
CONFIG5
CONFIG6
DVDD_57
SEL_OSC
XTAL1
XTAL2
VSSC
VDDOH_52
N/C
TDO
TCK
PHY_CONFIG4
PHY_CONFIG5
PHY_LED_RX
PHY_RXD0
PHY_RXD2
PHY_RXD1
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_RXCTL_RXDV
PHY_RXD[0:3]
PHY_RXD[4:7]
PHY_CRS
PHY_COL
SGMII_TXP
SGMII_TXN
C459 0.01UF
C458 0.01UF
PHY_AVDD0
SGMII_RXP
SGMII_RXN
PHY_LED_LINK10
PHY_LED_LINK100
PHY_LED_LINK1000
PHY_LED_DUPLEX
PHY_LED_RX
PHY_LED_TX
C461 0.01UF
C460 0.01UF
GREEN DS209
GREEN DS207
GREEN DS208
GREEN DS210
GREEN DS16
GREEN DS17
R203 249R
R201 249R
R202 249R
R204 249R
R92 249R
R93 249R
C85 0.1UF
C87 0.01UF
C86 0.1UF
C88 1000PF
C378 10UF
C379 10UF
C83 0.01UF
C84 0.01UF
C89 0.01UF
C90 1000PF
C91 1000PF
C92 1000PF
25.000MHZ
XTAL_SMD
X3
R94 1M
22PF C103
22PF C104
DEVICE=M88E1111
U70
PARTS=1
XILINX
Title:
SCHEM, ML405 EVAL PLATFORM
10/100/1000 PHY
0381199
Date: 12-11-2007_19:56
Ver: C
Sheet Size: B
Rev: 03
Sheet 14 of 32
Drawn By BF

J48, J49 pins 1-2: GMII/MII to Cu
J48, J49 pins 2-3: SGMII to Cu, no clk
J48 pins 1-2, J57 ON: RGMII, modified MII in Cu



Pin to Constant Mapping	
Pin	Bit[2:0]
VCC2V5	111
PHY_LED_LINK10	110
PHY_LED_LINK100	101
PHY_LED_LINK1000	100
PHY_LED_DUPLEX	011
PHY_LED_RX	010
PHY_LED_TX	001
GND	000

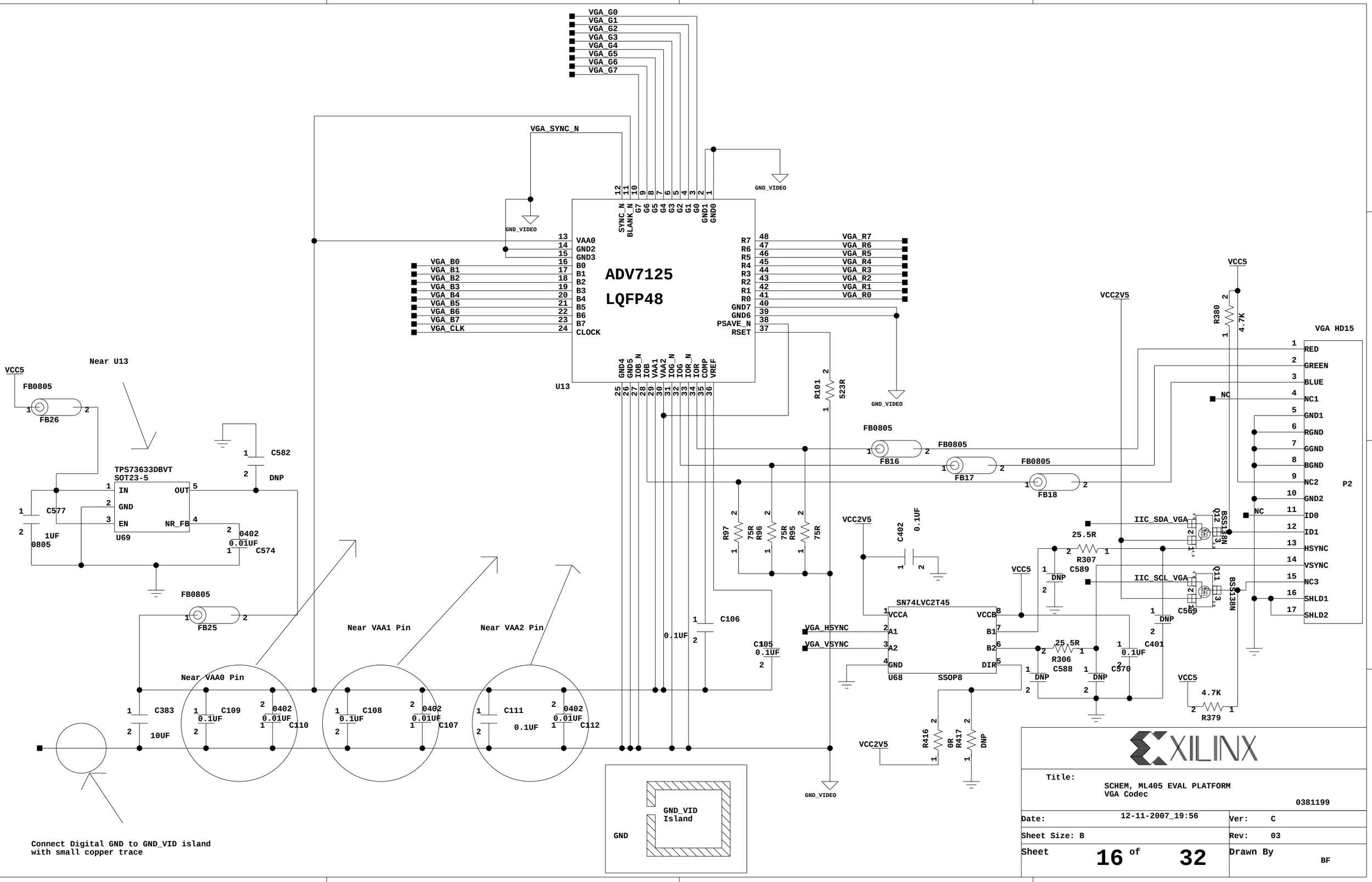


Pin	Bit[2]	Bit[1]	Bit[0]		
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddress "00000". Do not advertise the PAUSE bit
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg enabled, advertise all capabilities; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CONFIG3	ANEG[0]	ENA_XC	DIS_125	111	
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	111	
CONFIG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW Interrupt. 50Ohm SERDES option.

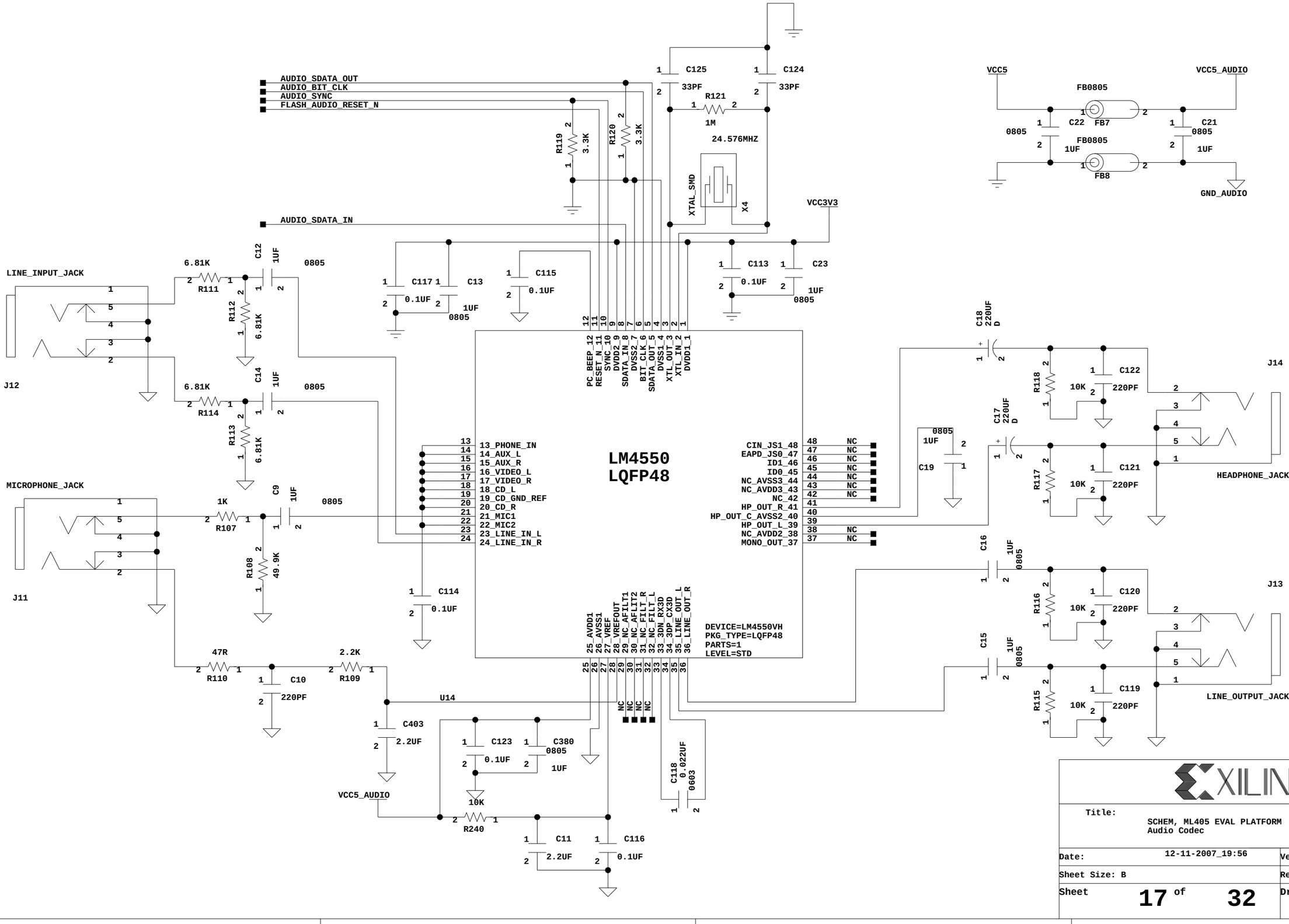
XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
RJ45 Connector and
PHY Decoupling
0381199

Date: 12-11-2007_19:56	Ver: C
Sheet Size: B	Rev: 03
Sheet 15 of 32	Drawn By BF



Title:	SCHEM, ML405 EVAL PLATFORM VGA Codec 0381199
Date: 12-11-2007_19:56	Ver: C
Sheet Size: B	Rev: 03
Sheet 16 of 32	Drawn By BF

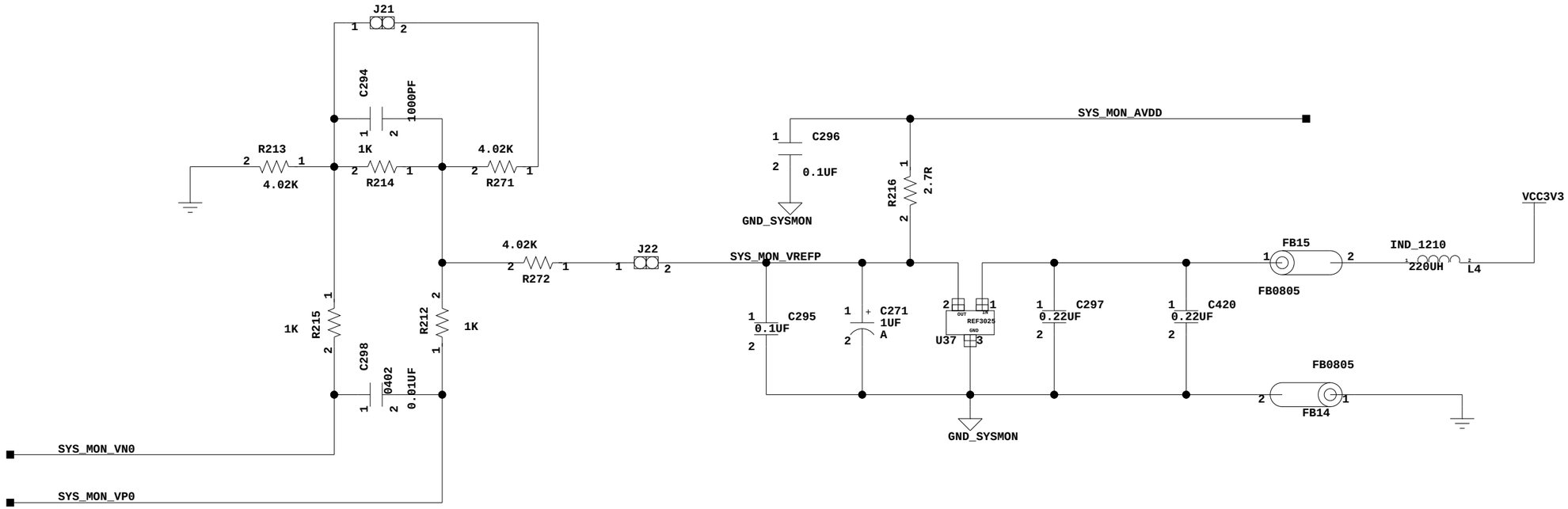


XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
Audio Codec

0381199

Date: 12-11-2007_19:56	Ver: C
Sheet Size: B	Rev: 03
Sheet 17 of 32	Drawn By BF



XILINX

Title: SCHEM, ML405 EVAL PLATFORM System Monitor DVM Circuit			0381199
Date:	12-11-2007_19:56	Ver:	C
Sheet Size: B		Rev:	03
Sheet	18 of 32	Drawn By	BF

USB Peripheral 2

USB_B

VCC 1
D- 2
D+ 3
GND 4
J1

20.0K
R275
R276 49.9K
USB_GPIO25
C425
0.1UF

USB Peripheral 1

USB_B

VCC 1
D- 2
D+ 3
GND 4
J2

20.0K
R283
R284 49.9K
C426
0.1UF

VCC5

C419
0.1UF

MIC2525-2B
U44
SOP8
OUT2
IN
OUT1
NC2
EN
FLG
GND
NC1
NC
NC
USB_GPIO29
R268 4.7K
0R
R277
USB_GPIO26

FB0805
FB9
C42
150UF
D

J28

USB Host 1

USB Power

USB_A

VCC 1
D- 2
D+ 3
GND 4
J19

FB0805
FB13
C418
0.01UF
0402

VCC3V3

C128 0.1UF
C129 0.1UF
C130 0.1UF
C131 0.1UF
C132 0.1UF

Bypass cap for USB chip

U11

CY7C67300-100AI
TQFP100
(DIE UP)

1_A1
2_A2
3_A3
4_DM2B
5_DP2B
6_AGND
7_A4
8_A5
9_DM2A
10_DP2A
11_OTGVBUS
12_CSWITCHB
13_CSWITCHA
14_VSWITCH
15_BOOSTGND
16_BOOSTVCC
17_A6
18_DM1B
19_DP1B
20_A7
21_AVCC
22_DM1A
23_DP1A
24_A8
25_A9

GND2_75
D8_MISO_74
D9_nSSI_73
D10_SCK_72
D11_MOSI_71
D12_TXD_70
D13_RXD_69
D14_RTS_68
D15_CTS_67
GPIO8_D8_MISO_66
GPIO9_D9_nSSI_65
nWR_64
VCC0_63
nRD_62
GPIO10_D10_SCK_61
GPIO11_D11_MOSI_60
GPIO12_D12_59
GPIO13_D13_58
GPIO14_D14_57
GPIO15_D15_nSSI_56
GPIO16_A0_TXD_PWM0_55
GPIO17_A1_RXD__54
GPIO18_A2_RTS__53
GPIO19_A0_CS0_52
GND1_51

SYSACE_USB_D8
SYSACE_USB_D9
SYSACE_USB_D10
SYSACE_USB_D11
SYSACE_USB_D12
SYSACE_USB_D13
SYSACE_USB_D14
SYSACE_USB_D15
SYSACE_A1_USB_A0

GND3_100
nBEL_A0_99
nBEH_98
A16_97
A18_96
A17_95
GPIO0_D0_94
GPIO1_D1_93
GPIO2_D2_92
GPIO3_D3_91
GPIO4_D4_90
GPIO5_D5_89
VCC2_88
GPIO6_D6_87
GPIO7_D7_86
nRESET_85
Reserved_84
D0_83
D1_82
D2_81
D3_80
D4_79
D5_78
D6_77
D7_76

SYSACE_USB_D0
SYSACE_USB_D1
SYSACE_USB_D2
SYSACE_USB_D3
SYSACE_USB_D4
SYSACE_USB_D5
SYSACE_USB_D6
SYSACE_USB_D7

USB_RESET_N
R282 4.7K

POR for USB
Reset Supervisor
U46
MCP130
C427
0.1UF

GND0
A10
XTALOUT
XTALIN
A11
A12
A13
A14
nMEMSEL
nROMSEL
nRAMSEL
VCC1
A15
GPIO31_SCK
GPIO30_SDA
GPIO29_OTGID
GPIO28_TX
GPIO27_RX
GPIO26_CTS_PWM3
GPIO25_IRQ1
GPIO24_INT_IORDY_IRQ0
GPIO23_nRD_IOR
GPIO22_nWR_IOW
GPIO21_nCS
GPIO20_A1_CS1

C126 22PF
C127 22PF
C133 0.1UF
12MHZ X5
XTAL_SMD
R122 1M
R273 2.80K
R274 49.9K
R264 10K
R265 10K

USB_GPIO30
USB_GPIO29
USB_SERIAL_TX
USB_SERIAL_RX
USB_GPIO26
USB_GPIO25
USB_INT
SYSACE_MPOE_USB_RD_N
SYSACE_MPWE_USB_WR_N
USB_CS_N
SYSACE_A2_USB_A1

24LC128IST
U17
TSSOP8
A0
A1
A2
VSS
VCC
WP
SCL
SDA
IIC_SCL_USB
IIC_SDA_USB

DNP
R278 0R
DNP
R279 0R
R280 0R
R281 0R
J32
J31

1Kb to 16Kb EEPROM

SCL -> GPIO31
SDA -> GPIO30

Above 16Kb EEPROM

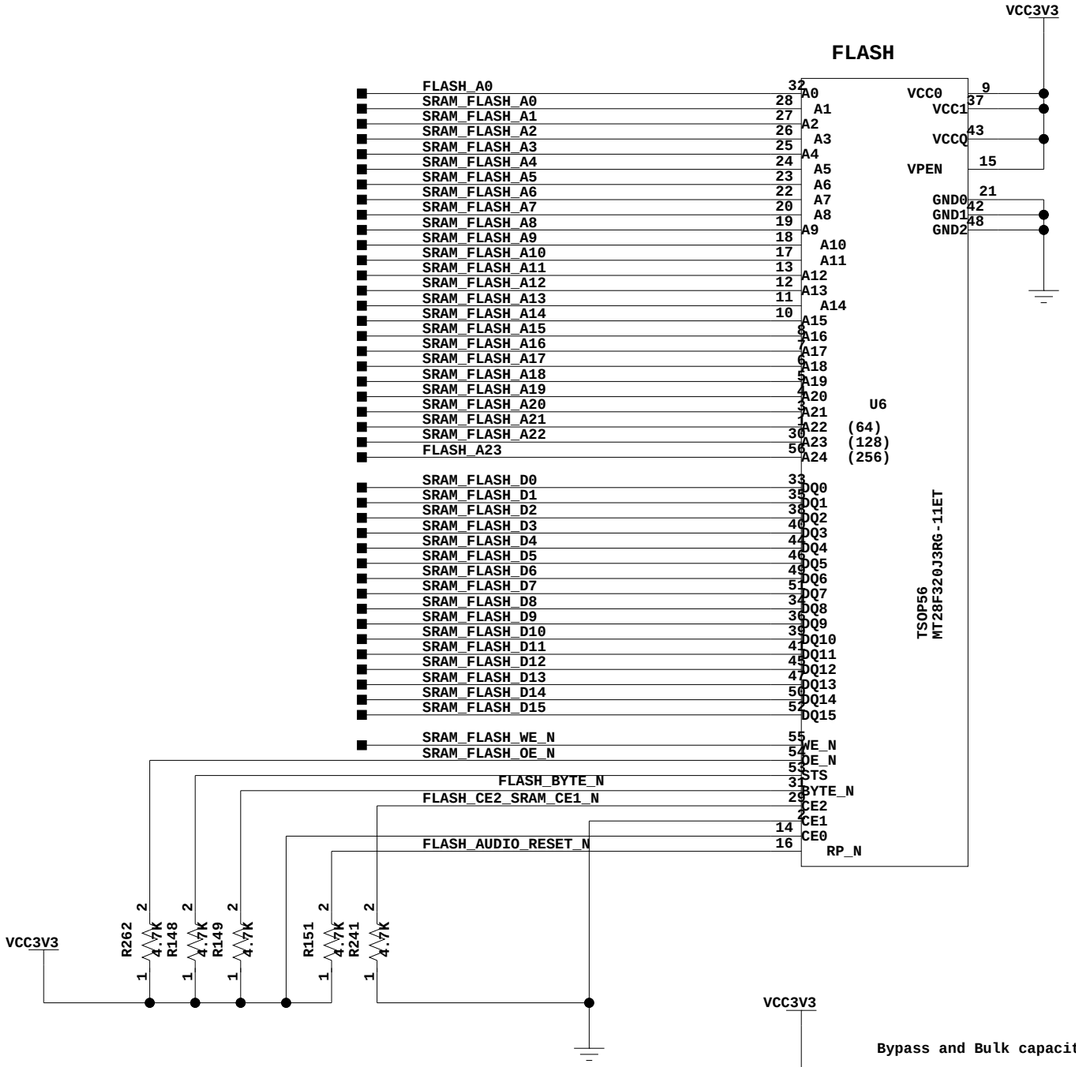
SCL -> GPIO30
SDA -> GPIO31

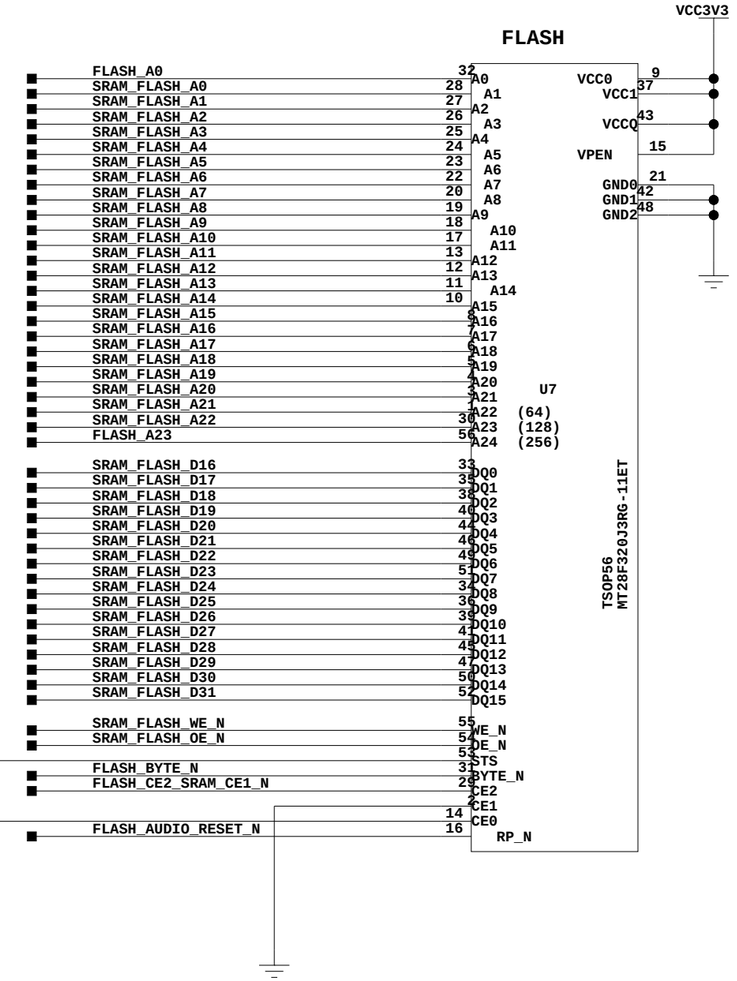
XILINX

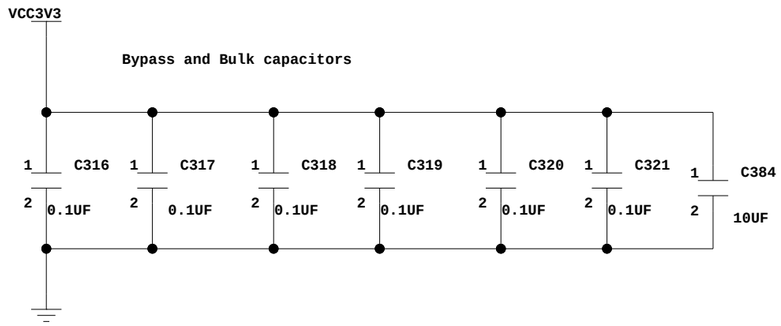
Title: SCHEM, ML405 EVAL PLATFORM USB

0381199

Date: 12-11-2007_19:56	Ver: C
Sheet Size: B	Rev: 03
Sheet 19 of 32	Drawn By BF







Title: SCHEM, ML405 EVAL PLATFORM Flash Memory	0381199
Date: 12-11-2007_19:56	Ver: C
Sheet Size: B	Rev: 03
Sheet 20 of 32	Drawn By BF

The burst order mode of the SRAM is set to "Linear" by default

VCC3V3

R210 4.7K
R209 4.7K
R208 4.7K
R211 4.7K
R424 2.2K

FLASH_CE2_SRAM_CE1_N	98	98_CE1_N
SRAM_MODE	31	MODE_31
SRAM_ZZ	64	ZZ_64
SRAM_BW1	93	93_BWA_N
SRAM_BW0	94	94_BWB_N
SRAM_BW3	95	95_BWC_N
SRAM_BW2	96	96_BWD_N
SRAM_ADV_LD_N	85	85_ADV/LD_N
SRAM_FLASH_OE_N	86	86_OE_N
SRAM_FLASH_WE_N	88	88_WE_N
SRAM_CLK	89	89_CLK
SRAM_FLASH_A0	37	37_A0
SRAM_FLASH_A1	36	36_A1
SRAM_FLASH_A2	35	35_A
SRAM_FLASH_A3	34	34_A
SRAM_FLASH_A4	33	33_A
SRAM_FLASH_A5	32	32_A
SRAM_FLASH_A6	44	44_A
SRAM_FLASH_A7	45	45_A
SRAM_FLASH_A8	46	46_A
SRAM_FLASH_A9	47	47_A
SRAM_FLASH_A10	48	48_A
SRAM_FLASH_A11	49	49_A
SRAM_FLASH_A12	50	50_A
SRAM_FLASH_A13	81	81_A
SRAM_FLASH_A14	82	82_A
SRAM_FLASH_A15	83	83_A
SRAM_FLASH_A16	99	99_A
SRAM_FLASH_A17	100	100_A
SRAM_FLASH_A18	84	84_E18
SRAM_FLASH_A19	43	43_E36
SRAM_FLASH_A20	42	42_E72
SRAM_FLASH_A21	39	39_E144
SRAM_FLASH_A22	38	38_E288
SRAM_DQP2	1	1_DQPC
SRAM_FLASH_D31_RES	2	2_DQC
SRAM_FLASH_D30_RES	3	3_DQC
SRAM_FLASH_D29_RES	6	6_DQC
SRAM_FLASH_D28_RES	7	7_DQC
SRAM_FLASH_D27_RES	8	8_DQC
SRAM_FLASH_D26_RES	9	9_DQC
SRAM_FLASH_D25_RES	12	12_DQC
SRAM_FLASH_D24_RES	13	13_DQC
SRAM_FLASH_D23_RES	18	18_DQD
SRAM_FLASH_D22_RES	19	19_DQD
SRAM_FLASH_D21_RES	22	22_DQD
SRAM_FLASH_D20_RES	23	23_DQD
SRAM_FLASH_D19_RES	24	24_DQD
SRAM_FLASH_D18_RES	25	25_DQD
SRAM_FLASH_D17_RES	28	28_DQD
SRAM_FLASH_D16_RES	29	DQD_29
SRAM_DQP3	30	DQPD_30
SRAM_DQP0	51	DQPA_51
SRAM_FLASH_D15_RES	52	DQA_52
SRAM_FLASH_D14_RES	53	DQA_53
SRAM_FLASH_D13_RES	56	DQA_56
SRAM_FLASH_D12_RES	57	DQA_57
SRAM_FLASH_D11_RES	58	DQA_58
SRAM_FLASH_D10_RES	59	DQA_59
SRAM_FLASH_D9_RES	62	DQA_62
SRAM_FLASH_D8_RES	63	DQA_63
SRAM_FLASH_D7_RES	68	DQB_68
SRAM_FLASH_D6_RES	69	DQB_69
SRAM_FLASH_D5_RES	72	DQB_72
SRAM_FLASH_D4_RES	73	DQB_73
SRAM_FLASH_D3_RES	74	DQB_74
SRAM_FLASH_D2_RES	75	DQB_75
SRAM_FLASH_D1_RES	78	DQB_78
SRAM_FLASH_D0_RES	79	DQB_79
SRAM_DQP1	80	DQPB_80

R287 47R
R288 47R
R286 47R
R285 47R

U41 CY7C1354B TQFP100

NC_66	66	NC
NC_16	16	NC
NC_14	14	NC
VSS_90	90	
VSS_76	76	
VSS_71	71	
VSS_67	67	
VSS_60	60	
VSS_55	55	
VSS_40	40	
VSS_26	26	
VSS_21	21	
VSS_17	17	
VSS_10	10	
VSS_5	5	
VDD_91	91	
VDDQ_77	77	
VDDQ_70	70	
VDD_65	65	
VDDQ_61	61	
VDDQ_54	54	
VDD_41	41	
VDDQ_27	27	
VDDQ_20	20	
VDDQ_15	15	
VDDQ_11	11	
VDDQ_4	4	

VCC3V3

VCC3V3
C282 0.1UF
C283 0.1UF
C284 0.1UF
C285 0.1UF
C286 0.1UF

VCC3V3
C287 0.1UF
C288 0.1UF
C289 0.1UF

VCC3V3
C269 10UF

RP24 47R
RP23 47R
RP22 47R
RP21 47R
RP17 47R
RP19 47R
RP18 47R
RP20 47R

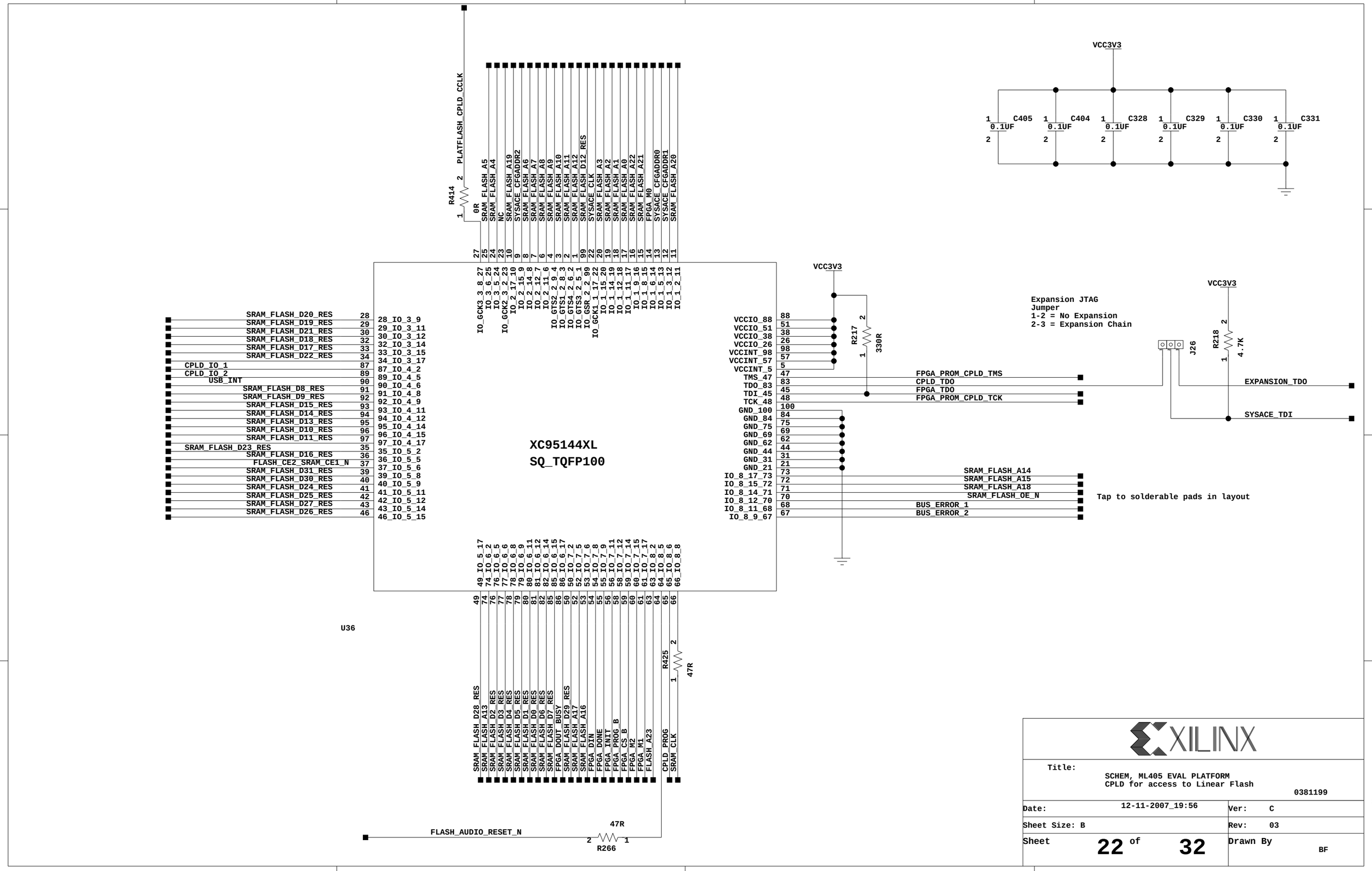
SRAM_FLASH_D23	SRAM_FLASH_D23_RES
SRAM_FLASH_D22	SRAM_FLASH_D22_RES
SRAM_FLASH_D21	SRAM_FLASH_D21_RES
SRAM_FLASH_D20	SRAM_FLASH_D20_RES
SRAM_FLASH_D19	SRAM_FLASH_D19_RES
SRAM_FLASH_D18	SRAM_FLASH_D18_RES
SRAM_FLASH_D17	SRAM_FLASH_D17_RES
SRAM_FLASH_D16	SRAM_FLASH_D16_RES
SRAM_FLASH_D31	SRAM_FLASH_D31_RES
SRAM_FLASH_D30	SRAM_FLASH_D30_RES
SRAM_FLASH_D29	SRAM_FLASH_D29_RES
SRAM_FLASH_D28	SRAM_FLASH_D28_RES
SRAM_FLASH_D27	SRAM_FLASH_D27_RES
SRAM_FLASH_D26	SRAM_FLASH_D26_RES
SRAM_FLASH_D25	SRAM_FLASH_D25_RES
SRAM_FLASH_D24	SRAM_FLASH_D24_RES
SRAM_FLASH_D7	SRAM_FLASH_D7_RES
SRAM_FLASH_D6	SRAM_FLASH_D6_RES
SRAM_FLASH_D5	SRAM_FLASH_D5_RES
SRAM_FLASH_D4	SRAM_FLASH_D4_RES
SRAM_FLASH_D3	SRAM_FLASH_D3_RES
SRAM_FLASH_D2	SRAM_FLASH_D2_RES
SRAM_FLASH_D1	SRAM_FLASH_D1_RES
SRAM_FLASH_D0	SRAM_FLASH_D0_RES
SRAM_FLASH_D15	SRAM_FLASH_D15_RES
SRAM_FLASH_D14	SRAM_FLASH_D14_RES
SRAM_FLASH_D13	SRAM_FLASH_D13_RES
SRAM_FLASH_D12	SRAM_FLASH_D12_RES
SRAM_FLASH_D11	SRAM_FLASH_D11_RES
SRAM_FLASH_D10	SRAM_FLASH_D10_RES
SRAM_FLASH_D9	SRAM_FLASH_D9_RES
SRAM_FLASH_D8	SRAM_FLASH_D8_RES

XILINX

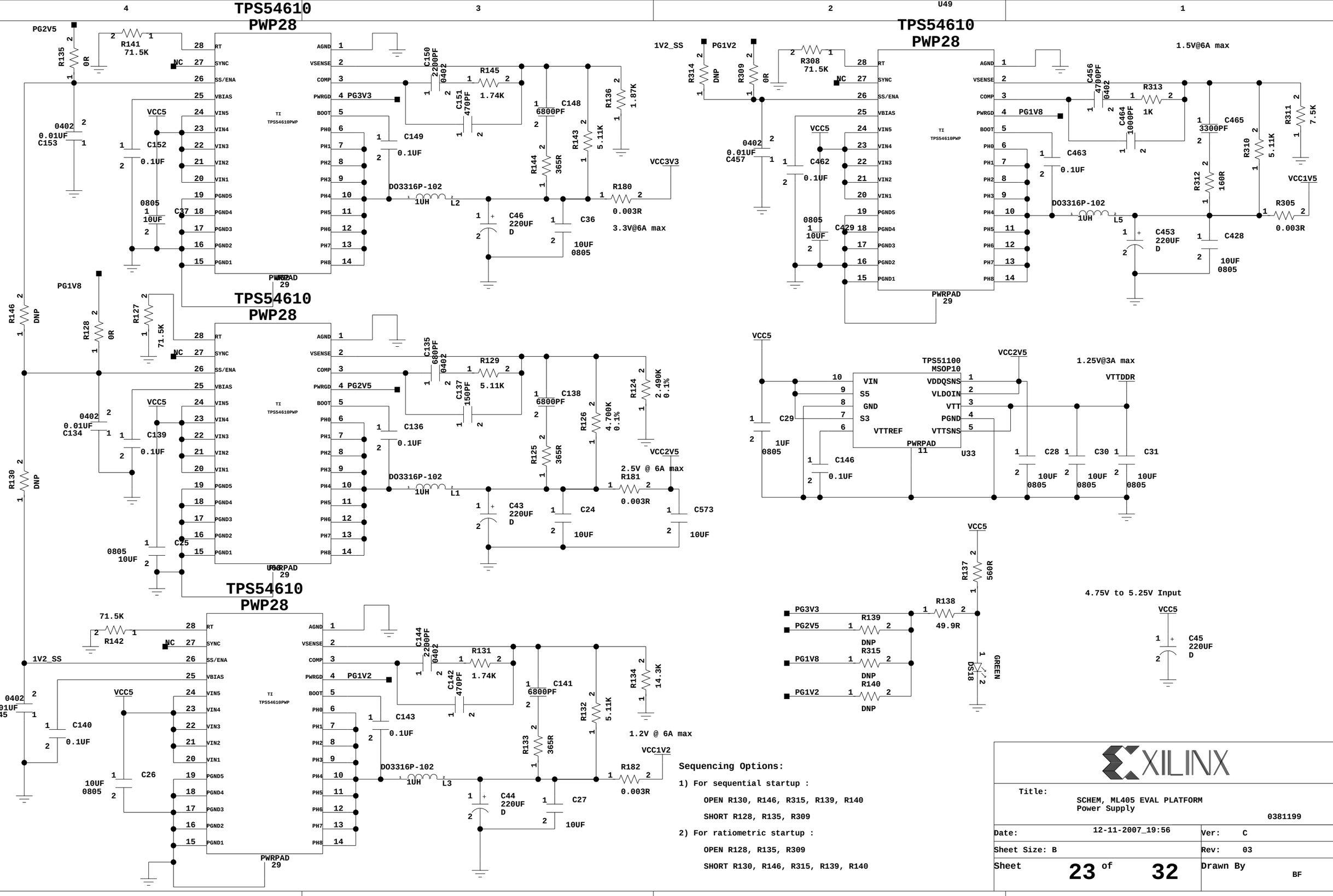
Title: SCHEM, ML405 EVAL PLATFORM
ZBT SRAM

0381199

Date: 12-11-2007_19:56	Ver: C
Sheet Size: B	Rev: 03
Sheet 21 of 32	Drawn By BF



Title:	SCHEM, ML405 EVAL PLATFORM CPLD for access to Linear Flash 0381199
Date: 12-11-2007_19:56	Ver: C
Sheet Size: B	Rev: 03
Sheet 22 of 32	Drawn By BF


TPS54610 PWP28
U49
PG2V5
R135 0R
R141 71.5K
NC
VCC5
C153 0.01UF 0402
C152 0.1UF
C37 10UF 0805
C150 2200PF 0402
R145 1.74K
C151 470PF
C149 0.1UF
C148 6800PF
R144 365R
R143 5.11K
R136 1.87K
DO3316P-102
1UH L2
C46 220UF D
C36 10UF 0805
VCC3V3
R180 0.003R
3.3V@6A max
PWRPAD 29
1V2_SS
PG1V2
R314 DNP
R309 0R
R308 71.5K
C457 0.01UF 0402
C462 0.1UF
C429 10UF 0805
C456 470PF 0402
R313 1K
C464 1000PF
PG1V8
C463 0.1UF
C465 3300PF
R312 160R
R310 5.11K
R311 7.5K
VCC1V5
DO3316P-102
1UH L5
C453 220UF D
C428 10UF 0805
R305 0.003R
1.5V@6A max
PG1V8
R146 DNP
R128 0R
R127 71.5K
C134 0.01UF 0402
C139 0.1UF
C25 10UF 0805
C135 680PF 0402
R129 5.11K
C137 150PF
C136 0.1UF
C138 6800PF
R125 365R
R126 4.700K 0.1%
R124 2.490K 0.1%
DO3316P-102
1UH L1
C43 220UF D
C24 10UF
R181 0.003R
C573 10UF
VCC2V5
2.5V @ 6A max
R130 DNP
TPS54610 PWP28
R142 71.5K
1V2_SS
C145 0.01UF 0402
C140 0.1UF
C26 10UF 0805
C144 2200PF 0402
R131 1.74K
C142 470PF
C143 0.1UF
C141 6800PF
R133 365R
R132 5.11K
R134 14.3K
DO3316P-102
1UH L3
C44 220UF D
C27 10UF
R182 0.003R
VCC1V2
1.2V @ 6A max
Sequencing Options:
1) For sequential startup :
OPEN R130, R146, R315, R139, R140
SHORT R128, R135, R309
2) For ratiometric startup :
OPEN R128, R135, R309
SHORT R130, R146, R315, R139, R140
VCC5
TPS51100 MSOP10
U33
C29 1UF 0805
C146 0.1UF
VCC2V5
VTTDDR
1.25V@3A max
C28 10UF 0805
C30 10UF 0805
C31 10UF 0805
R137 560R
4.75V to 5.25V Input
PG3V3
PG2V5
PG1V8
PG1V2
R139 DNP
R315 DNP
R140 DNP
R138 49.9R
DS18 GREEN
C45 220UF D
XILINX
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SCHEM, ML405 EVAL PLATFORM
Power Supply
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3.3V VCCO

VCC3V3

C259 0.047UF, C238 0.047UF, C239 0.047UF, C240 0.047UF, C241 0.047UF, C245 0.047UF, C246 0.047UF, C247 0.047UF, C248 0.047UF, C252 0.047UF, C267 0.047UF, C261 0.047UF

(all 0402)

VCC3V3

C260 0.22UF, C262 0.22UF, C268 0.22UF, C266 0.22UF, C249 0.22UF, C258 0.22UF

VCC3V3

C333 0.22UF, C335 0.22UF, C332 0.22UF

VCC3V3

C357 2.2UF, C351 2.2UF

VCC3V3

C376 330UF D

VCC3V3

J61 SMP_MINI

J60 SMP_MINI

3.3V Supply Analysis

2.5V VCCO and VCCAUX

VCC2V5

C220 0.047UF, C219 0.047UF, C218 0.047UF, C217 0.047UF, C224 0.047UF, C225 0.047UF, C226 0.047UF, C227 0.047UF, C263 0.047UF, C210 0.047UF, C211 0.047UF, C212 0.047UF, C213 0.047UF, C214 0.047UF, C215 0.047UF, C216 0.047UF

(all 0402)

VCC2V5

C413 0.047UF, C412 0.047UF

VCC2V5

C223 0.22UF, C222 0.22UF, C221 0.22UF, C228 0.22UF, C229 0.22UF, C230 0.22UF, C206 0.22UF, C207 0.22UF, C208 0.22UF

VCC2V5

C334 0.22UF, C338 0.22UF, C339 0.22UF, C348 0.22UF

VCC2V5

C355 2.2UF, C356 2.2UF, C352 2.2UF

VCC2V5

C373 330UF D, C370 330UF D

VCC2V5

J59 SMP_MINI

J58 SMP_MINI

2.5V Supply Analysis

1.2V VCCINT

VCC1V2

C178 0.047UF, C179 0.047UF, C180 0.047UF, C181 0.047UF, C182 0.047UF, C183 0.047UF, C184 0.047UF, C185 0.047UF, C410 0.047UF

(all 0402)

C186 0.047UF, C187 0.047UF, C188 0.047UF, C189 0.047UF, C190 0.047UF, C191 0.047UF, C192 0.047UF, C193 0.047UF, C411 0.047UF

(all 0402)

C194 0.22UF, C195 0.22UF, C196 0.22UF, C197 0.22UF, C198 0.22UF

C199 0.22UF, C200 0.22UF, C201 0.22UF

C343 0.22UF, C344 0.22UF, C345 0.22UF, C346 0.22UF

C361 2.2UF, C362 2.2UF, C417 2.2UF

C371 330UF D

VCC1V2

J63 SMP_MINI

J62 SMP_MINI

1.2V Supply Analysis

Place these near Bank 7 VCCO

VCCO_7

C231 0.047UF, C232 0.047UF, C233 0.047UF, C234 0.047UF, C236 0.22UF, C237 0.22UF, C337 0.22UF, C358 2.2UF, C409 330UF D

(all 0402 except C236, C237, C337, C358, C409)

XILINX

Title: SCHEM, ML405 EVAL PLATFORM
FPGA Decoupling

0381199

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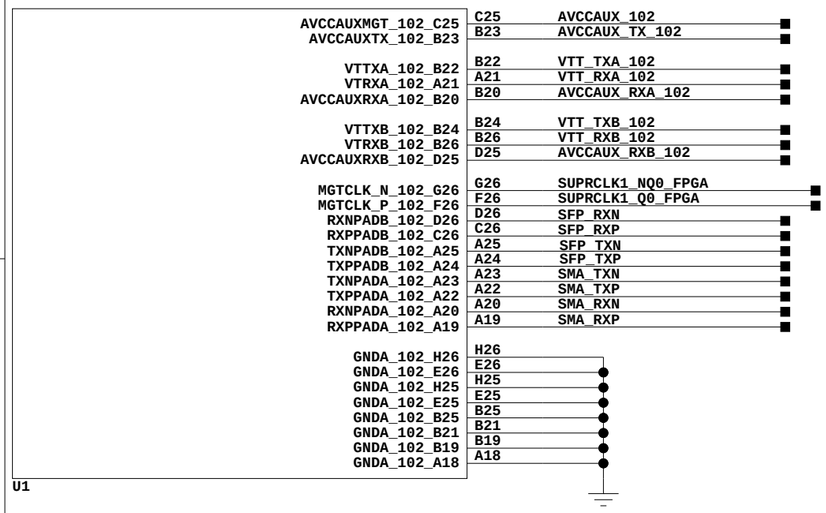

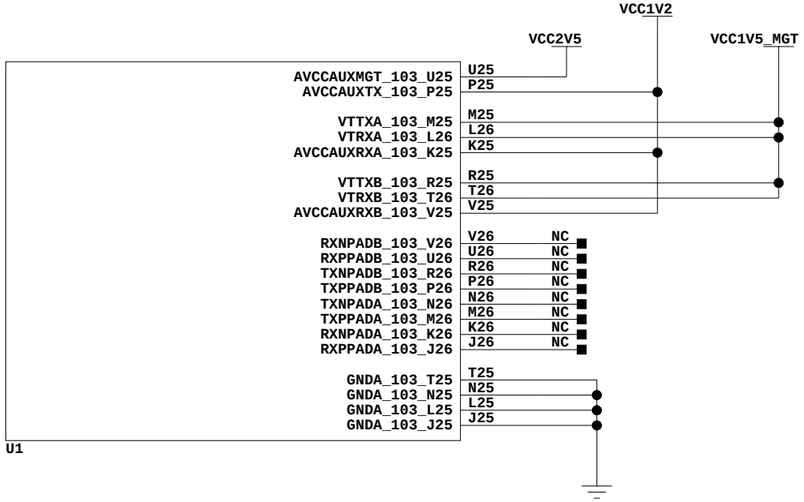

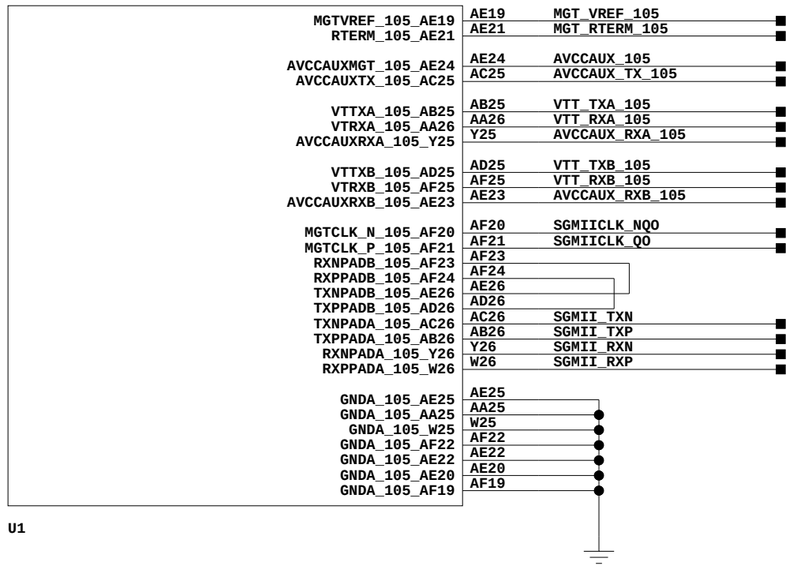

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
MGT Banks

0381199

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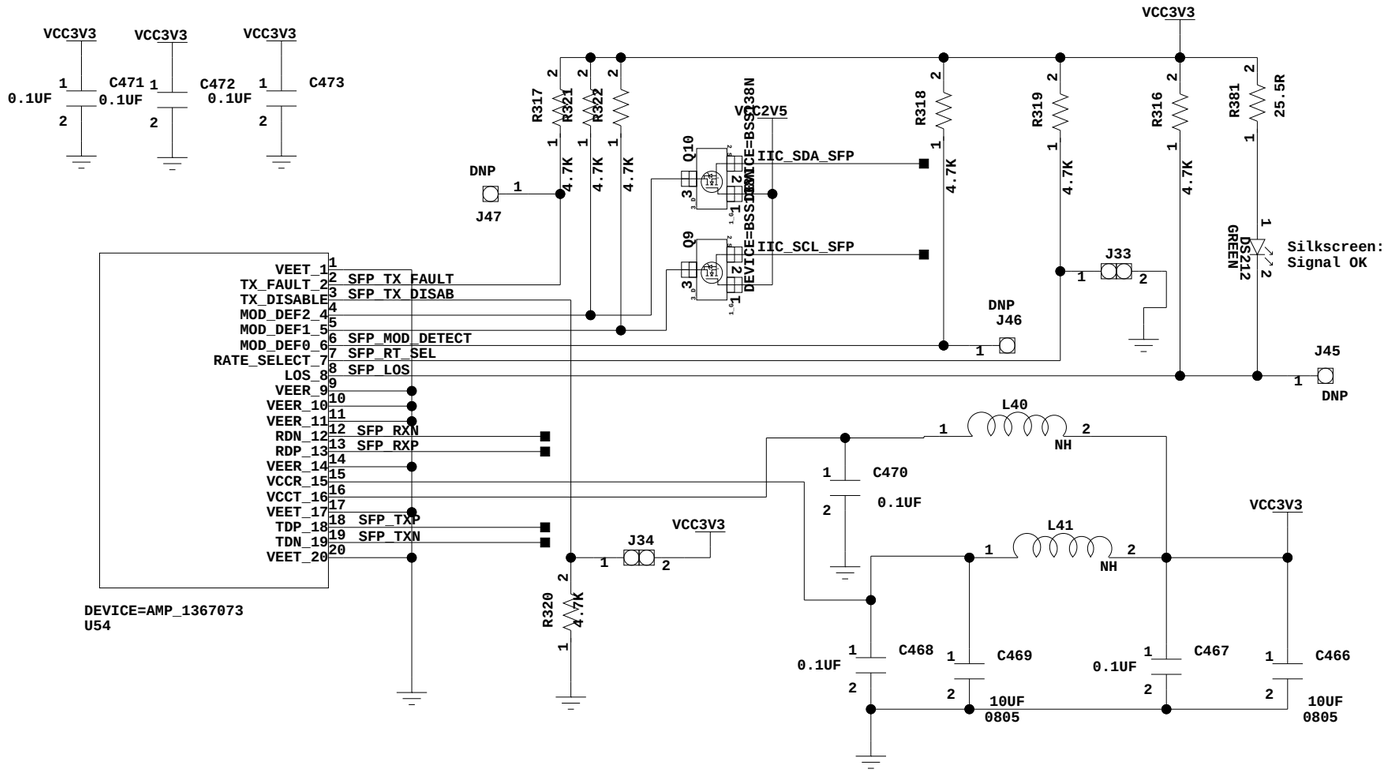
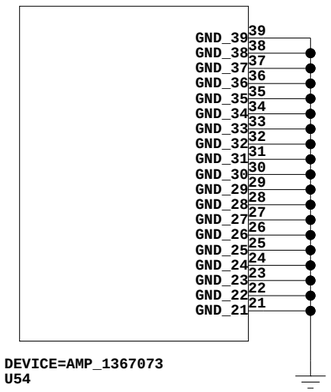
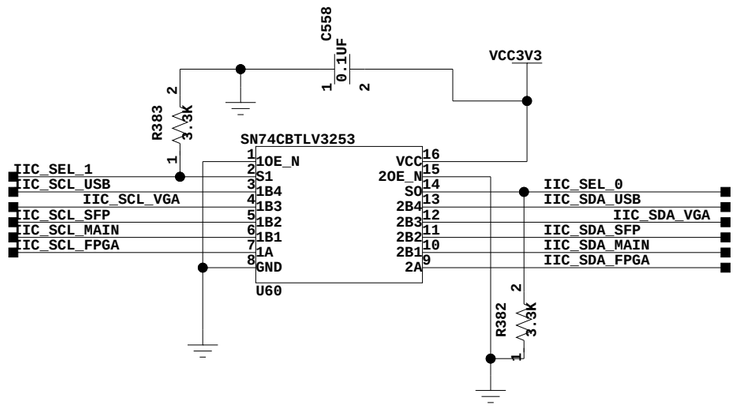
SFP MODULE
MGT_102B

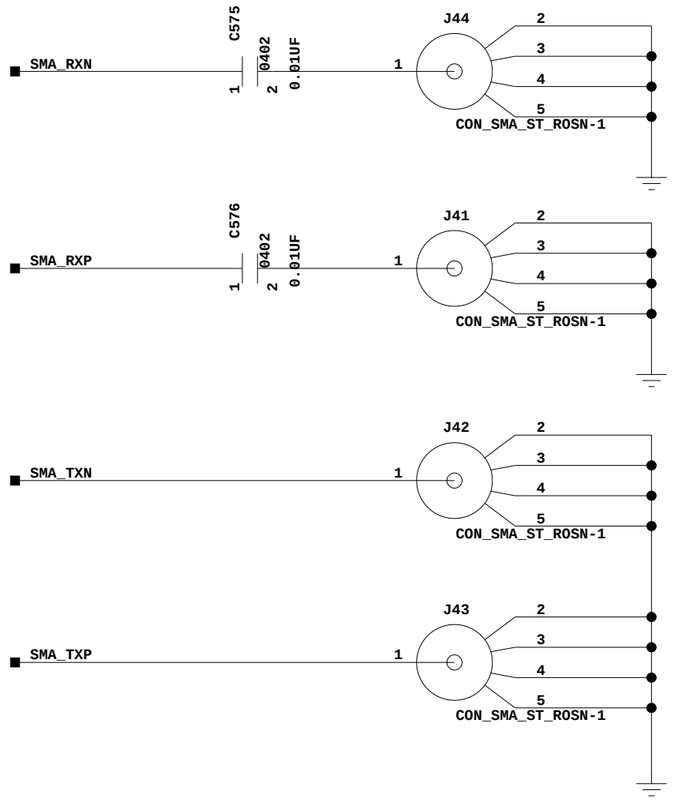




IIC MUX



SMA Connectors
MGT_102A



Title: SCHEM, ML405 EVAL PLATFORM SFP Module, SMA Connectors IIC MUX			0381199
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SATA Host 1

MGT 113B

SATA Host 2

MGT 113A

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
SATA Connectors

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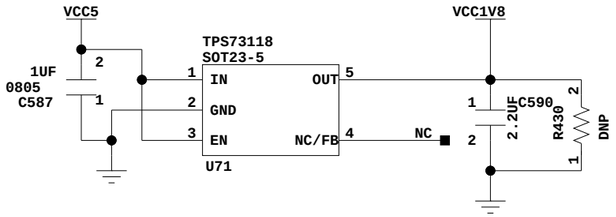
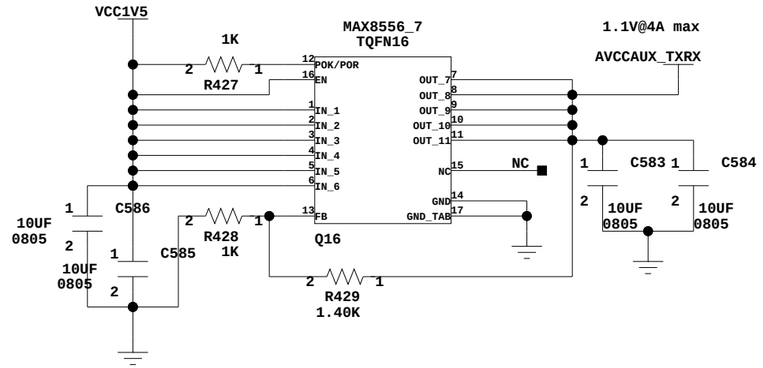
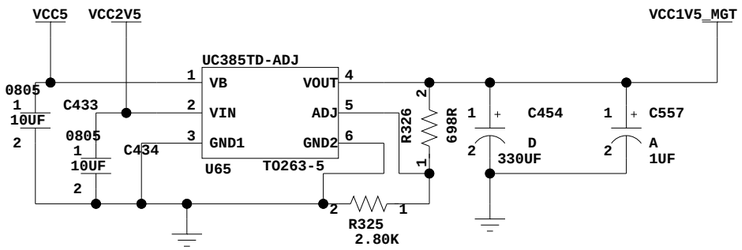
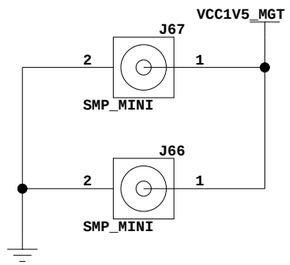
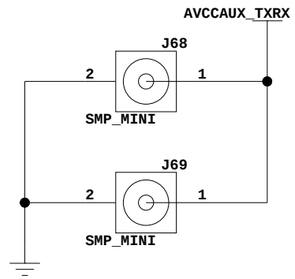




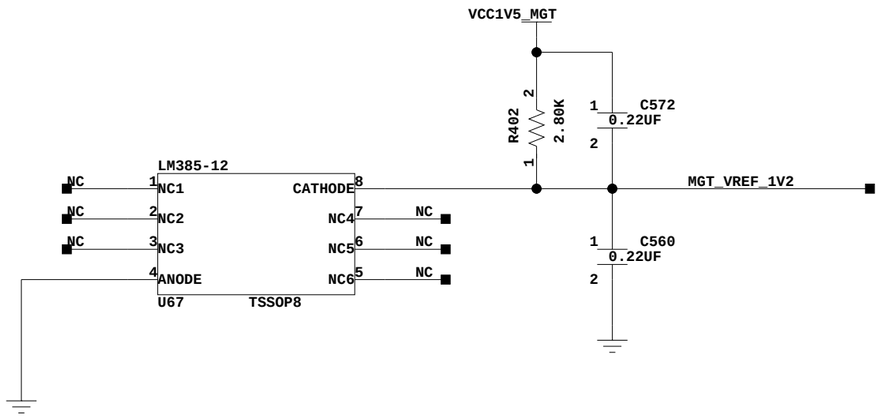




1.5V MGT Supply Analysis



1.0V or 1.2V MGT Supply Analysis



XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
MGT Linear Power Supplies
0381199

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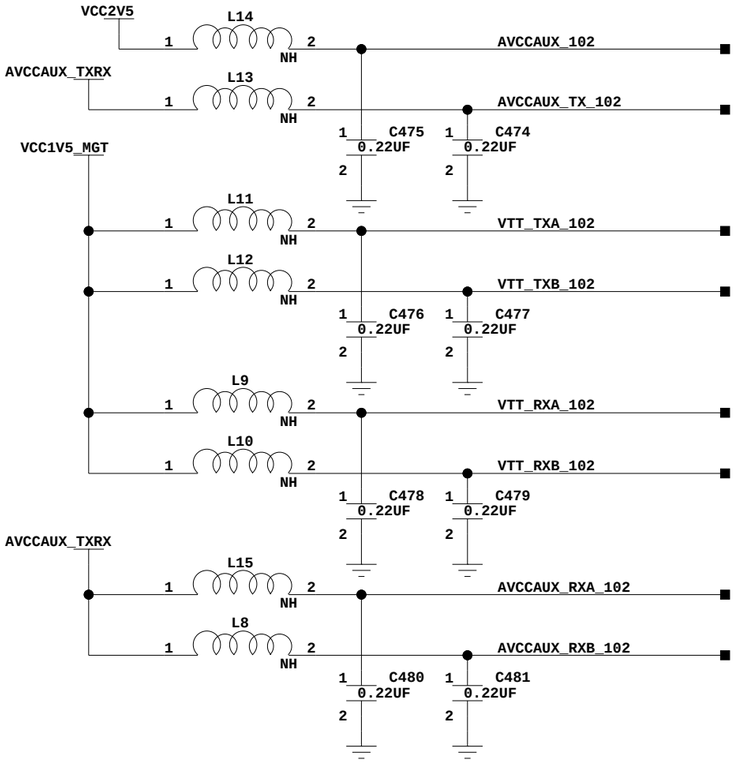

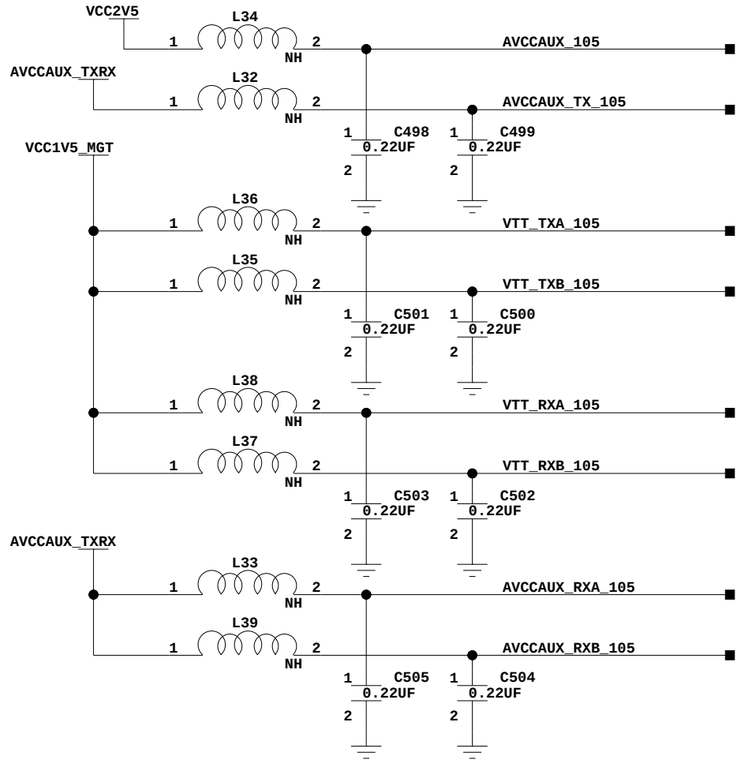

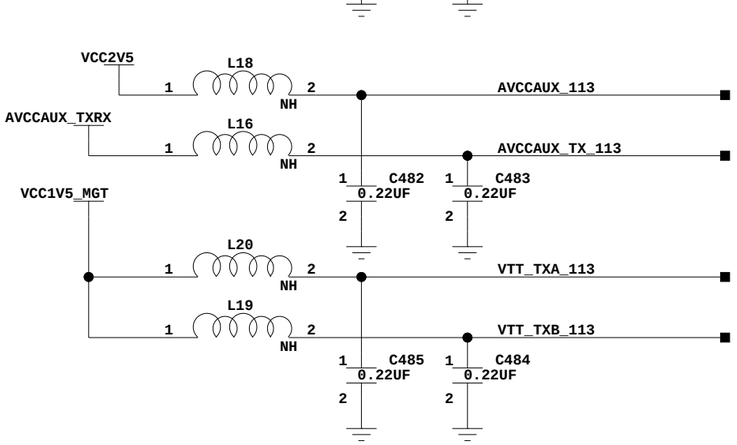

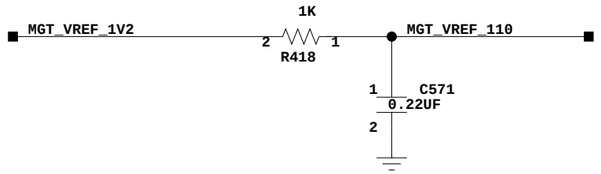

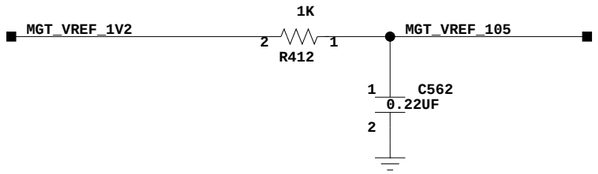

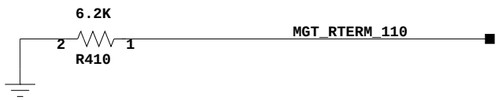

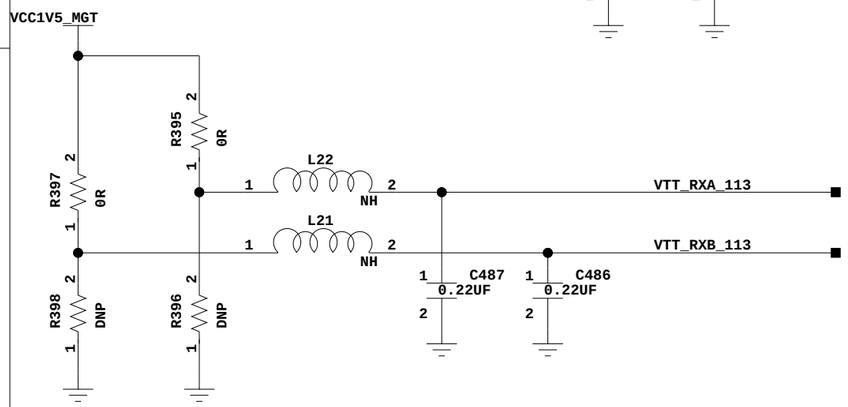

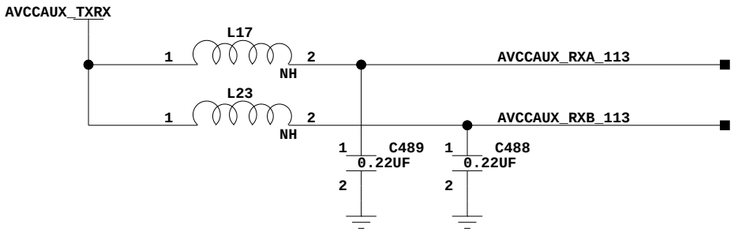

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
MGT Power Decoupling
0381199

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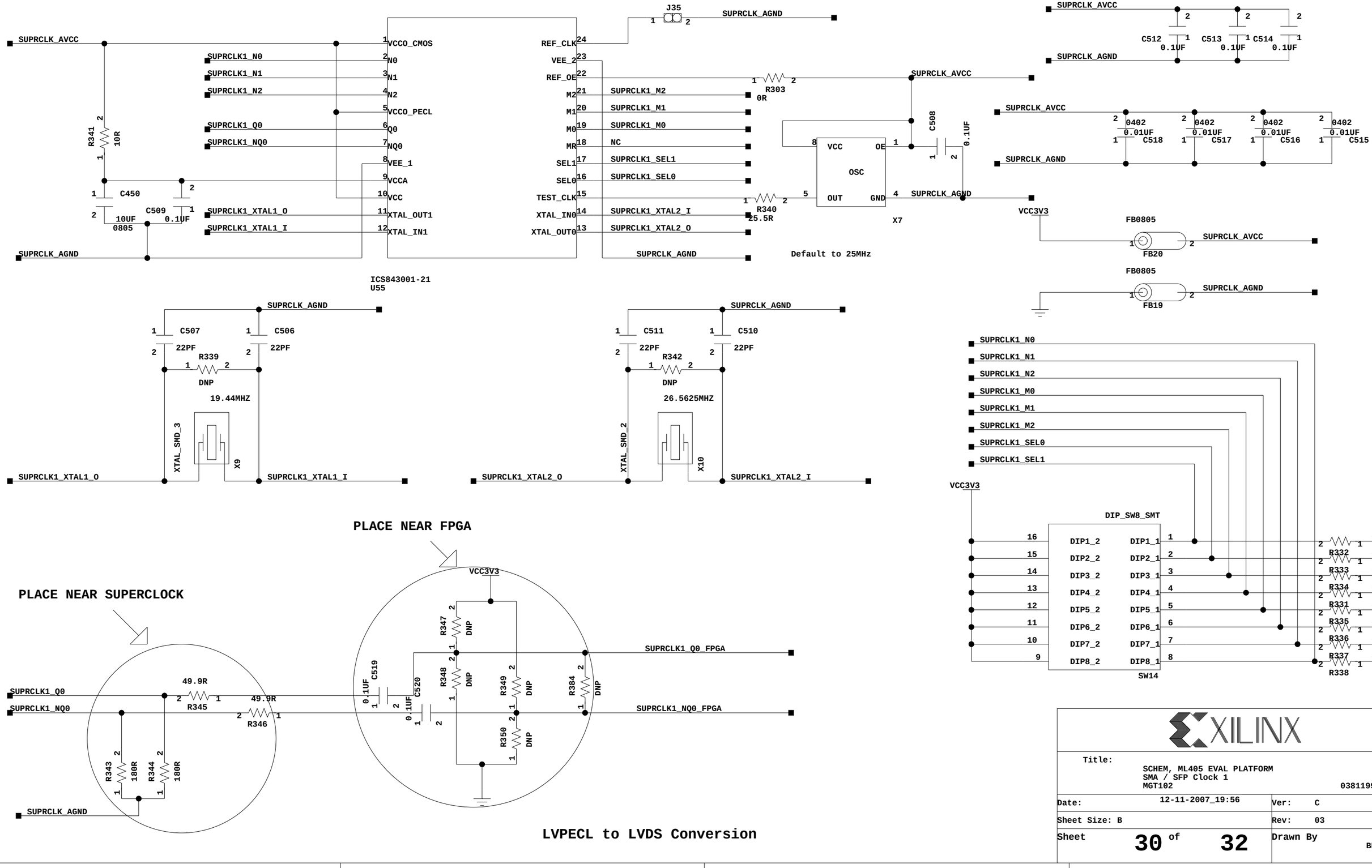

Title:	SCHEM, ML405 EVAL PLATFORM SMA / SFP Clock 1 MGT102 0381199
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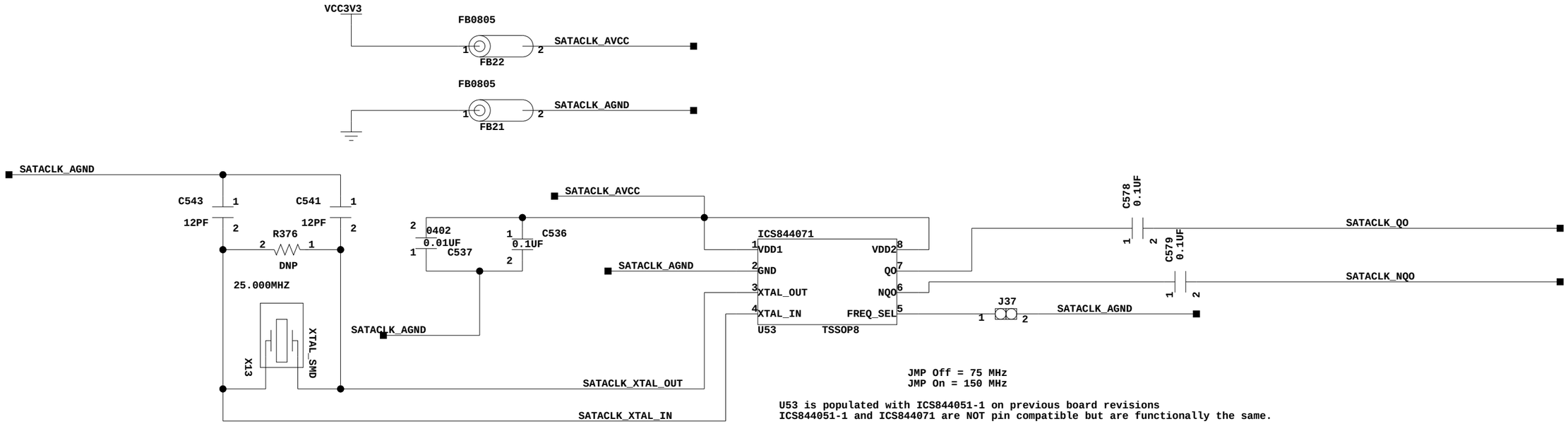

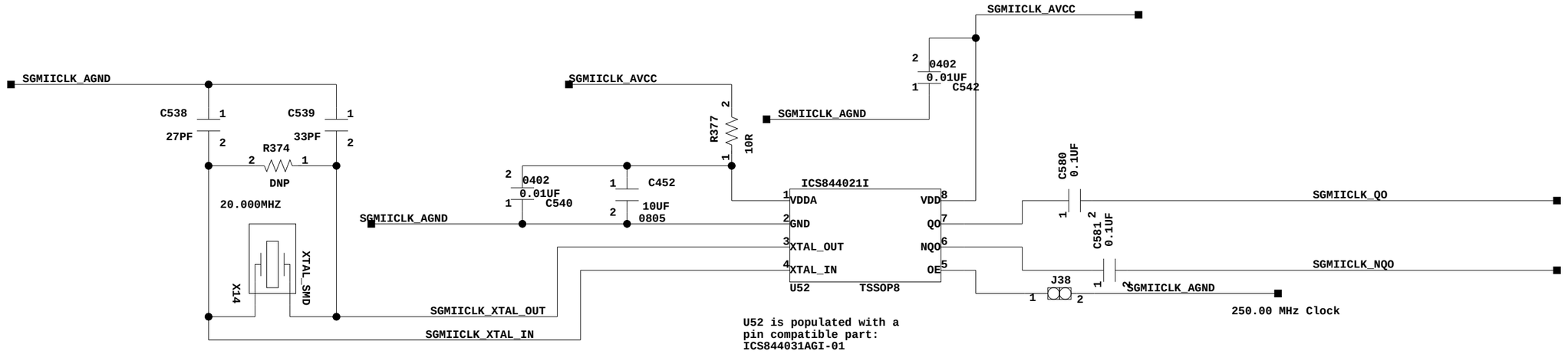

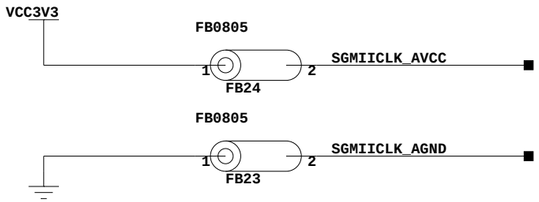

XILINX

Title:
SCHEM, ML405 EVAL PLATFORM
SGMII / SATA Clocks
MGT 110 / MGT 113
0381199

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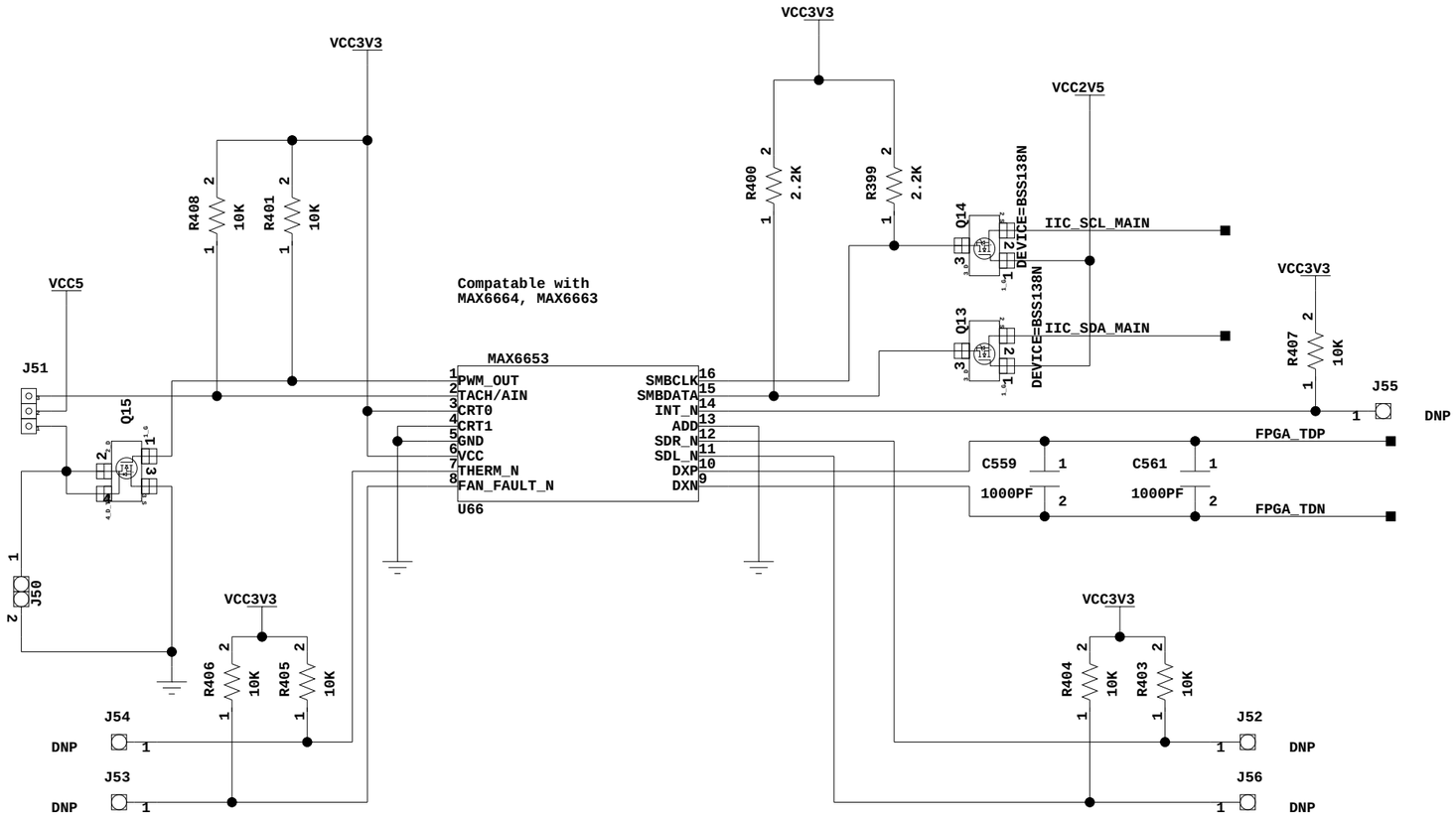

Title: SCHEM, ML405 EVAL PLATFORM FPGA Fan Controller and IIC temp sensor			0381199
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