NOTE: PLEASE REVIEW THE ML410 BOM FOR ITEMS DESIGNATED AS "NOSTUFF".

NOSTUFF ITEMS ARE NOT POPULATED ON THE PCB.

THE ML410 BOM CONTAINS THE MOST ACCURATE INFORMATION ABOUT

NOSTUFF DISCRETES AND COMPONENTS.

XILINX PART NUMBERS

SCHEMATICS	0381203
PCB ARTWORK	0531499
PCB FABRICATION	1280372

XILINX

SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

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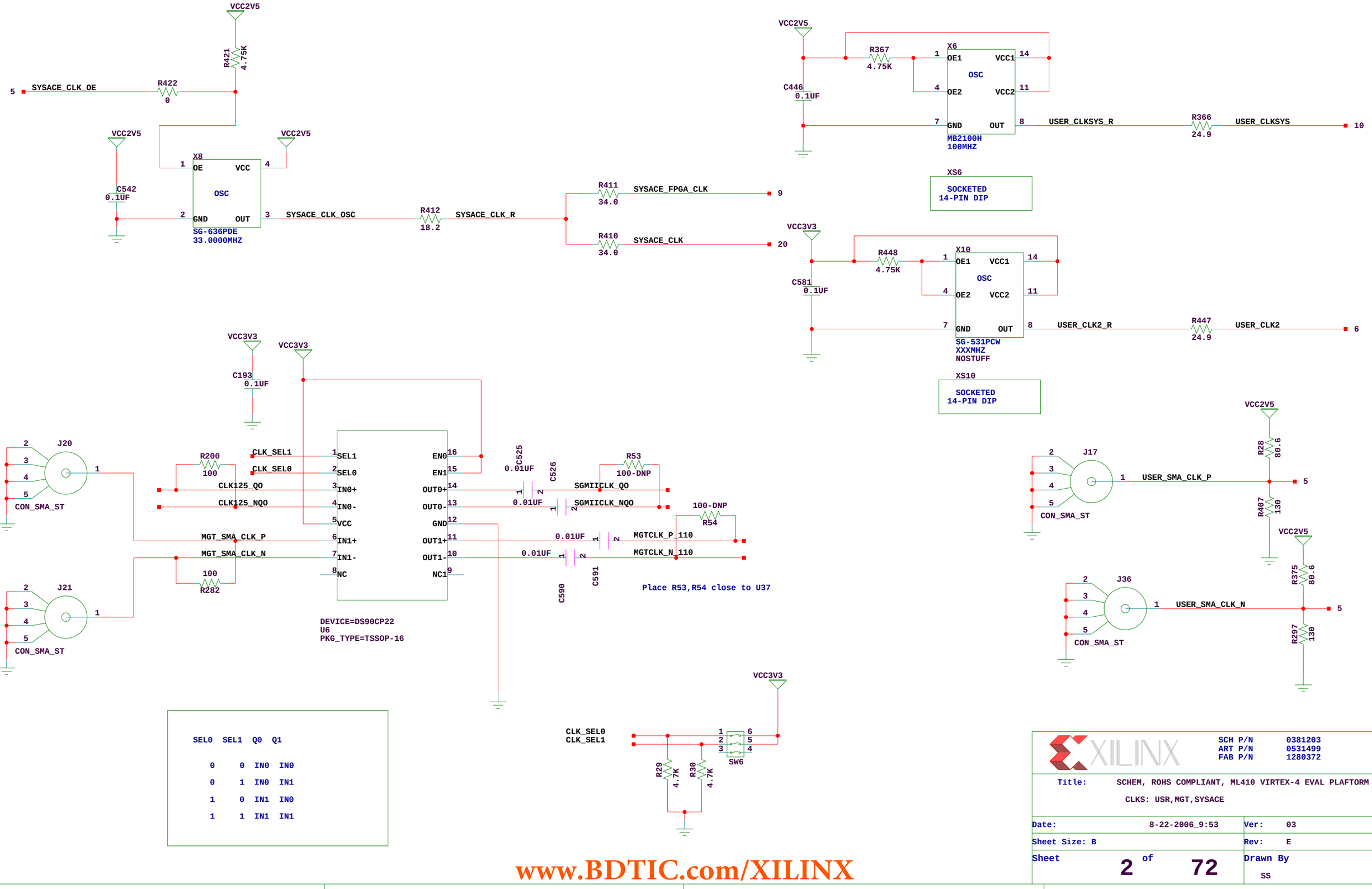
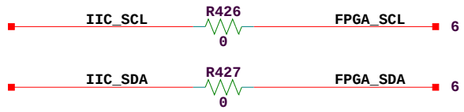
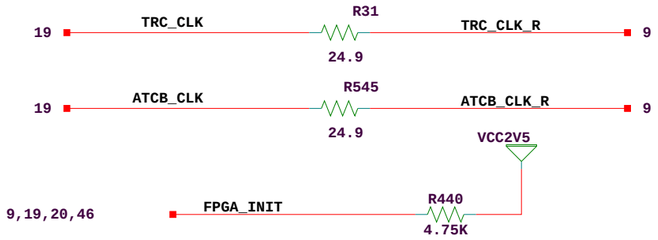
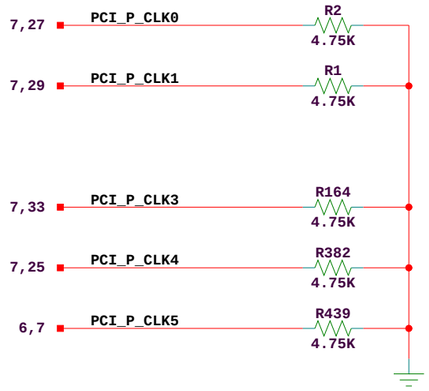


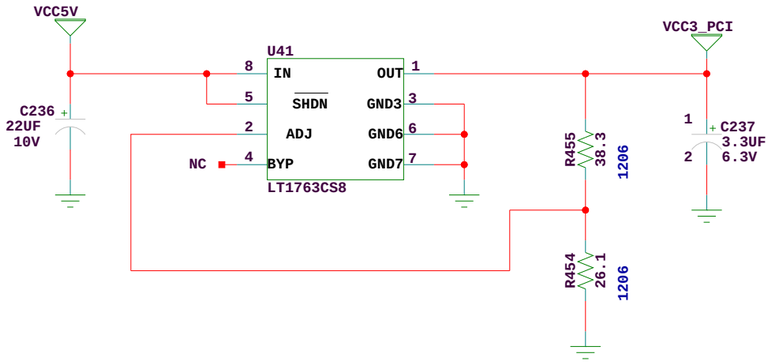


NOTE: TRC_CLK RESISTOR ALLOWS CLOCK TERMINATION
TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.



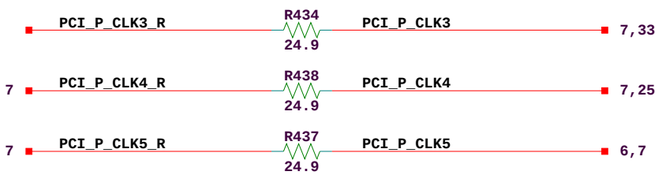


NOTE: THE PCI SPEC RECOMMENDS THAT
CLOCKS BE PULLED LOW WHEN THE
BUS IS NOT ACTIVELY CLOCKED.



NOTE: THE COMPONENT VALUES FOR THIS REGULATOR ARE TAKEN
FROM XAPP653. THIS DESIGN IS INTENDED TO SINK CURRENT
THROUGH THE 1206 RESISTORS WHEN THE CLAMP DIODES ON
THE FPGA ARE CONDUCTING DURING OVERSHOOT. THIS IS WHY
THE VALUES ARE UNUSUAL RELATIVE TO THE LT1763 DATASHEET.

NOTE: PCI_CLK RESISTORS ALLOW CLOCK TERMINATION
TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.



XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
PCI_SUPPLY ....

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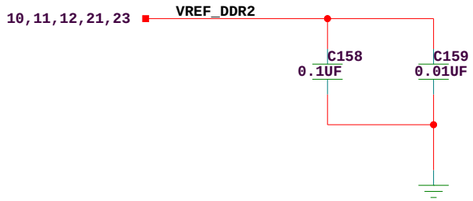
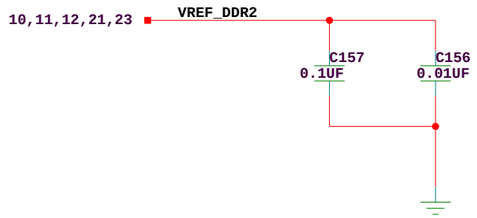
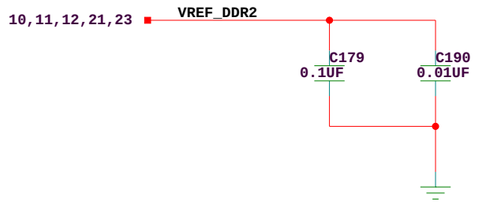
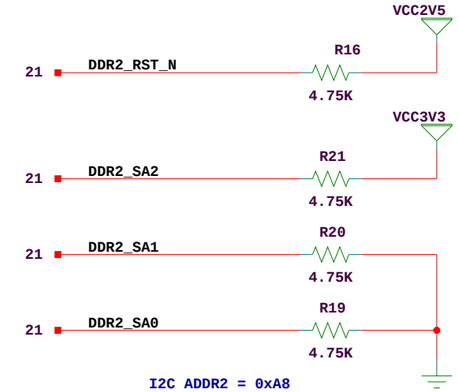
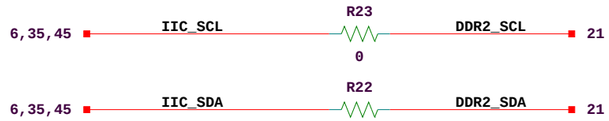


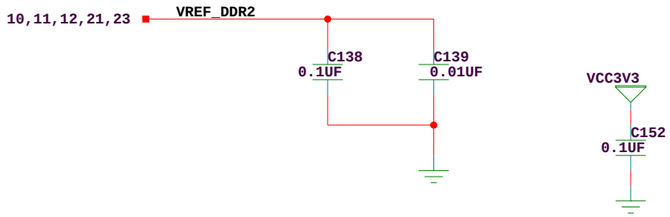


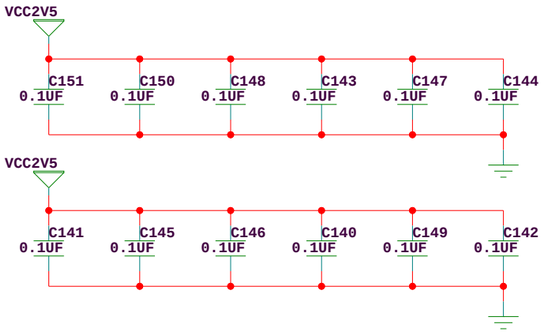




I2C ADDR2 = 0xA8







NOTE: THE PINOUT OF THE DDR2 DQ AND DQS
SIGNALS IS INTENDED TO ALLOW THE
USE OF LOCAL CLOCKING RESOURCES
AS DESCRIBED IN XAPP609.

XILINX

SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
DDR2 DECOUPLING

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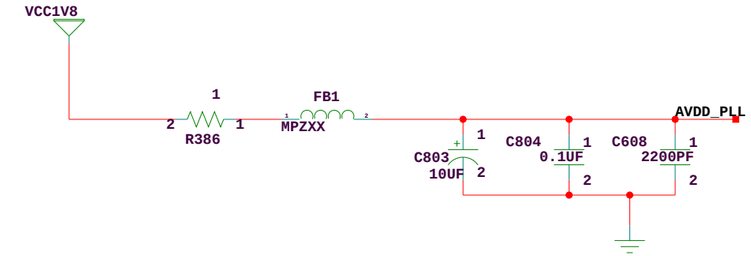
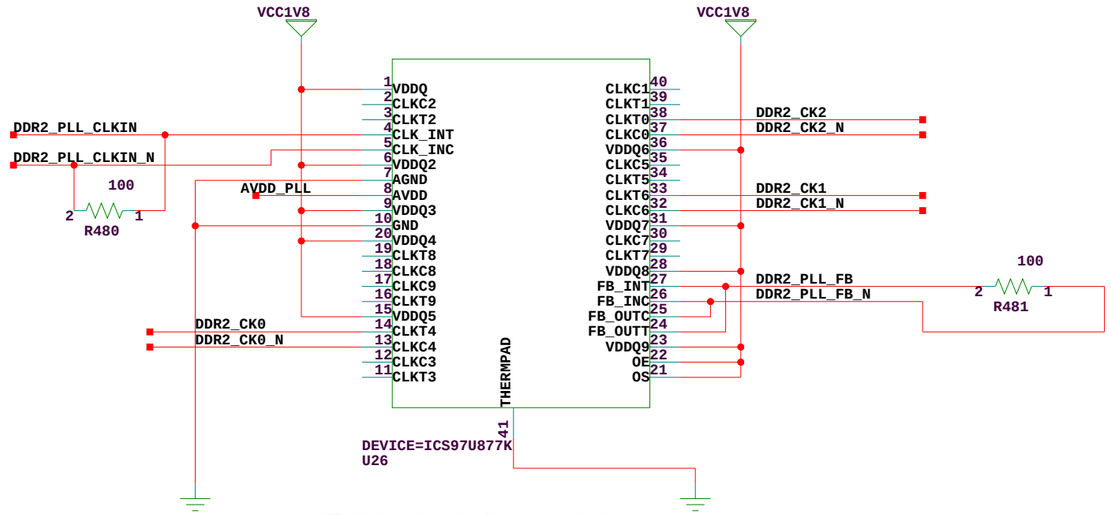
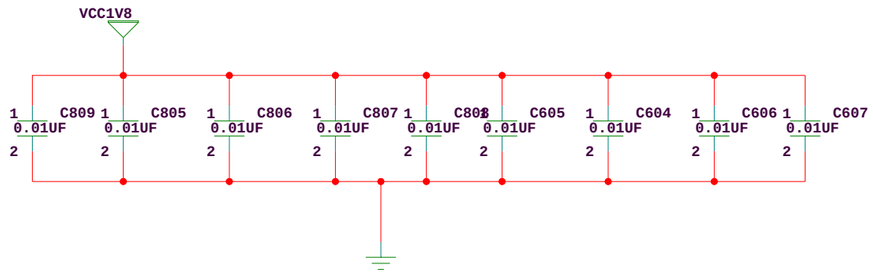
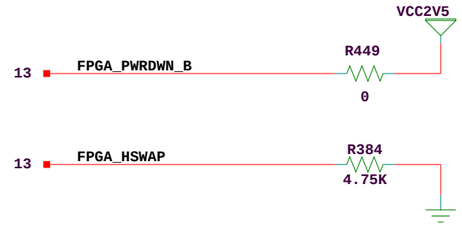


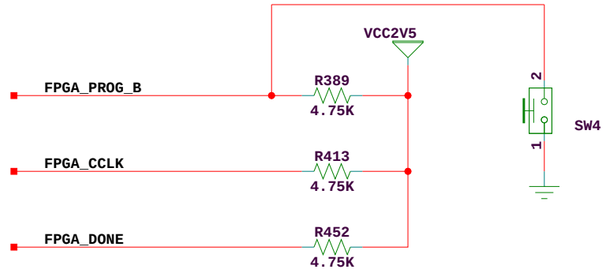


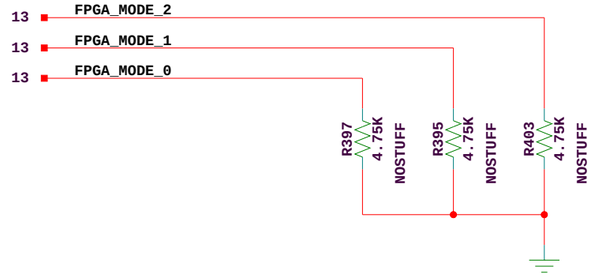
All DDR2_CK* to be length matched

DDR2_PLL_FB* to be length matched to DDR2_CK*









NOTE: MODE BITS HAVE INTERNAL PULLUPS AND DEFAULT
TO SLAVE-SERIAL MODE. THERE MAY BE SOME
CONFLCITS BETWEEN THE JTAG MODES AND ICAP
HOWEVER SLAVE-SERIAL MODE IS KNOWN TO WORK.

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
FPGA CONFIG AND MISC I/O

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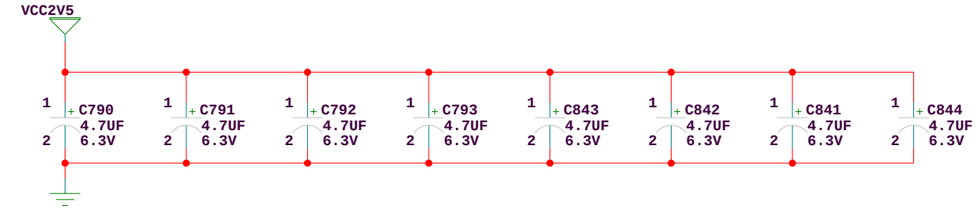

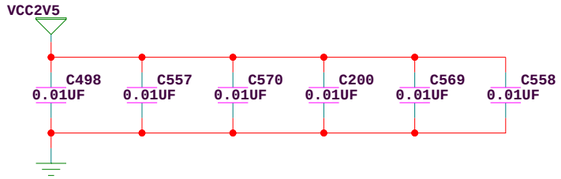

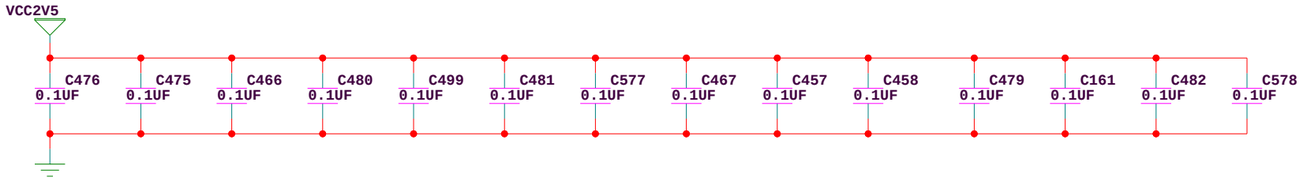

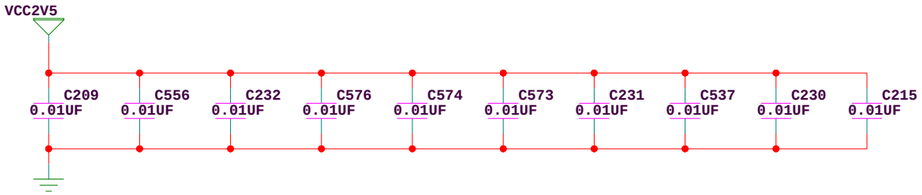

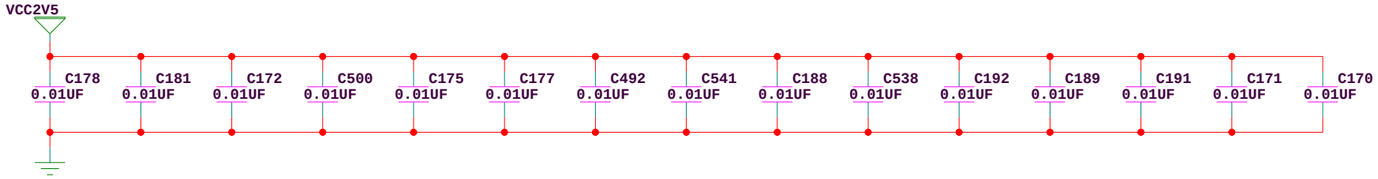

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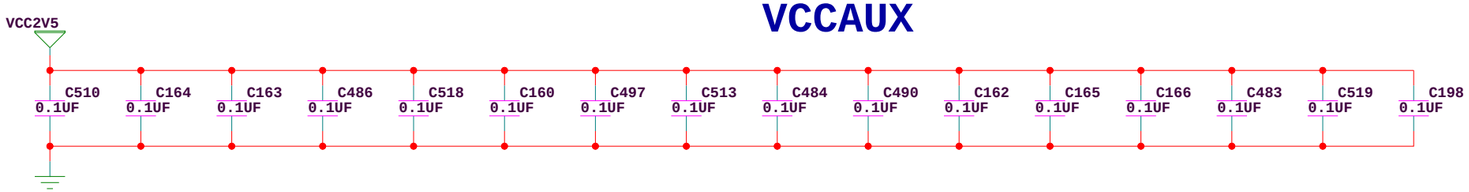
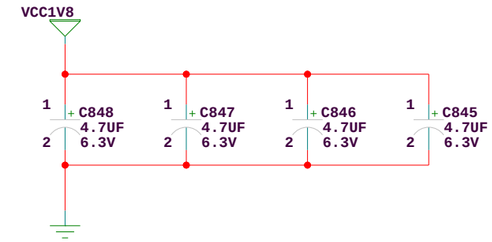
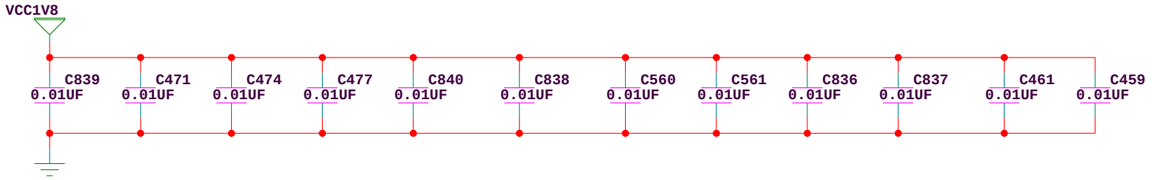
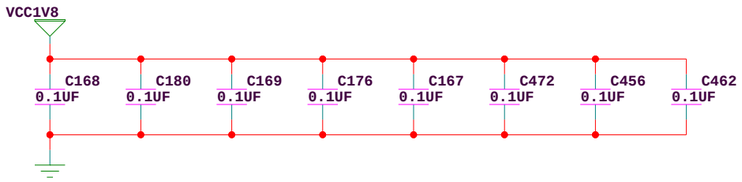


BANK 1,2,3,4,5,7,8,9,11







XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA DECOUPLING

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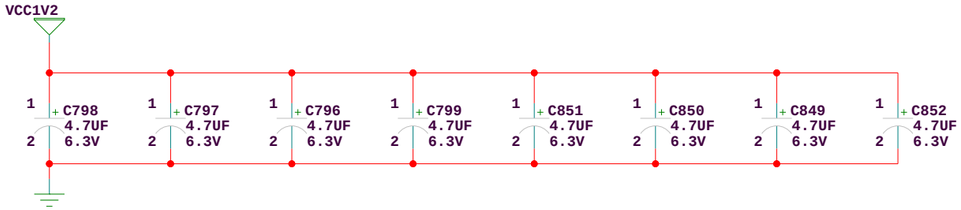
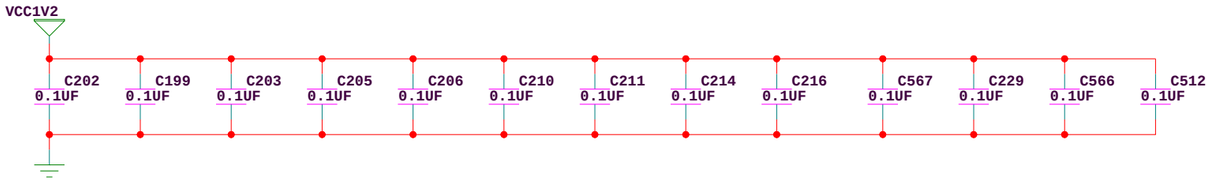
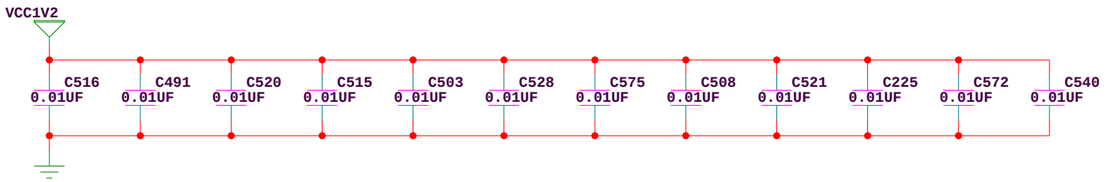
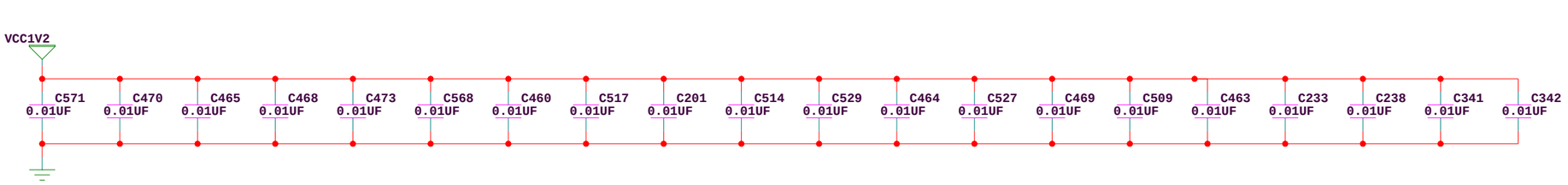
VCORE

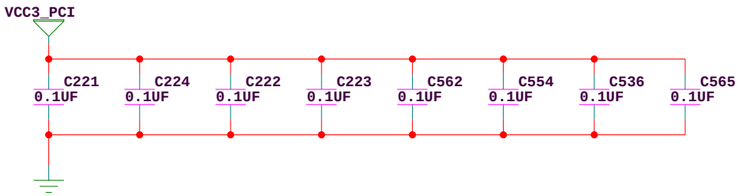


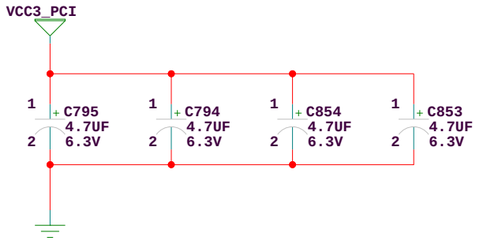


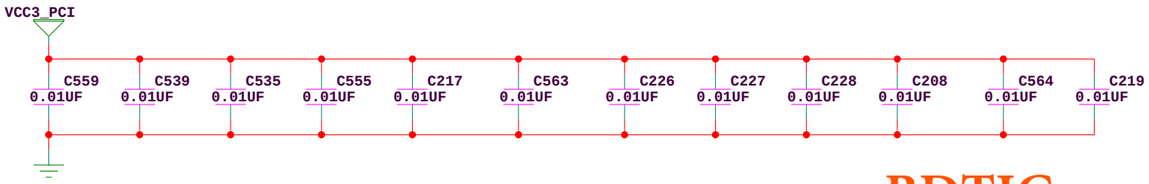




BANK 6,10,12







XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
FPGA DECOUPLING

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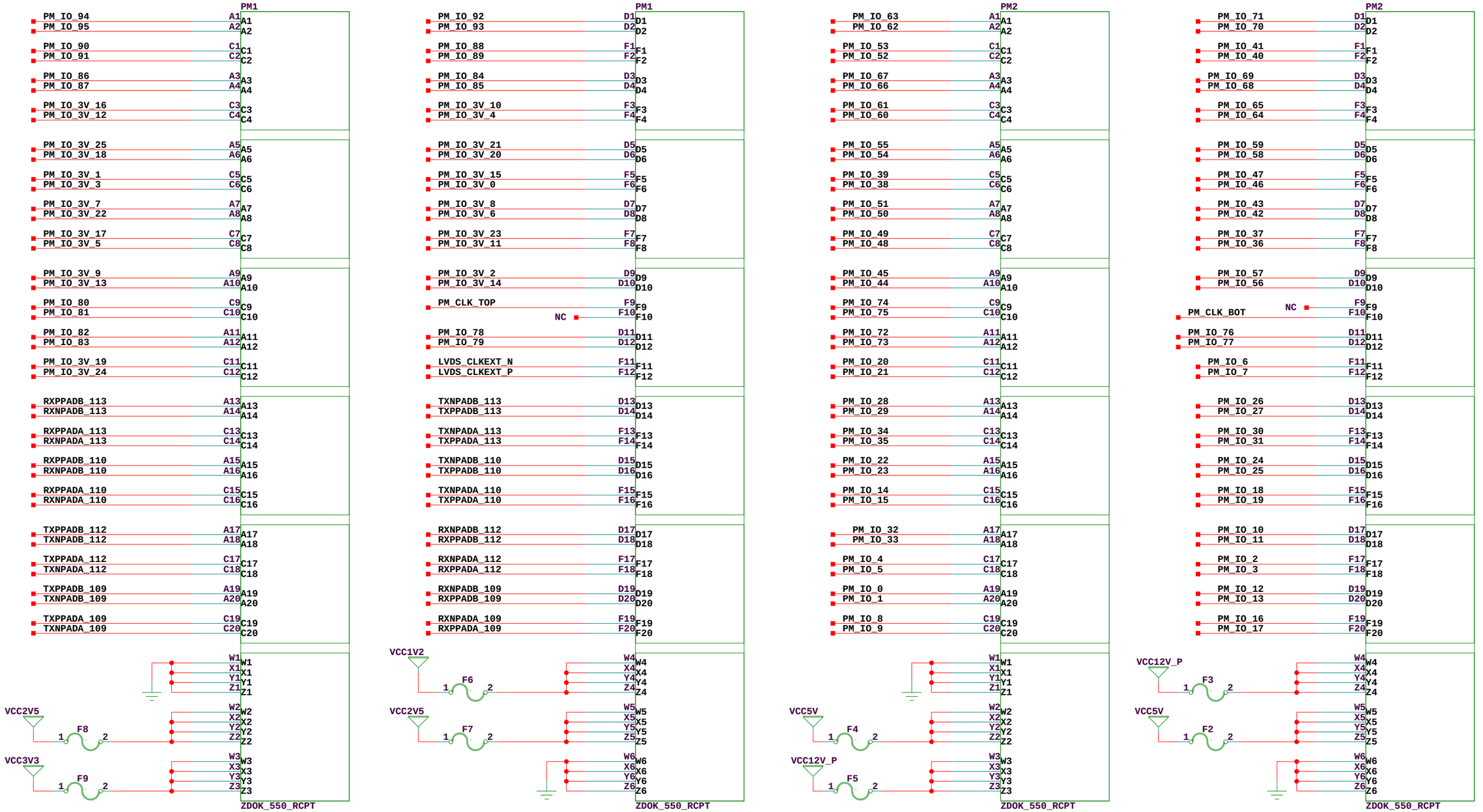

GND;B1,B2,B3,B4,B5
GND;B6,B7,B8,B9,B10
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GND;E11,E12,E13,E14,E15
GND;E16,E17,E18,E19,E20

GND;B1,B2,B3,B4,B5
GND;B6,B7,B8,B9,B10
GND;B11,B12,B13,B14,B15
GND;B16,B17,B18,B19,B20
GND;E1,E2,E3,E4,E5
GND;E6,E7,E8,E9,E10
GND;E11,E12,E13,E14,E15
GND;E16,E17,E18,E19,E20

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PERSONALITY MODULE CONNECTORS

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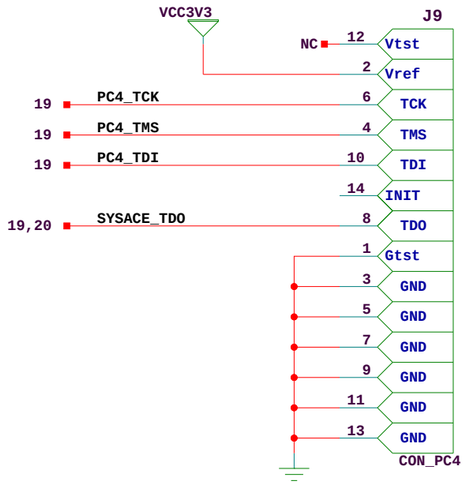
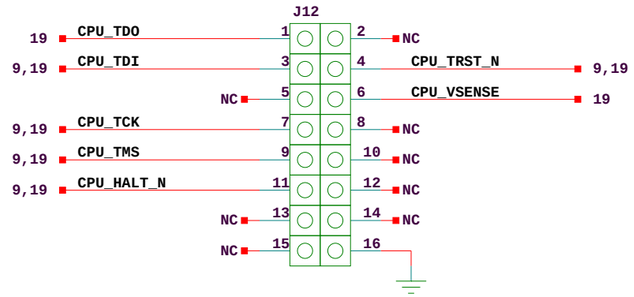
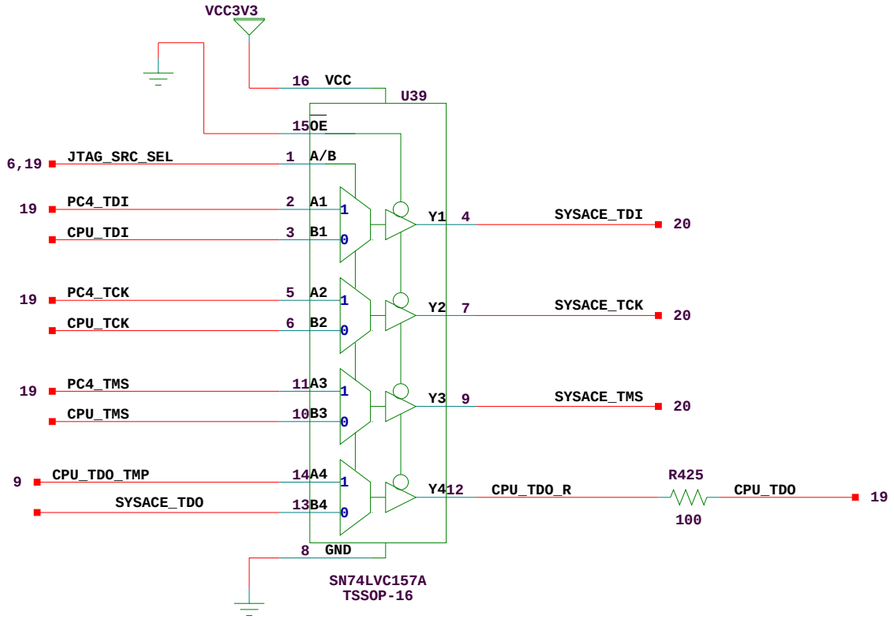
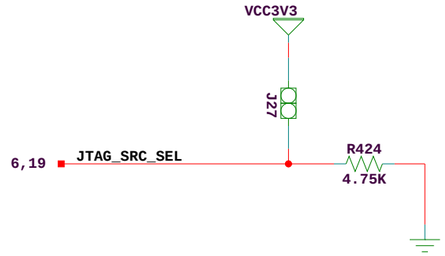
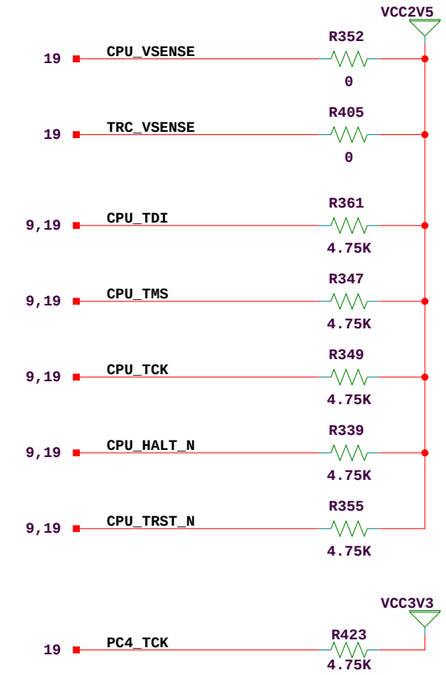
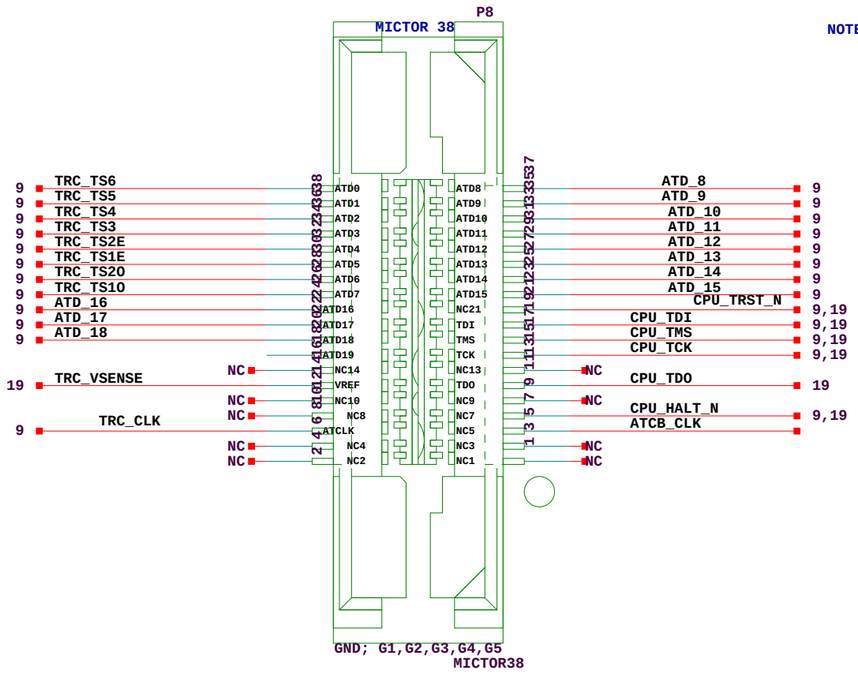




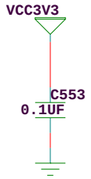








NOTE: THIS MUX INTRODUCES AN IMPLICIT 2.5V TO
3.3V LEVEL-SHIFT FOR THE CPU JTAG SIGNALS.
THE SERIES RESISTOR ON CPU_TDO IS INTENDED
TO PROVIDE PROTECTION FOR A 2.5V JTAG PROBE.



XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
JTAG, DEBUG, TRACE CONNECTORS

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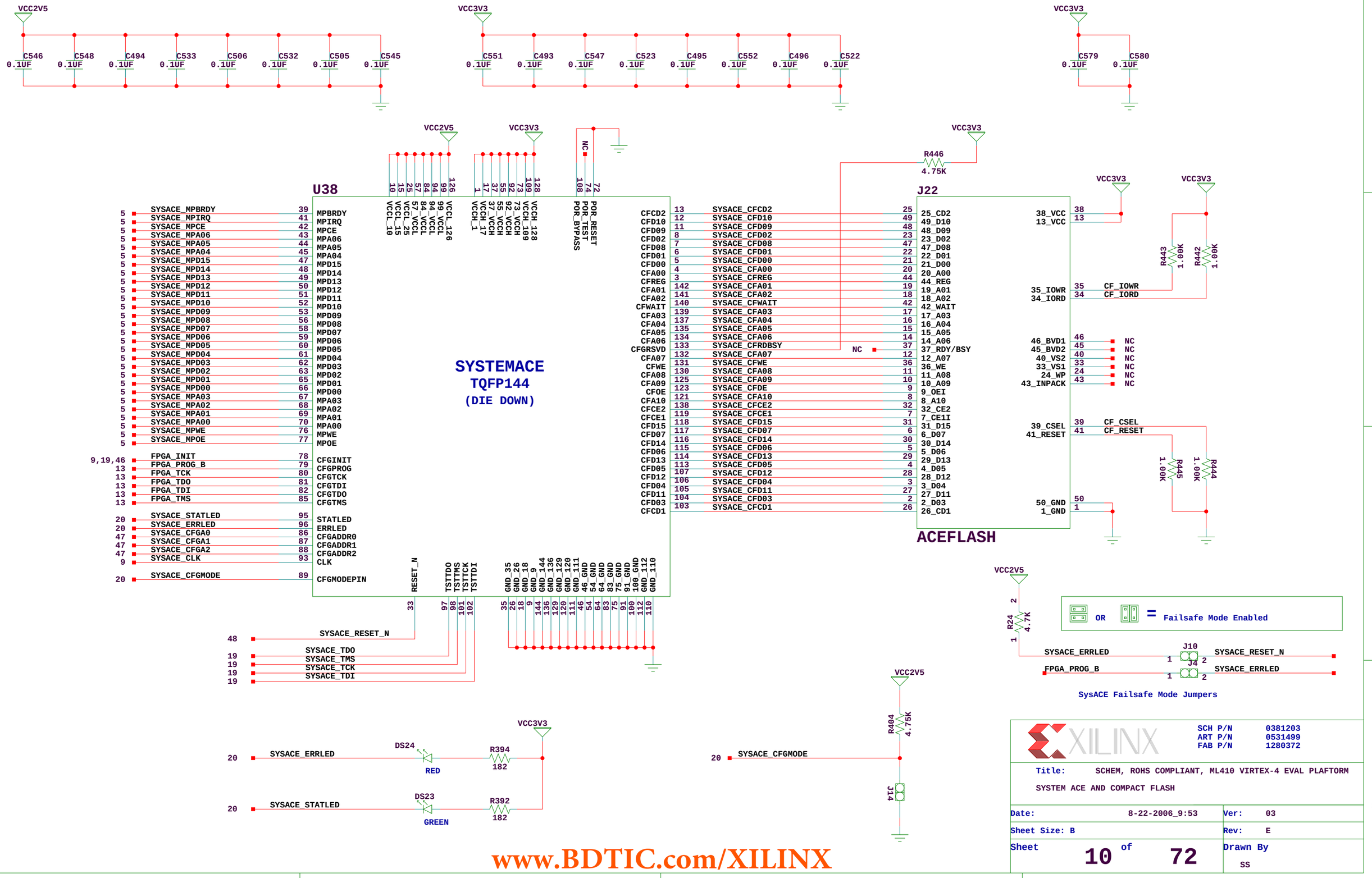

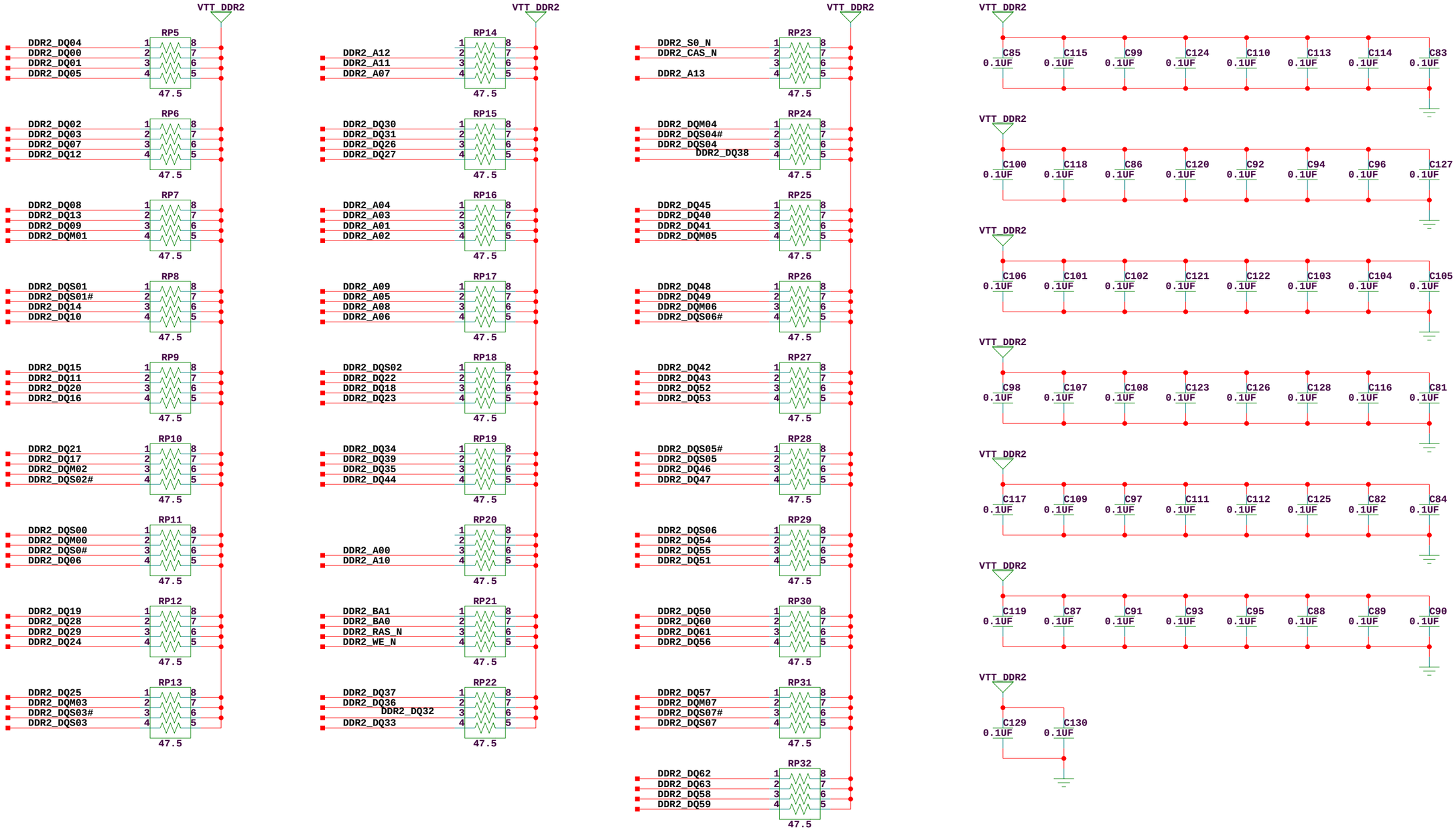

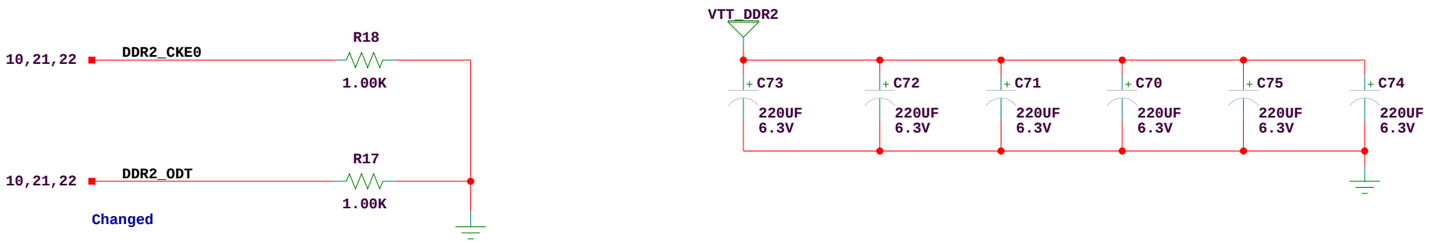

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

DDR2 SSTL-2 TERMINATION

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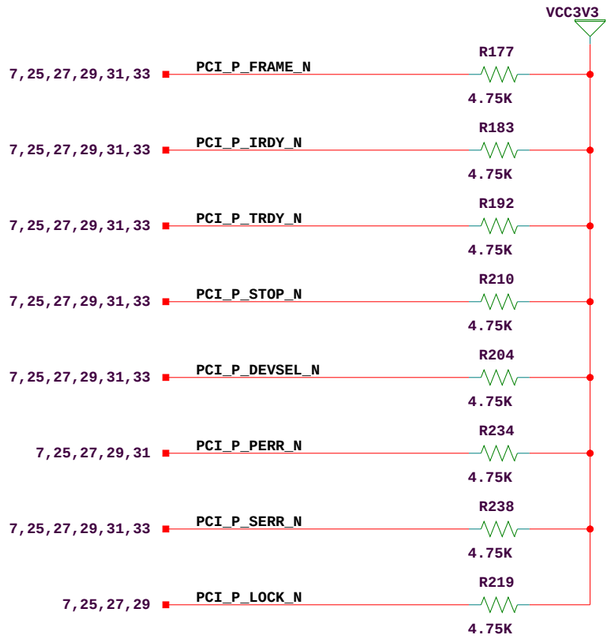

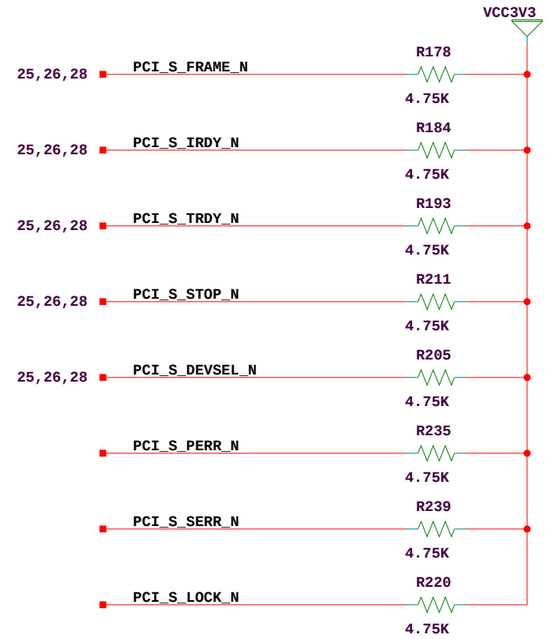

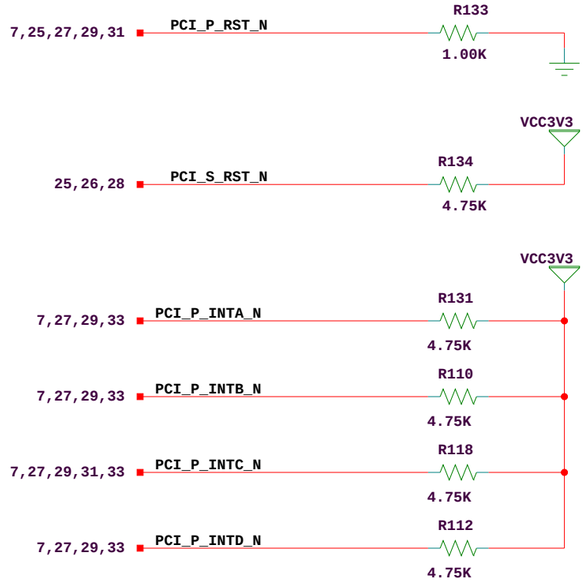

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI BUS PULLUPS

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PCI-PCI BRIDGE
PCI2250_PGF

U32

PRIMARY

7,27,29,31,33	PCI_P_AD00	147	P_AD0
7,27,29,31,33	PCI_P_AD01	146	P_AD1
7,27,29,31,33	PCI_P_AD02	144	P_AD2
7,27,29,31,33	PCI_P_AD03	143	P_AD3
7,27,29,31,33	PCI_P_AD04	141	P_AD4
7,27,29,31,33	PCI_P_AD05	140	P_AD5
7,27,29,31,33	PCI_P_AD06	138	P_AD6
7,27,29,31,33	PCI_P_AD07	137	P_AD7
7,27,29,31,33	PCI_P_AD08	128	P_AD8
7,27,29,31,33	PCI_P_AD09	127	P_AD9
7,27,29,31,33	PCI_P_AD10	125	P_AD10
7,27,29,31,33	PCI_P_AD11	124	P_AD11
7,27,29,31,33	PCI_P_AD12	123	P_AD12
7,27,29,31,33	PCI_P_AD13	121	P_AD13
7,27,29,31,33	PCI_P_AD14	120	P_AD14
7,27,29,31,33	PCI_P_AD15	119	P_AD15
7,27,29,31,33	PCI_P_AD16	103	P_AD16
7,27,29,31,33	PCI_P_AD17	102	P_AD17
7,27,29,31,33	PCI_P_AD18	101	P_AD18
7,27,29,31,33	PCI_P_AD19	99	P_AD19
7,27,29,31,33	PCI_P_AD20	98	P_AD20
7,27,29,31,33	PCI_P_AD21	97	P_AD21
	PCI_P_AD22	95	P_AD22
	PCI_P_AD23	94	P_AD23
	PCI_P_AD24	86	P_AD24
	PCI_P_AD25	84	P_AD25
	PCI_P_AD26	83	P_AD26
	PCI_P_AD27	82	P_AD27
	PCI_P_AD28	80	P_AD28
	PCI_P_AD29	79	P_AD29
	PCI_P_AD30	78	P_AD30
	PCI_P_AD31	76	P_AD31
	PCI_P_CBE0_N	135	P_C/BE0_N
	PCI_P_CBE1_N	117	P_C/BE1_N
	PCI_P_CBE2_N	105	P_C/BE2_N
	PCI_P_CBE3_N	91	P_C/BE3_N
7,24	PCI_P_GNT4_N	74	P_GNT_N
7,24	PCI_P_REQ4_N	75	P_REQ_N
7	PCI_P_CLK4	72	P_CLK
	PCI_P_DEVSEL_N	110	P_DEVSEL_N
	PCI_P_FRAME_N	106	P_FRAME_N
	PCI_P_IRDY_N	107	P_IRDY_N
	PCI_P_LOCK_N	112	P_MFUNC
	PCI_P_PAR	116	P_PAR
	PCI_P_PERR_N	114	P_PERR_N
	PCI_P_RST_N	70	P_RST_N
	PCI_P_SERR_N	115	P_SERR_N
	PCI_P_STOP_N	111	P_STOP_N
	PCI_P_TRDY_N	109	P_TRDY_N
25	PCI_P_IDSEL	93	P_IDSEL
	PCIBR_GOZ_N	69	GOZ_N
NC		68	NO/HSLED
25	PCIBR_MS0	132	MS0
25	PCIBR_MS1	174	MS1/BPCC
	VCC3V3	73	P_VCCP

SECONDARY

S_AD0	148	PCI_S_AD00	26,28
S_AD1	150	PCI_S_AD01	26,28
S_AD2	151	PCI_S_AD02	26,28
S_AD3	152	PCI_S_AD03	26,28
S_AD4	154	PCI_S_AD04	26,28
S_AD5	155	PCI_S_AD05	26,28
S_AD6	156	PCI_S_AD06	26,28
S_AD7	158	PCI_S_AD07	26,28
S_AD8	160	PCI_S_AD08	26,28
S_AD9	162	PCI_S_AD09	26,28
S_AD10	163	PCI_S_AD10	26,28
S_AD11	164	PCI_S_AD11	26,28
S_AD12	166	PCI_S_AD12	26,28
S_AD13	167	PCI_S_AD13	26,28
S_AD14	169	PCI_S_AD14	26,28
S_AD15	170	PCI_S_AD15	26,28
S_AD16	16	PCI_S_AD16	26,28
S_AD17	18	PCI_S_AD17	26,28
S_AD18	19	PCI_S_AD18	26,28
S_AD19	20	PCI_S_AD19	26,28
S_AD20	22	PCI_S_AD20	26,28
S_AD21	23	PCI_S_AD21	26,28
S_AD22	24	PCI_S_AD22	26,28
S_AD23	26	PCI_S_AD23	26,28
S_AD24	28	PCI_S_AD24	26,28
S_AD25	30	PCI_S_AD25	26,28
S_AD26	31	PCI_S_AD26	26,28
S_AD27	33	PCI_S_AD27	26,28
S_AD28	34	PCI_S_AD28	26,28
S_AD29	35	PCI_S_AD29	26,28
S_AD30	37	PCI_S_AD30	26,28
S_AD31	38	PCI_S_AD31	26,28
S_C/BE0_N	159	PCI_S_CBE0_N	26,28
S_C/BE1_N	172	PCI_S_CBE1_N	26,28
S_C/BE2_N	15	PCI_S_CBE2_N	26,28
S_C/BE3_N	27	PCI_S_CBE3_N	26,28
S_GNT0_N	49	PCI_S_GNT0_N	24,26
S_GNT1_N	50	PCI_S_GNT1_N	24,28
S_GNT2_N	51	PCI_S_GNT2_N	24
S_GNT3_N	53	PCI_S_GNT3_N	24
S_REQ0_N	39	PCI_S_REQ0_N	24,26
S_REQ1_N	40	PCI_S_REQ1_N	24,28
S_REQ2_N	42	PCI_S_REQ2_N	24
S_REQ3_N	47	PCI_S_REQ3_N	24
S_CLKOUT0	59	PCI_S_CLK0_R	25
S_CLKOUT1	61	PCI_S_CLK1_R	25
S_CLKOUT2	63	PCI_S_CLK2_R	25
S_CLKOUT3	65	PCI_S_CLK3_R	25
S_CLKOUT4	67	PCI_S_CLK4_R	25
S_CLK	57	PCI_S_CLK4	25
S_DEVSEL_N	9	PCI_S_DEVSEL_N	24,26,28
S_FRAME_N	13	PCI_S_FRAME_N	24,26,28
S_IRDY_N	12	PCI_S_IRDY_N	24,26,28
S_MFUNC	7	PCI_S_LOCK_N	24,26,28
S_PAR	3	PCI_S_PAR	24,26,28
S_PERR_N	6	PCI_S_PERR_N	24,26,28
S_RST_N	54	PCI_S_RST_N	24,26,28
S_SERR_N	5	PCI_S_SERR_N	24,26,28
S_STOP_N	8	PCI_S_STOP_N	24,26,28
S_TRDY_N	11	PCI_S_TRDY_N	24,26,28
S_VCCP	58	VCC5V	
S_C/CFN_N	55	PCIBR_CFN_N	25

PCI2250

VCC3V3;10,17,25,32,44,52,62,66,81,88,100
VCC3V3;108,118,126,139,145,153,161,168,176

GND;1,14,21,29,36,45,56,60,64,71,77,89
GND;96,104,113,122,130,133,142,149,157,165,171

NC=2,4,41,43,46,48,85,87,90,92,129,131,134,136,173,175

VCC3V3 — 4.75K — R25 — PCIBR_GOZ_N

VCC3V3

C437	C439	C442
0.1UF	0.1UF	0.1UF
C445	C453	C431
0.1UF	0.1UF	0.1UF
C432	C452	C450
0.1UF	0.1UF	0.1UF
C451		
0.1UF		

VCC3V3

C449	C448	C444
0.1UF	0.1UF	0.1UF
C441	C438	C436
0.1UF	0.1UF	0.1UF
C427	C428	C430
0.1UF	0.1UF	0.1UF
C429		
0.1UF		

VCC3V3

25	PCIBR_MS0	R335 4.75K	
25	PCIBR_MS1	R365 4.75K	
25	PCIBR_CFN_N	R377 0	
	PCI_P_AD25	R383 0	
25	PCI_P_IDSEL		

25	PCI_S_CLK0_R	R378 24.9	PCI_S_CLK0 26
25	PCI_S_CLK1_R	R379 24.9	PCI_S_CLK1 28
25	PCI_S_CLK2_R	R380 24.9	NC
25	PCI_S_CLK3_R	R381 24.9	NC
25	PCI_S_CLK4_R	R363 24.9	PCI_S_CLK4 25

VCC5V — C434 0.1UF

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI-PCI BRIDGE

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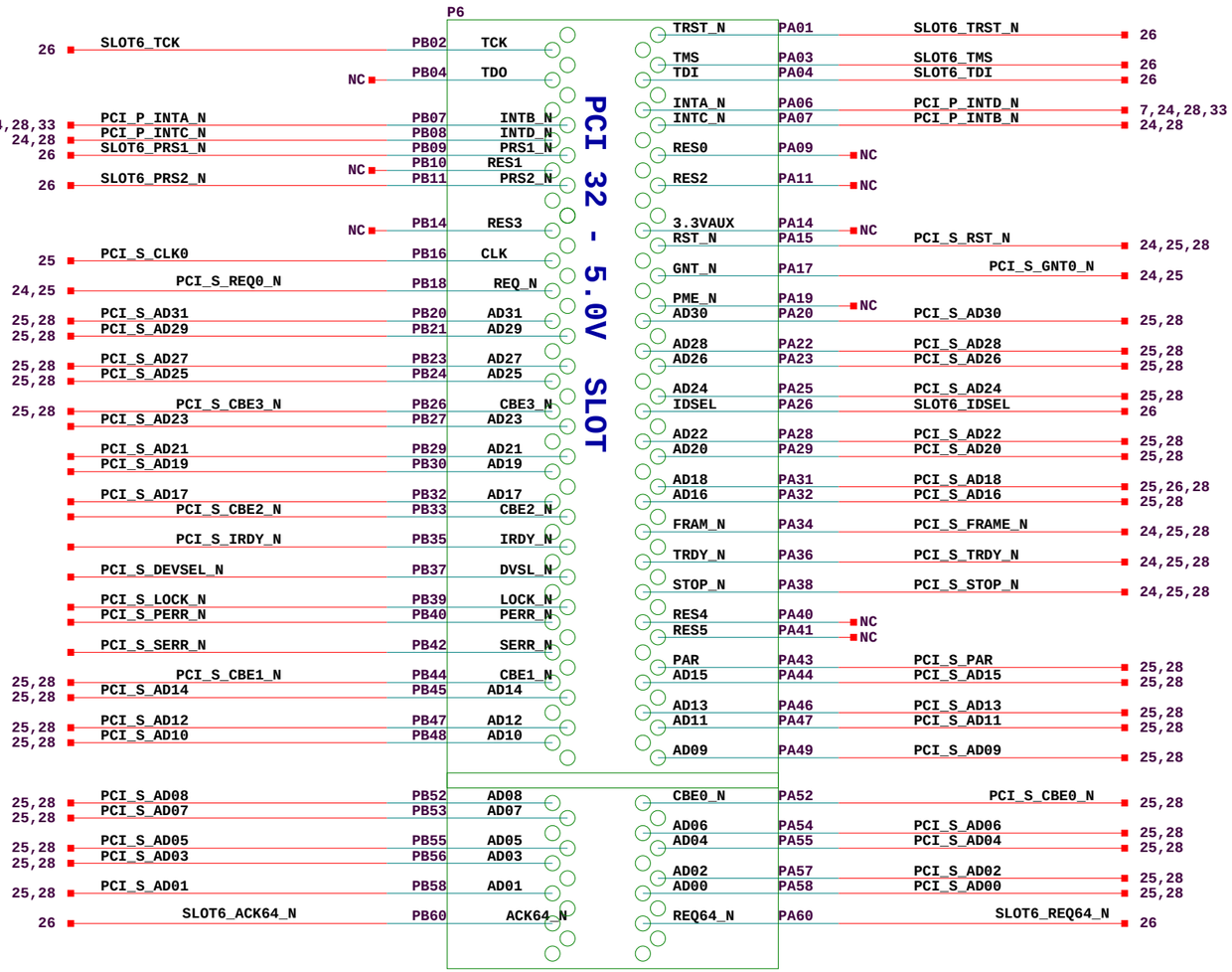
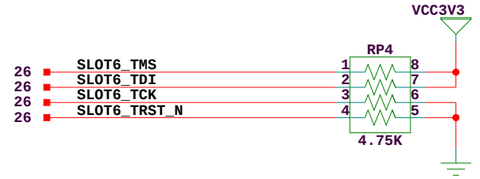
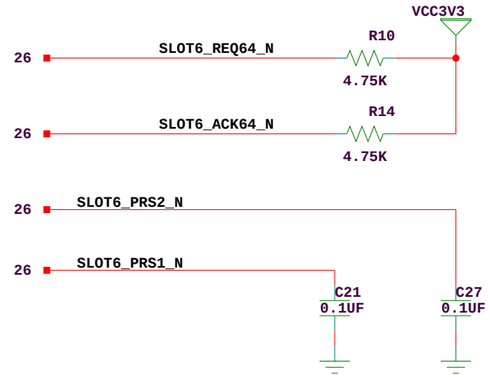


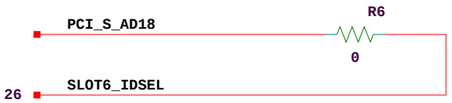
VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

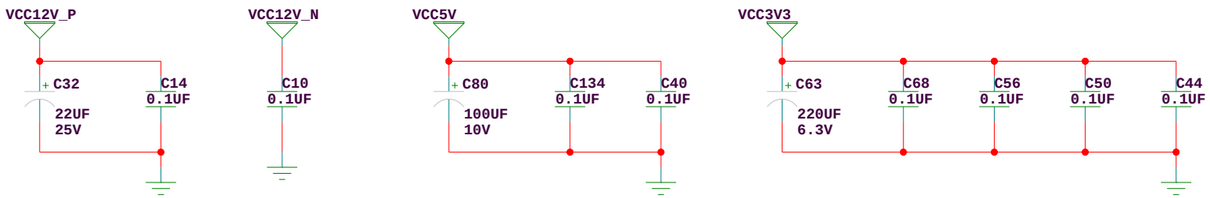
VCCIO VCC5V;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB12,PA12,PB13,PA13









XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOT 6, 5.0V, SECONDARY BUS

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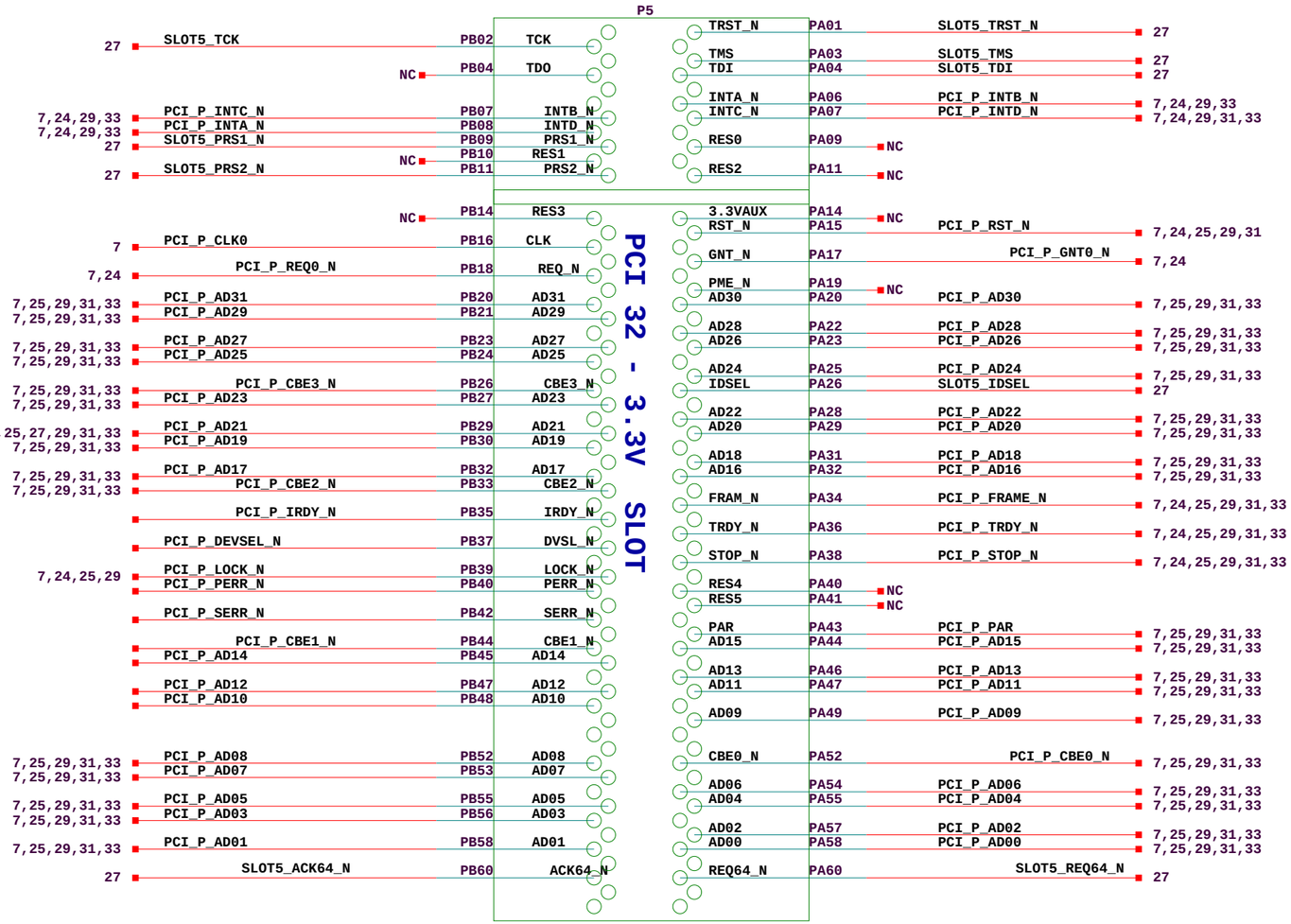
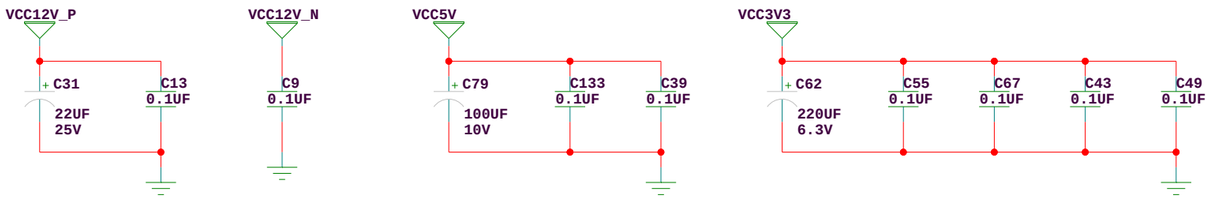
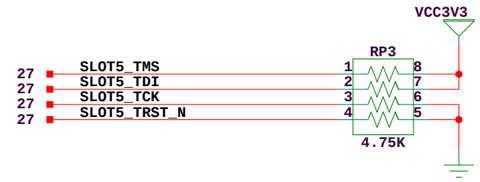


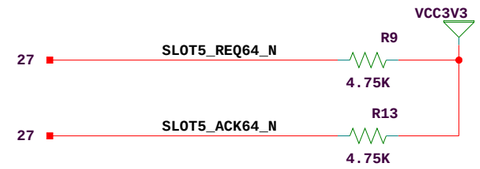
VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

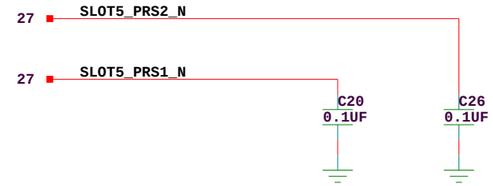
VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59

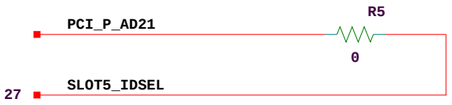
GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB50,PA50,PB51,PA51











XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOT 5, 3.3V, PRIMARY BUS

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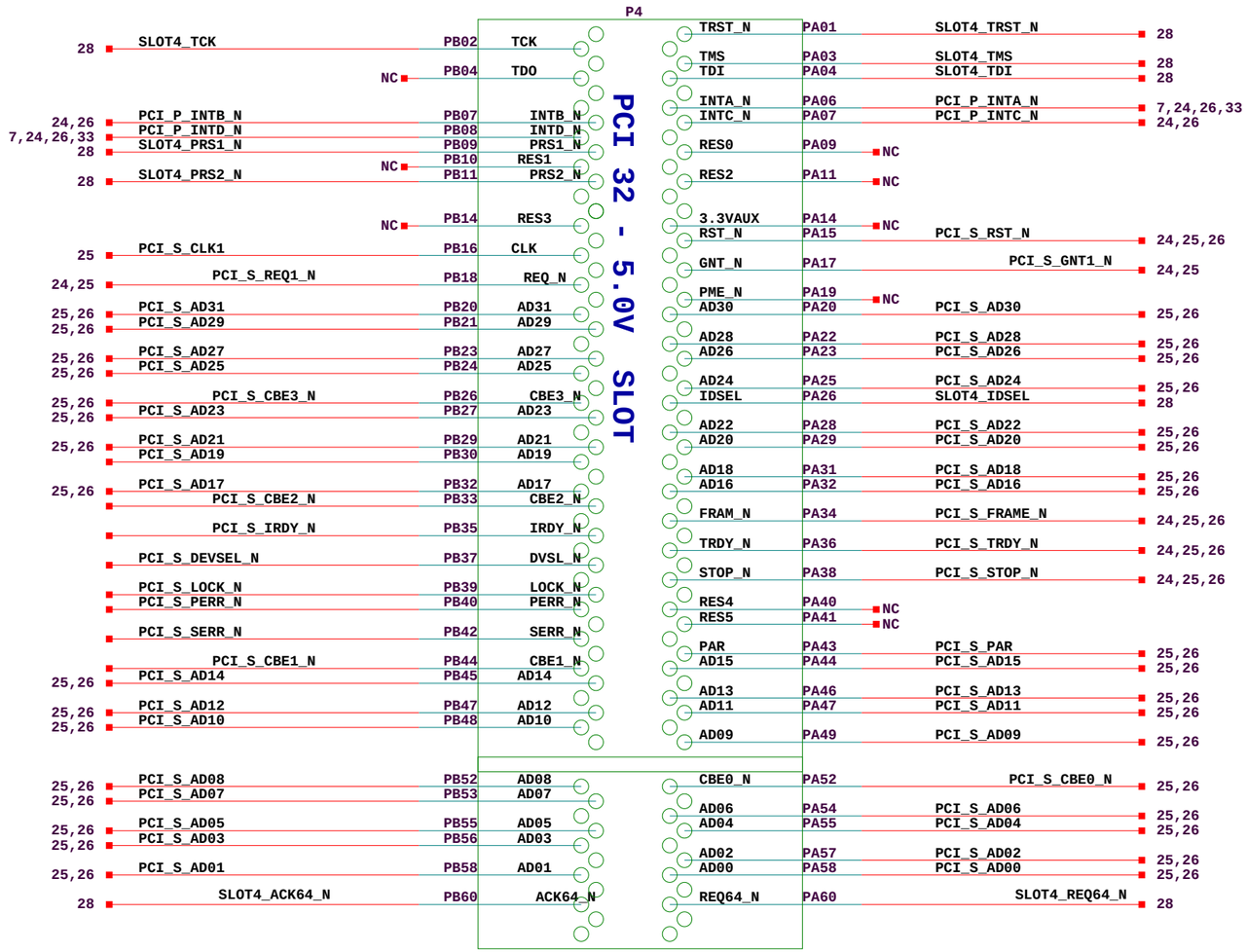
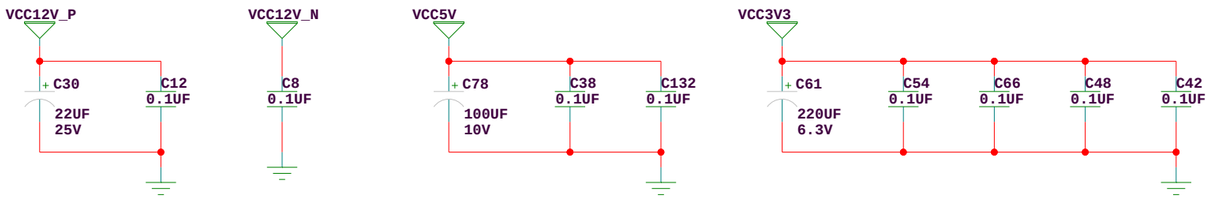
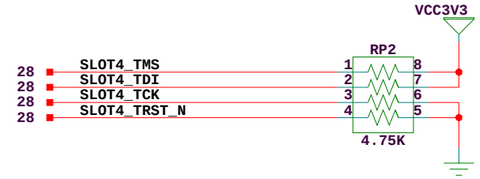


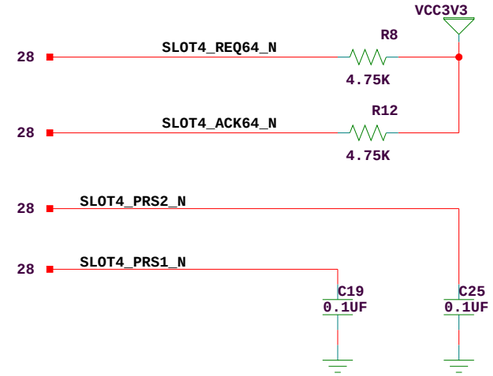
VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

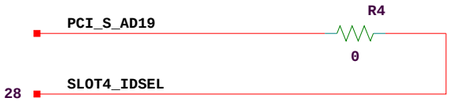
VCCIO VCC5V;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB12,PA12,PB13,PA13









XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOT 4, 5.0V, SECONDARY BUS

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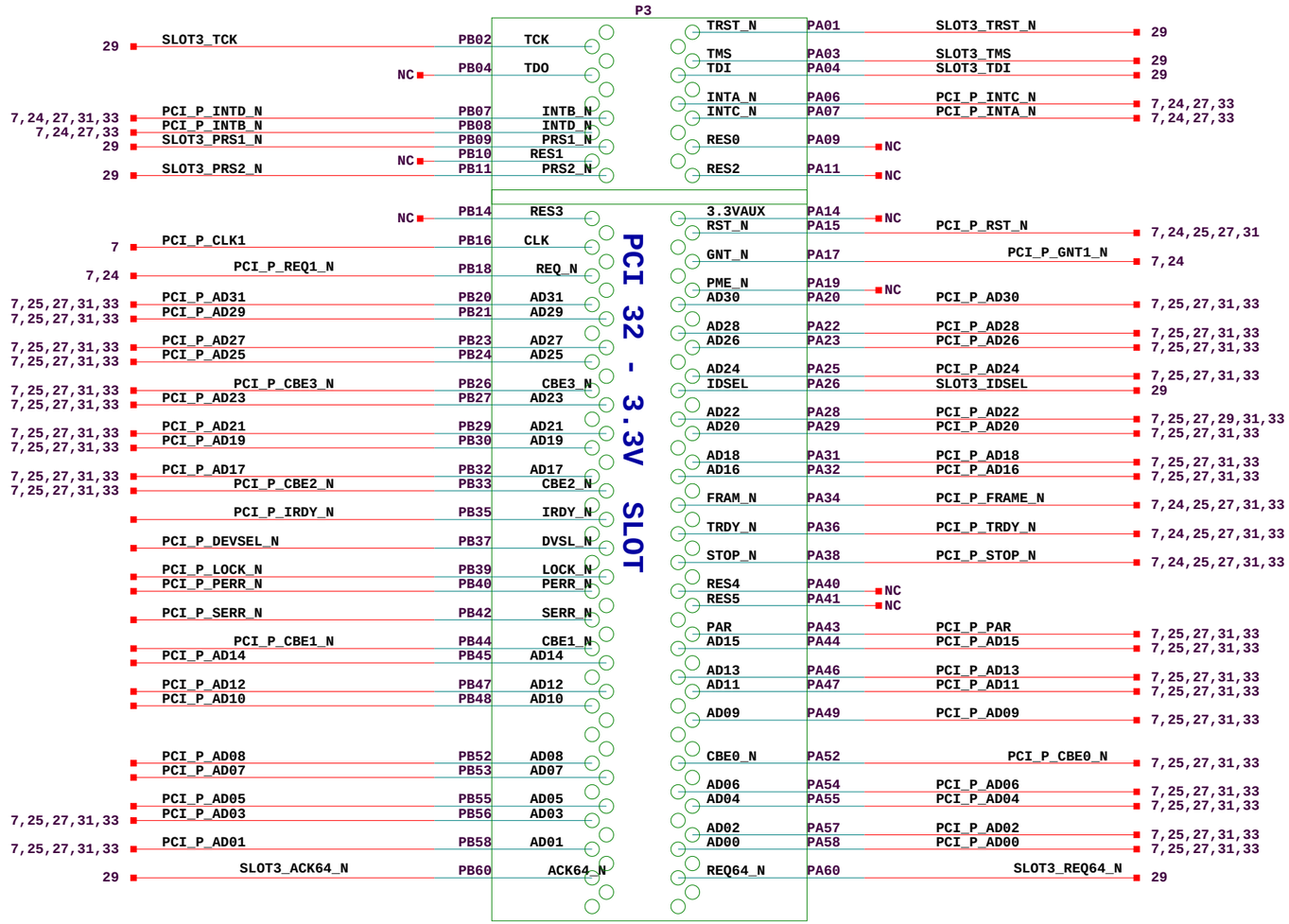
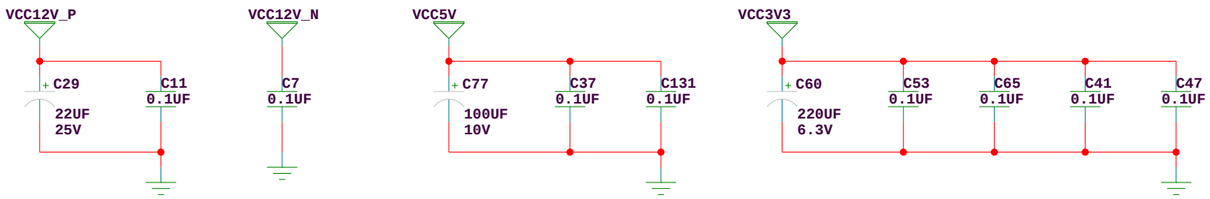
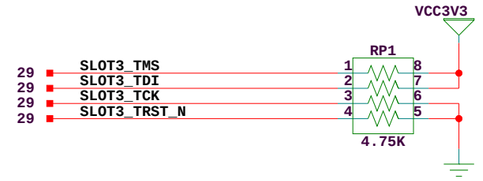


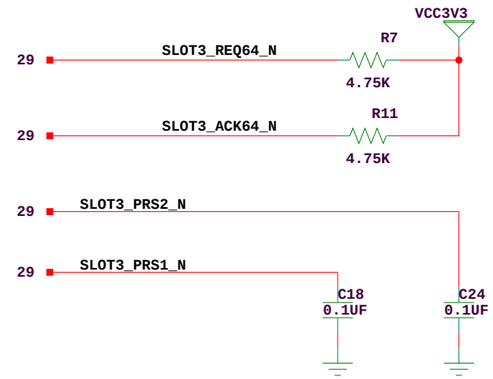
VCC12V_P;PA02
VCC12V_N;PB01
VCC5V;PA05,PB05,PB06,PA08
VCC5V;PA61,PB61,PA62,PB62
VCC3V3;PA21,PB25,PA27,PB31,PA33,PB36
VCC3V3;PA39,PB41,PB43,PA45,PA53,PB54

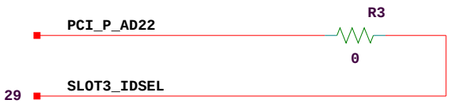
VCCIO VCC3V3;PA10,PA16,PB19,PB59,PA59

GND;PB03,PB15,PB17,PA18,PB22,PA24
GND;PB28,PA30,PB34,PA35,PA37,PB38
GND;PA42,PB46,PA48,PB49,PA56,PB57
GND;PB50,PA50,PB51,PA51









XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOT 3, 3.3V, PRIMARY BUS

Date:	8-22-2006_9:53	Ver:	03
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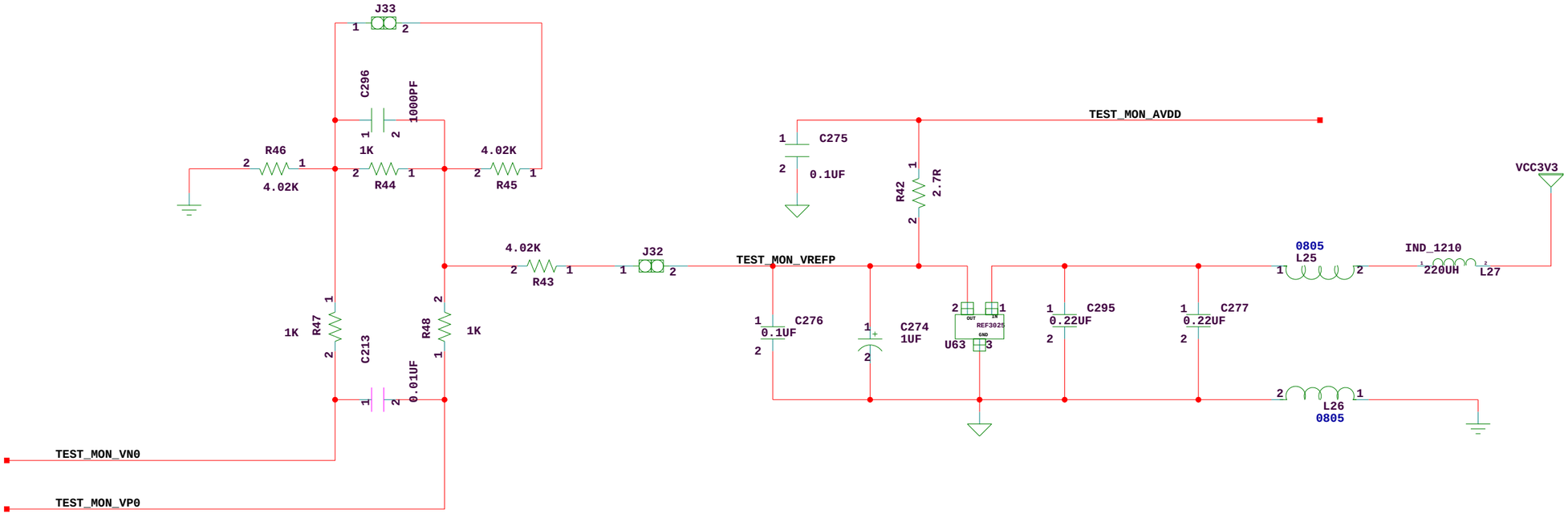

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
TEST INTERFACE

Date: 8-22-2006_9:53	Ver: 03
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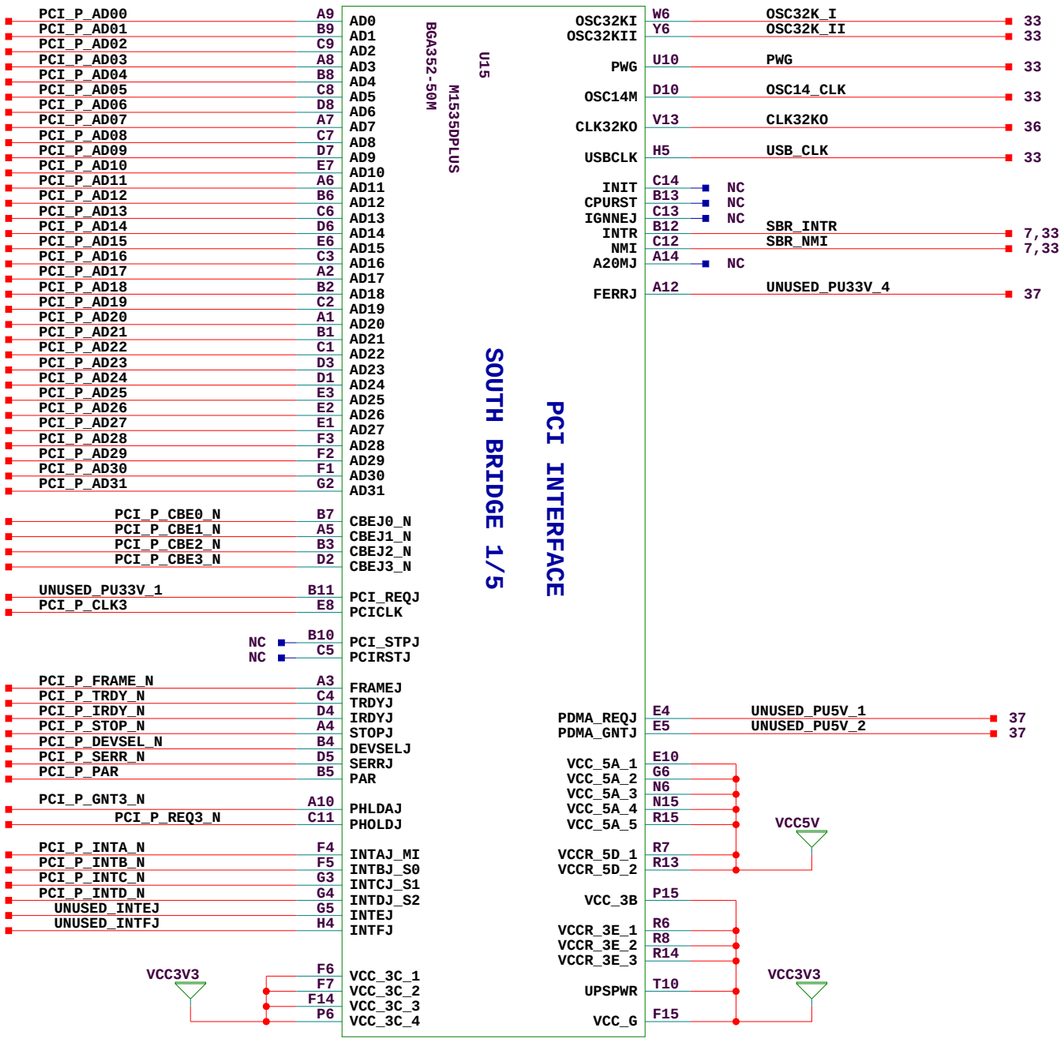

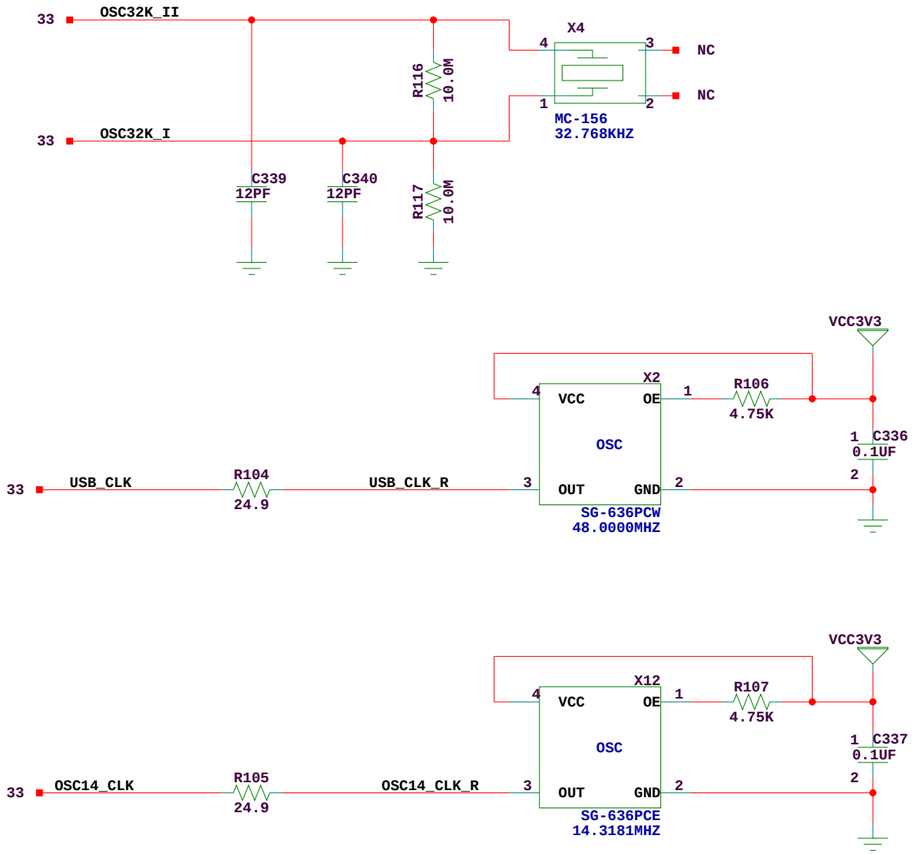

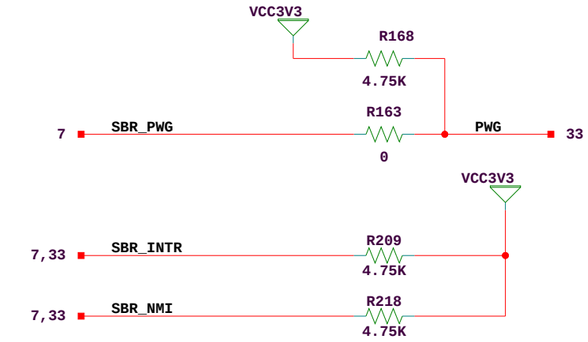

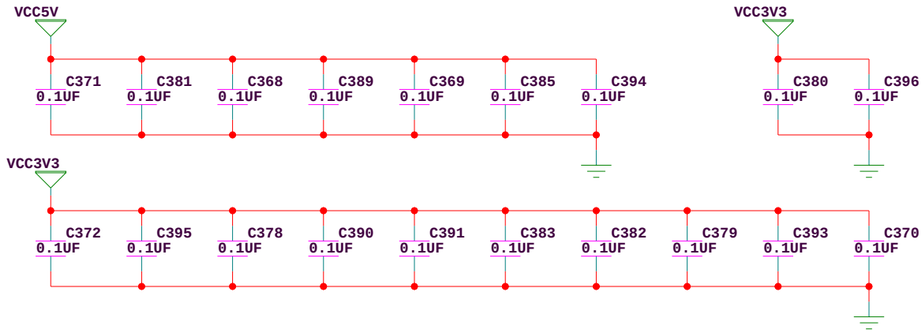

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
PCI SOUTH BRIDGE, PART 1

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M1535D+

U15 — B6A352-50M — M1535DPLUS

SOUTH BRIDGE 2/5

PARALLEL PORT

STROBJ	P1	PP_STROBE_N_R	38
AUTOFDJ	R1	PP_AUTOFD_N_R	38
PD0	P2	PP_DATA0_R	38
ERRORJ	T1	PP_ERROR_N_R	38
PD1	P3	PP_DATA1_R	38
PRINITJ	R2	PP_INIT_N_R	38
PD2	N1	PP_DATA2_R	38
SLCTINJ	R3	PP_SLCTIN_N_R	38
PD3	N2	PP_DATA3_R	38
PD4	N3	PP_DATA4_R	38
PD5	N4	PP_DATA5_R	38
PD6	N5	PP_DATA6_R	38
PD7	M2	PP_DATA7_R	38
PRNACKJ	M3	PP_ACK_N_R	38
BUSY	M4	PP_BUSY_R	38
PE	M5	PP_PEND_R	38
SLCT	L5	PP_SELECT_R	38

SERIAL PORT1

SIN1	H2		
SOUT1	J5		
RTS1J	H1		
DTR1J	J3		
CTS1J	J4		
DSR1J	H3		
DCD1J	G1		
RI1J	J2		

SERIAL PORT2

SIN2	K4		
SOUT2	K2		
RTS2J	K3		
DTR2J	L2		
CTS2J	K1		
DSR2J	K5		
DCD2J	J1		
RI2J	L1		

USB PORTS

OVCRJ1	T6	USB1_OVCR_N	40
OVCRJ0	T5	USB0_OVCR_N	40
USB_PWENJ	V9	USB_POWEN_N	40
GPIO22	U5	GPIO_23	42
GPIO23	U6	GPIO_22	42
USBP0+	W8	USB0_DP_R	40
USBP0-	V8	USB0_DN_R	40
USBP1+	U9	USB1_DP_R	40
USBP1-	Y7	USB1_DN_R	40
USBP2+	W7	GPI_34	42
USBP2-	V7	UNUSED_PD_1	37
USBP3+	U8	GPI_36	42
USBP3-	T8	UNUSED_PD_2	37

IrDA

IRRXH	L4	UNUSED_PD_3	37
IRRX	L3	UNUSED_PD_4	37
IRTX	M1	NC	

KEYBRD MOUSE

KBCLK	U11	KBCLK_R	40
KBDATA	U12	KBDATA_R	40
KBINH	V12	KBINH	34,47
MSCLK	T11	MSCLK_R	40
MSDATA	T12	MSDATA_R	40

M1535D+

U15 — B6A352-50M — M1535DPLUS

SOUTH BRIDGE 3/5

IDE INTERFACE

PIDED0	G17	PIDE_D0_R	41
PIDED1	F20	PIDE_D1_R	41
PIDED2	F18	PIDE_D2_R	41
PIDED3	F16	PIDE_D3_R	41
PIDED4	E19	PIDE_D4_R	41
PIDED5	D20	PIDE_D5_R	41
PIDED6	D18	PIDE_D6_R	41
PIDED7	B20	PIDE_D7_R	41
PIDED8	C20	PIDE_D8_R	41
PIDED9	D19	PIDE_D9_R	41
PIDED10	E18	PIDE_D10_R	41
PIDED11	E20	PIDE_D11_R	41
PIDED12	F17	PIDE_D12_R	41
PIDED13	F19	PIDE_D13_R	41
PIDED14	G16	PIDE_D14_R	41
PIDED15	G18	PIDE_D15_R	41
PIDEA0	H20	PIDE_A0_R	41
PIDEA1	H19	PIDE_A1_R	41
PIDEA2	J16	PIDE_A2_R	41
SIRQI	N16	PIDE_INTRQ_R	41
PIDEDRQ	G19	PIDE_DMARQ_R	41
PIDEDAKJ	H18	PIDE_DMACK_N_R	41
PIDERDY	H17	PIDE_IORDY_R	41
PIDEIORJ	H16	PIDE_DIOR_N_R	41
PIDEIOWJ	G20	PIDE_DIOW_N_R	41
PIDECS1J	J17	PIDE_CS1_N_R	41
PIDECS3J	J18	PIDE_CS3_N_R	41
CBLID_P	D11	PIDE_PDIAG_N_R	41
SIDED0	A17	SIDE_D0_R	41
SIDED1	D16	SIDE_D1_R	41
SIDED2	B16	SIDE_D2_R	41
SIDED3	E15	SIDE_D3_R	41
SIDED4	C15	SIDE_D4_R	41
SIDED5	A15	SIDE_D5_R	41
SIDED6	D14	SIDE_D6_R	41
SIDED7	E13	SIDE_D7_R	41
SIDED8	D13	SIDE_D8_R	41
SIDED9	E14	SIDE_D9_R	41
SIDED10	B15	SIDE_D10_R	41
SIDED11	D15	SIDE_D11_R	41
SIDED12	A16	SIDE_D12_R	41
SIDED13	C16	SIDE_D13_R	41
SIDED14	E16	SIDE_D14_R	41
SIDED15	B17	SIDE_D15_R	41
SIDEA0	A19	SIDE_A0_R	41
SIDEA1	C18	SIDE_A1_R	41
SIDEA2	B19	SIDE_A2_R	41
SIRQII	P16	SIDE_INTRQ_R	41
SIDEDRQ	C17	SIDE_DMARQ_R	41
SIDEDAKJ	B18	SIDE_DMACK_N_R	41
SIDERDY	A18	SIDE_IORDY_R	41
SIDEIORJ	E17	SIDE_DIOR_N_R	41
SIDEIOWJ	D17	SIDE_DIOW_N_R	41
SIDECS1J	C19	SIDE_CS1_N_R	41
SIDECS3J	A20	SIDE_CS3_N_R	41
CBLID_S	E11	SIDE_PDIAG_N_R	41
VCC_F1	G15	VCC3V3	
VCC_F2	K16		

GROUP F
VCC=3.3V

VCC5V

34,47 — KBINH — R202 — 4.75K

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SOUTH BRIDGE, PART 2-3

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M1535D+

U15 M1535DPLUS BGA352-50M

SOUTH BRIDGE 4/5

POWER MANAGEMENT UNIT1

RSM_RSTJ	W10	RSM_RSTJ	
SUSPENDJ	W13	NC	
PWRBTNJ	Y15	UNUSED_PU33V_5	
SLPBTNJ	V10	UNUSED_PU33V_6	
OFF_PWR0	V14	NC	
OFF_PWR1	W14	NC	
OFF_PWR2	Y14	NC	
SPLED	Y13	SPLED	
RSM_ENT0	W11	RSM_ENT0	
RSM_ENT1	Y11	UNUSED_PU5V_3	
RSM_ENT8	Y10	UNUSED_PD_5	
PMEJ	W12	UNUSED_PU33V_7	
RI	V11	UNUSED_PD_6	
IRQ8J	Y12	UNUSED_PU5V_4	
RSM_ENT3	T9	UNUSED_PD_7	

POWER MANAGEMENT UNIT2

SMIJ	A13	NC	
STPCLKJ	B14	NC	
SLEEPJ	D12	NC	
ZZ	E12	UNUSED_PU5V_5	37
NUINP1	A11	UNUSED_PD_8	37
CPU_STPJ	C10	NC	
THRMJ	T18	IIC_THERM_N	6,45
SQWO	V6	SQWO	36
SMBCLK	T7	SMB_SCL	35
SMBDATA	U7	SMB_SDA	35
SMBALERTJ	T2	IIC_ALERT_N	6,45
GPI25	E9	GPI_25	42
GPO34	P18	GPO_34	36,42
GPO35	P19	GPO_35	36,42

AC97 INTERFACE

ACRESETJ	Y9	AC_RESET_N	43
ACSDATA_IN0	W9	AC_SDATA_IN0	43
ACSDATA_IN1	Y8	UNUSED_PD_9	37
ACSDATA_OUT	U1	AC_SDATA_OUT	43
ACSYNC	P4	AC_SYNC	43
ACBIT_CLK	P5	AC_BIT_CLK	43
ACMIDI_TXD	R4	NC	
ACMIDI_RXD	T4	UNUSED_PD_10	37
ACGAME0	V1	NC	
ACGAME1	V2	NC	
ACGAME2	V3	NC	
ACGAME3	W1	NC	
ACGAME4	W2	NC	
ACGAME5	W3	NC	
ACGAME6	Y1	NC	
ACGAME7	Y2	NC	

SOUND CNTRL

ACGP_UPJ	U3	UNUSED_PU5V_7	37
ACGP_MUTEJ	U2	UNUSED_PU5V_8	37
ACGP_DOWNJ	R5	UNUSED_PU5V_9	37
FANOUT1	W5	NC	
FANOUT2	V5	NC	
FANIN2	Y5	UNUSED_PU5V_6	37
SPDIF_OUT	D9	NC	
SPDIF_IN	U4	UNUSED_PU5V_10	37

M1535D+

U15 M1535DPLUS BGA352-50M

SOUTH BRIDGE 5/5

XD(ISA) BUS

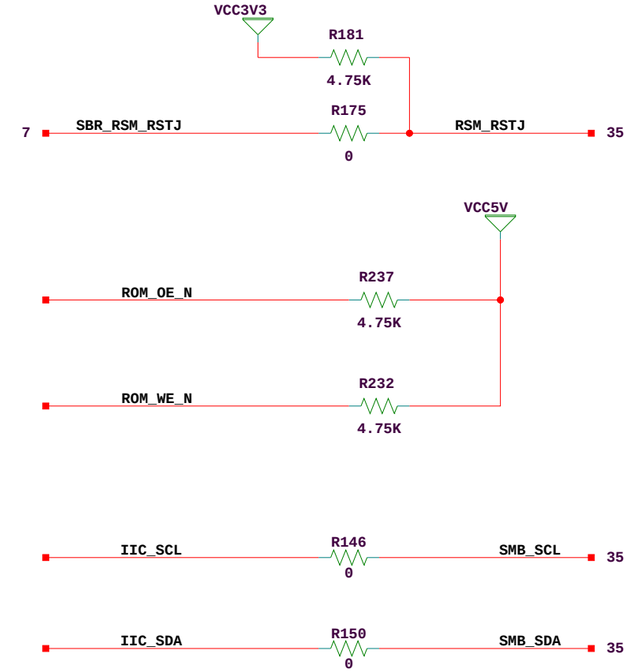
XD0	U20	ROM_D0	42
XD1	U19	ROM_D1	42
XD2	U18	ROM_D2	42
XD3	Y20	ROM_D3	42
XD4	W20	ROM_D4	42
XD5	V20	ROM_D5	42
XD6	Y19	ROM_D6	42
XD7	W19	ROM_D7	42
SA0	V19	ROM_A0	42
SA1	Y18	ROM_A1	42
SA2	W18	ROM_A2	42
SA3	V18	ROM_A3	42
SA4	Y17	ROM_A4	42
SA5	W17	ROM_A5	42
SA6	V17	ROM_A6	42
SA7	U17	ROM_A7	42
SA8	T17	ROM_A8	42
SA9	R17	ROM_A9	42
SA10	Y16	ROM_A10	42
SA11	W16	ROM_A11	42
SA12	V16	ROM_A12	42
SA13	U16	ROM_A13	42
SA14	T16	ROM_A14	42
SA15	W15	ROM_A15	42
BIOSA16	V15	ROM_A16	42
BIOSA17	U15	ROM_A17	42
BIOSA18	T15	ROM_A18	42
MEMRJ	T14	ROM_OE_N	35,42
MEMWJ	U14	ROM_WE_N	35,42
IORJ	T13	NC	
IOWJ	U13	NC	

FLOPPY DISK

RDATAJ	M18	UNUSED_PU5V_11	37
WGATEJ	L19	NC	
WDATAJ	L18	NC	
HDSELJ	M19	NC	
FD_DIRJ	L16	NC	
STEPJ	L17	NC	
DSKCHGJ	M20	UNUSED_PU5V_12	37
DRV0J	K19	NC	
DRV1J	K20	NC	
MOT0J	K17	NC	
MOT1J	K18	NC	
WPROTJ	M16	UNUSED_PU5V_13	37
TRK0J	L20	UNUSED_PU5V_14	37
INDEXJ	J20	UNUSED_PU5V_15	37
DENSEL	J19	NC	

MISCELLANEOUS LOGIC

SPKR	T19	SPKR	43,47
RTCAS	R20	NC	
RTCRW	R19	NC	
RTCDS	R18	NC	
ROMKBCSJ	T20	ROMKBCSJ	36,42
IRQSER	N19	UNUSED_PU5V_16	37
GPI24	M17	GPI_24	42
GPO29	N17	GPO_29	36,42
GPO30	N18	GPO_30	36,42
PCSOJ	P20	PCS0J	36
PCS1J	R16	PCS1J	36
RUN_ENT0	Y3	GPIO_0	42
RUN_ENT1	V4	GPIO_1	42
RUN_ENT2	W4	GPIO_2	42
RUN_ENT3	Y4	GPIO_3	42
GPO10	T3	GPO_10	42
LFRAMEJ	N20	UNUSED_PU5V_17	37
LDRQJ	P17	UNUSED_PU5V_18	37



XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SOUTH BRIDGE, PART 4-5

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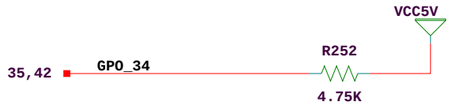
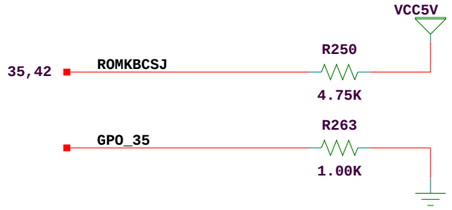
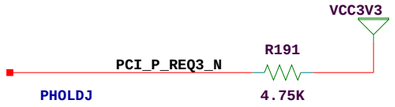


RESERVED/PULLED HIGH FOR NORMAL OPERATION



FLASH ROM FUNCTION MODE SELECT

DISABLED



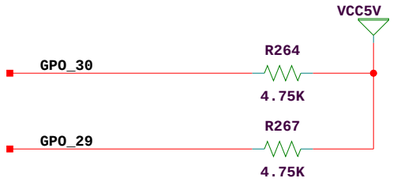
RESERVED/PULLED HIGH FOR NORMAL OPERATION

4MBIT FLASH ROM LINEAR MODE

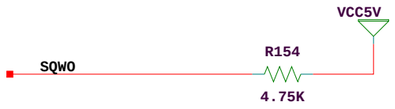
ENABLED

SWITCH GPI24/IOCHRDY AND GPO30/AEN FUNCTIONS

GPI24 AND GPO30 ENABLED

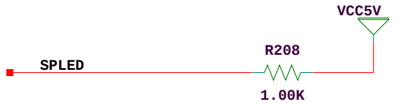


RESERVED/PULLED HIGH FOR NORMAL OPERATION



CPU SUPPORT SELECT

PENTIUM-II MODE

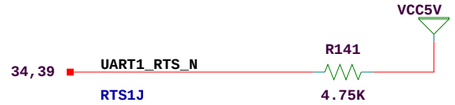


AT/ATX MODE SELECT

AT MODE

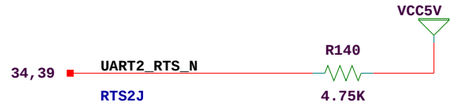
NOTE: AT MODE IS USED HERE TO DISABLE THE SOFT-POWER FUNCTIONALITY OF THE SOUTH BRIDGE

PULLED DOWN FOR NORMAL OPERATION



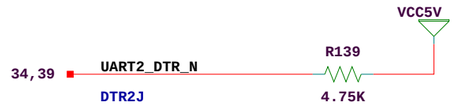
SIO BASE ADDRESS CONFIGURATION

BASE ADDR = 0x3F0



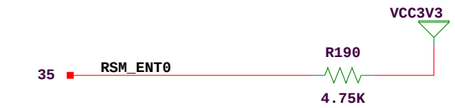
INTERNAL KEYBOARD CONTROLLER ENABLE

ENABLED



KEYBOARD CONTROLLER MODE SELECT

PS/2 MODE



POWER CONTROL ACTIVE LEVEL SELECT

ACTIVE HIGH

XILINX	SCH P/N 0381203 ART P/N 0531499 FAB P/N 1280372		
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM PCI SOUTH BRIDGE, CONFIG RESISTORS			
Date: 8-22-2006_9:53		Ver: 03	
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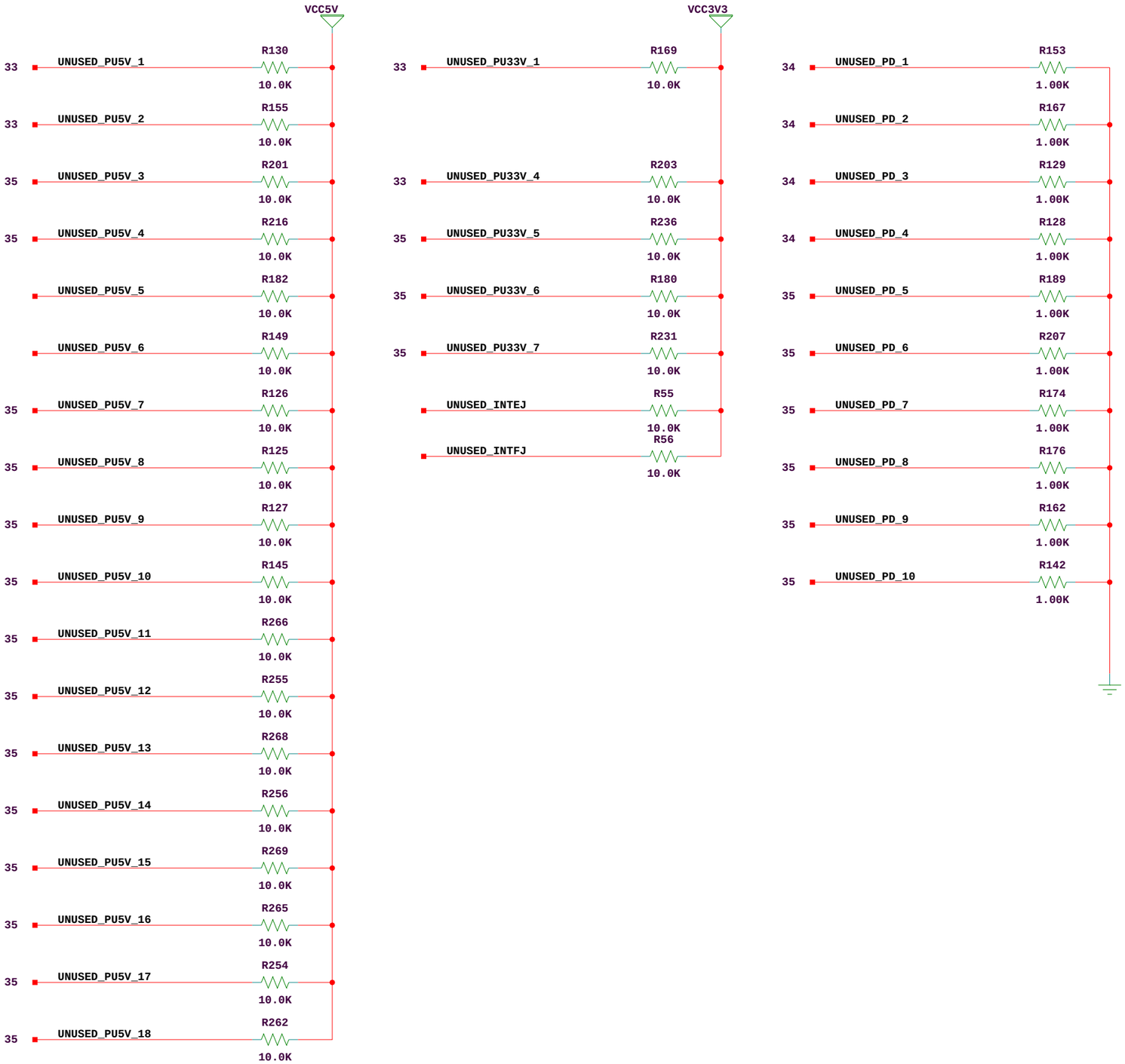

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
PCI SOUTH BRIDGE, UNUSED PIN RESISTORS

Date:	8-22-2006_9:53	Ver:	03
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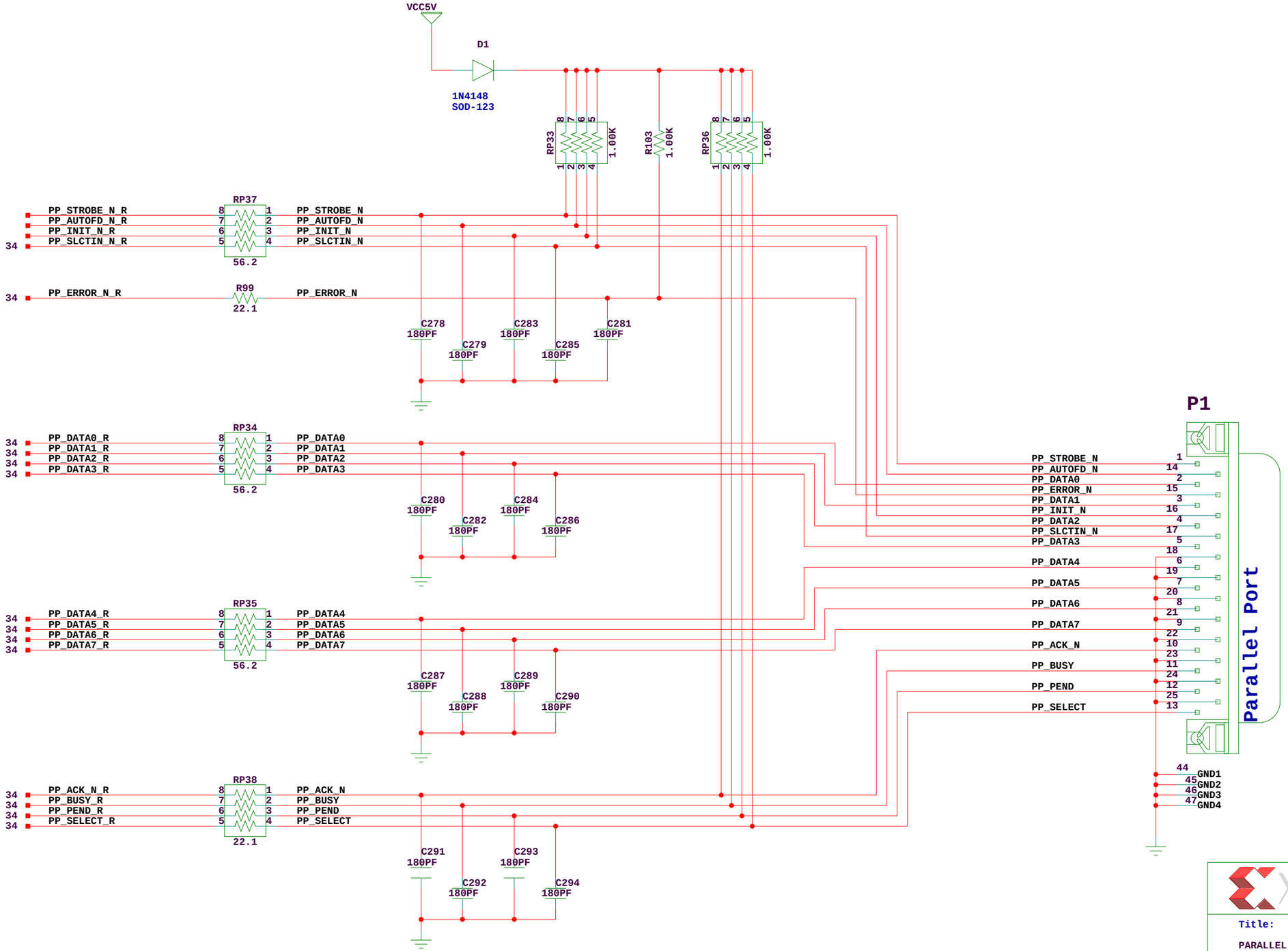

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PARALLEL PORT INTERFACE

Date:	8-22-2006_9:53	Ver:	03
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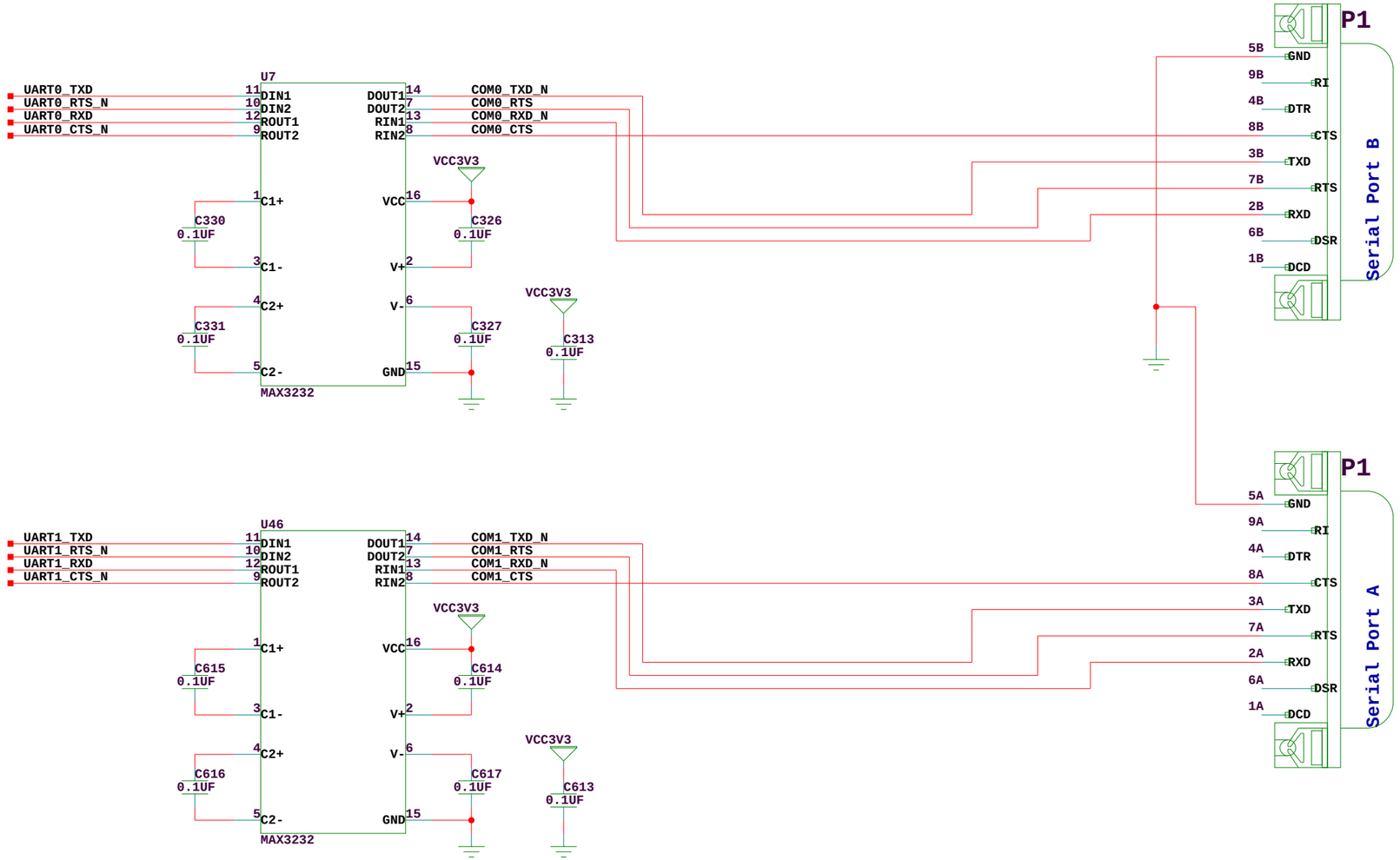

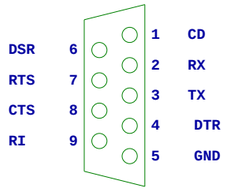

LOOKING INTO DB9 PLUG

RS232 DTE PINOUT
CONNECTS TO PC WITH
F/F NULL MODEM CABLE.

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
RS232 SERIAL PORT INTERFACE

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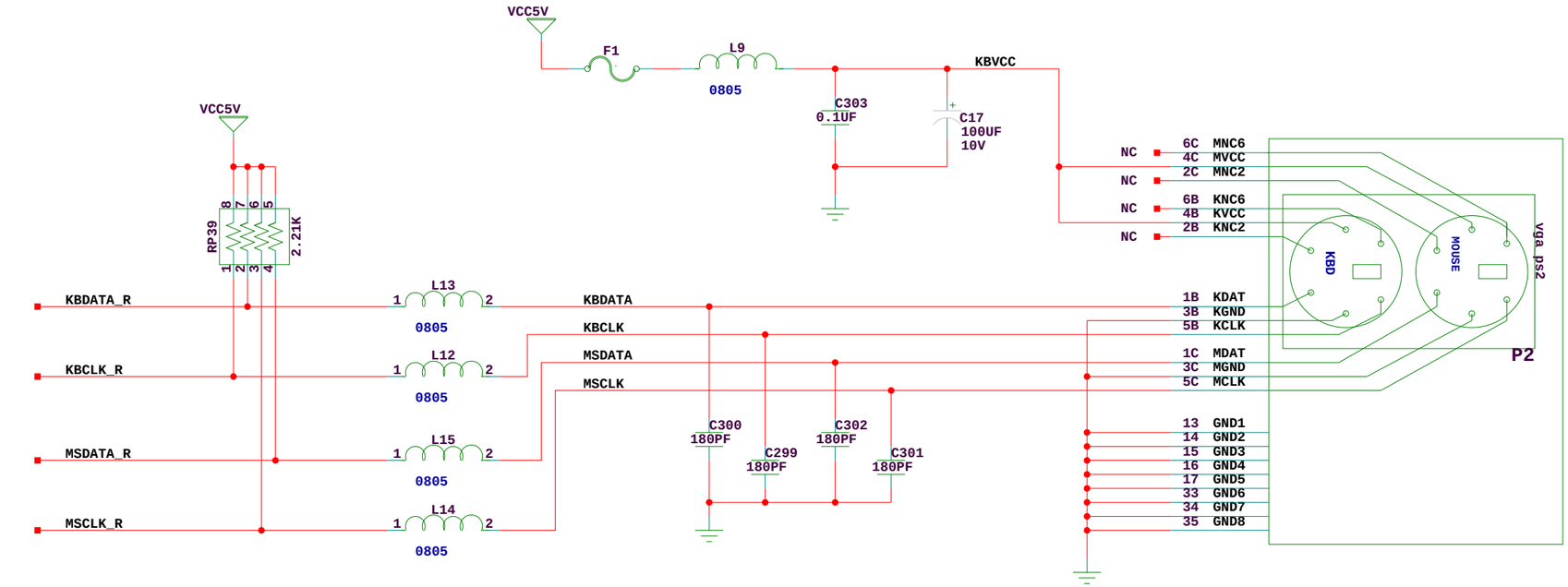

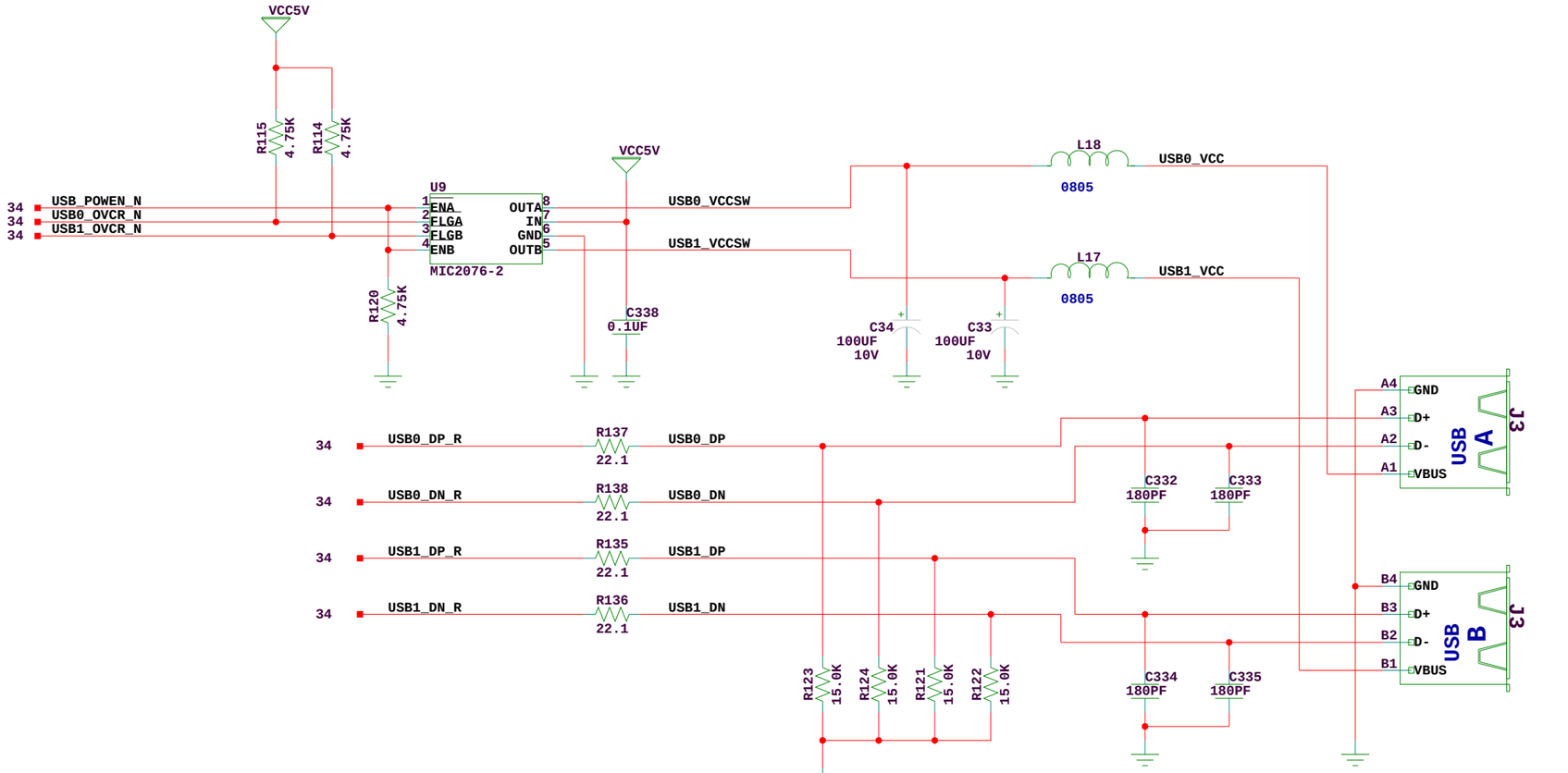

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
KBD/MOUSE AND USB INTERFACES

Date:	8-22-2006_9:53	Ver:	03
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Pin 20 must be removed.
Silkscreen:
"IDE PRIMARY"

RP51
34 PIDE_D7_R 8 1 PIDE_D7 41
34 PIDE_D8_R 7 2 PIDE_D8 41
34 PIDE_D6_R 6 3 PIDE_D6 41
34 PIDE_D9_R 5 4 PIDE_D9 41
47.5

RP50
34 PIDE_D5_R 8 1 PIDE_D5 41
34 PIDE_D10_R 7 2 PIDE_D10 41
34 PIDE_D4_R 6 3 PIDE_D4 41
34 PIDE_D11_R 5 4 PIDE_D11 41
47.5

RP49
PIDE_D3_R 8 1 PIDE_D3 41
PIDE_D12_R 7 2 PIDE_D12 41
PIDE_D2_R 6 3 PIDE_D2 41
PIDE_D13_R 5 4 PIDE_D13 41
47.5

RP48
PIDE_D1_R 8 1 PIDE_D1 41
PIDE_D14_R 7 2 PIDE_D14 41
PIDE_D0_R 6 3 PIDE_D0 41
PIDE_D15_R 5 4 PIDE_D15 41
47.5

34 PIDE_DMARQ_R 1 R303 2 PIDE_DMARQ 41
82.0

RP47
34 PIDE_DIOW_N_R 8 1 PIDE_DIOW_N 41
34 PIDE_DIOR_N_R 7 2 PIDE_DIOR_N 41
34 PIDE_IORDY_R 6 3 PIDE_IORDY 41
34 PIDE_DMACK_N_R 5 4 PIDE_DMACK_N 41
33.2

34 PIDE_INTRQ_R 1 R301 2 PIDE_INTRQ 41
82.0

RP46
34 PIDE_A1_R 8 1 PIDE_A1 41
34 PIDE_A0_R 7 2 PIDE_A0 41
34 PIDE_A2_R 6 3 PIDE_A2 41
34 PIDE_CS1_N_R 5 4 PIDE_CS1_N 41
33.2

34 PIDE_CS3_N_R R302 PIDE_CS3_N 41
33.2

34 PIDE_PDIAG_N_R R304 PIDE_PDIAG_N 41
0

VCC3V3
41 PIDE_IORDY R311 10.0K
41 PIDE_INTRQ R306 4.75K
41 PIDE_D7 R313 10.0K
41 PIDE_DMARQ R309 5.62K
41 PIDE_CSEL R299 475
41 PIDE_PDIAG_N R314 100K
C425
0.047UF

Mark Pin 1
Pin20=Key

J16
41 PIDE_RESET_N 1
2
41 PIDE_D7 3
41 PIDE_D8 4
41 PIDE_D6 5
41 PIDE_D9 6
41 PIDE_D5 7
41 PIDE_D10 8
41 PIDE_D4 9
41 PIDE_D11 10
41 PIDE_D3 11
41 PIDE_D12 12
41 PIDE_D2 13
41 PIDE_D13 14
41 PIDE_D1 15
41 PIDE_D14 16
41 PIDE_D0 17
41 PIDE_D15 18
19
NC 20
41 PIDE_DMARQ 21
22
41 PIDE_DIOW_N 23
24
41 PIDE_DIOR_N 25
26
41 PIDE_IORDY 27
41 PIDE_CSEL 28
41 PIDE_DMACK_N 29
30
41 PIDE_INTRQ 31
NC 32
41 PIDE_A1 33
41 PIDE_PDIAG_N 34
41 PIDE_A0 35
41 PIDE_A2 36
41 PIDE_CS1_N 37
41 PIDE_CS3_N 38
41,47 PIDE_DASP_N 39
40
CON_IDE40

IDE PRIMARY CONN

VCC3V3
R390 182
GREEN
DS22
41,47 PIDE_DASP_N

Silkscreen:
"IDE P LED"

7,41 SBR_IDE_RST_N R288 0 SIDE_RESET_N 41
7,41 SBR_IDE_RST_N R300 PIDE_RESET_N 41

Pin 20 must be removed.
Silkscreen:
"IDE SECONDARY"

RP40
34 SIDE_D7_R 8 1 SIDE_D7 41
34 SIDE_D8_R 7 2 SIDE_D8 41
34 SIDE_D6_R 6 3 SIDE_D6 41
34 SIDE_D9_R 5 4 SIDE_D9 41
47.5

RP41
34 SIDE_D5_R 8 1 SIDE_D5 41
34 SIDE_D10_R 7 2 SIDE_D10 41
34 SIDE_D4_R 6 3 SIDE_D4 41
34 SIDE_D11_R 5 4 SIDE_D11 41
47.5

RP42
34 SIDE_D3_R 8 1 SIDE_D3 41
34 SIDE_D12_R 7 2 SIDE_D12 41
34 SIDE_D2_R 6 3 SIDE_D2 41
34 SIDE_D13_R 5 4 SIDE_D13 41
47.5

RP44
34 SIDE_D1_R 8 1 SIDE_D1 41
34 SIDE_D14_R 7 2 SIDE_D14 41
34 SIDE_D0_R 6 3 SIDE_D0 41
34 SIDE_D15_R 5 4 SIDE_D15 41
47.5

34 SIDE_DMARQ_R 1 R291 2 SIDE_DMARQ 41
82.0

RP43
34 SIDE_DIOW_N_R 8 1 SIDE_DIOW_N 41
34 SIDE_DIOR_N_R 7 2 SIDE_DIOR_N 41
34 SIDE_IORDY_R 6 3 SIDE_IORDY 41
34 SIDE_DMACK_N_R 5 4 SIDE_DMACK_N 41
33.2

34 SIDE_INTRQ_R 1 R289 2 SIDE_INTRQ 41
82.0

RP45
34 SIDE_A1_R 8 1 SIDE_A1 41
34 SIDE_A0_R 7 2 SIDE_A0 41
34 SIDE_A2_R 6 3 SIDE_A2 41
34 SIDE_CS1_N_R 5 4 SIDE_CS1_N 41
33.2

34 SIDE_CS3_N_R R292 SIDE_CS3_N 41
33.2

34 SIDE_PDIAG_N_R R290 SIDE_PDIAG_N 41
0

VCC3V3
41 SIDE_IORDY R312 10.0K
41 SIDE_INTRQ R305 4.75K
41 SIDE_D7 R307 10.0K
41 SIDE_DMARQ R310 5.62K
41 SIDE_CSEL R287 475
41 SIDE_PDIAG_N R308 100K
C424
0.047UF

Mark Pin 1
Pin20=Key

J15
41 SIDE_RESET_N 1
2
41 SIDE_D7 3
41 SIDE_D8 4
41 SIDE_D6 5
41 SIDE_D9 6
41 SIDE_D5 7
41 SIDE_D10 8
41 SIDE_D4 9
41 SIDE_D11 10
41 SIDE_D3 11
41 SIDE_D12 12
41 SIDE_D2 13
41 SIDE_D13 14
41 SIDE_D1 15
41 SIDE_D14 16
41 SIDE_D0 17
41 SIDE_D15 18
19
NC 20
41 SIDE_DMARQ 21
22
41 SIDE_DIOW_N 23
24
41 SIDE_DIOR_N 25
26
41 SIDE_IORDY 27
41 SIDE_CSEL 28
41 SIDE_DMACK_N 29
30
41 SIDE_INTRQ 31
NC 32
41 SIDE_A1 33
41 SIDE_PDIAG_N 34
41 SIDE_A0 35
41 SIDE_A2 36
41 SIDE_CS1_N 37
41 SIDE_CS3_N 38
41,47 SIDE_DASP_N 39
40
CON_IDE40

IDE SECONDARY CONN

VCC3V3
R387 182
GREEN
DS21
SIDE_DASP_N

Silkscreen:
"IDE S LED"

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
IDE INTERFACES

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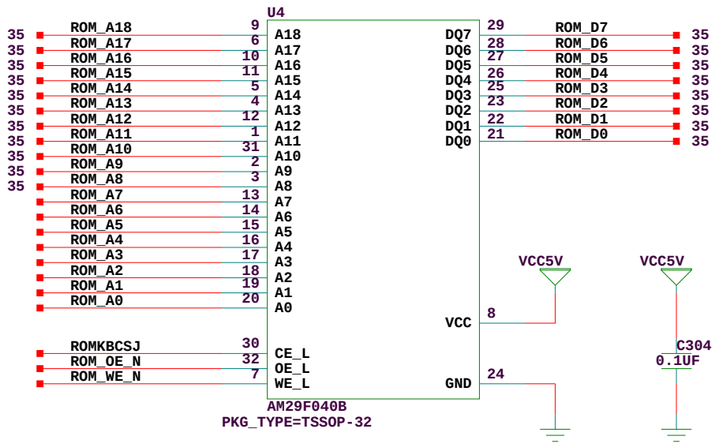
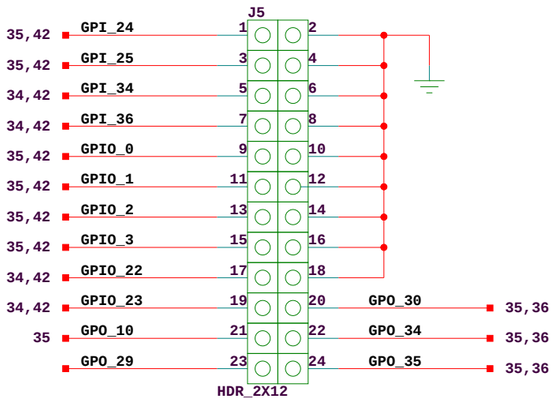
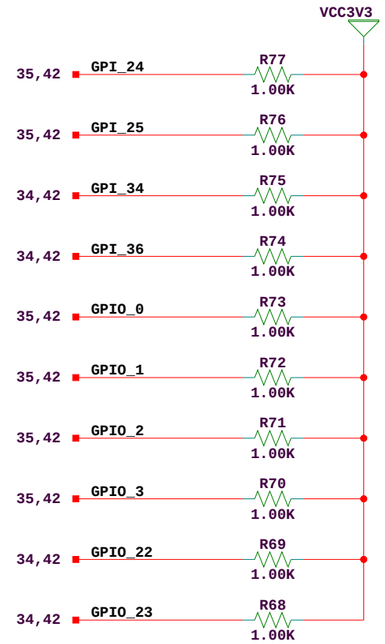
SOUTH BRIDGE

GPIO HEADER







XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

SOUTH BRIDGE ROM AND GPIO

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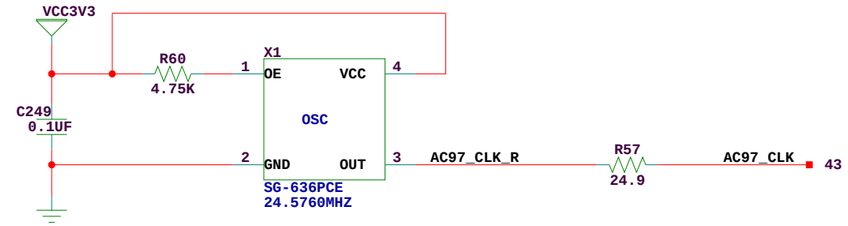

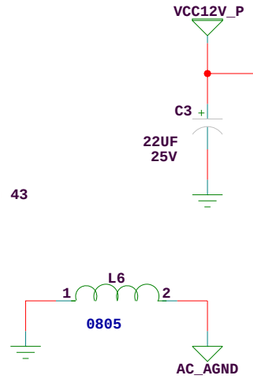

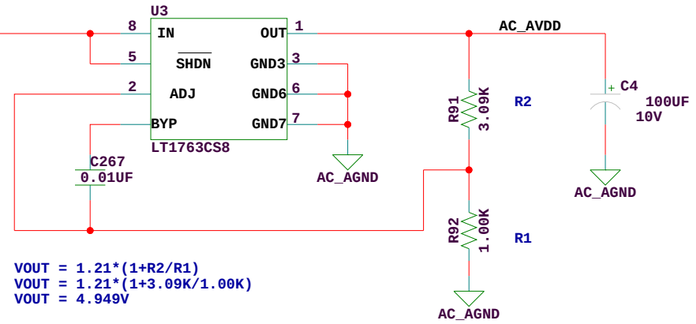

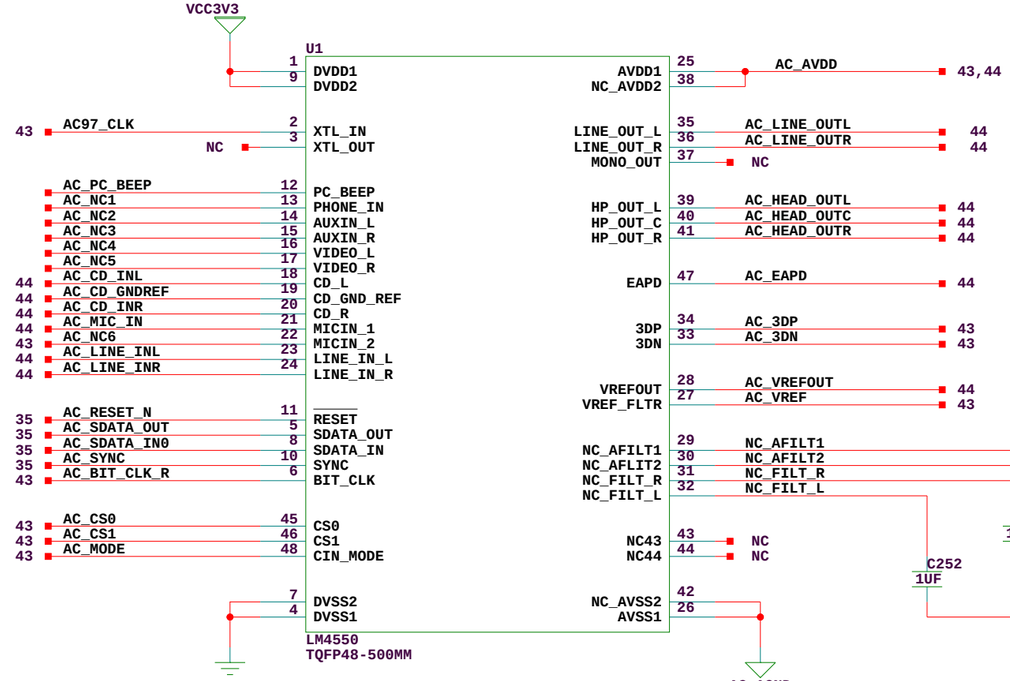

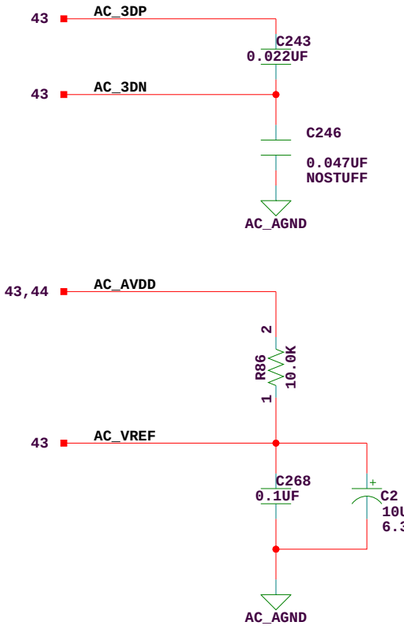

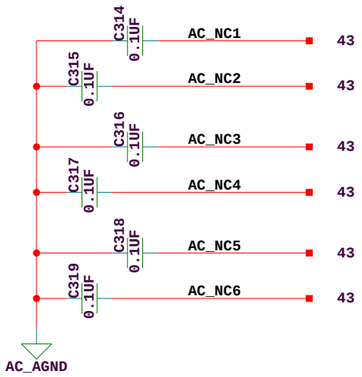

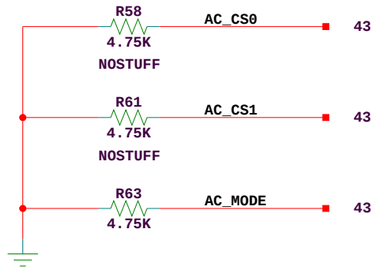

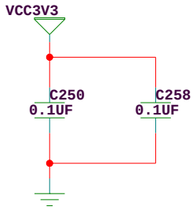

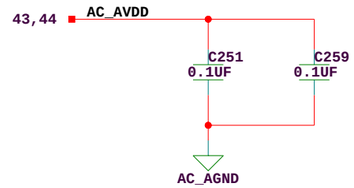

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

AC97 CODEC

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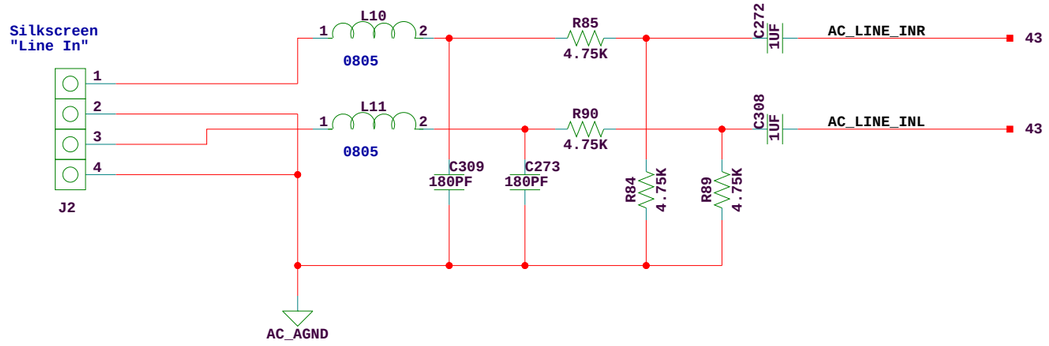

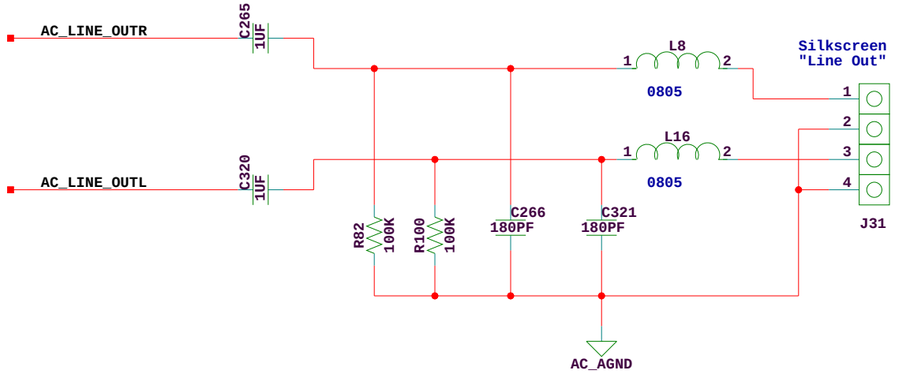

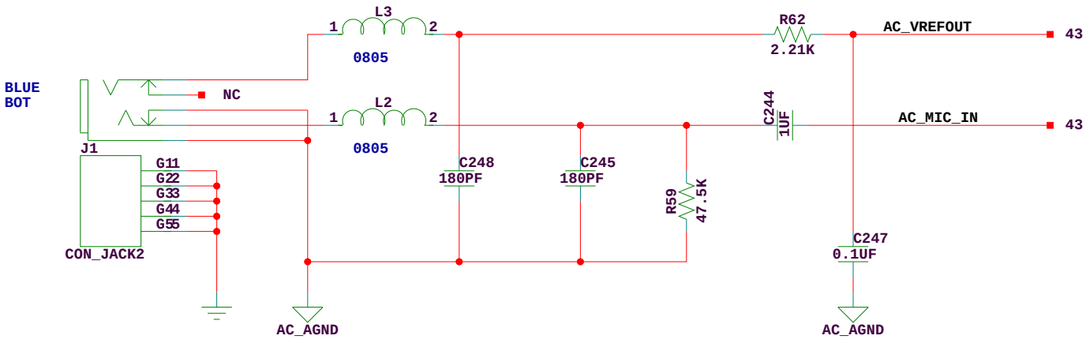

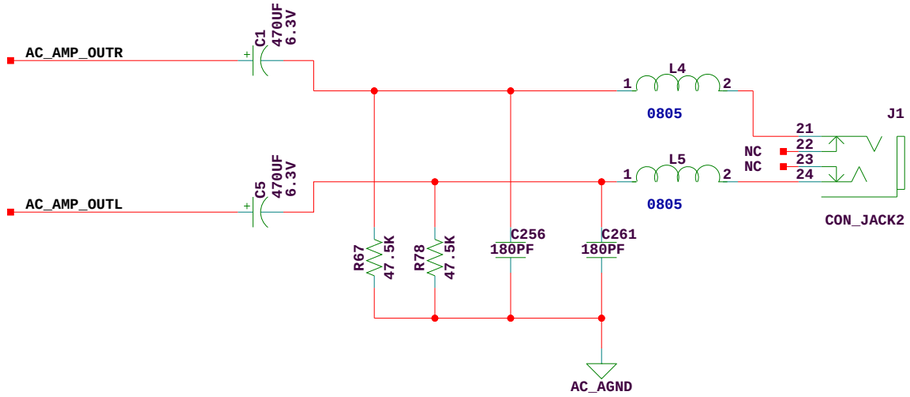

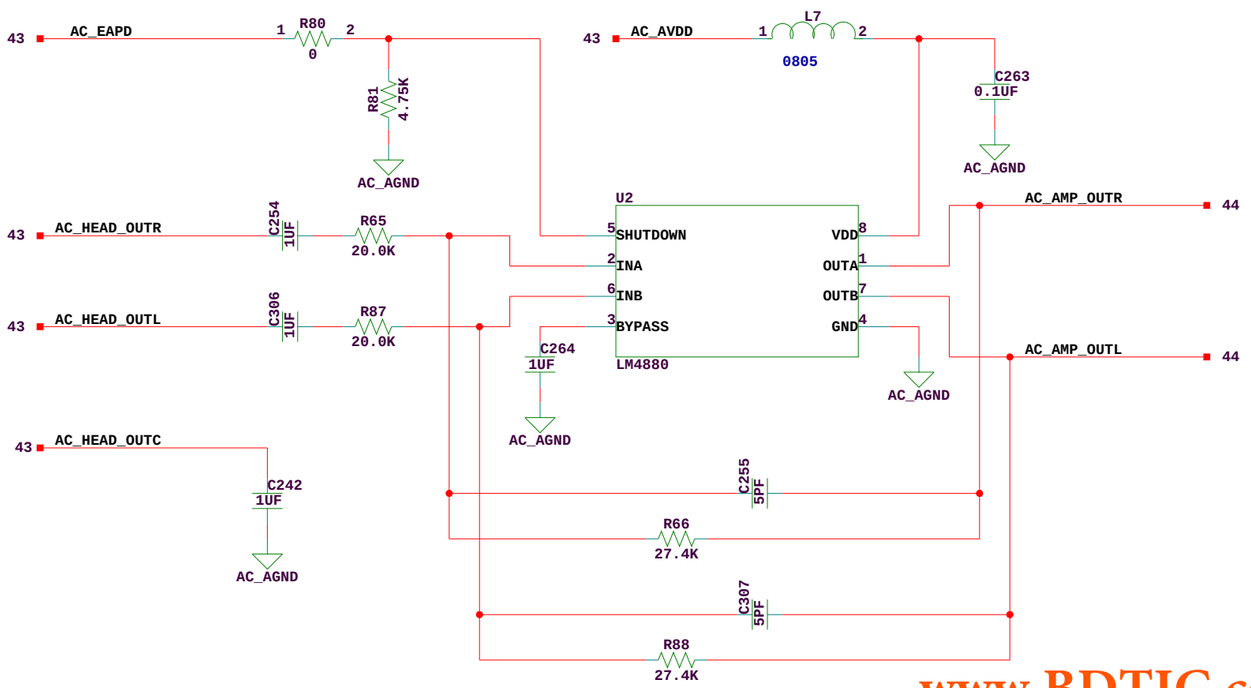

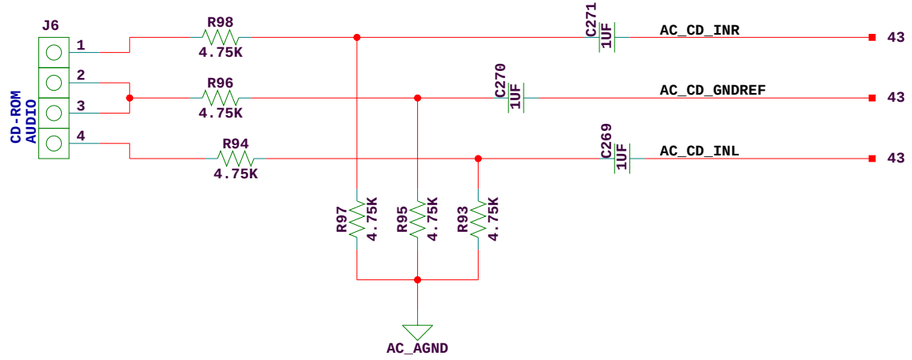

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

AC97 CONNECTORS

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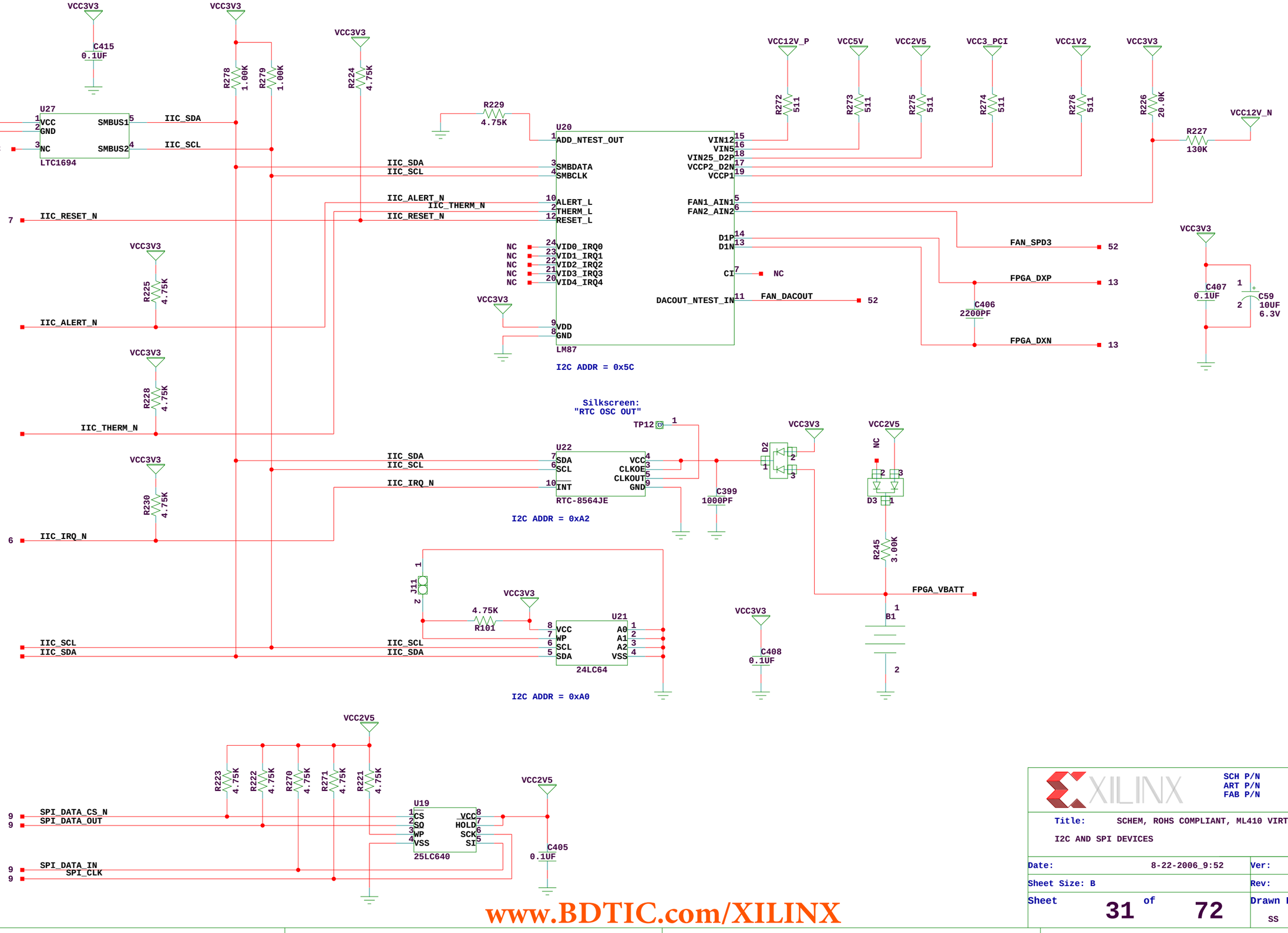

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

I2C AND SPI DEVICES

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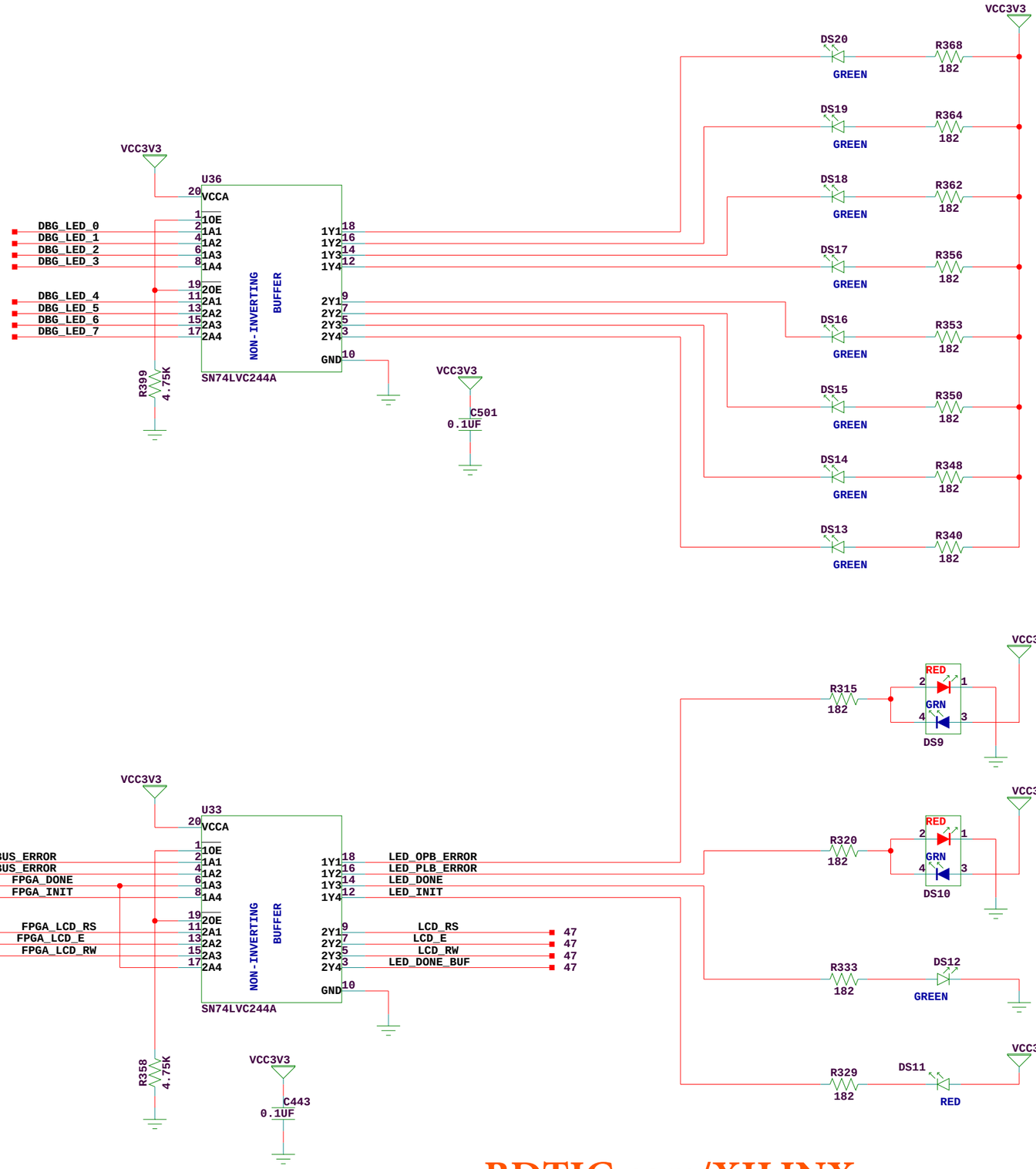

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

DEBUG AND STATUS LEDS

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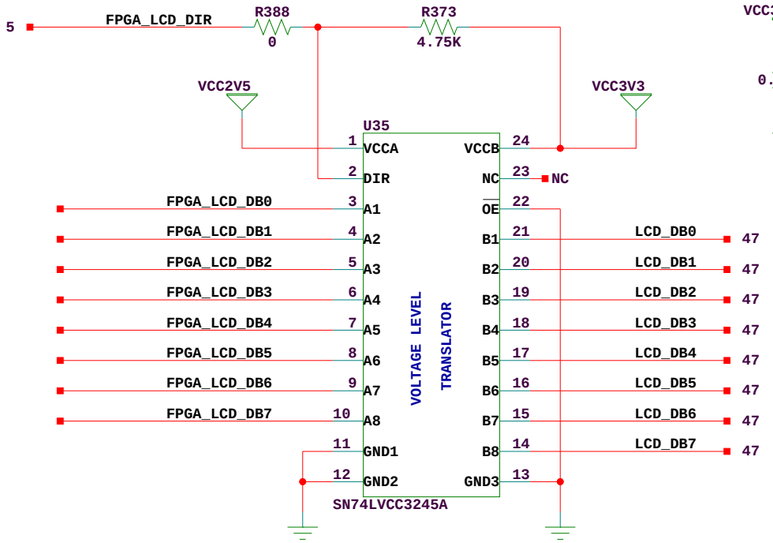

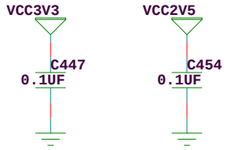

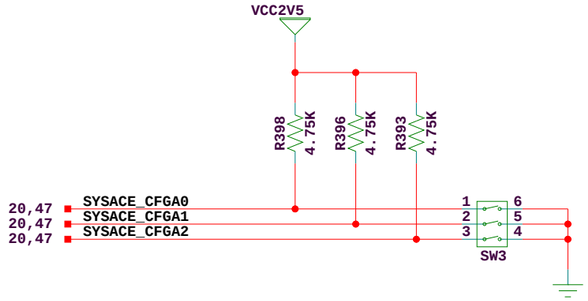

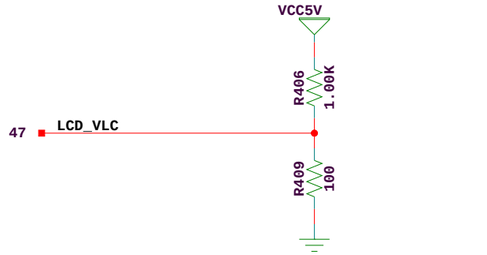

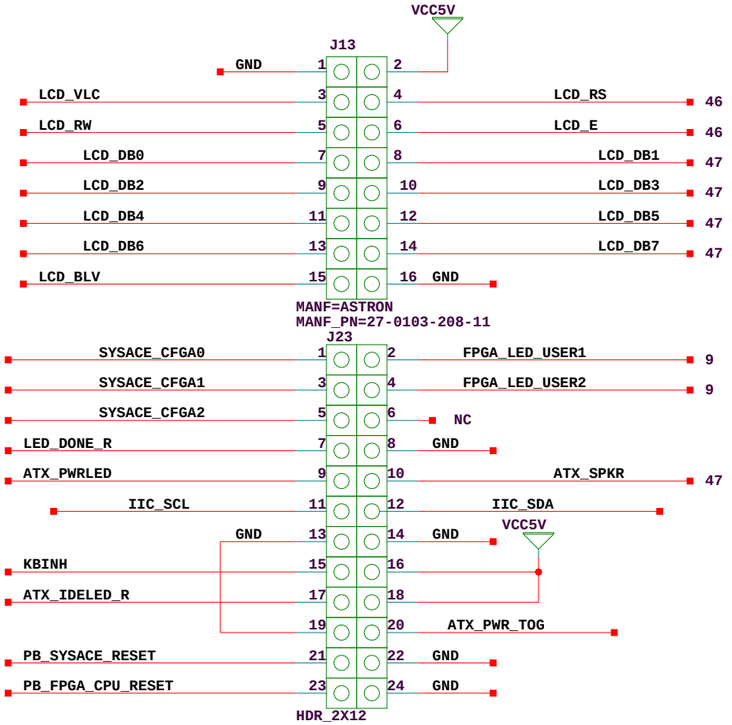

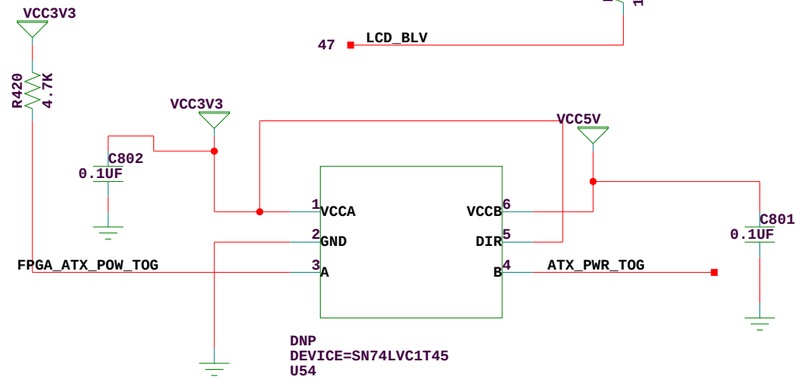

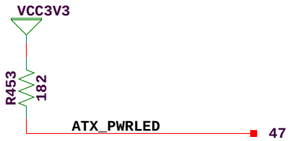

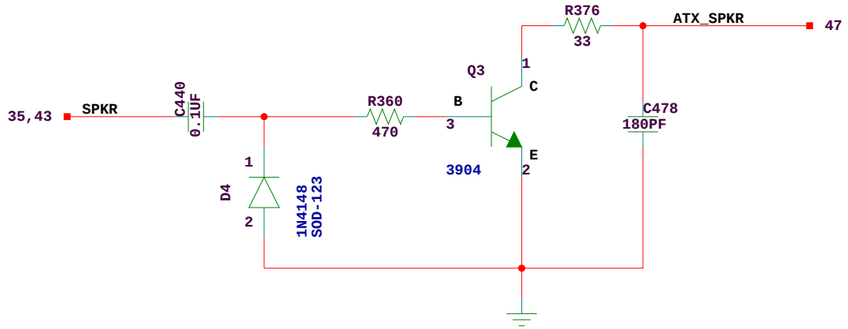

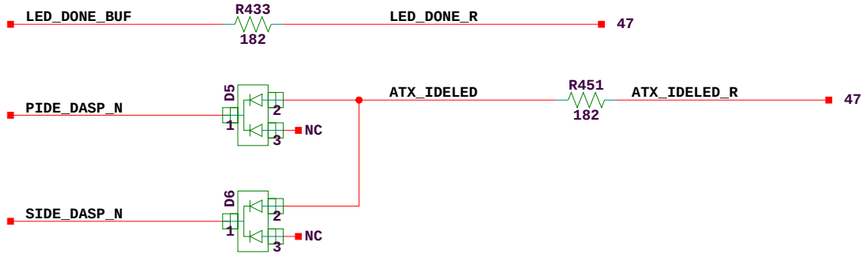

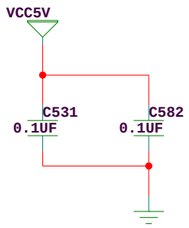

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

ATX AND FRONT PANEL CONNECTORS

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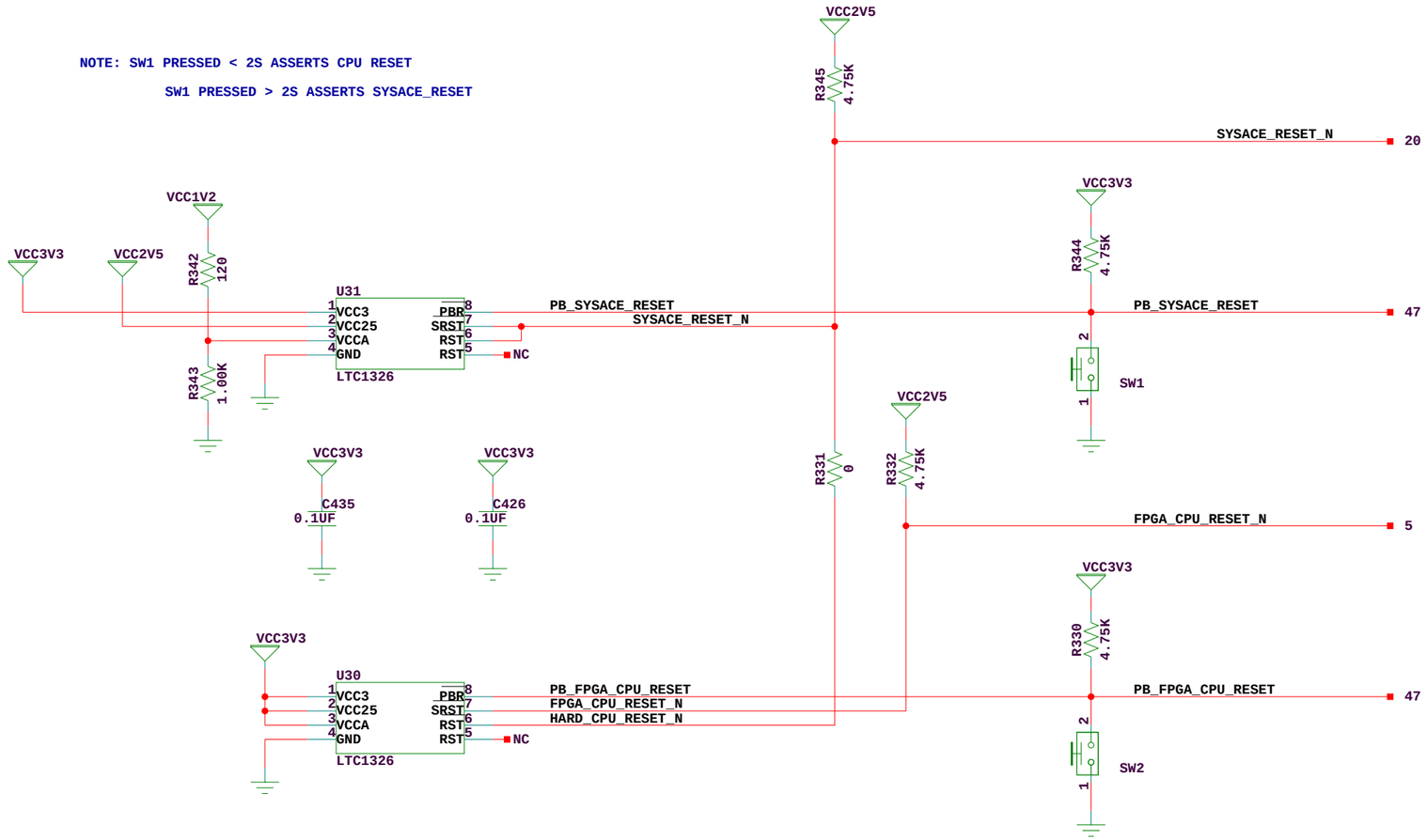
NOTE: SW1 PRESSED < 2S ASSERTS CPU RESET

SW1 PRESSED > 2S ASSERTS SYSACE_RESET



SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

RESET SWITCHES

Date:	8-22-2006_9:52	Ver:	03
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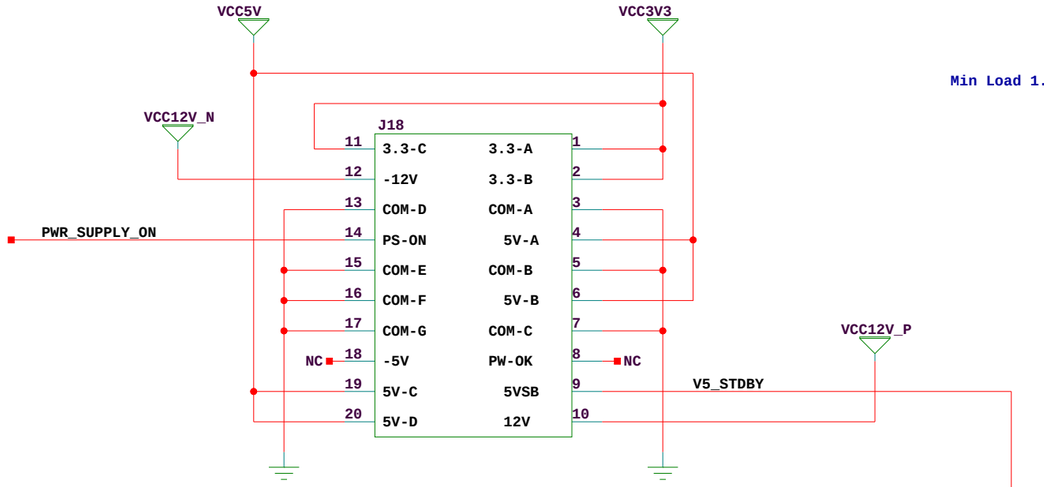
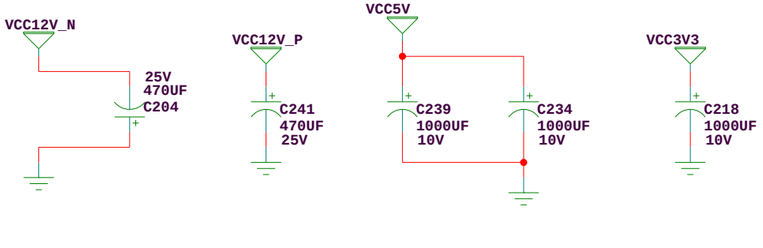
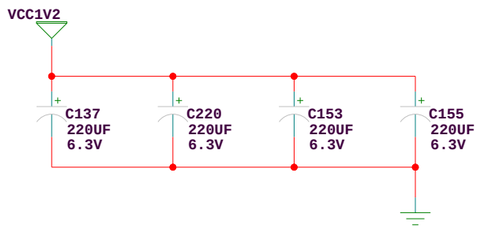
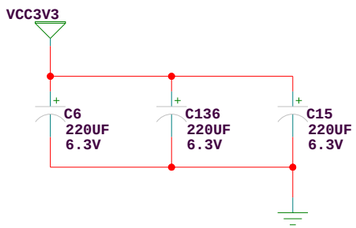
Min Load 1.5A on 5v, 0.8A on 3.3V and 0.5A on 12V

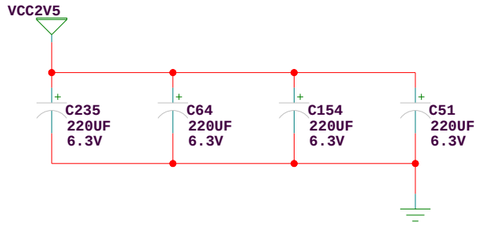


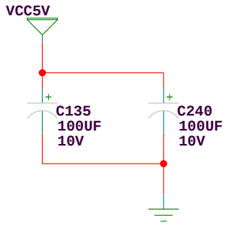


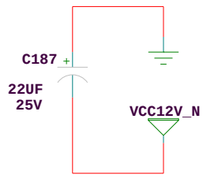
ATX Power Connector





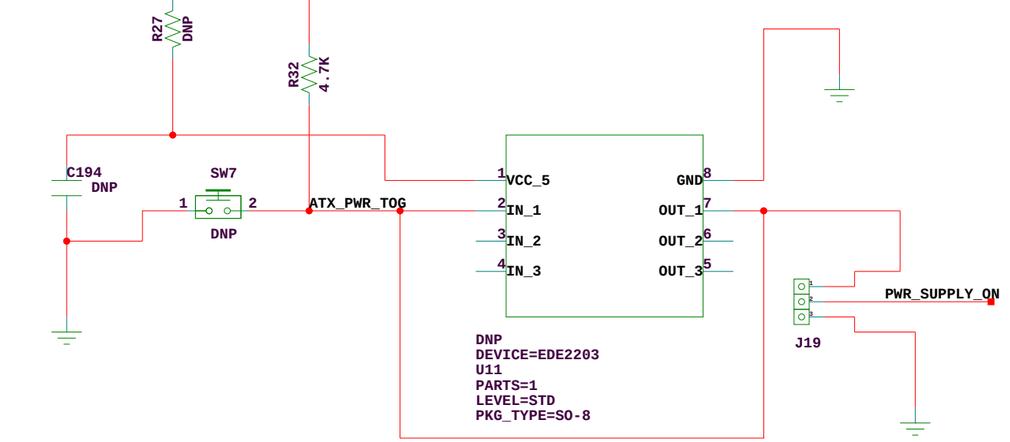






BULK CAPS DISTRIBUTED AROUND BOARD.

Power_ON/OFF Toggle



XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
ATX CONNECTOR, PWR TOGGLE AND HEADER

Date:	8-22-2006_9:52	Ver:	03
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VCCA <= 1V implies ~RST is low
VCCA > 1V implies ~RST is high

VCC1V2 R483 120 R482 1.00K
VCC3V3
U5 LTC1326 (VCC3, VCC25, VCCA, GND, PBR, SRST, RST, RST)
Silkscreen: "VCC 1.2V"
DS8 (RED, GRN) R298 330 R283 330
VCC5V C423 0.1UF

VCC5V C416 0.1UF
VCC5V R280 4.42K R295 1.62K
U28 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 5.0V"
DS7 (RED, GRN) R296 330 R281 330
VCC5V C422 0.1UF

VCC2V5 C401 0.1UF
VCC2V5 R242 1.33K R248 1.62K
U24 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 2.5V"
DS6 (RED, GRN) R249 330 R243 330
VCC5V C410 0.1UF

VTT_DDR2 C400 0.1UF
VTT_DDR2 R132 10
U23 DEVICE=NCP300 (NC1, NC2, RESET, INPUT, GND)
Silkscreen: "VTT_DDR2"
DS5 (RED, GRN) R247 15K R241 120
VCC5V C409 0.1UF

VCC3_PCI C388 0.1UF
VCC3_PCI R196 1.96K R214 1.62K
U18 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 3.0V"
DS4 (RED, GRN) R215 330 R197 330
VCC5V C398 0.1UF

AVCCAUXMGT
2.5V
C387 0.1UF
R194 1.33K R212 1.62K
U17 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "AVCCAUXMGT"
DS3 (RED, GRN) R213 330 R195 330
VCC5V C397 0.1UF

VCC3V3 C360 0.1UF
VCC3V3 R160 2.32K R172 1.62K
U13 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 3.3V"
DS2 (RED, GRN) R173 330 R161 330
VCC5V C367 0.1UF

1.8V
VCC1V8 C359 0.1UF
VCC1V8 R158 523 R170 1.62K
U12 MC34161D (VEF, IN1, IN2, GND, VCC, MODE, OUT1, OUT2)
Silkscreen: "VCC 1.8"
DS1 (RED, GRN) R171 330 R159 330
VCC5V C366 0.1UF

"1.2V" VCC1V2 TP17
"2.5V" VCC2V5 TP14
"VCC3_PCI" VCC3_PCI TP10
"3.3V" VCC3V3 TP8
"5V" VCC5V TP16
"VTT_DDR2" VTT_DDR2 TP13
VCC12V_N TP19
VCC12V_P TP18
"1.8V" VCC1V8 TP7

AVCCAUXMGT TP9

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
POWER SUPPLY MONITORS AND LEDS

Date:	8-22-2006_9:52	Ver:	03
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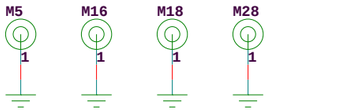
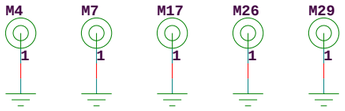
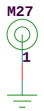
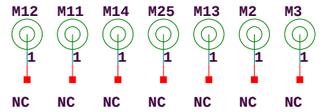
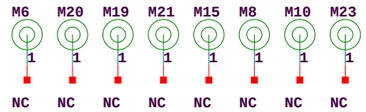
Mounting holes for ATX Form Factor

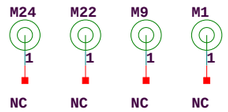




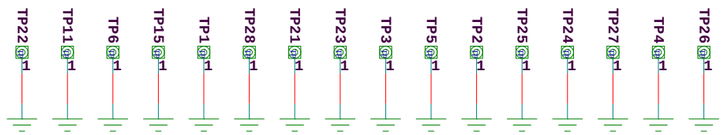






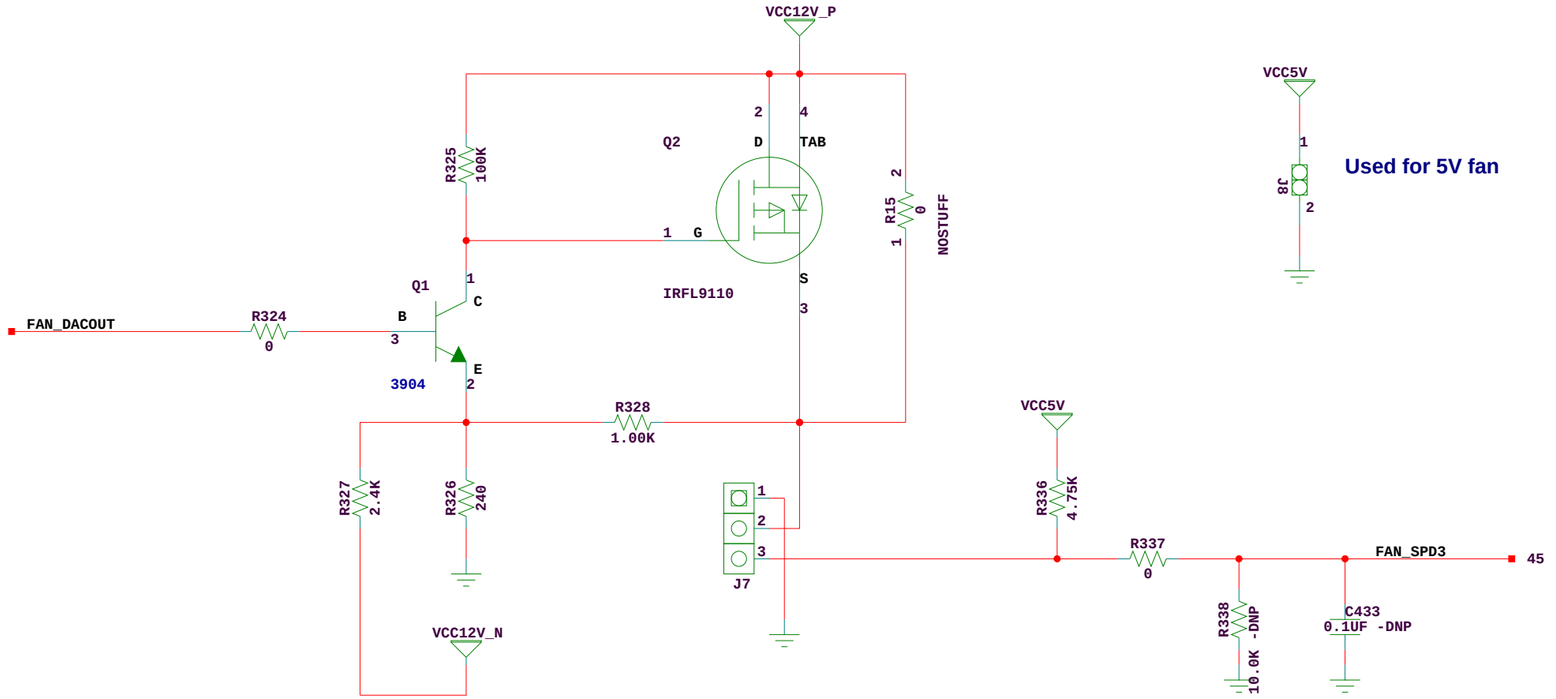


Spread out on the board.



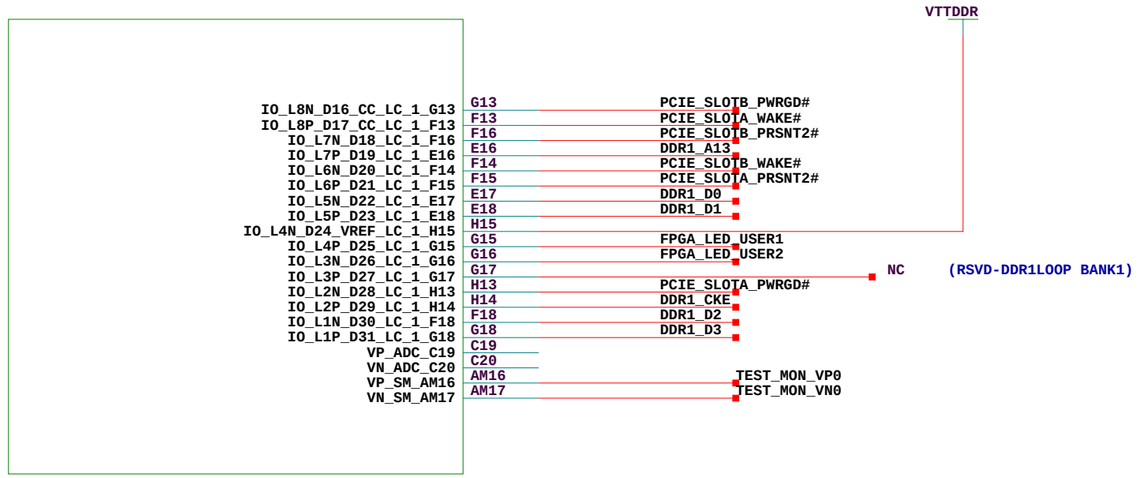
Silkscreen:
"GND"

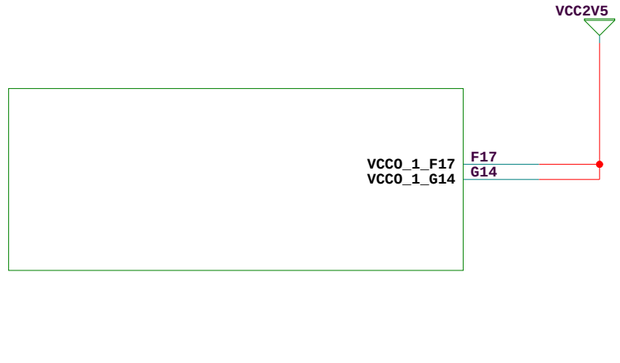
XILINX	SCH P/N 0381203 ART P/N 0531499 FAB P/N 1280372
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM ATX MOUNTING HOLES AND TEST POINTS	
Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 37 of 72	Drawn By SS

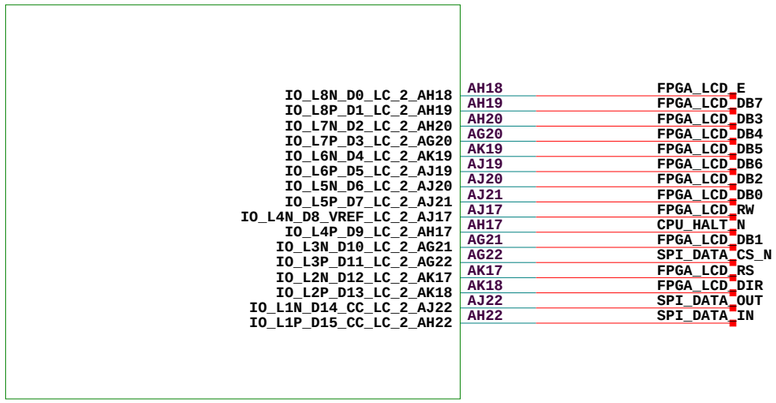


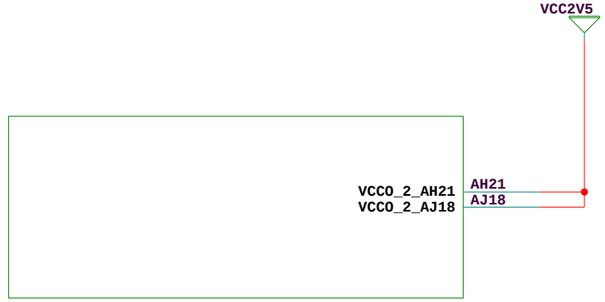
Used for 5V fan

XILINX	SCH P/N	0381203
	ART P/N	0531499
	FAB P/N	1280372
Title:	SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM FPGA FAN SWITCH AND TACH	
Date:	8-22-2006_9:52	Ver: 03
Sheet Size: B		Rev: E
Sheet 38 of 72		Drawn By SS









XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK1,2 - PCI-E CTRL, DDR1, LCD

Date:	8-22-2006_9:52	Ver:	03
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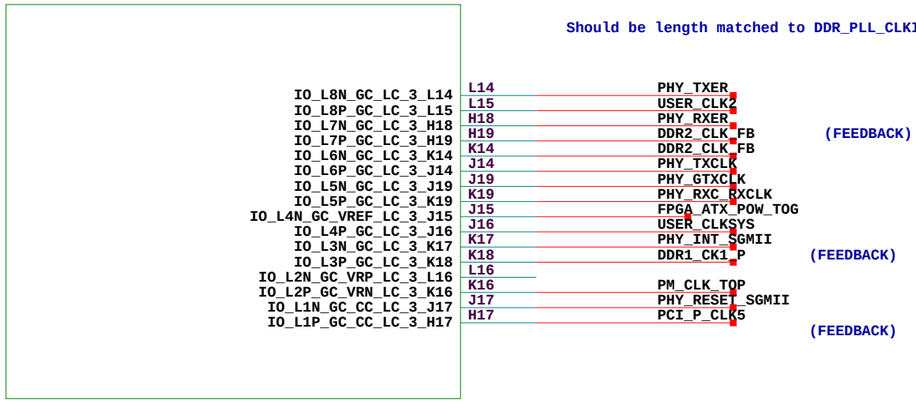
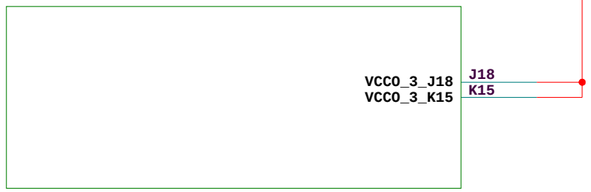
Should be length matched to DDR_PLL_CLKIN



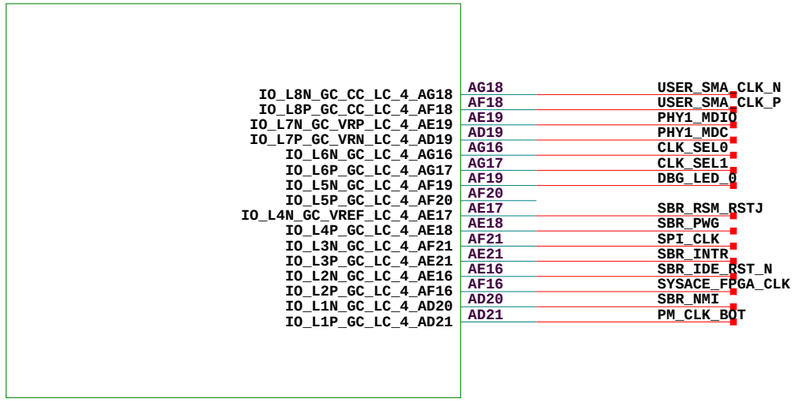
U37

VCC2V5



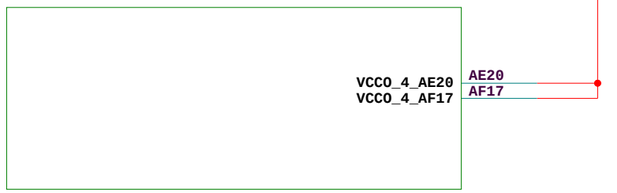
CU37

Feedback nets should be length matched



U37

VCC2V5



U37

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK3,4 - PHY_CTL,USR CLKS, SBR

Date:	8-22-2006_9:52	Ver:	03
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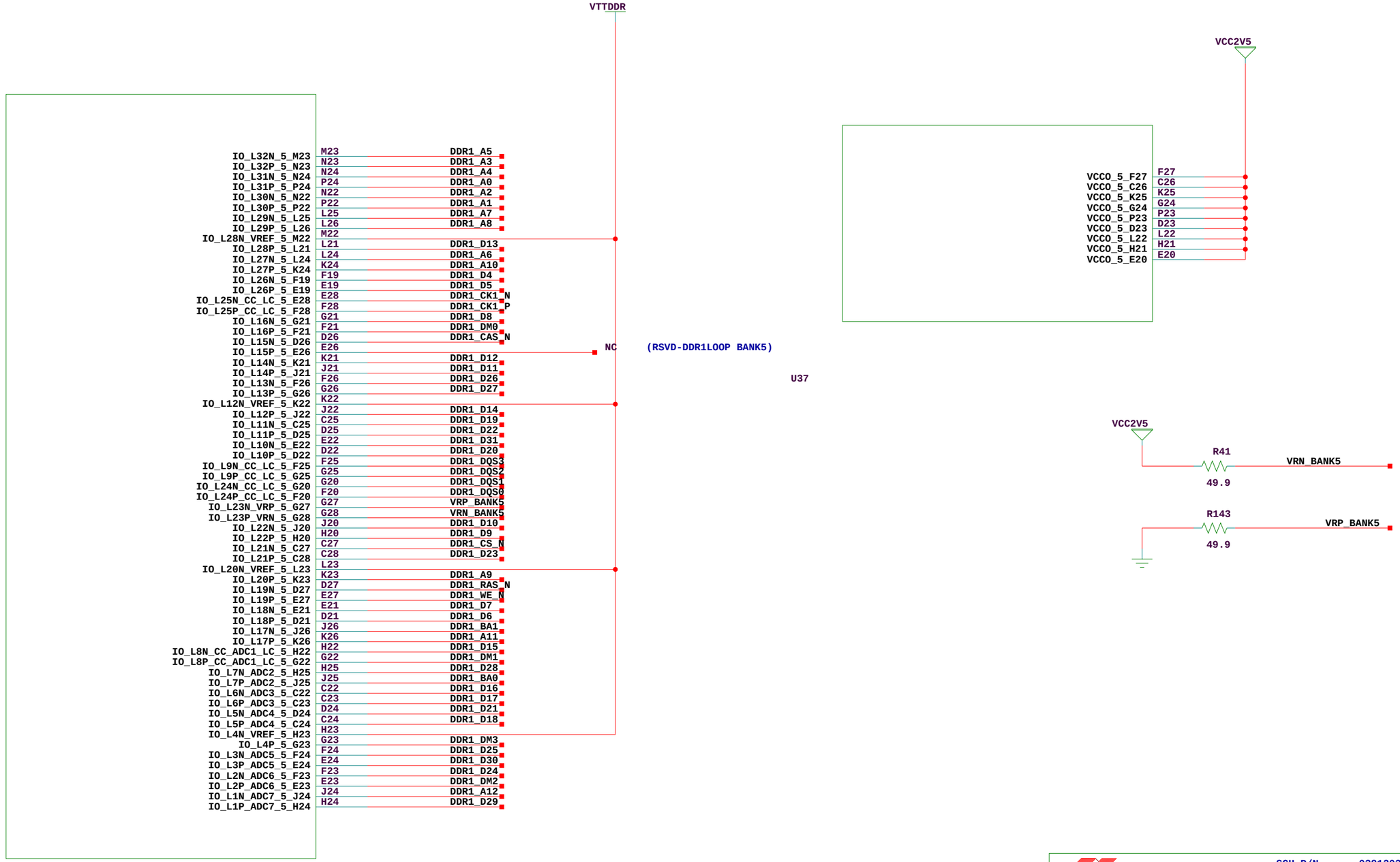

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK5 - DDR1

Date:	8-22-2006_9:52	Ver:	03
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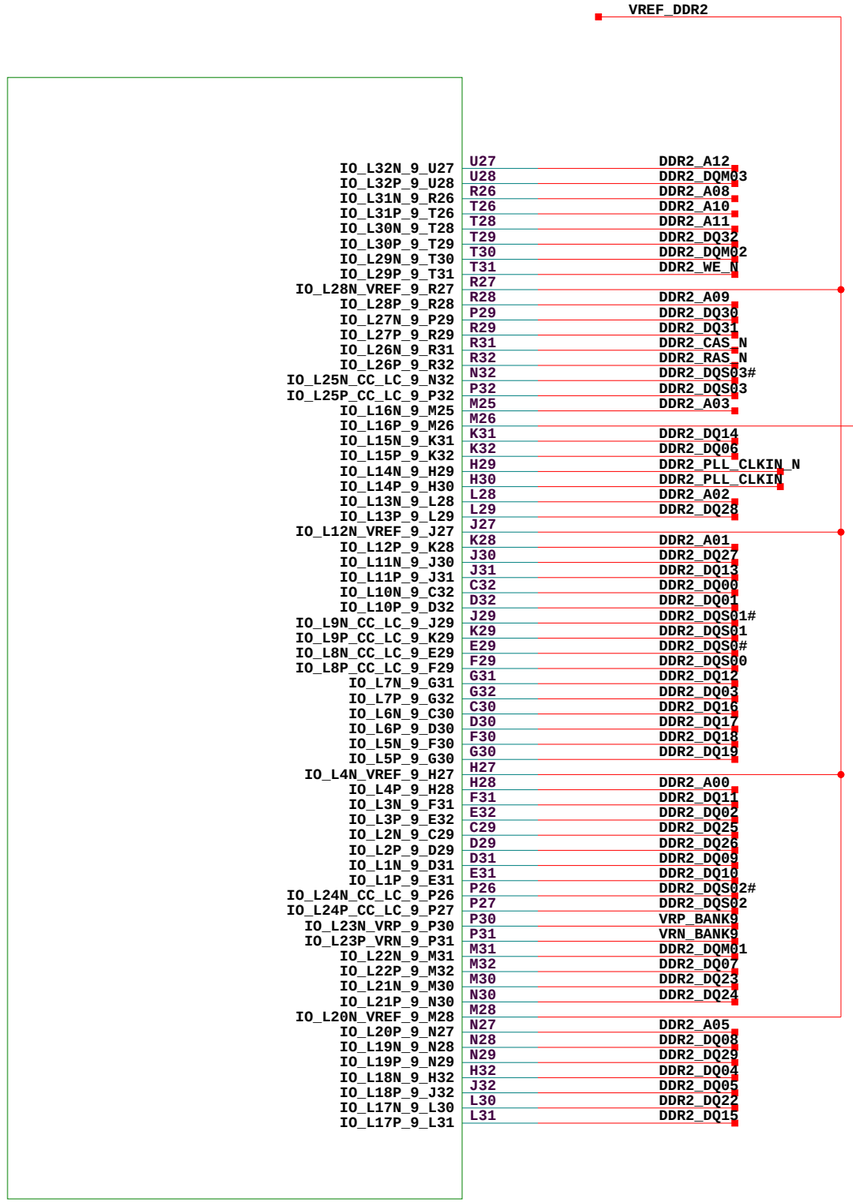

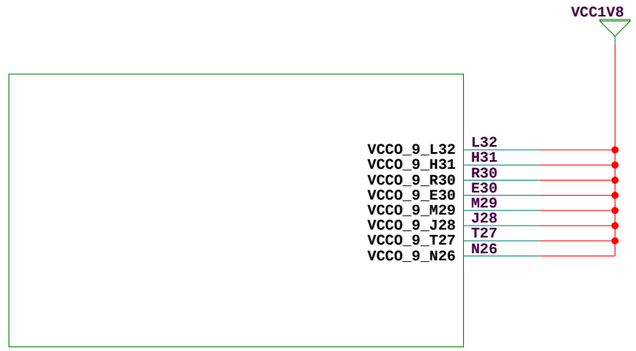

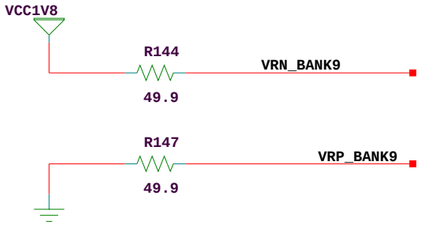

U37

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK9 - DDR2

Date:	8-22-2006_9:52	Ver:	03
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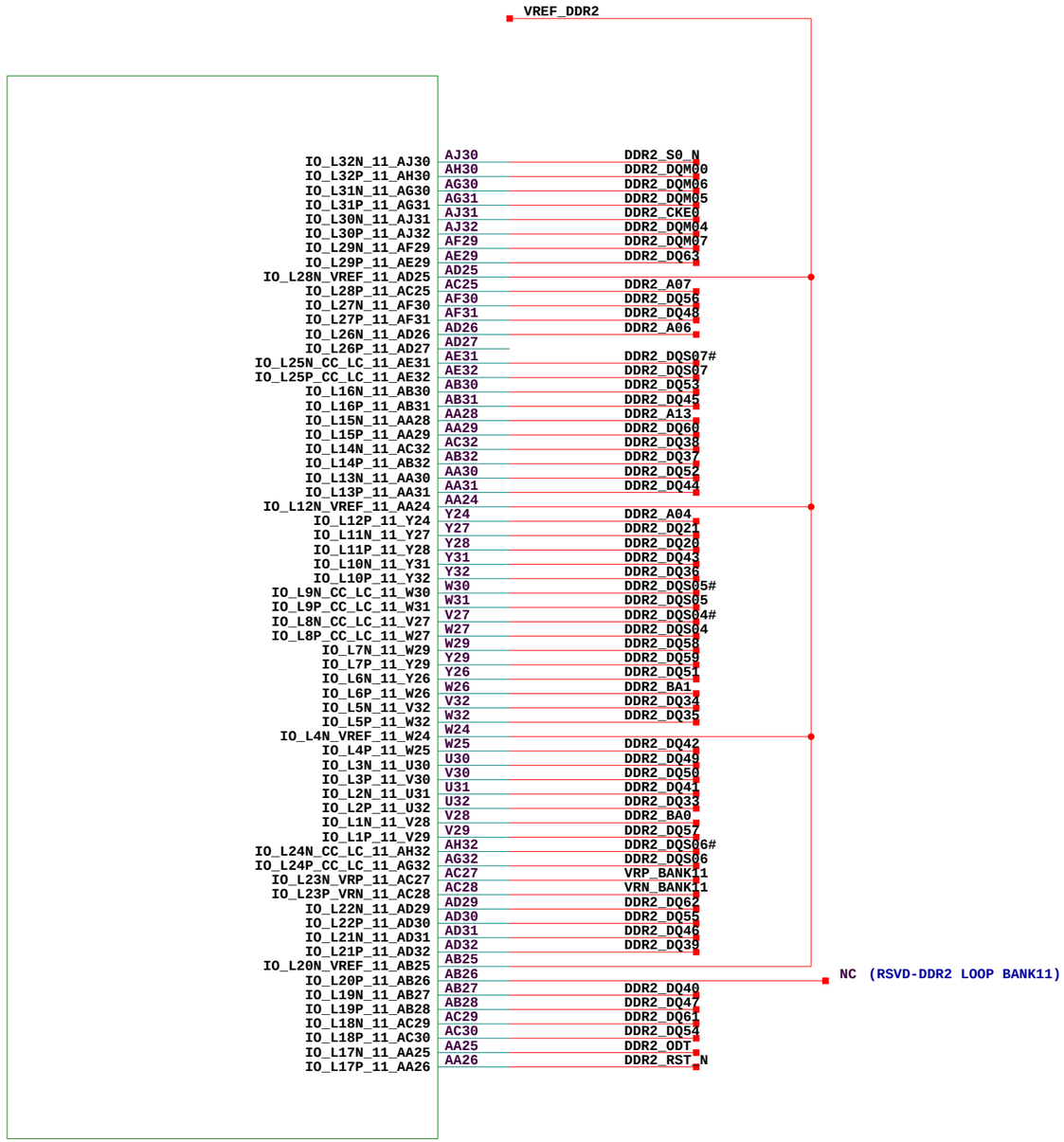
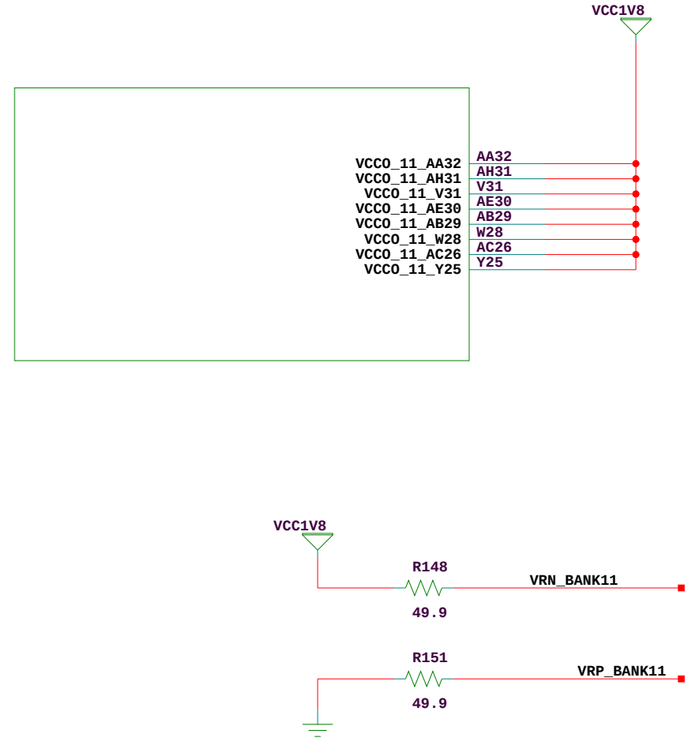
Sheet 42 of 72		Drawn By	SS





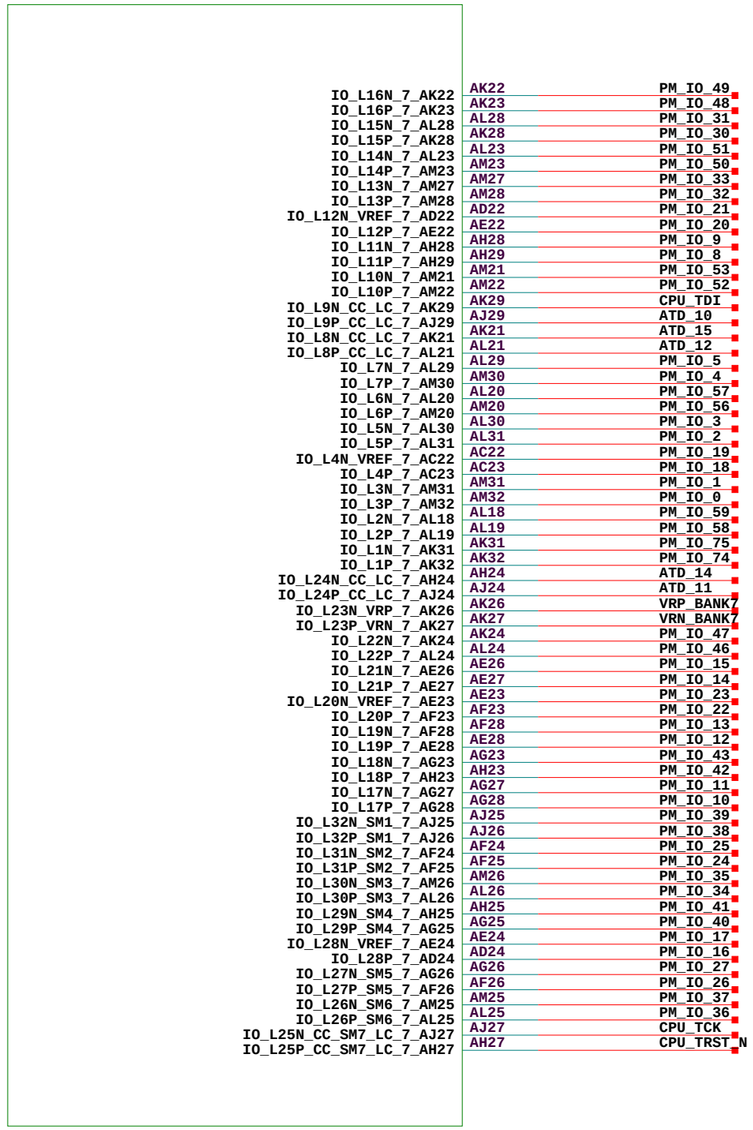
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

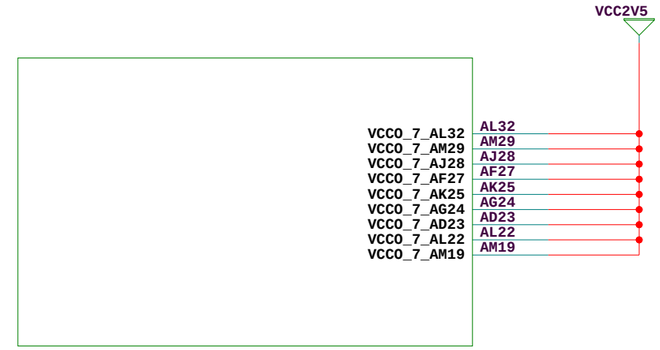
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

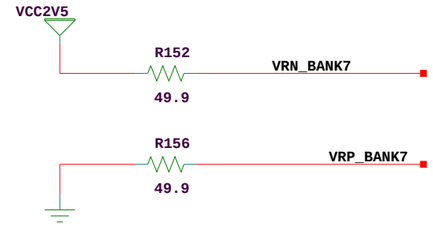
FPGA - BANK11 - DDR2

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 43 of 72	Drawn By SS



U37





U37

XILINX	SCH P/N 0381203 ART P/N 0531499 FAB P/N 1280372		
Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM FPGA - BANK7- PM_IO_*			
Date: 8-22-2006_9:52		Ver: 03	
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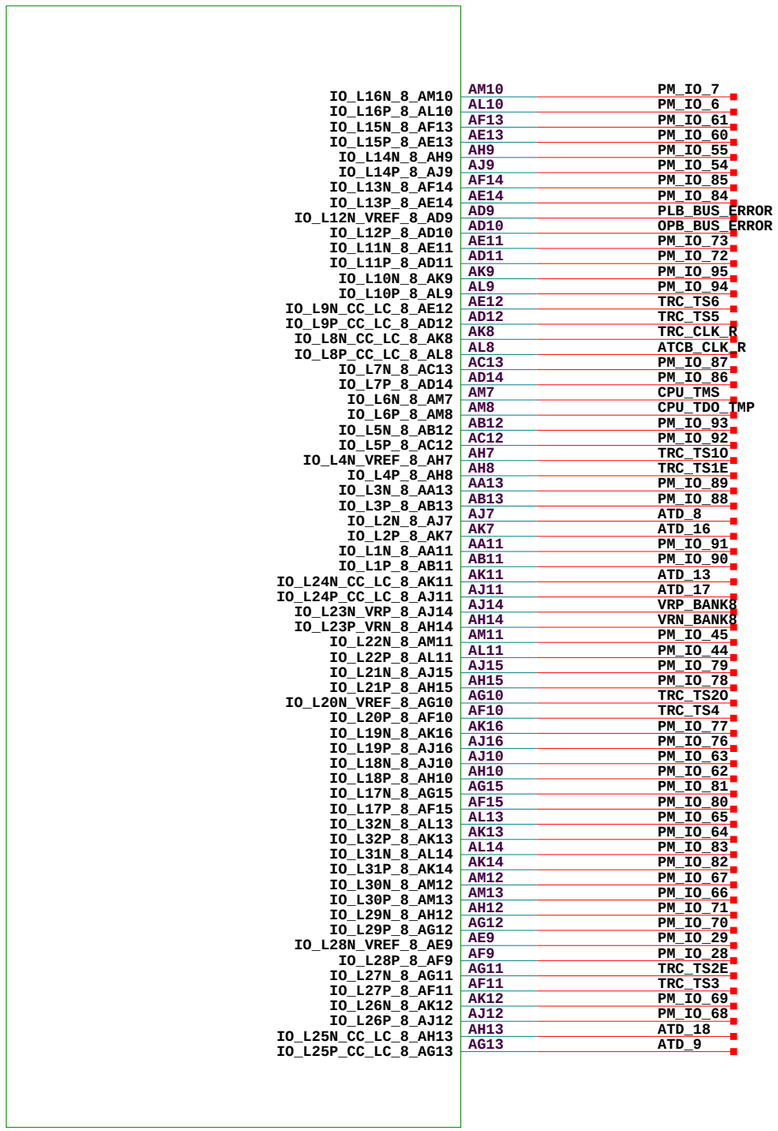
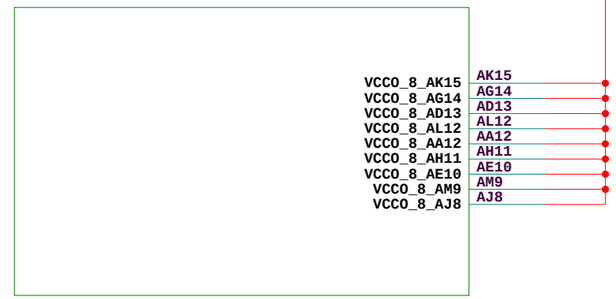
Sheet 44 of 72		Drawn By SS	



U37



U37

VCC2V5

VCC2V5

R157

49.9

VRN_BANK8

R165

49.9

VRP_BANK8

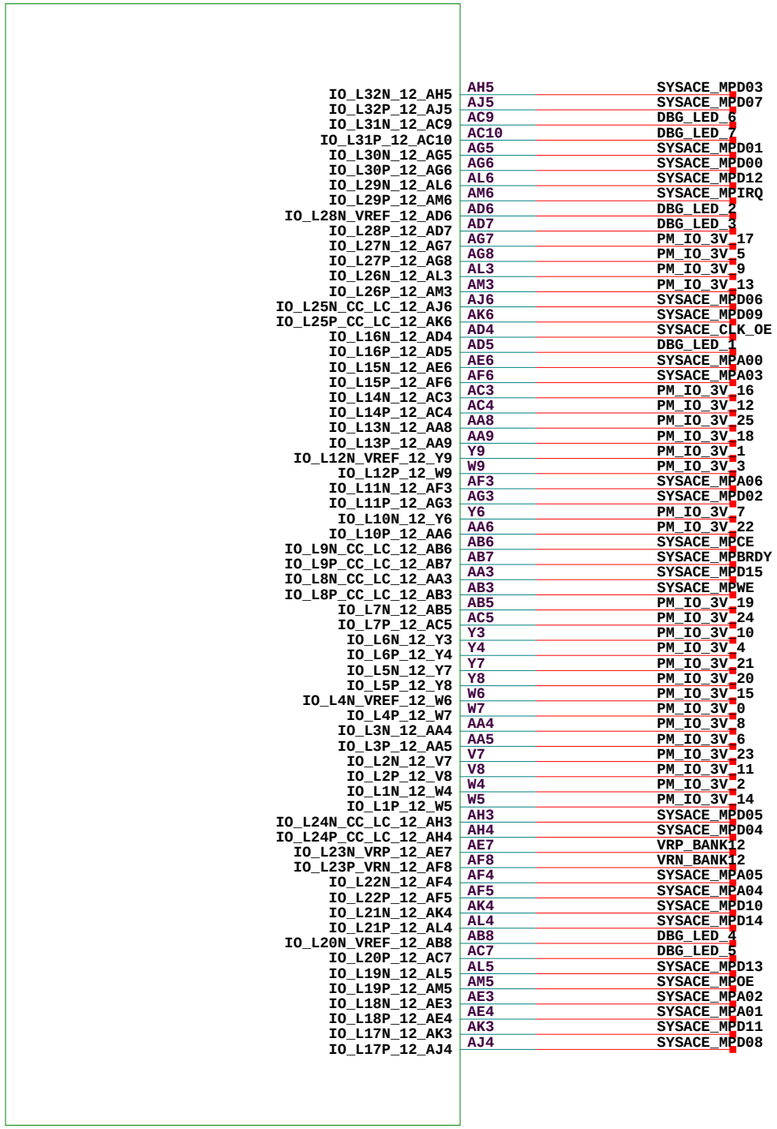
XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK8 - PM_IO,MICTOR, CPU_DEBUG

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
Sheet	45 of 72	Drawn By	SS



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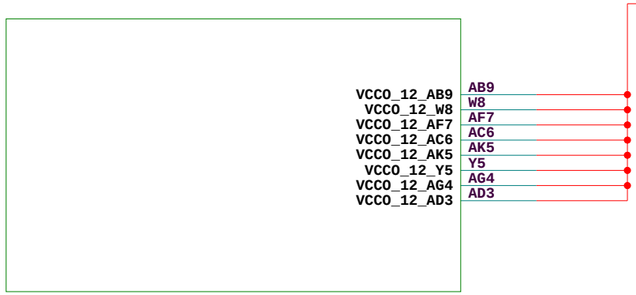
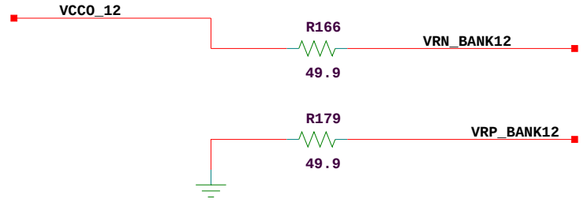
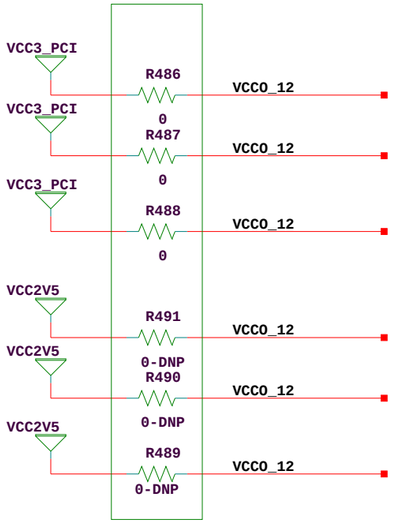


U37





XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK12 - SYSACE, PM_IO_3,DBG_LED

Date:	8-22-2006_9:52	Ver:	03
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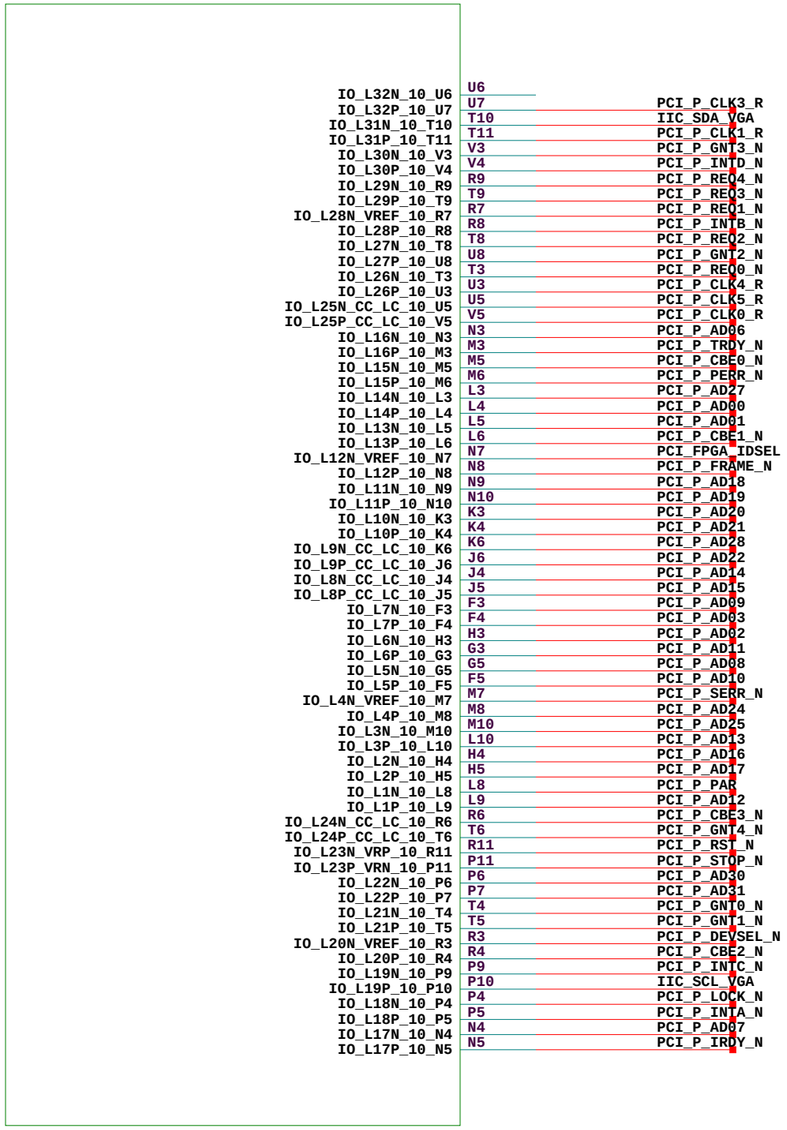
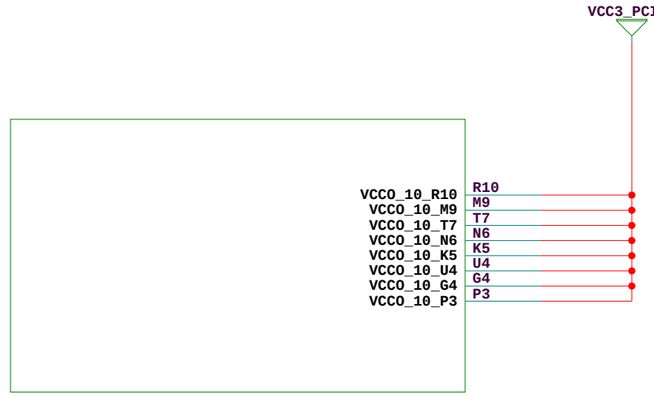
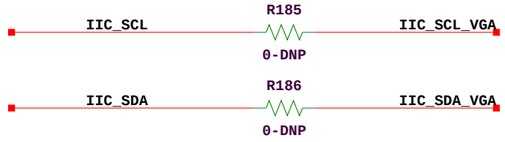


U37



U37



XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA - BANK10 - PCI

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
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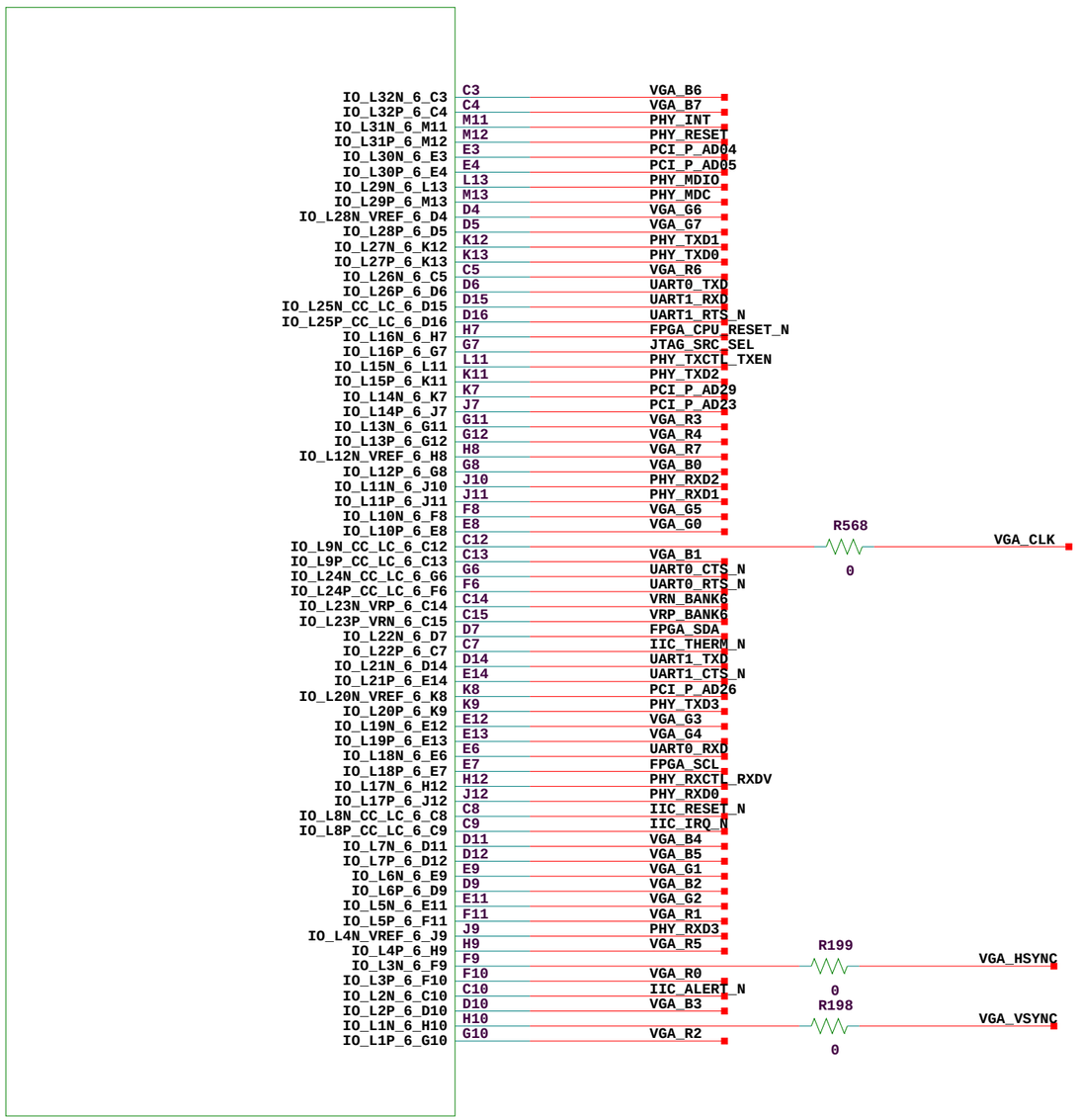

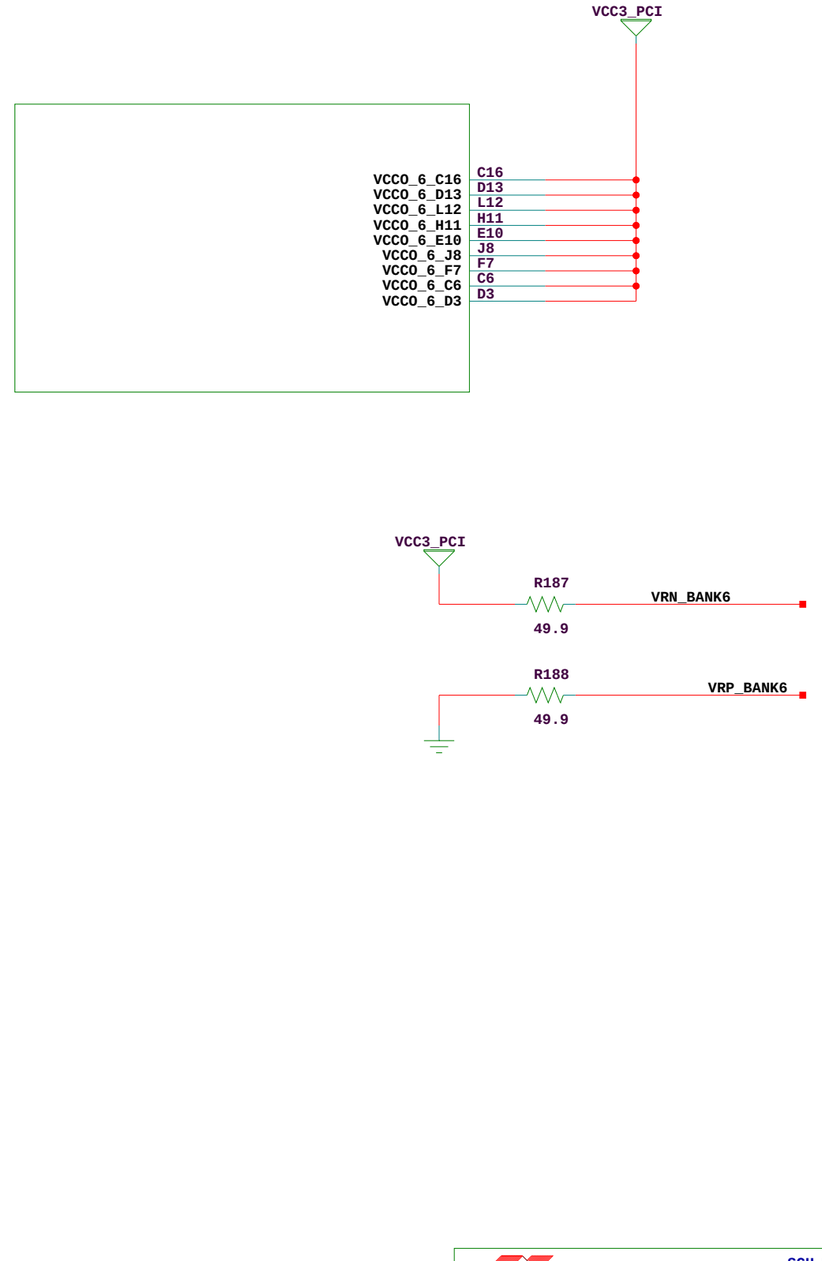

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA-BANK6, VGA, UART, PHY

Date:	8-22-2006_9:52	Ver:	03
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U37

VTRXB_101_A27	A27 MGT_101_VTRXB
AVCCAUXRXB_101_B30	B30 MGT_101_AVCCAUXRXB
VTTXB_101_B26	B26 MGT_101_VTTXB
AVCCAUXMGT_101_B28	B28 MGT_101_AVCCAUX
AVCCAUXTX_101_B25	B25 MGT_101_AVCCAUXTX
VTTXA_101_B23	B23 MGT_101_VTTXA
AVCCAUXRXA_101_B21	B21 MGT_101_AVCCAUXRXA
VTRXA_101_A22	A22 MGT_101_VTRXA

U37

VTRXB_102_H34	H34 MGT_102_VTRXB
AVCCAUXRXB_102_K33	K33 MGT_102_AVCCAUXRXB
VTTXB_102_G33	G33 MGT_102_VTTXB
AVCCAUXMGT_102_J33	J33 MGT_102_AVCCAUX
AVCCAUXTX_102_F33	F33 MGT_102_AVCCAUXTX
VTTXA_102_D33	D33 MGT_102_VTTXA
AVCCAUXRXA_102_B32	B32 MGT_102_AVCCAUXRXA
VTRXA_102_C34	C34 MGT_102_VTRXA

U37

VTRXB_103_AB34	AB34 MGT_103_VTRXB
AVCCAUXRXB_103_AE33	AE33 MGT_103_AVCCAUXRXB
VTTXB_103_AA33	AA33 MGT_103_VTTXB
AVCCAUXMGT_103_AC33	AC33 MGT_103_AVCCAUX
AVCCAUXTX_103_Y33	Y33 MGT_103_AVCCAUXTX
VTTXA_103_V33	V33 MGT_103_VTTXA
AVCCAUXRXA_103_T33	T33 MGT_103_AVCCAUXRXA
VTRXA_103_U34	U34 MGT_103_VTRXA

U37

TXNPADA_101_C	C8181 10NF 2	TXNPADA_101	
TXPPADA_101_C	C8191 10NF 2	TXPPADA_101	
TXNPADB_101_C	C8161 10NF 2	TXNPADB_101	
TXPPADB_101_C	C8171 10NF 2	TXPPADB_101	
TXNPADA_102_C	C8101 10NF 2	TXNPADA_102	
TXPPADA_102_C	C8111 10NF 2	TXPPADA_102	
TXNPADA_103_C	C8121 10NF 2	TXNPADA_103	
TXPPADA_103_C	C8131 10NF 2	TXPPADA_103	
TXNPADB_103_C	C8141 10NF 2	TXNPADB_103	
TXPPADB_103_C	C8151 10NF 2	TXPPADB_103	

Available only on FX100

4x PCIE_SLOTB

U37

RXNPADB_101_A29	A29	RXNPADB_101
RXPPADB_101_A28	A28	RXPPADB_101
TXNPADB_101_A26	A26	TXNPADB_101_C
TXPPADB_101_A25	A25	TXPPADB_101_C
TXNPADA_101_A24	A24	TXNPADA_101_C
TXPPADA_101_A23	A23	TXPPADA_101_C
RXNPADA_101_A21	A21	RXNPADA_101
RXPPADA_101_A20	A20	RXPPADA_101

U37

MGTCLK_N_102_N34	N34	SGMIICLK_NQO
MGTCLK_P_102_M34	M34	SGMIICLK_QO
RXNPADB_102_K34	K34	RXNPADB_102
RXPPADB_102_J34	J34	RXPPADB_102
TXNPADB_102_G34	G34	TXNPADB_102
TXPPADB_102_F34	F34	TXPPADB_102
TXNPADA_102_E34	E34	TXNPADA_102_C
TXPPADA_102_D34	D34	TXPPADA_102_C
RXNPADA_102_A32	A32	RXNPADA_102
RXPPADA_102_A31	A31	RXPPADA_102

SGMII

1X PCIE_SLOTB

U37

4X PCIE_SLOTA

RXNPADB_103_AD34	AD34	RXNPADB_103
RXPPADB_103_AC34	AC34	RXPPADB_103
TXNPADB_103_AA34	AA34	TXNPADB_103_C
TXPPADB_103_Y34	Y34	TXPPADB_103_C
TXNPADA_103_W34	W34	TXNPADA_103_C
TXPPADA_103_V34	V34	TXPPADA_103_C
RXNPADA_103_T34	T34	RXNPADA_103
RXPPADA_103_R34	R34	RXPPADA_103

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT 101, 102 AND 103 - SGMII, PCIE-A & B

Date:	8-22-2006_9:52	Ver:	03
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SATA Clock

4X PCIE_SLOTA

U37

MGTCLK_N_105_AP28	AP28	SATACLK_N00
MGTCLK_P_105_AP29	AP29	SATACLK_00
RXNPADB_105_AP31	AP31	RXNPADB_105
RXPPADB_105_AP32	AP32	RXPPADB_105
TXNPADB_105_AM34	AM34	TXNPADB_105_C
TXPPADB_105_AL34	AL34	TXPPADB_105_C
TXNPADA_105_AK34	AK34	TXNPADA_105_C
TXPPADA_105_AJ34	AJ34	TXPPADA_105_C
RXNPADA_105_AG34	AG34	RXNPADA_105
RXPPADA_105_AF34	AF34	RXPPADA_105

U37

MGTVREF_105_AN27	AN27	MGTVREF_105
RTERM_105_AN29	AN29	MGT_RTERM_105
VTRXB_105_AN33	AN33	MGT_105_VTRXB
AVCCAUXRXB_105_AN31	AN31	MGT_105_AVCCAUXRXB
VTTXB_105_AM33	AM33	MGT_105_VTTXB
AVCCAUXMGT_105_AN32	AN32	MGT_105_AVCCAUX
AVCCAUXTX_105_AL33	AL33	MGT_105_AVCCAUXTX
VTTXA_105_AJ33	AJ33	MGT_105_VTTXA
AVCCAUXRXA_105_AG33	AG33	MGT_105_AVCCAUXRXA
VTRXA_105_AH34	AH34	MGT_105_VTRXA

U37

RXNPADB_106_AP17	AP17	RXNPADB_106
RXPPADB_106_AP18	AP18	RXPPADB_106
TXNPADB_106_AP20	AP20	TXNPADB_106
TXPPADB_106_AP21	AP21	TXPPADB_106
TXNPADA_106_AP22	AP22	TXNPADA_106
TXPPADA_106_AP23	AP23	TXPPADA_106
RXNPADA_106_AP25	AP25	RXNPADA_106
RXPPADA_106_AP26	AP26	RXPPADA_106

SATA

U37

VTRXB_106_AP19	AP19	MGT_106_VTRXB
AVCCAUXRXB_106_AN17	AN17	MGT_106_AVCCAUXRXB
VTTXB_106_AN20	AN20	MGT_106_VTTXB
AVCCAUXMGT_106_AN18	AN18	MGT_106_AVCCAUX
AVCCAUXTX_106_AN22	AN22	MGT_106_AVCCAUXTX
VTTXA_106_AN23	AN23	MGT_106_VTTXA
AVCCAUXRXA_106_AN25	AN25	MGT_106_AVCCAUXRXA
VTRXA_106_AP24	AP24	MGT_106_VTRXA

U37

RXNPADB_109_AP15	AP15	RXNPADB_109
RXPPADB_109_AP14	AP14	RXPPADB_109
TXNPADB_109_AP12	AP12	TXNPADB_109
TXPPADB_109_AP11	AP11	TXPPADB_109
TXNPADA_109_AP10	AP10	TXNPADA_109
TXPPADA_109_AP9	AP9	TXPPADA_109
RXNPADA_109_AP7	AP7	RXNPADA_109
RXPPADA_109_AP6	AP6	RXPPADA_109

PM

U37

VTRXB_109_AP13	AP13	MGT_109_VTRXB	
AVCCAUXRXB_109_AN15	AN15	MGT_109_AVCCAUXRXB	
VTTXB_109_AN12	AN12	MGT_109_VTTXB	
AVCCAUXMGT_109_AN14	AN14	MGT_109_AVCCAUX	
AVCCAUXTX_109_AN10	AN10	MGT_109_AVCCAUXTX	
VTTXA_109_AN9	AN9	MGT_109_VTTXA	
AVCCAUXRXA_109_AN7	AN7	MGT_109_AVCCAUXRXA	
VTRXA_109_AP8	AP8	MGT_109_VTRXA	

U37

TXNPADA_105_C	C8221 10NF	2	TXNPADA_105
TXPPADA_105_C	C8231 10NF	2	TXPPADA_105
TXNPADB_105_C	C8201 10NF	2	TXNPADB_105
TXPPADB_105_C	C8211 10NF	2	TXPPADB_105

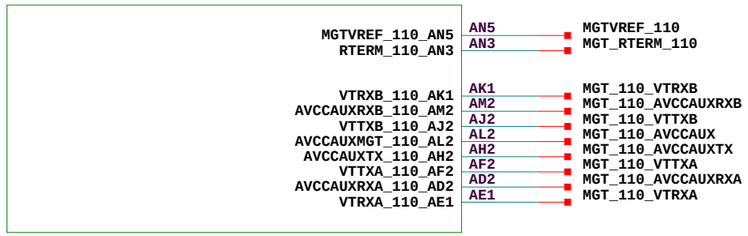
XILINX

SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT 105, 106 AND 109 - PM, SATA+CLK, PCIE

Date: 8-22-2006_9:52	Ver: 03
Sheet Size: B	Rev: E
Sheet 50 of 72	Drawn By SS



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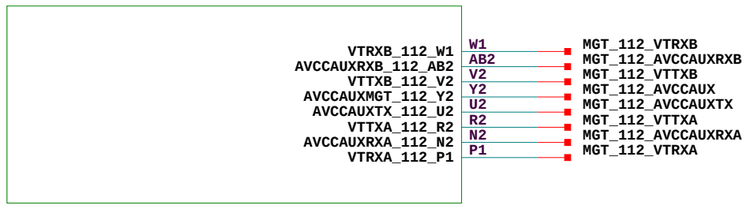

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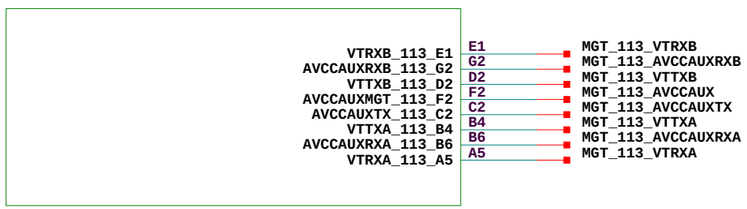

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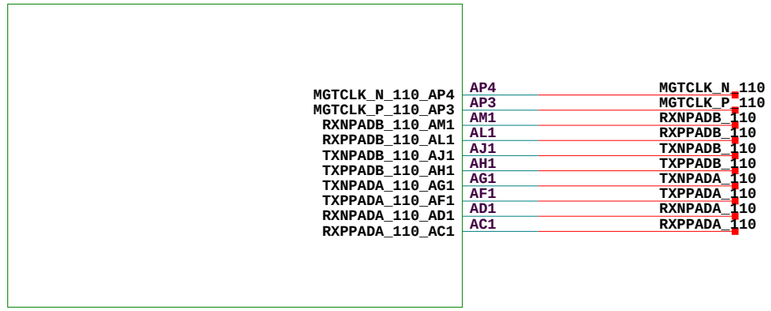

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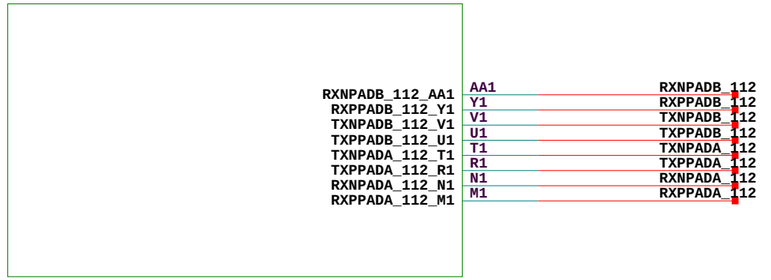

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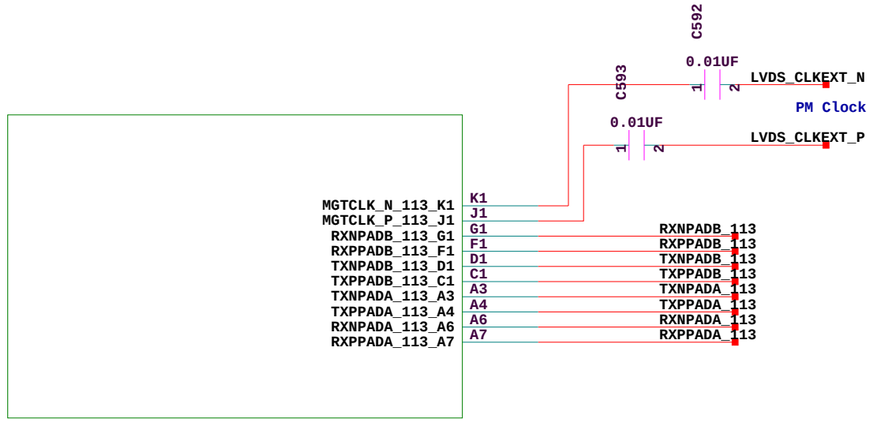

U37

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT - 110 , 112 AND 113

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Available only on FX100

4x PCIE_SLOTB

U37

RXNPADB_114_A9	A9	RXNPADB_114
RXPPADB_114_A10	A10	RXPPADB_114
TXNPADB_114_A12	A12	TXNPADB_114_C
TXPPADB_114_A13	A13	TXPPADB_114_C
TXNPADA_114_A14	A14	TXNPADA_114
TXPPADA_114_A15	A15	TXPPADA_114
RXNPADA_114_A17	A17	RXNPADA_114
RXPPADA_114_A18	A18	RXPPADA_114

Unused

U37

VTRXB_114_A11	A11	MGT_114_VTRXB
AVCCAUXRXB_114_B8	B8	MGT_114_AVCCAUXRXB
VTTXB_114_B12	B12	MGT_114_VTTXB
AVCCAUXMGT_114_B10	B10	MGT_114_AVCCAUX
AVCCAUXTX_114_B13	B13	MGT_114_AVCCAUXTX
VTTXA_114_B15	B15	MGT_114_VTTXA
AVCCAUXRXA_114_B17	B17	MGT_114_AVCCAUXRXA
VTRXA_114_A16	A16	MGT_114_VTRXA

U37

TXNPADB_114_C — C8241 10NF — 2 — TXNPADB_114

TXPPADB_114_C — C8251 10NF — 2 — TXPPADB_114

VCC2V5

U37

VCCO_0_R20	R20
VCCO_0_W18	W18
VCCO_0_T17	T17
VCCO_0_Y15	Y15

U37

AVSS_ADC_C18	C18	
AVDD_ADC_D18	D18	
VREFP_ADC_D19	D19	
VREFN_ADC_D20	D20	
AVSS_SM_AM15	AM15	
AVDD_SM_AL15	AL15	TEST_MON_AVDD
VREFP_SM_AL16	AL16	TEST_MON_VREFP
VREFN_SM_AL17	AL17	

U37

Should be routed differentially

TDP_0_C17	C17	FPGA_DXP
TDN_0_D17	D17	FPGA_DXN
TDI_0_AA15	AA15	FPGA_TDI
DOUT_BUSY_0_Y18	Y18	
M1_0_W19	W19	FPGA_MODE_1
TCK_0_AA14	AA14	FPGA_TCK
TDO_0_W17	W17	FPGA_TDO
M0_0_V18	V18	FPGA_MODE_0
TMS_0_Y14	Y14	FPGA_TMS
PWRDWN_B_0_AA16	AA16	FPGA_PWRDWN_B
M2_0_T20	T20	FPGA_MODE_2
VBATT_0_R21	R21	FPGA_VBATT
RDWR_B_0_W15	W15	
DONE_0_R19	R19	FPGA_DONE
CS_B_0_T16	T16	
INIT_0_P19	P19	FPGA_INIT
PROGRAM_B_0_P21	P21	FPGA_PROG_B
D_IN_0_R17	R17	
CCLK_0_T18	T18	FPGA_CCLK
HSWAPEN_0_P20	P20	FPGA_HSWAP

R206 4.7K (1–2) — R244 4.7K (1–2) — R257 4.7K (1–2)

FPGA_VBATT — C534 0.1UF

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT_114, VCCO_0, CONFIG,MISC

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VCC2V5

VCCAUX_K27	K27
VCCAUX_U26	U26
VCCAUX_N25	N25
VCCAUX_V24	V24
VCCAUX_AB22	AB22
VCCAUX_W21	W21
VCCAUX_AC19	AC19
VCCAUX_V19	V19
VCCAUX_N19	N19
VCCAUX_L19	L19
VCCAUX_AD16	AD16
VCCAUX_AB16	AB16
VCCAUX_U16	U16
VCCAUX_M16	M16
VCCAUX_T14	T14
VCCAUX_N13	N13
VCCAUX_U11	U11
VCCAUX_AB10	AB10
VCCAUX_V9	V9
VCCAUX_AE8	AE8

U37

VCC1V2

VCCINT_M27	M27
VCCINT_V25	V25
VCCINT_T25	T25
VCCINT_P25	P25
VCCINT_AC24	AC24
VCCINT_U24	U24
VCCINT_R24	R24
VCCINT_AB23	AB23
VCCINT_Y23	Y23
VCCINT_V23	V23
VCCINT_T23	T23
VCCINT_AA22	AA22
VCCINT_W22	W22
VCCINT_U22	U22
VCCINT_R22	R22
VCCINT_AB21	AB21
VCCINT_Y21	Y21
VCCINT_V21	V21
VCCINT_T21	T21
VCCINT_M21	M21
VCCINT_AC20	AC20
VCCINT_AA20	AA20
VCCINT_W20	W20
VCCINT_U20	U20
VCCINT_N20	N20
VCCINT_L20	L20
VCCINT_AB19	AB19
VCCINT_Y19	Y19
VCCINT_T19	T19
VCCINT_M19	M19
VCCINT_AC18	AC18
VCCINT_AA18	AA18
VCCINT_U18	U18
VCCINT_R18	R18
VCCINT_N18	N18
VCCINT_L18	L18
VCCINT_AD17	AD17
VCCINT_AB17	AB17
VCCINT_Y17	Y17
VCCINT_V17	V17
VCCINT_P17	P17
VCCINT_M17	M17
VCCINT_AC16	AC16
VCCINT_W16	W16
VCCINT_R16	R16
VCCINT_N16	N16
VCCINT_AD15	AD15
VCCINT_AB15	AB15
VCCINT_V15	V15
VCCINT_T15	T15
VCCINT_P15	P15
VCCINT_M15	M15
VCCINT_AC14	AC14
VCCINT_W14	W14
VCCINT_U14	U14
VCCINT_R14	R14
VCCINT_N14	N14
VCCINT_Y13	Y13
VCCINT_V13	V13
VCCINT_T13	T13
VCCINT_P13	P13
VCCINT_W12	W12
VCCINT_U12	U12
VCCINT_R12	R12
VCCINT_N12	N12
VCCINT_Y11	Y11
VCCINT_V11	V11
VCCINT_AA10	AA10
VCCINT_W10	W10
VCCINT_U10	U10
VCCINT_AC8	AC8

U37

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA CORE AND VCCAUX PINS

Date:	8-22-2006_9:52	Ver:	03
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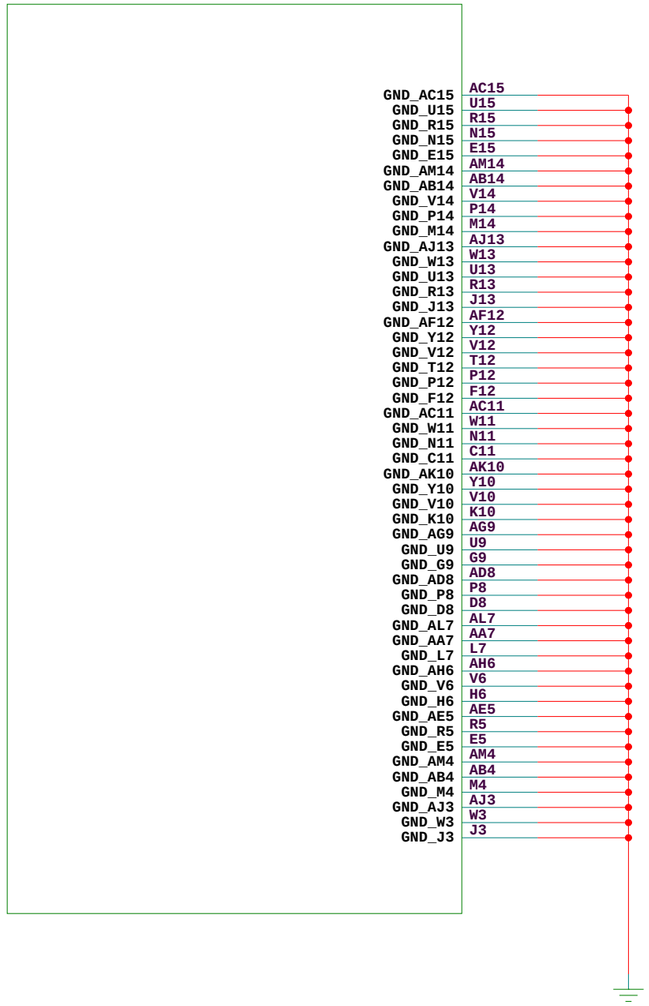

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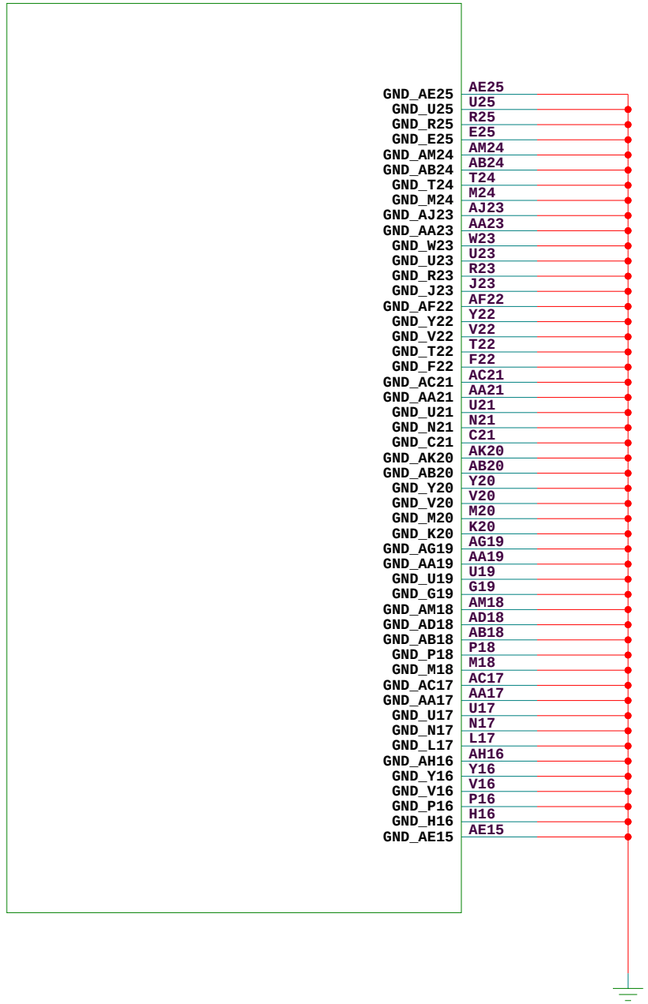

U37

XILINX

SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA GROUND PINS

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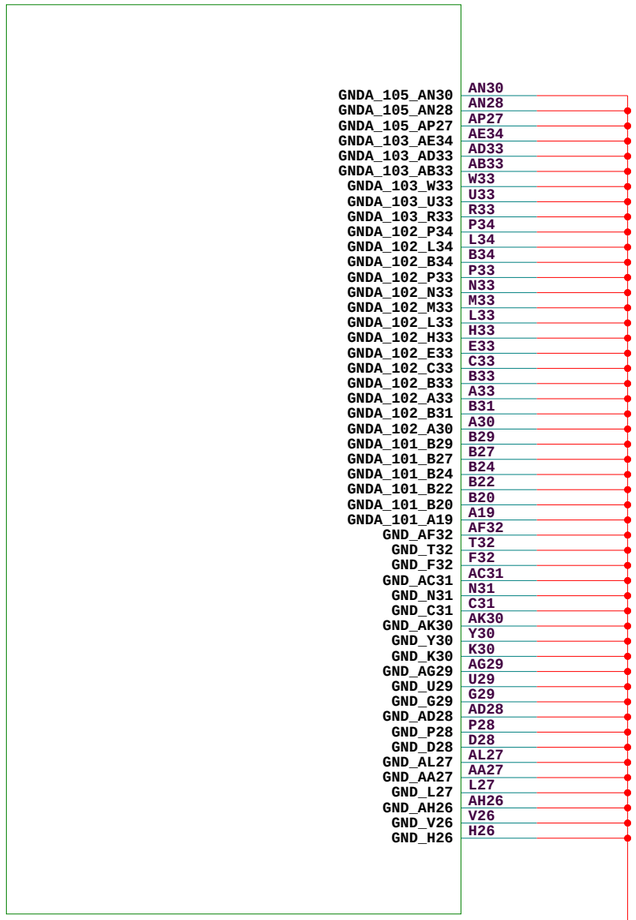

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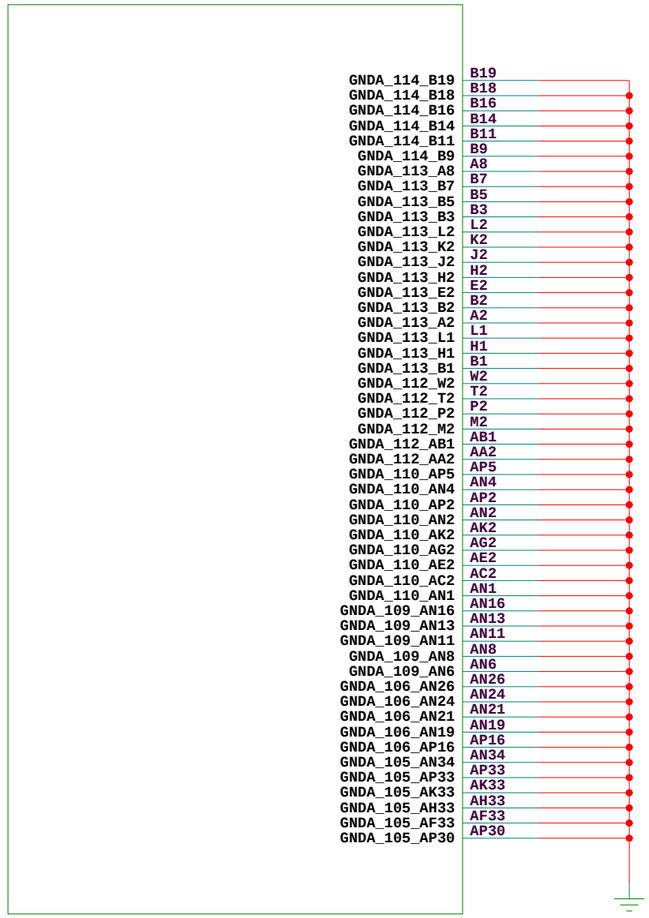

U37

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

FPGA GROUND PINS

Date:	8-22-2006_9:52	Ver:	03
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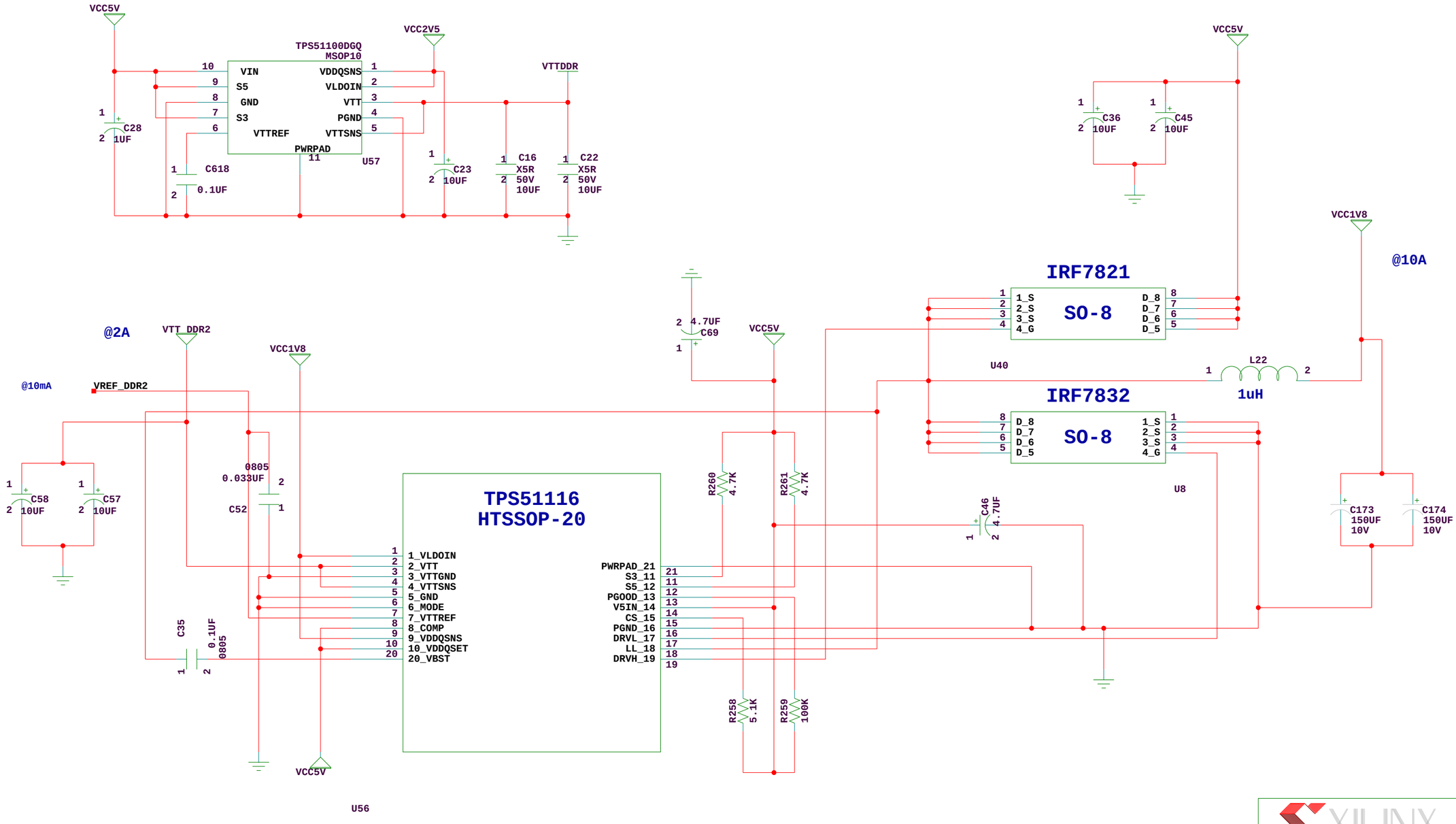

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

DDR1 AND DDR2 POWER SUPPLIES

Date:	8-22-2006_9:52	Ver:	03
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Matched Length Nets

DDR1_A3
DDR1_A2
DDR1_A1
DDR1_A0
DDR1_A10
DDR1_BA1
DDR1_BA0
DDR1_CS_N

DDR1_RAS_N
DDR1_CAS_N
DDR1_WE_N
DDR1_DM2
DDR1_A13
DDR1_DQS2
DDR1_D23
DDR1_D22

DDR1_D20
DDR1_D19
DDR1_D18
DDR1_D17
DDR1_D16

DDR1_DM3

DDR1_DQS3
DDR1_D24
DDR1_D25
DDR1_D26
DDR1_D27
DDR1_D28
DDR1_D29
DDR1_D30

DDR1_A7
DDR1_A6
DDR1_A5
DDR1_A4
DDR1_A12
DDR1_A11
DDR1_A9
DDR1_A8

DDR1_DM1
DDR1_CK1_N
DDR1_CK1_P
DDR1_CKE
DDR1_D10
DDR1_D9
DDR1_D8
DDR1_DQS1

DDR1_D14
DDR1_D13
DDR1_D12
DDR1_D11
DDR1_D7
DDR1_DQS0
DDR1_DM0
DDR1_D15

DDR1_D3
DDR1_D4
DDR1_D5
DDR1_D6
DDR1_D31
DDR1_D0
DDR1_D1
DDR1_D2
DDR1_D21

RP52 RP53 RP66 RP65 RP64 RP63 RP62 RP58 RP59 RP60 RP61 RP55 RP67 RP56 RP57 — 47R

NC
NC

VTTDDR
VCC2V5

C619 C636 C620 C623 C621 C635 C622 C624 — 0.1UF
C182 C183 C185 C186 C196 C197 — 100UF

R277 — 47R

U42 U43 — 64Mx16x4 DDR SDRAM — HYB25D256160BT-7F — TSOP66

C626 C625 — 0.1UF

C627 C628 C630 C629 C631 C632 C633 C634 — 0.1UF

XILINX

SCH P/N 0381203
ART P/N 0531499
FAB P/N 1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
DDR1 DISCRETES AND TERMINATION

Date: 8-22-2006_9:52
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Rev: E
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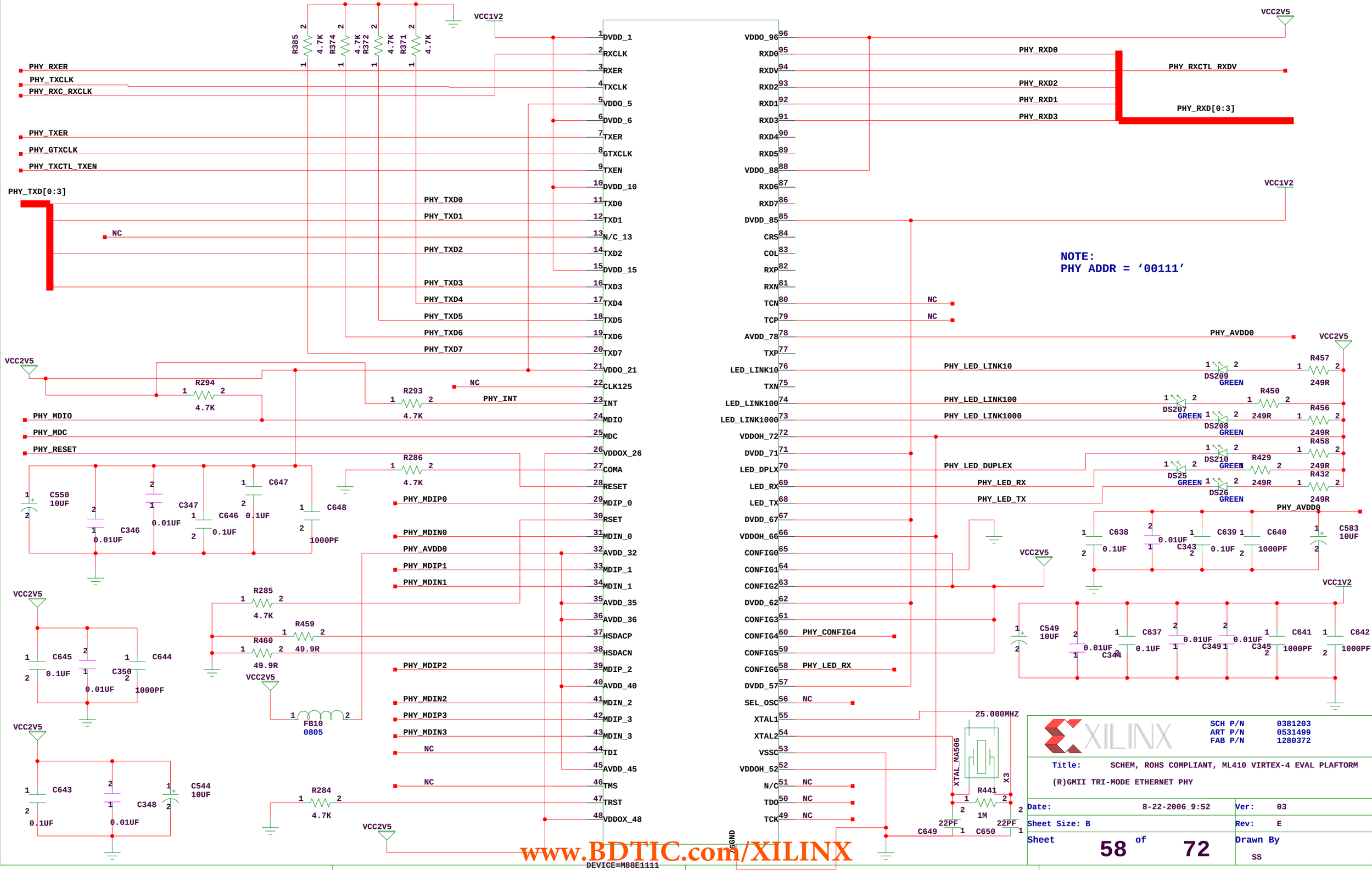
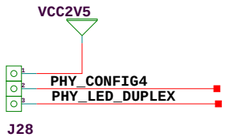
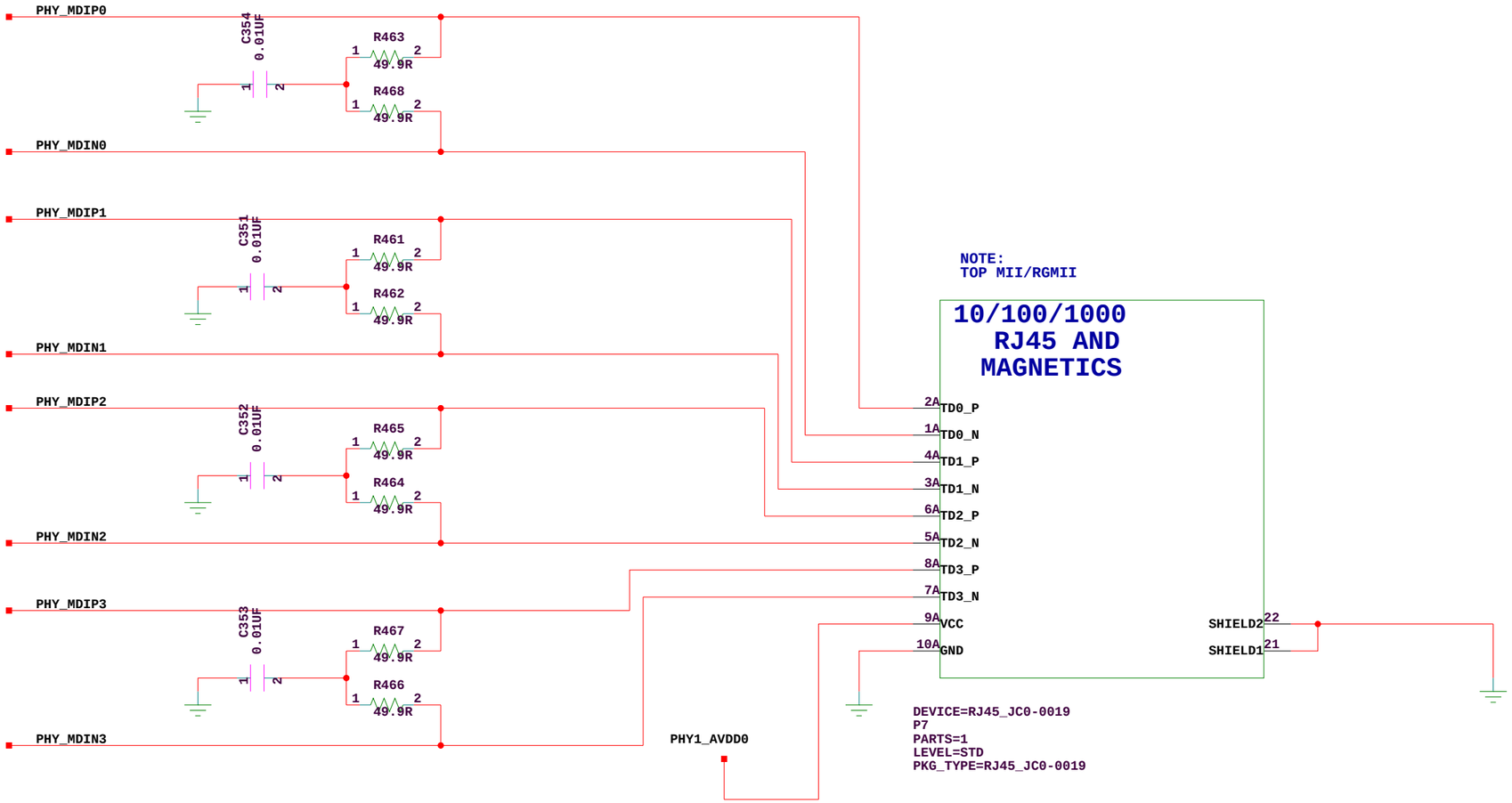


1-2: MII to Cu
2-3: RGMII to Cu





SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
(R)GMII RJ-45

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
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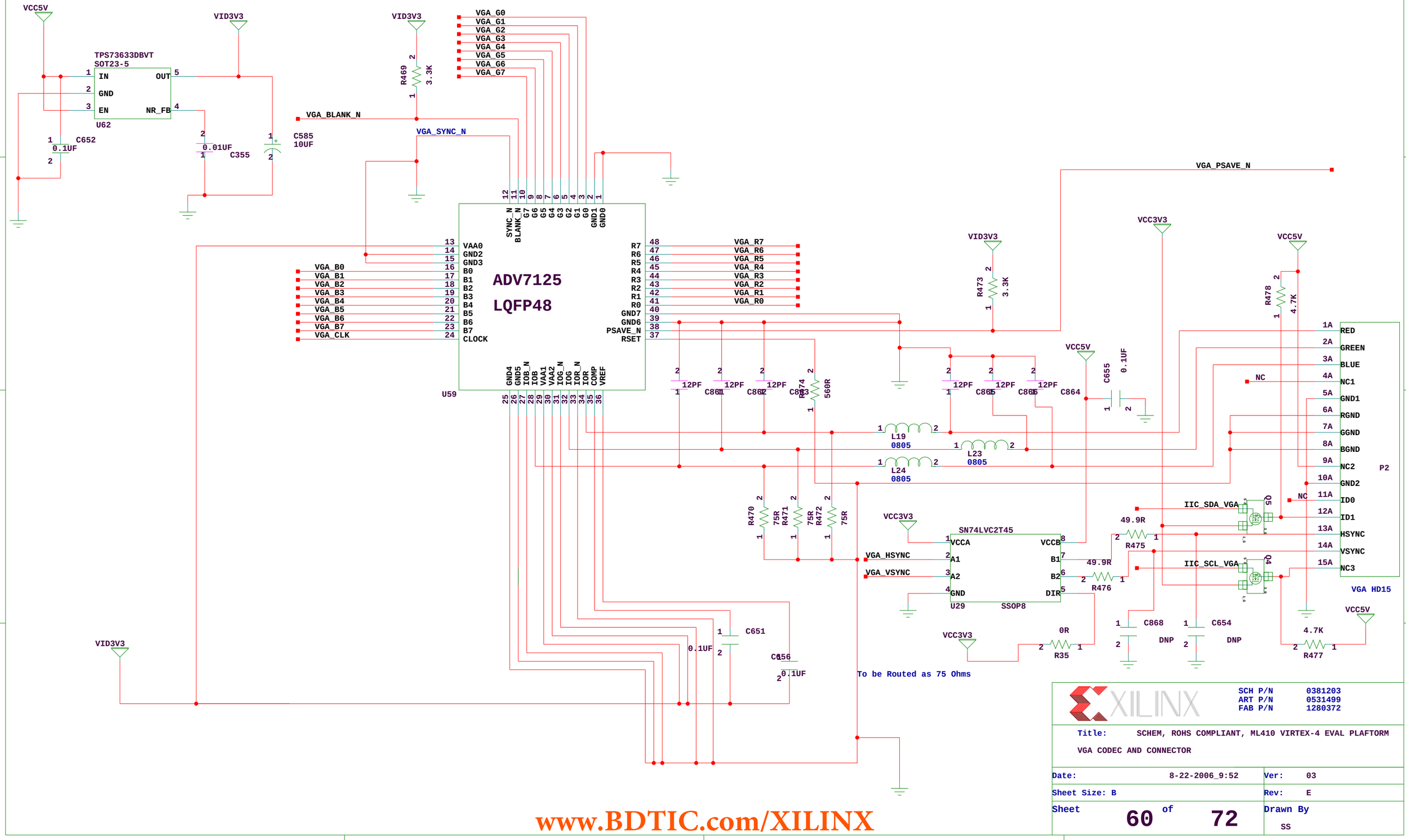
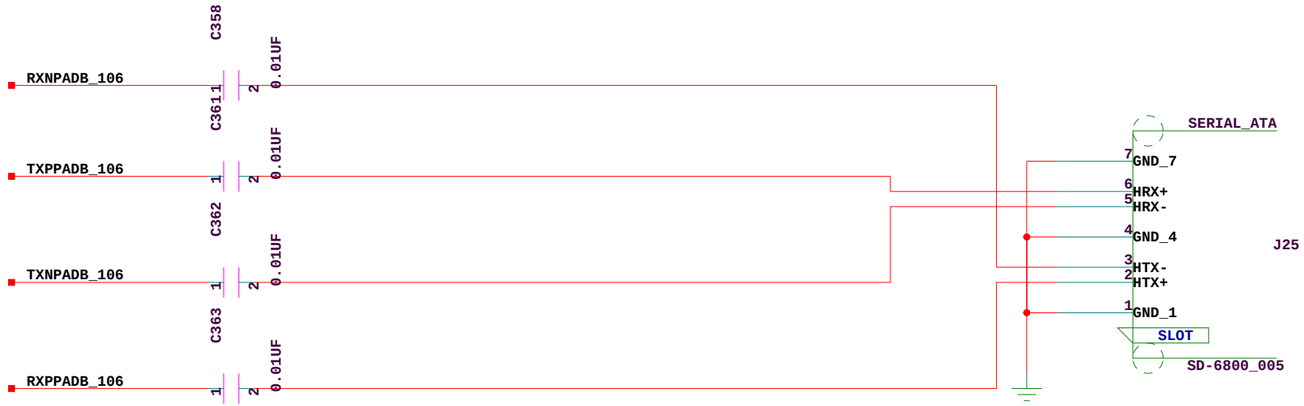


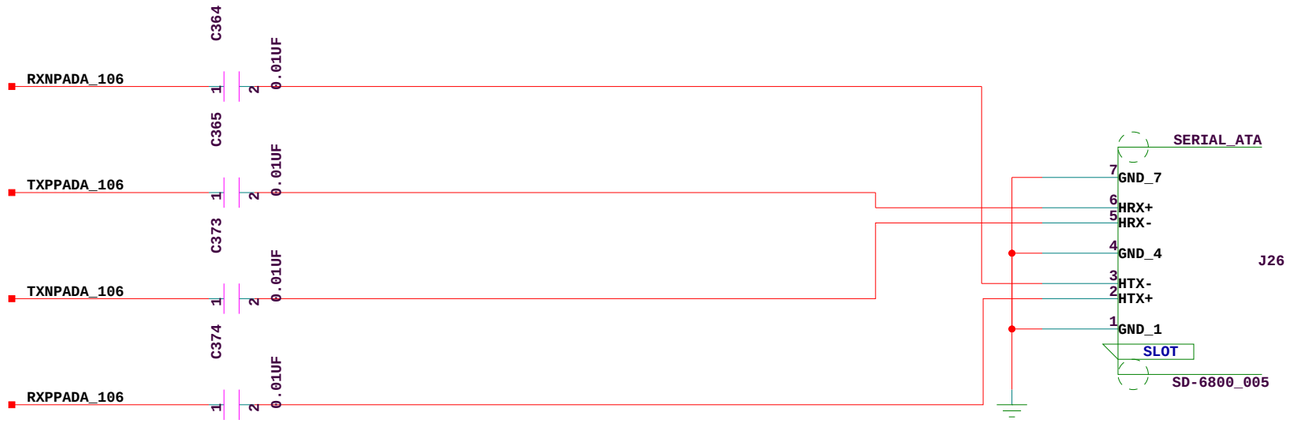
SATA Host 1

MGT 106B



SATA Host 2

MGT 106A



XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

SATA INTERFACE

Date:	8-22-2006_9:52	Ver:	03
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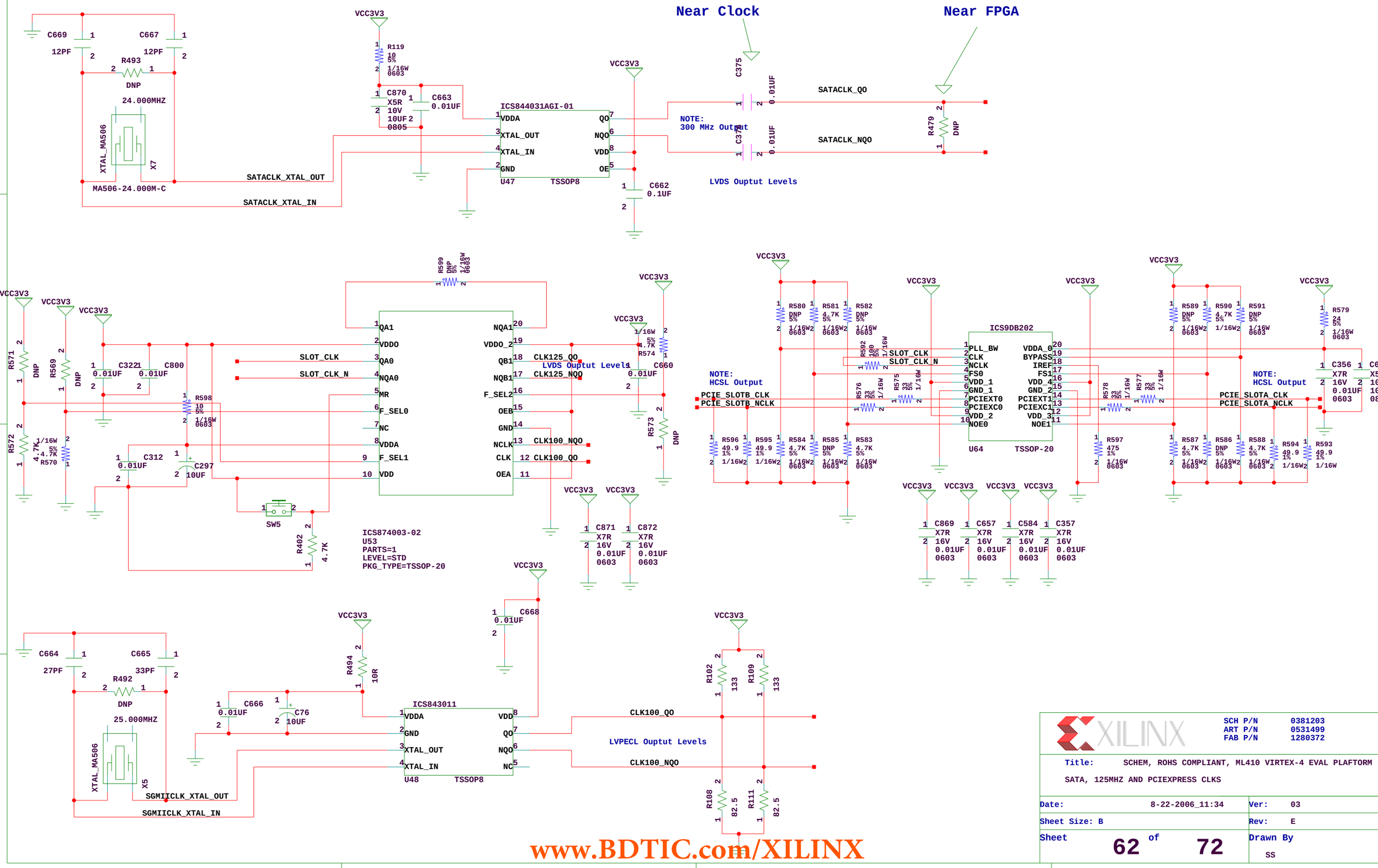

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

SATA, 125MHZ AND PCIEXPRESS CLKS

Date:	8-22-2006_11:34	Ver:	03
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MGT 102B

NOTE:
PHY ADDR = '00111'

DEVICE=M88E1111
U61
PARTS=1

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
SGMII TRI-MODE ETHERNET PHY

Date:	8-22-2006_9:52	Ver:	03
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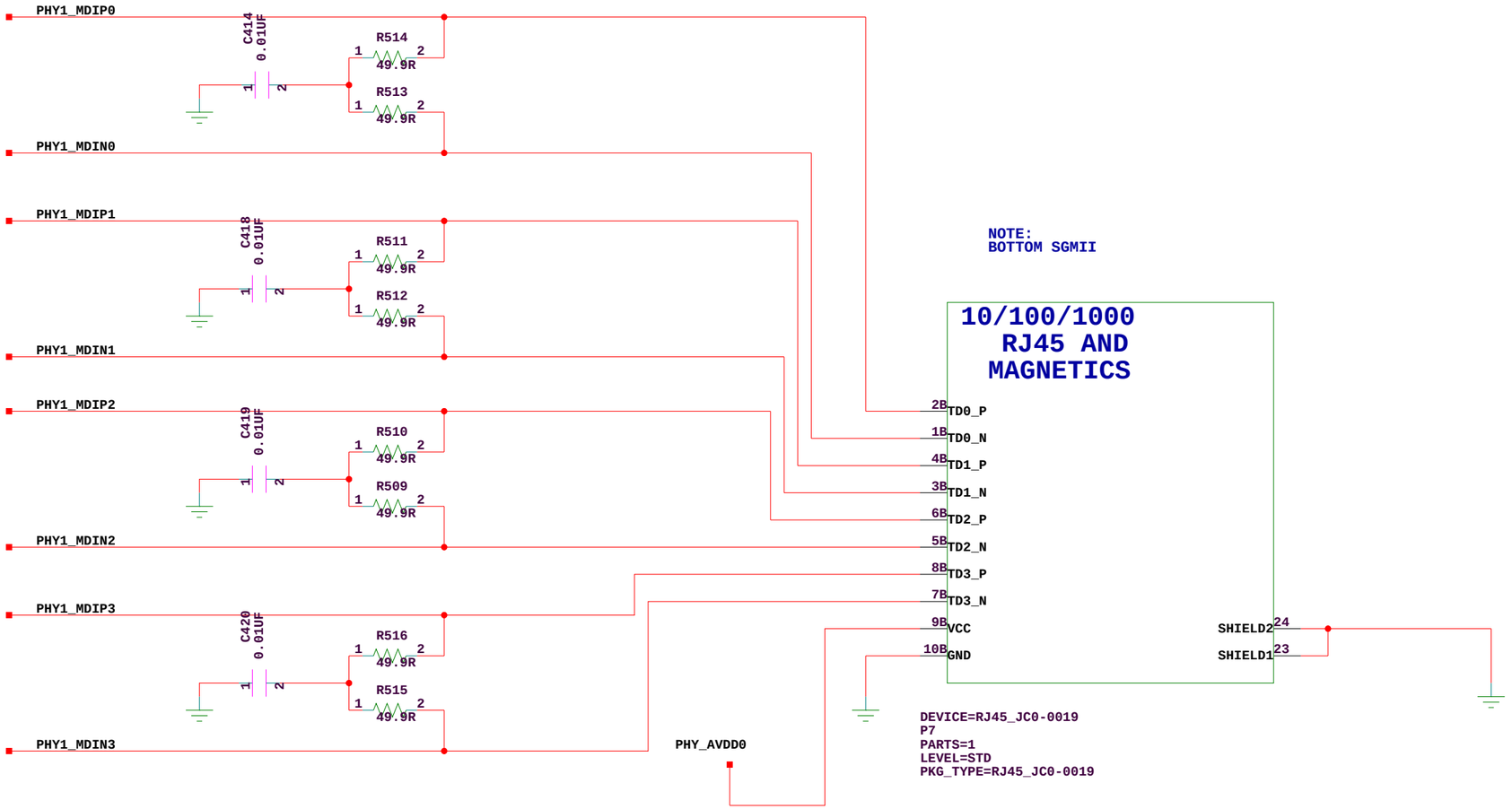

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

SGMII RJ-45

Date:	8-22-2006_9:52	Ver:	03
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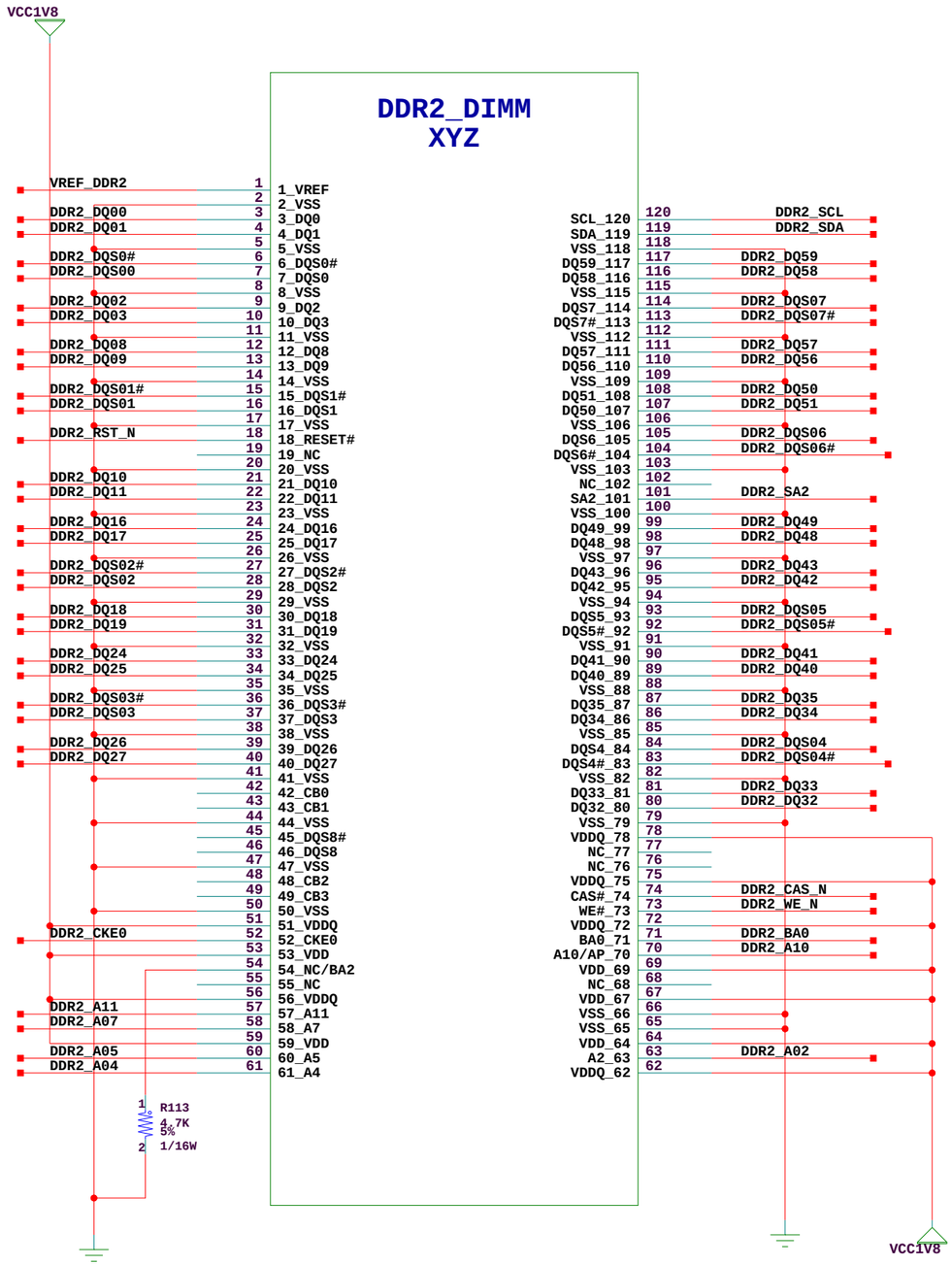

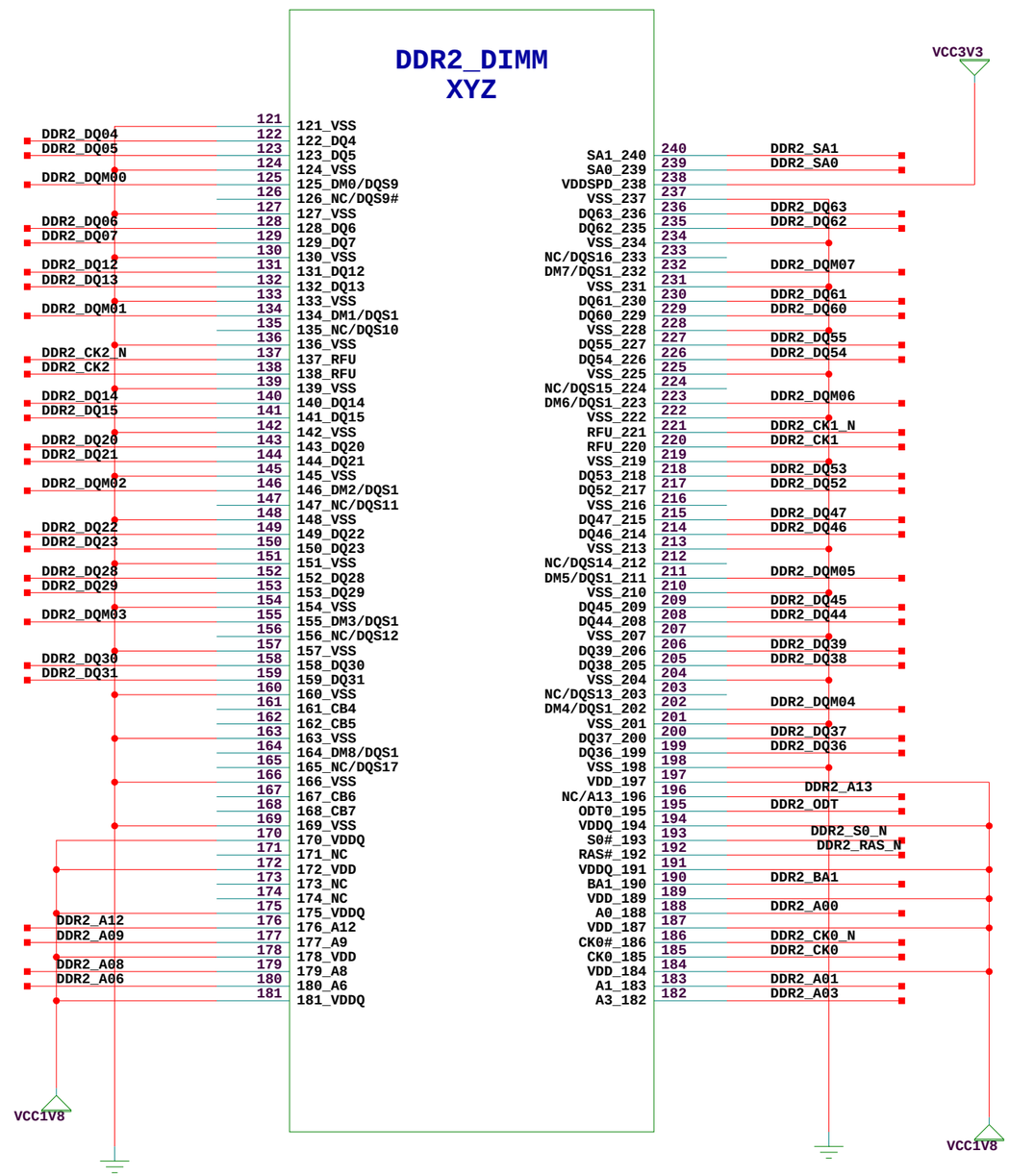

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

DDR2 DIMM CONNECTOR

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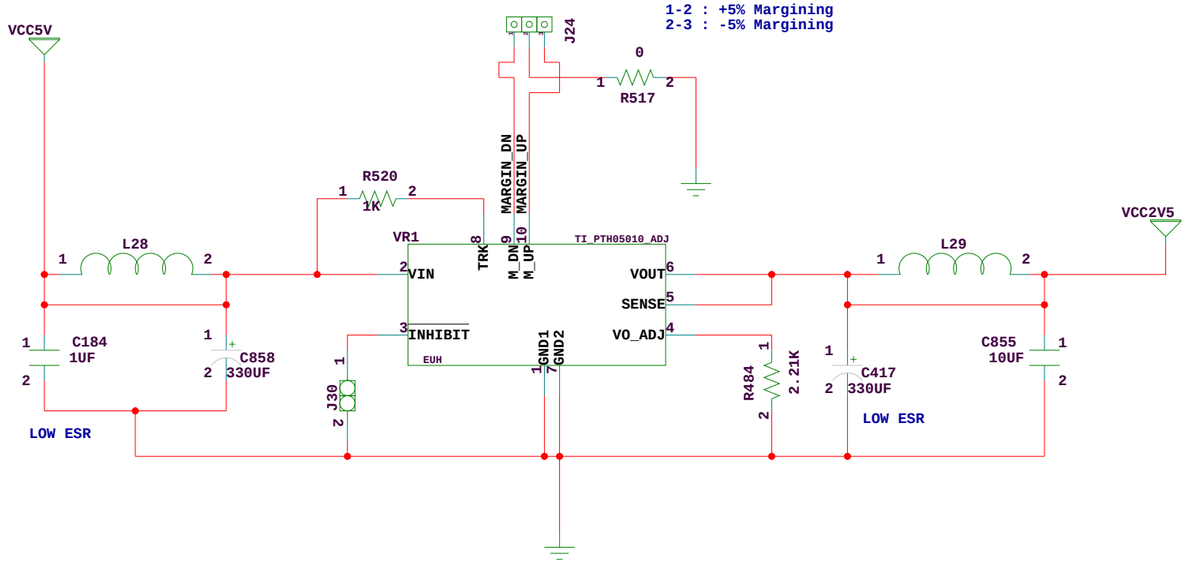
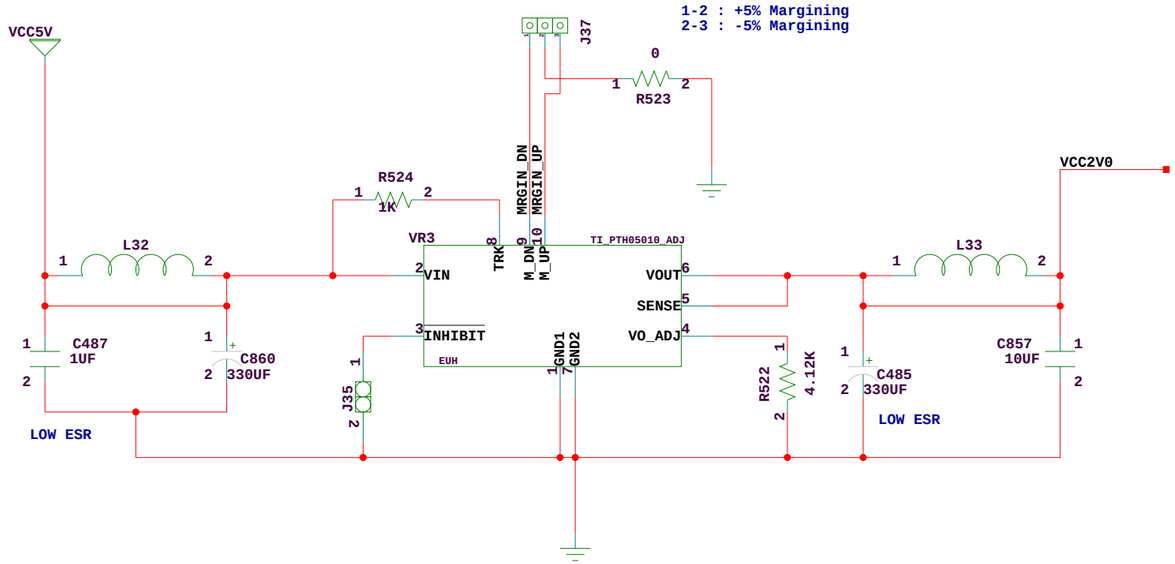
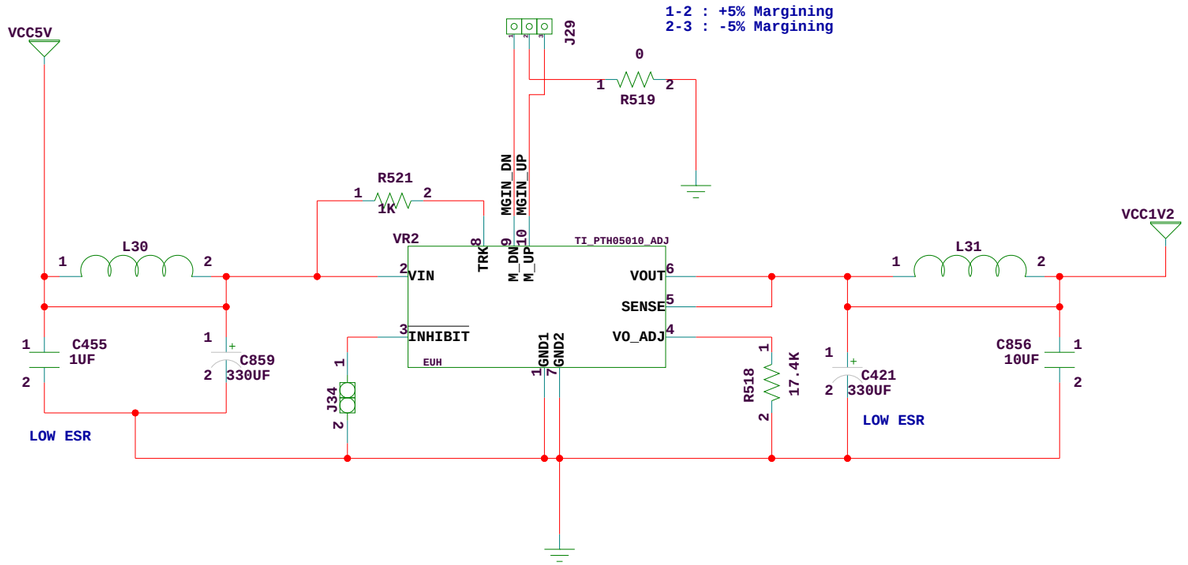
2.5V Supply @15A

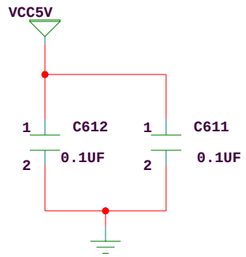


2.0V Supply @15A



1.2V Supply @15A





RSET=10K*(0.8V/(VOUT-0.8V)-2.49K
Vout=(8K/(RSET+2.49K))+0.8V

For 2.0V, R29 = 4.176K

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
FPGA CORE AND IO VOLTAGE

Date:	8-22-2006_9:52	Ver:	03
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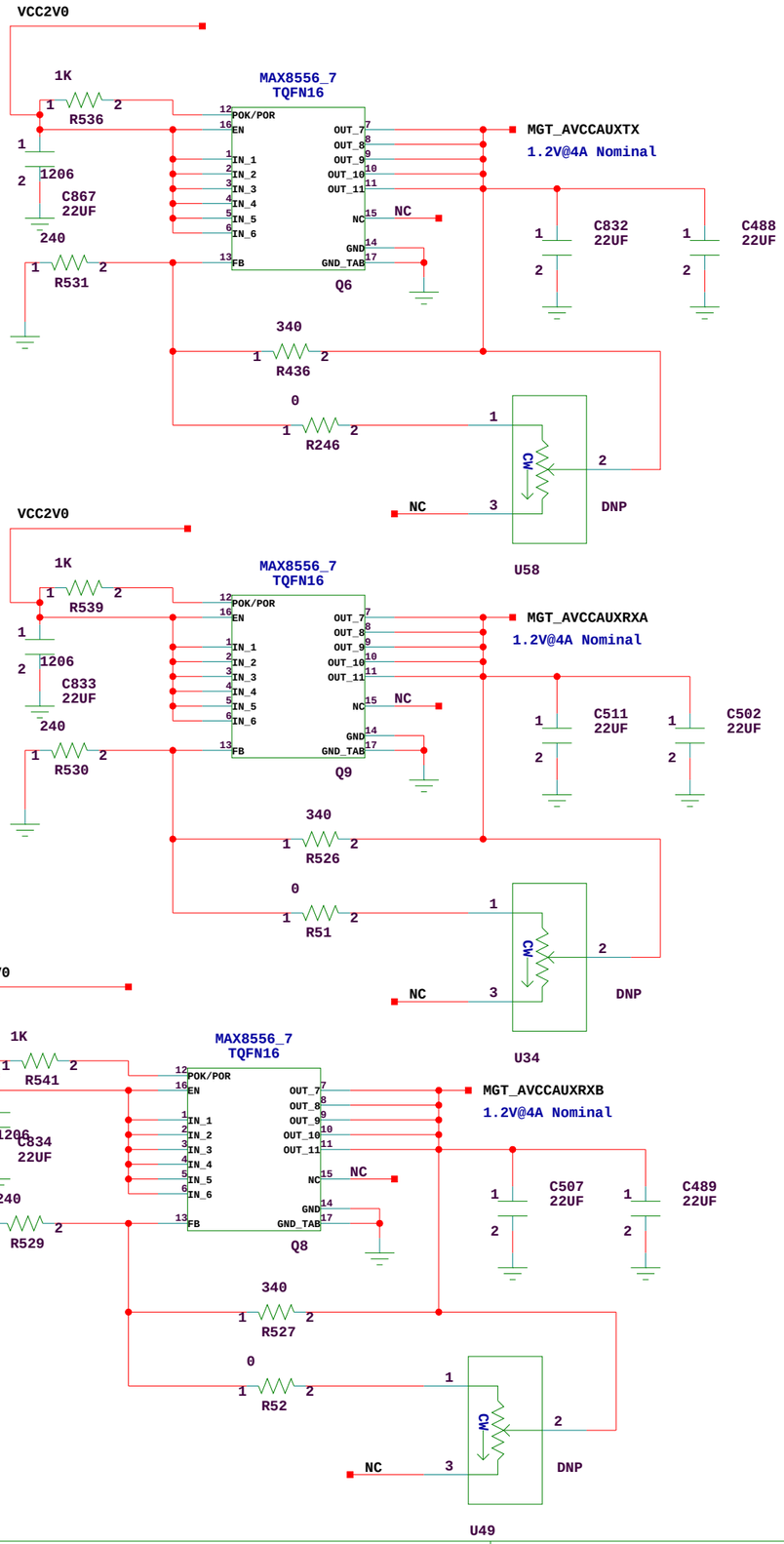

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM
MGT POWER SUPPLIES

Date:	8-22-2006_9:52	Ver:	03
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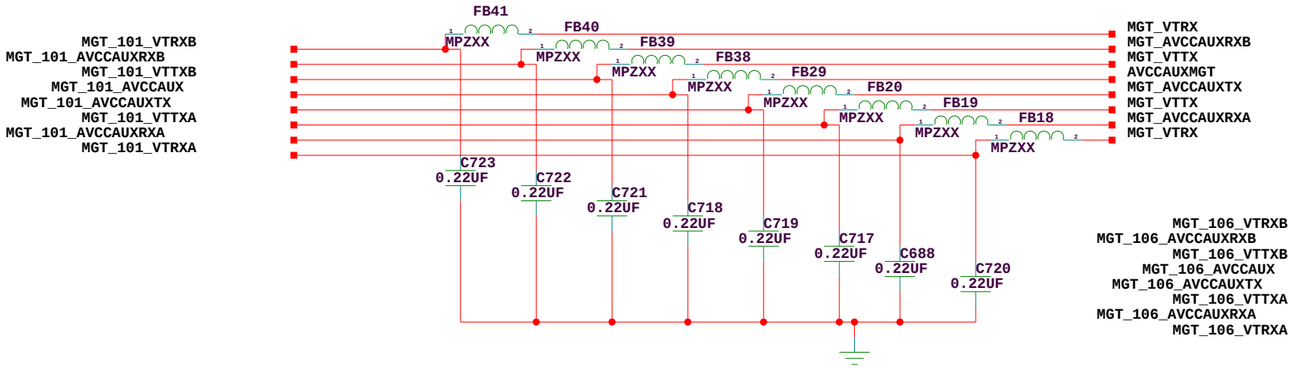

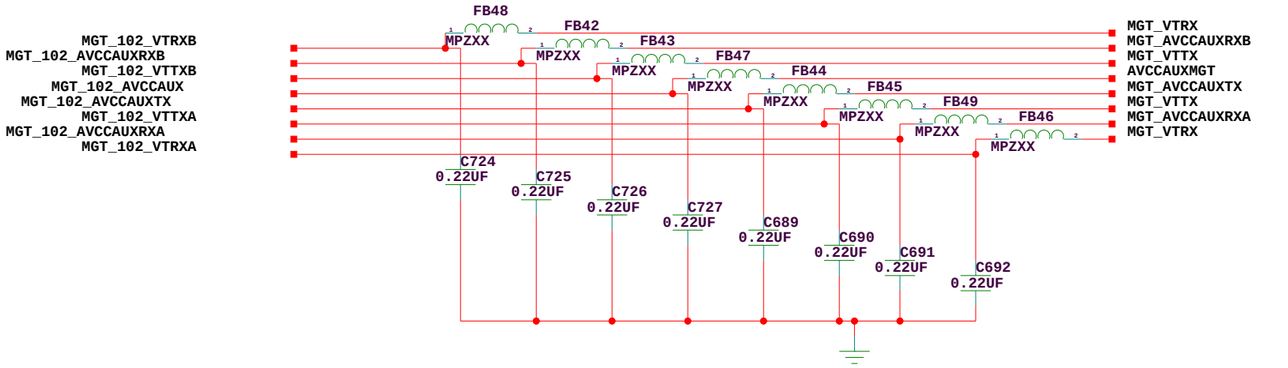

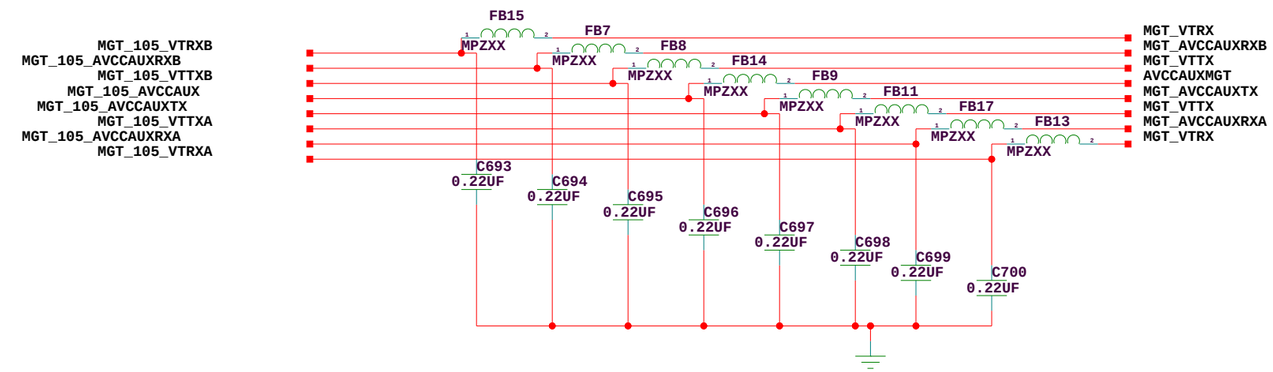

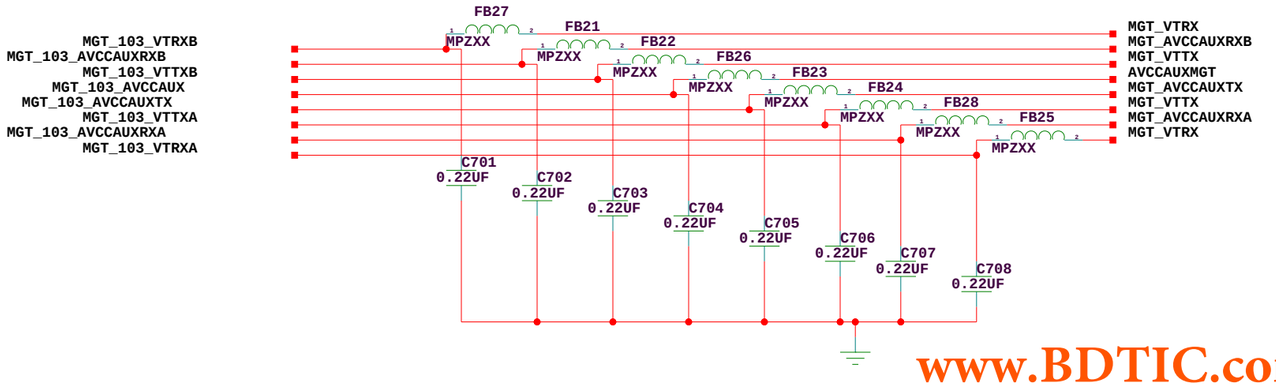

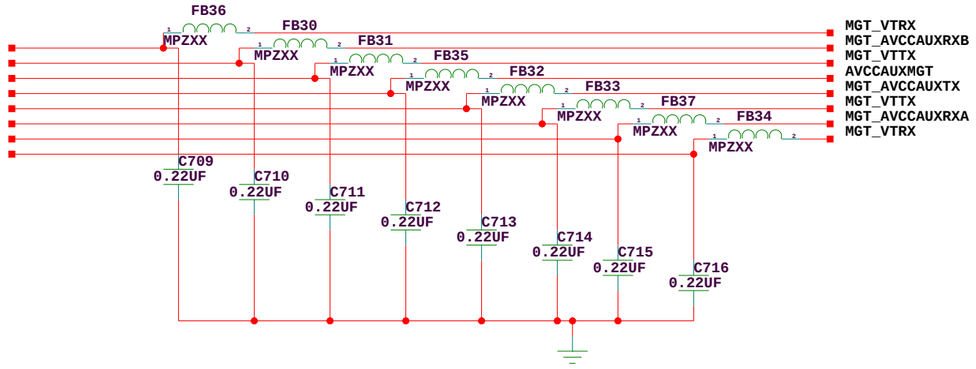

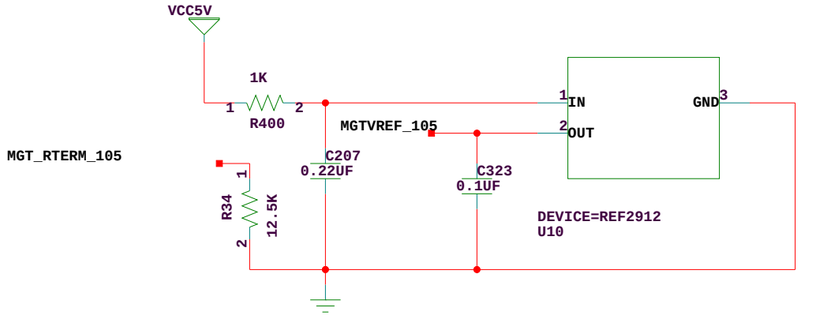

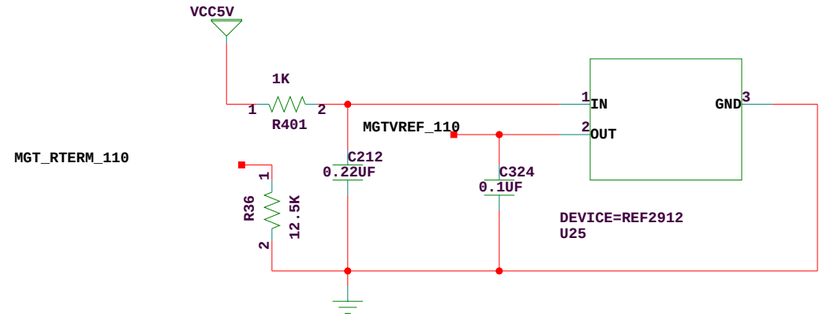

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT POWER FILTER-1, VTERM AND RTERM

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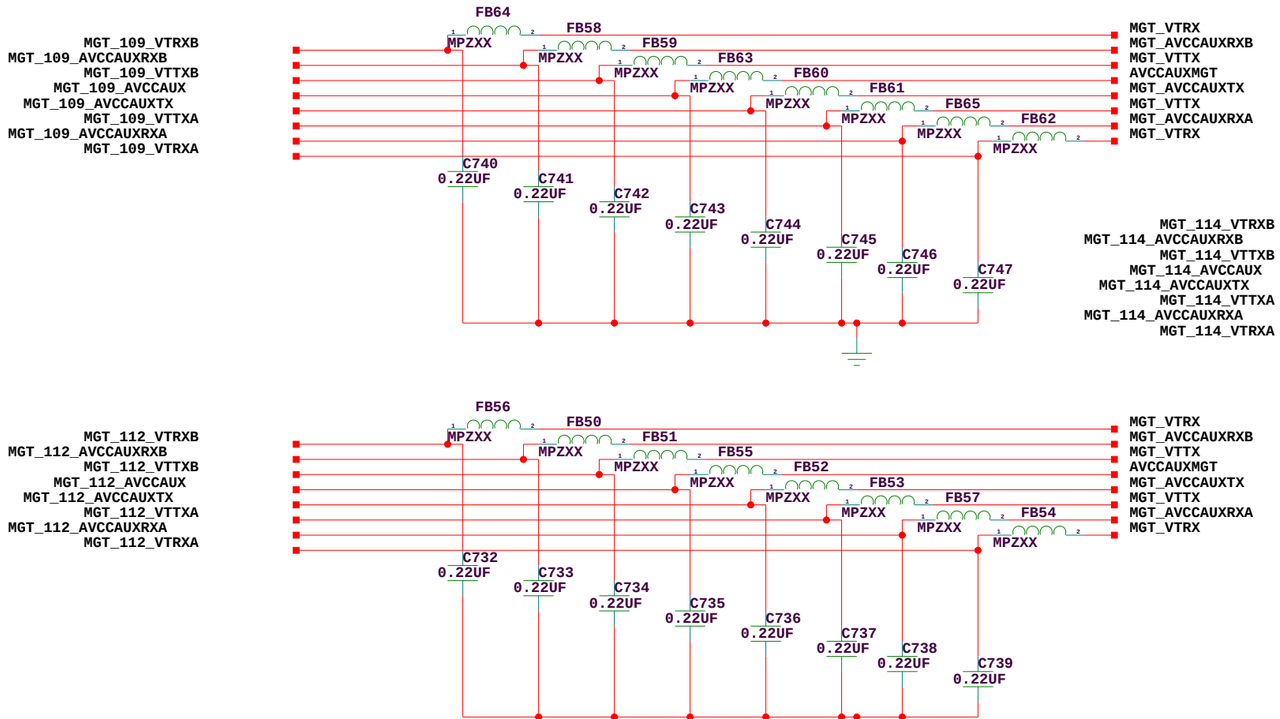

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

MGT POWER FILTER-2

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
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C595 22UF 25V
VCC12V_P
22PF
0.1UF
C769
C768
12VINA 5
R538 1 2 0.025
12VSENSEA 8
0.1UF
C770
15
12VGATEA 3
0.022UF
C771
R540 2 1
C596
12VOUTA 10
U16
PCIE_SLOTA_12V
Si4435DY
SO-8
1_S 2_S 3_S 4_G
D_8 D_7 D_6 D_5
1 2 3 4 8 7 6 5
C594 1 2 100UF

22UF
VCC3V3
22PF
0.1UF
C772
C773
3VINA 12
R33 1 2 0.01
3VSENSEA 13
0.01UF
C774
15
3VGATEA 14
R558 2 1
3VOUTA 16
U51
PCIE_SLOTA_3V3
Si4420DY
SO-8
D_8 D_7 D_6 D_5
1_S 2_S 3_S 4_G
8 7 6 5 1 2 3 4
C597 1 2 100UF

C600 22UF 25V
VCC12V_P
22PF
0.1UF
C778
C779
12VINB 32
R38 1 2 0.025
12VSENSEB 29
0.1UF
C826
15
12VGATEB 34
0.022UF
C827
R542 2 1
C1003
12VOUTB 27
U14
PCIE_SLOTB_12V
Si4435DY
SO-8
1_S 2_S 3_S 4_G
D_8 D_7 D_6 D_5
1 2 3 4 8 7 6 5
C599 1 2 100UF

22UF
VCC3V3
22PF
0.1UF
C776
C777
3VINB 25
R37 1 2 0.01
3VSENSEB 24
0.01UF
C775
15
3VGATEB 23
R543 2 1
3VOUTB 21
U52
PCIE_SLOTB_3V3
Si4420DY
SO-8
D_8 D_7 D_6 D_5
1_S 2_S 3_S 4_G
8 7 6 5 1 2 3 4
C598 1 2 100UF

VAUXA 15 PCIE_SLOTA_3V3AUX
VAUXB 22 PCIE_SLOTB_3V3AUX

DEVICE=MIC2592B
U55

IIC_SCL R428 0 IIC_SCL_PCIE
IIC_SDA R431 0 IIC_SDA_PCIE

I2C ADDR = 0x8E

Make sure IIC Address is set correctly

V5_STDBY
47UF C602 100UF
0.1UF C603
0.01UF C828 C829

VSTBYA 11
VSTDBYB 26
IREF 33
0 R544
CFILTERA 2
0.047UF C830
CFILTERB 35
0.047UF C831

ONA 44
ONB 43
AUXENA 45
AUXENB 42
FAULT_A 1
FAULT_B 36
PWRGDA 6
PWRGDB 31
FORCE_A 9
FORCE_B 28
GPIA_0 4
100K R565
NC 7
GPIB_0 38
100K R566
NC_1 30
100K R554 R546 R547 R548 R549 R550 R551 R552 R553 R555
A0 41
A1 40
A2 39
100K R557 R561 R564
V5_STDBY
INT 37
SCL 47
SDA 48
IIC_SCL_PCIE
IIC_SDA_PCIE
100K R556

RFILTER(AB) 20
NC46 19
GND2 46
NC3 18
GND1 17
DEVICE=MIC2592B
U55
R567 1 2 100K-DNP

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI-E PWR MGMT CONTROLLER

Date:	8-22-2006_9:52	Ver:	03
Sheet Size: B		Rev:	E
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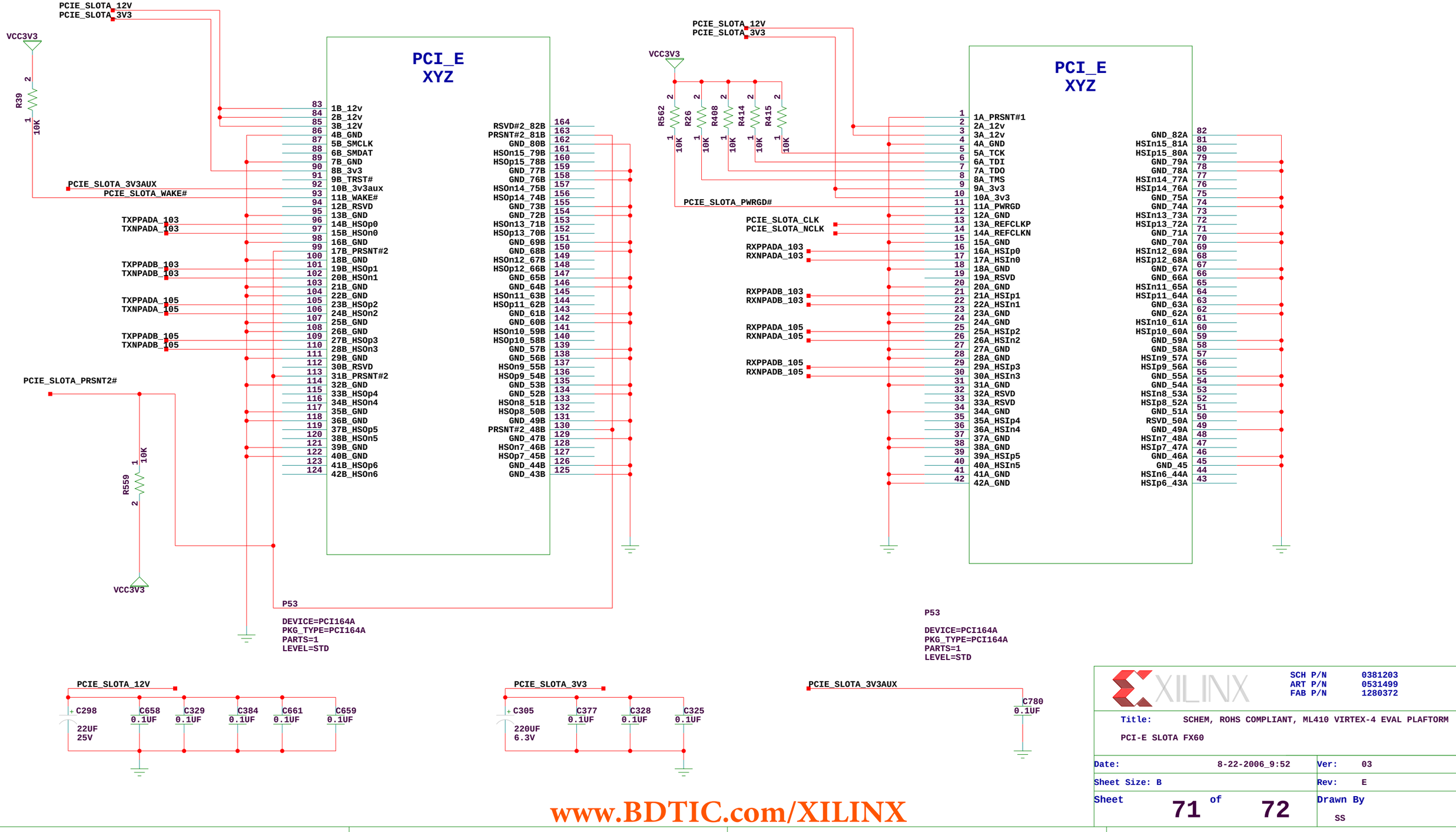

XILINX

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI-E SLOTA FX60

Date:	8-22-2006_9:52	Ver:	03
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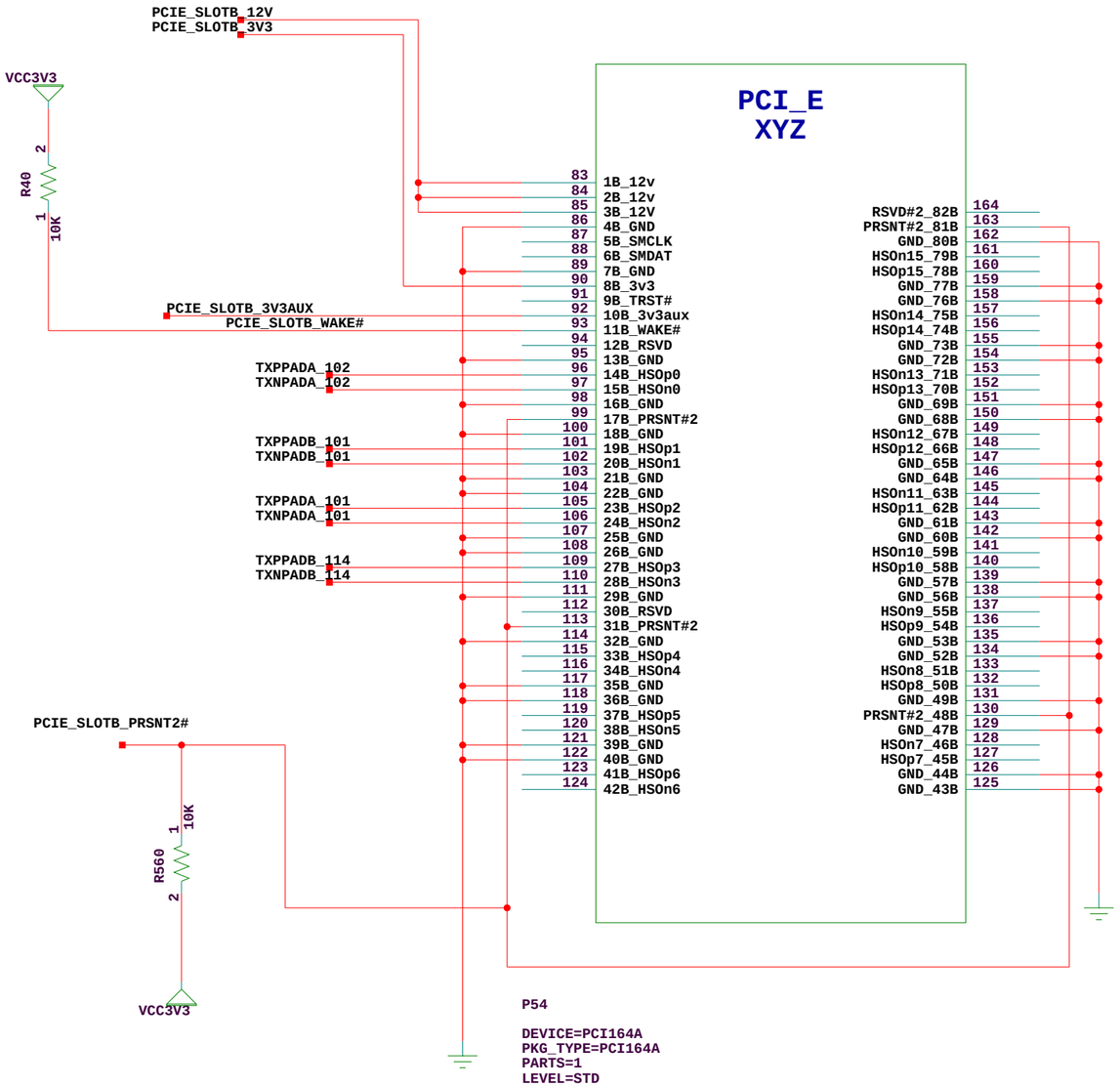

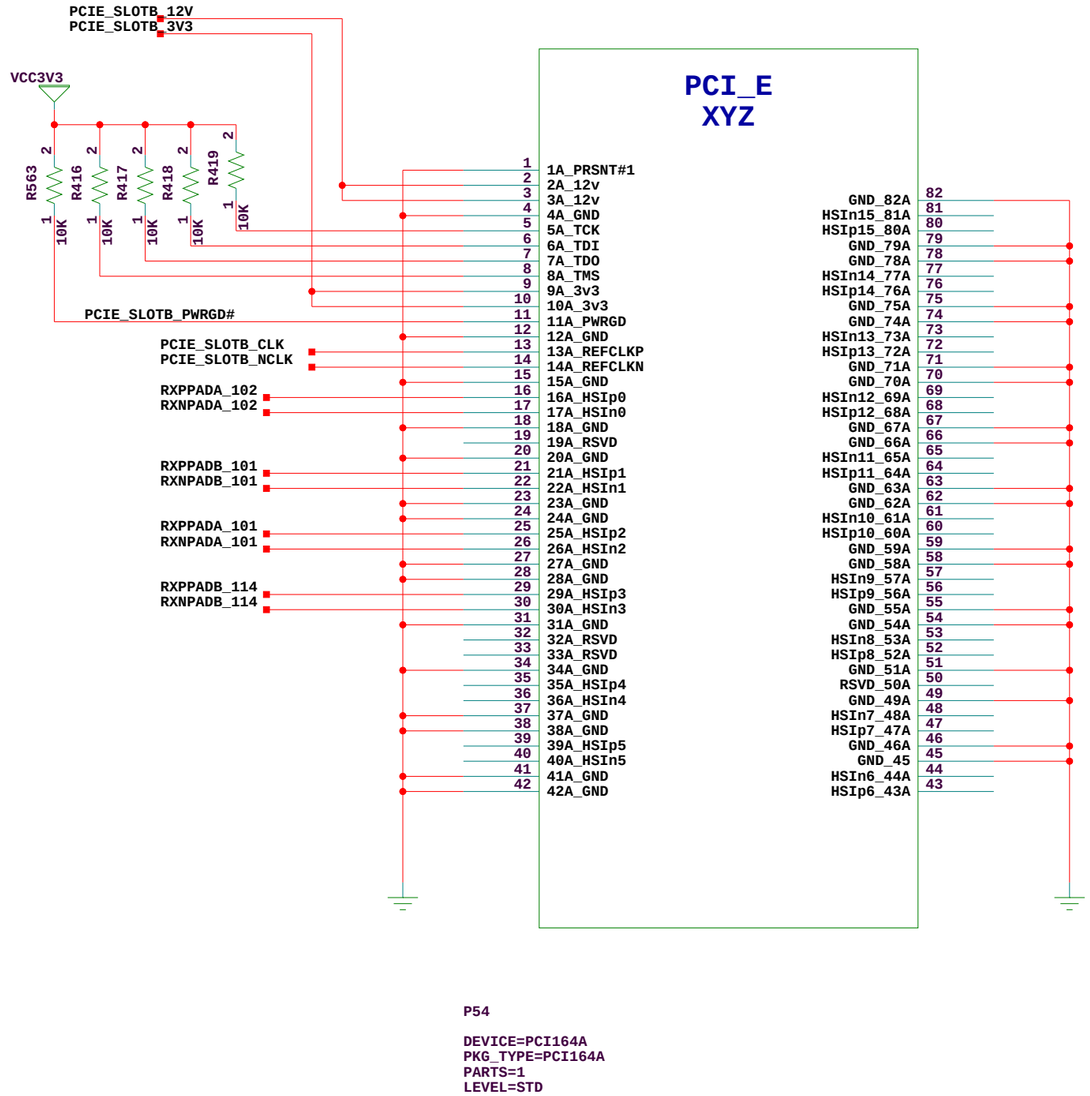

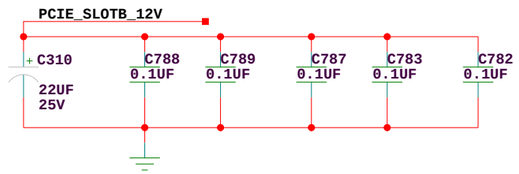

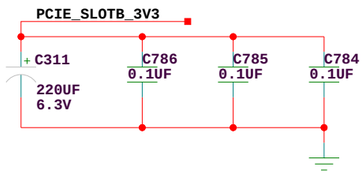

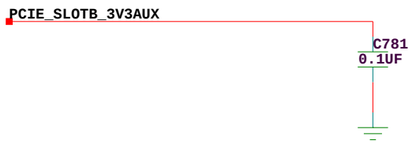

SCH P/N	0381203
ART P/N	0531499
FAB P/N	1280372

Title: SCHEM, ROHS COMPLIANT, ML410 VIRTEX-4 EVAL PLAFTORM

PCI SLOTB FX100

Date:	8-22-2006_9:52	Ver:	03
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