Virtex-5 Gigabit Ethernet Serial Protocol Standard

Characterization Test Report

RPT061 (v1.01) December 12, 2006

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/08/06	1.0	Initial Xilinx Confidential release.
12/12/06	1.01	Release to Xilinx website under license agreement.

Virtex-5 Gigabit Ethernet Serial Protocol Standard

Introduction

Virtex™-5 system connectivity technology delivers the lowest power solutions for building high-speed, high-bandwidth connections between devices, boards, and boxes. The RocketIO™ GTP transceiver design and proven SelectIO™ parallel I/O technologies enable flexible bridging between emerging serial standards and existing parallel standards. The features of the Virtex-5 GTP transceivers include:

- Current Mode Logic (CML) drivers/buffers with configurable termination, voltage swing, and coupling.
- Programmable transmit pre-emphasis and receive equalization for optimal signal integrity.
- Line rates from 500 Mb/s to 3.2 Gb/s with optional 5x over-sampling for data rates from 100 Mb/s to 500 Mb/s.
- Optional built-in PCS features, such as 8B/10B encoding/decoding, comma alignment, channel bonding, and clock correction.
- Fixed latency modes for minimized, deterministic datapath latency.
- Out-of-band signaling support (specifically designed to address the requirements of PCI Express® and Serial ATA protocols).
- Built-in pseudo-random bitstream (PRBS) generation/checking logic for easier bit-error rate checking.
- A configuration wizard provided in the CORE Generator™ tool and a bit error rate tester (IBERT) integrated into the ChipScope™ Pro tools for easy implementation of GTP transceiver interfaces.

This document presents the GTP transceiver electrical performance against the various specifications for Gigabit Ethernet across process, voltage, and temperature conditions. GTP transmitter and receiver electrical characteristics were measured using a combination of lab bench setups and a High Volume Characterization (HVC) system.The methods used to characterize the transceiver are based on the standards specifications and also follow the best-practice methods for some parameters.

A high-level description of the Virtex-5 device (LXT Platform) GTP transceiver testing against the specifications for the IEEE 802.3-2002 [Ref 3] clause 35-39 is included.

Background

The Gigabit Ethernet (GE) specification was heavily leveraged from work done on the 1G Fibre Channel (FC). The GE standard references the test methodologies developed by FC in the FC-PH-2 document and the MJSQ document. The increase in baud rate from 1.0625 G (FC) to 1.25 G (GE) was done to maintain the 1G raw data rate required by Ethernet (FC runs at a 800 Mb/s raw data rate). Although the test methodologies are the same, the actual jitter numbers are slightly different due to the fiber distances supported by Ethernet.

The system diagram Figure 1 shows the test points in the GE standard. TP1 (TX output) and TP4 (RX input) are standardized reference points used to certify component conformance. The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points. They are not readily testable in a system implementation. It is expected that in many implementations, TP1 and TP4 will be common between 1000BASE-SX, 1000BASE-LX, and 1000BASE-CX (Clause 39). The test specifications in this document refer to TP1 and TP4. The tests performed do not include an optical module described in the specification. The signal path is confined to the electrical domain and detailed test setups are described in the individual sections. The measurement setup contains additional PCB traces, connectors, and cable that can add additional jitter to the measurement.

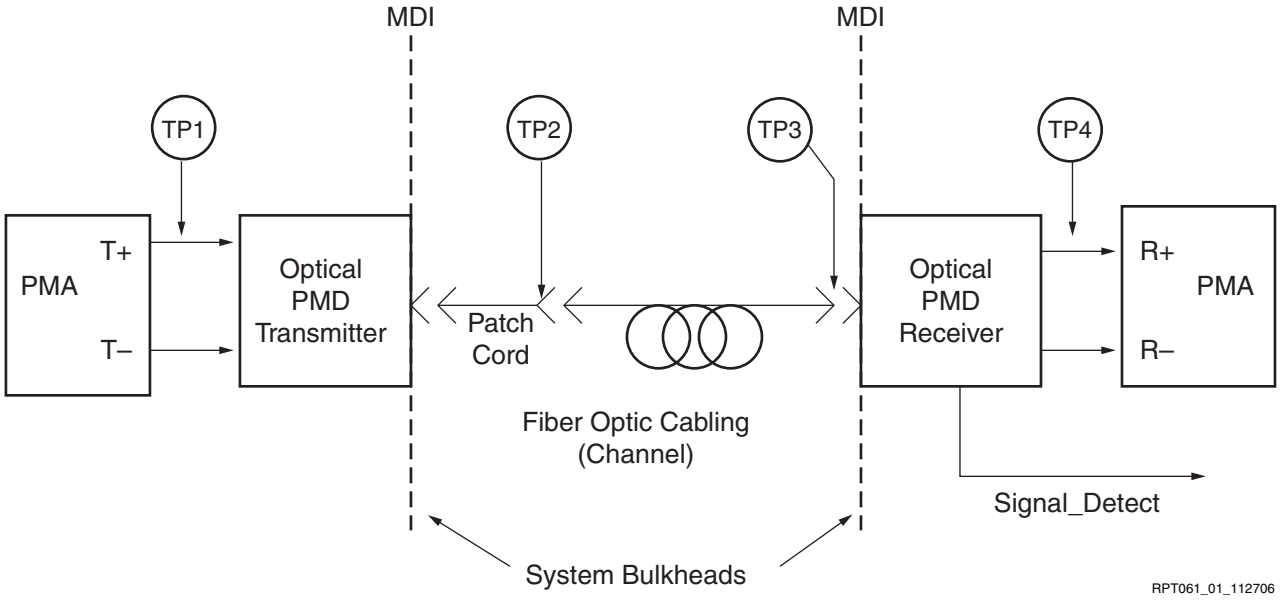

Figure 1: **1000BASE-X Block Diagram**

Test Equipment

Both bench and ATE based test equipment was used to characterize the GTP transceivers. Bench setups were used for the majority of the RX jitter and TX amplitude measurements. The ATE setup was based on a multi-channel ParBERT and was used for TX jitter and general characterization.

Test Conditions

Table 1 shows the operating supply voltages and Table 2 shows the operating temperatures.

Table 1: **Operating Supply Voltages**

Condition	MGTAVCC	MGTAVCCPLL	MGTAVTTRX	MGTAVTTTX	Units
V_{MIN}	0.95	1.14V	1.14V	1.14V	V
V_{NOM}	1.0	1.20V	1.20V	1.20V	V
V_{MAX}	1.05	1.26V	1.26V	1.26V	V

Notes:

1. Other FPGA voltages remain at nominal values.
2. Some tests performed at ±10% V_{CC}.

Table 2: **Operating Temperatures**

Condition	Temperature (Case for Bench Measurements)
T_{MAX}	100°C
T_{ROOM}	25°C
T_{MIN}	–40°C

The devices chosen for characterization cover the process corner material. The number of devices varies. A minimum of two devices each were used from slow, typical, and fast process corners. The HVC system uses a larger sample size with five devices from each corner and 12 GTP transceivers tested per device across voltage and temperature specifications.

Summary of Results

Table 3 summarizes the Gigabit Ethernet specification requirements and the test results for the Virtex-5 GTP transceiver.

Table 3: **Summary of Test Results for the Gigabit Ethernet Specification**

	Gigabit Ethernet Specifications		Virtex-5 GTP Test Results		Units	Compliant?	Comments
	Min	Max	Min	Max			
Jitter Generation (TP1)							
TX TJ		192/.24		149/0.19	ps/UI	Yes	
Output Amplitude	800	1600	900	1100	mv p-p differential	Yes	Measured with TXCTRL = 3. Output levels are programmable.
Rise Time	85	327	93	156	ps	Yes	
Fall Time	85	327	73	144	ps	Yes(1)	Minimum value is 14% below specification.
Jitter Tolerance							
RX DJ	0.462		0.47		UI	Yes	
RX TJ	0.749		0.75		UI	Yes	
Baud Rate Tolerance	–100	100	–2700	2700	ppm	Yes	Performed at 2.5 Gb/s.
Input Sensitivity	370		135		mv p-p differential	Yes	

Notes:

1. Conditional compliance. See Figure 16, page 23.

Receiver Electrical Tests

Total Jitter Tolerance

Total jitter tolerance measurements at 1.25 Gb/s, the Gigabit Ethernet required data rate, are performed to test GTP performance. In this measurement, both jitter components of deterministic jitter (DJ) and random jitter (RJ) are added to the input data path. Based on channel calibration, DJ and RJ components are fixed to introduce 0.75 UI of total jitter, and the device is tested for at least 10^{12} error-free bits.

Receiver Specifications

Table 4 shows the receiver specification. Figure 2 shows the receiver input mask.

Table 4: **1000BASE-CX Receiver Specification**

Description	Value	Units
Data rate	1000	Mb/s
Nominal signalling speed	1250	MBd
Tolerance	±100	ppm
Minimum differential sensitivity (peak-to-peak)	400	mV
Maximum differential input (peak-to-peak)	2000	mV

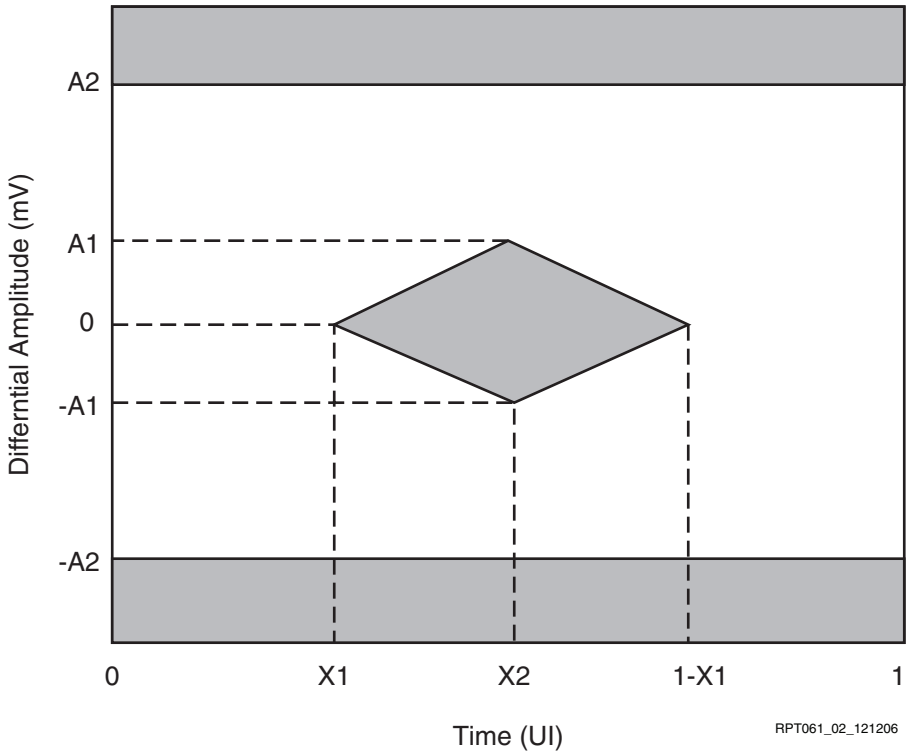

Figure 2: **Receiver Input Mask**

The input signals are driven from a 100Ω impedance, known-good source. The test setup is shown in Figure 5. The purpose of the test is to feed in a jittery signal which meets the jitter mask shown in Figure 2 and measure the receiver's lock status, stability, and data BER. The receiver must be AC coupled, and the input is measured at the output of the receiver's connector. The receiver mask parameters are shown in Table 5. Total jitter is composed of deterministic jitter and random jitter.

Table 5: **Receiver Mask Parameters**

Parameter	Value	Units
X1	0.375	UI
X2	0.500	UI
A1	185	mV
A2	1000	mV

DJ Component

The DJ component is generated by passing the CJPAT test pattern at 1.25 Gb/s through 90 inches of Xilinx standard FR4 trace board. The jitter decomposition measurement is made using the Agilent DCA-J scope, as shown in Figure 3. In this case, the additional RJ component is turned off and only the DJ component of 379 ps (0.47 UI) is recorded from the DCA-J measurement.

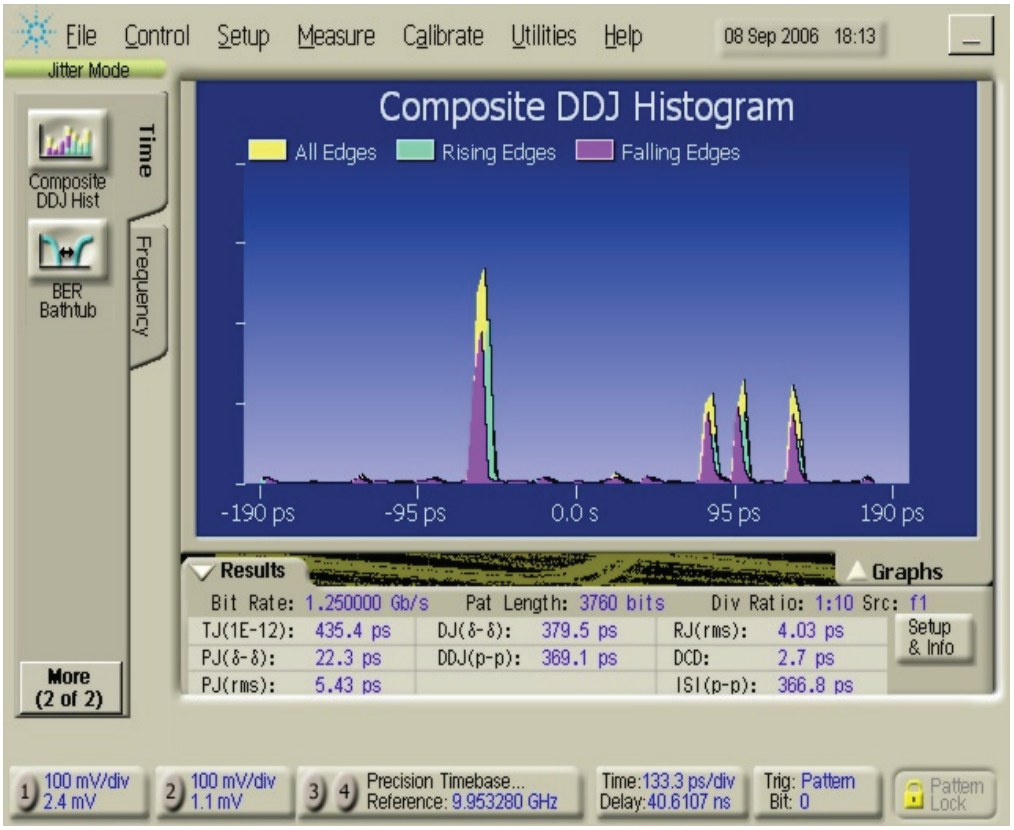

Figure 3: **Jitter Decomposition at 1.25 Gb/s over a 90-inch Xilinx FR4 Trace Board**

RJ Component

The RJ component from the NoiseCom random noise source is added to the pattern generator clock source using a power splitter. The measurement of the RJ component is made separately with the standard jitter function of the Agilent DCA scope as the signal RMS jitter using the K28.7 test pattern (see Figure 4). To compute the total jitter in this measurement at 10^{-12} BER, the RJ rms value is multiplied by 14 and then added to the DJ value.

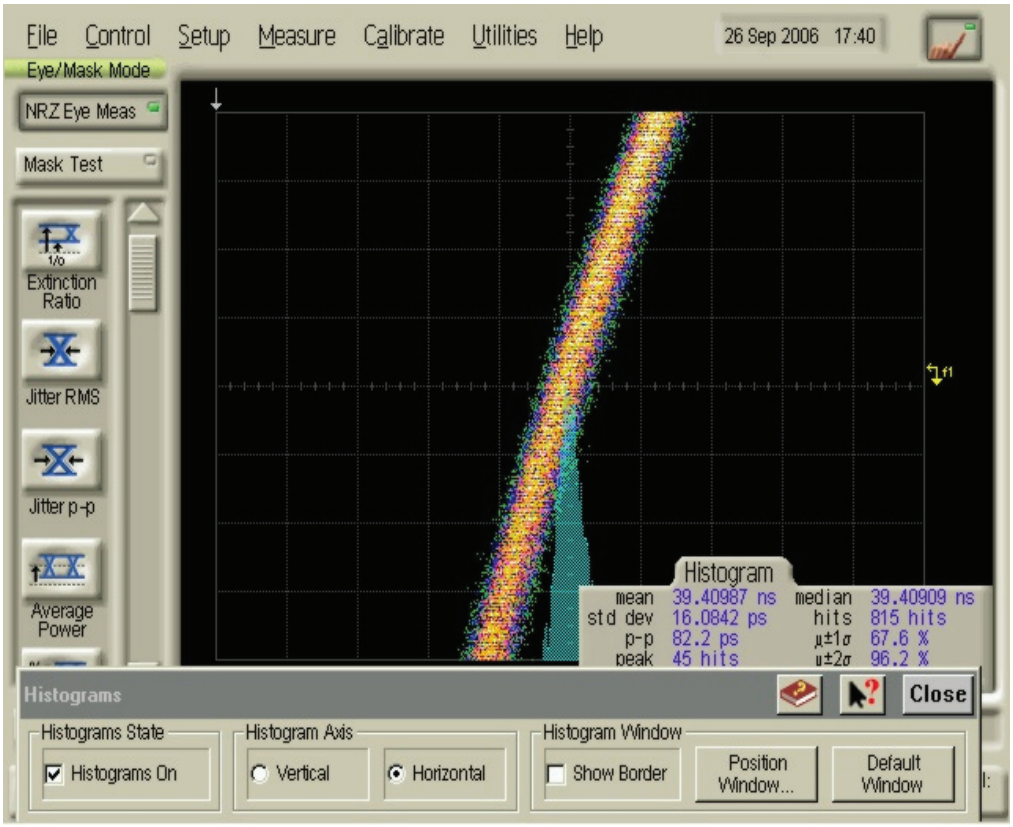

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Figure 4: **Random Jitter**

Lab Board Set Up

An ML523 evaluation board, with an Oztek socket hosting FF1136 package, is used to test the Virtex-5 devices. The Xilinx GUI-based XBERT platform is used for DRP loadings. A Chipscope Pro™ analyzer is used to configure the part.

Test Setup

Figure 5 shows the receiver jitter tolerance and input sensitivity test setup.

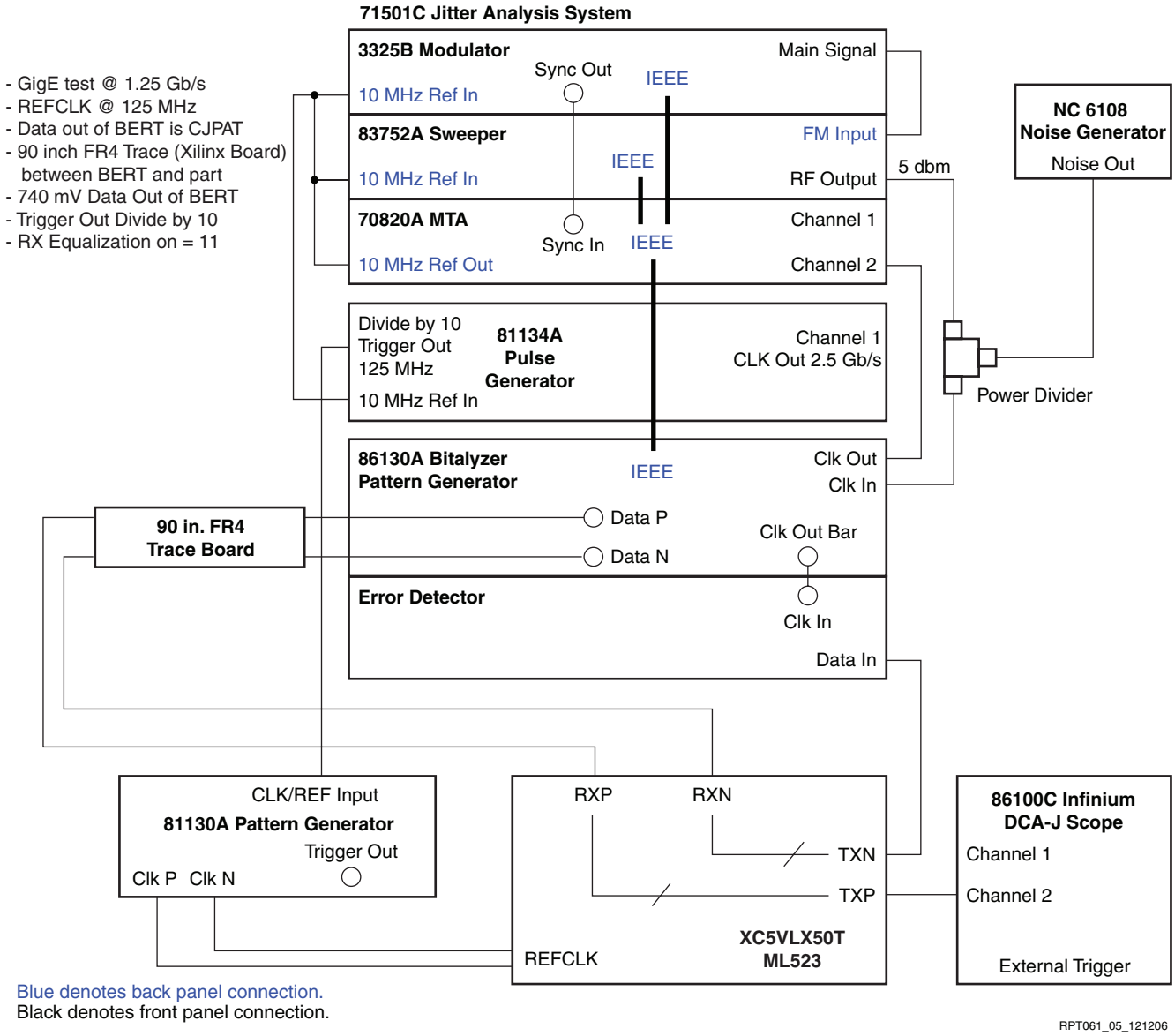

Figure 5: **Gigabit Ethernet RX Bench Test Setup**

Jitter Tolerance Test Results

Table 6 shows the minimum tolerance results for each test case. These results were based on a data rate of 1.25 Gb/s, REFCLK = 125 MHz, f_{VCO} = 1.25 Gb/s, RX_EQ = `11`, a CJPAT pattern, and a Xilinx 90-inch FR4 board. The DJ is 0.47 UI, and the RJ is 0.28 UI. Each test corner is tested for 15 minutes of error-free operation. The decomposed DJ and RJ values are added for total jitter tolerance results.

Table 6: **Total Jitter Tolerance Test Conditions and Results at 1.25 Gb/s**

Device	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	Total Jitter (UI)
Typ-1	0.9	1.08	1.08	1.08	100	0.75
	1	1.2	1.2	1.2	25	0.75
	1.1	1.32	1.32	1.32	–40	0.75
Typ-2	0.9	1.08	1.08	1.08	100	0.75
	1	1.2	1.2	1.2	25	0.75
	1.1	1.32	1.32	1.32	–40	0.75
SS-1	0.9	1.08	1.08	1.08	100	0.75
	1	1.2	1.2	1.2	25	0.75
	1.1	1.32	1.32	1.32	–40	0.75
SS-2	0.9	1.08	1.08	1.08	100	0.75
	1	1.2	1.2	1.2	25	0.75
	1.1	1.32	1.32	1.32	–40	0.75
FF-1	0.9	1.08	1.08	1.08	100	0.75
	1	1.2	1.2	1.2	25	0.75
	1.1	1.32	1.32	1.32	–40	0.75
FF-2	0.9	1.08	1.08	1.08	100	0.75
	1	1.2	1.2	1.2	25	0.75
	1.1	1.32	1.32	1.32	–40	0.75

Figure 6 shows the passing input eye at 1.25 Gb/s.

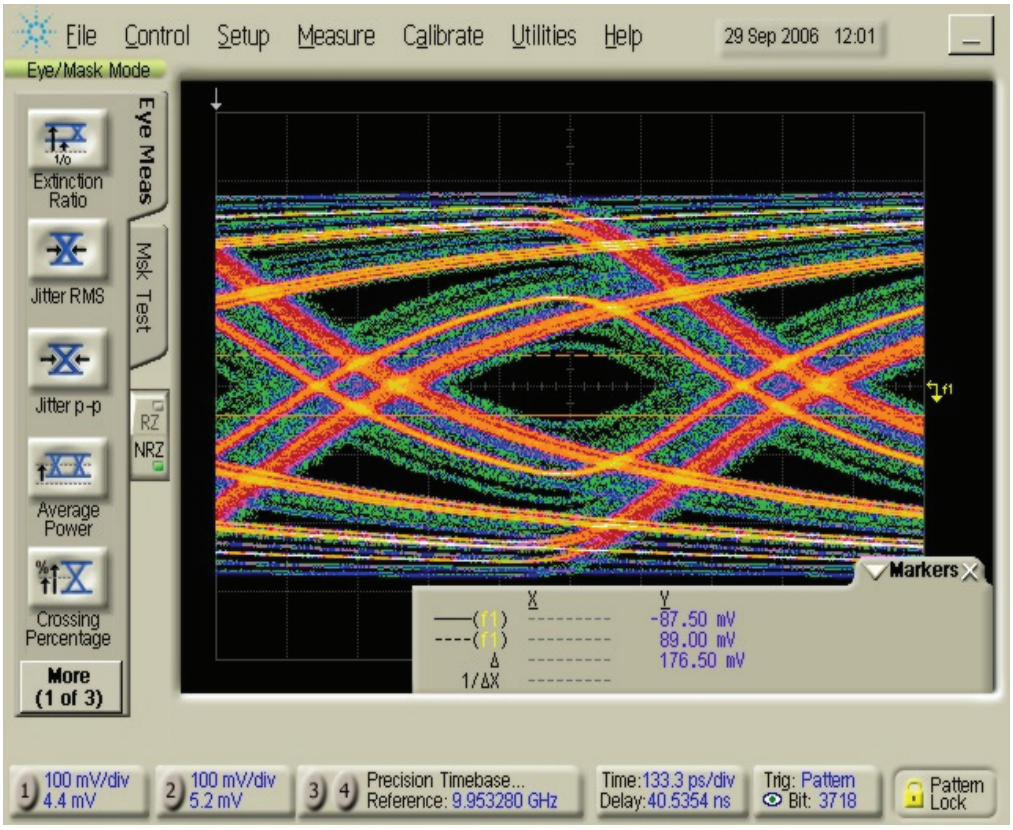

Figure 6: **Passing Input Eye at 1.25 Gb/s**

Receiver Baud Rate Tolerance Test Results

The receiver baud rate test measures the ability of the receiver to operate with input signals that vary over the allowed frequency range.

The input signals are driven from a 100Ω impedance, known-good source. The purpose of the test is to measure the performance of the receiver over ±100 ppm. The test measures the BER with a minimum input eye and maximum frequency offset.

Data is based on default symmetric ppm offsets in the ± direction. The test was done on five Virtex-5 XC5VLX50T devices at –40°C, 0°C, and 100°C with V_{CC} ±5% and ±10%. The results are shown in Figure 7 and Table 7 are for 2.5 Gb/s data rates. The measured performance margin at a 2.5 Gb/s data rate indicates sufficient margin for 1.25 Gb/s operation.

See the *Virtex-5 RocketIO GTP Transceiver User Guide* for attribute settings to skew the ppm offset in one direction.

For Reference: 0.28% frequency offset = 2800 ppm and CDR second-order loop filter = ON.

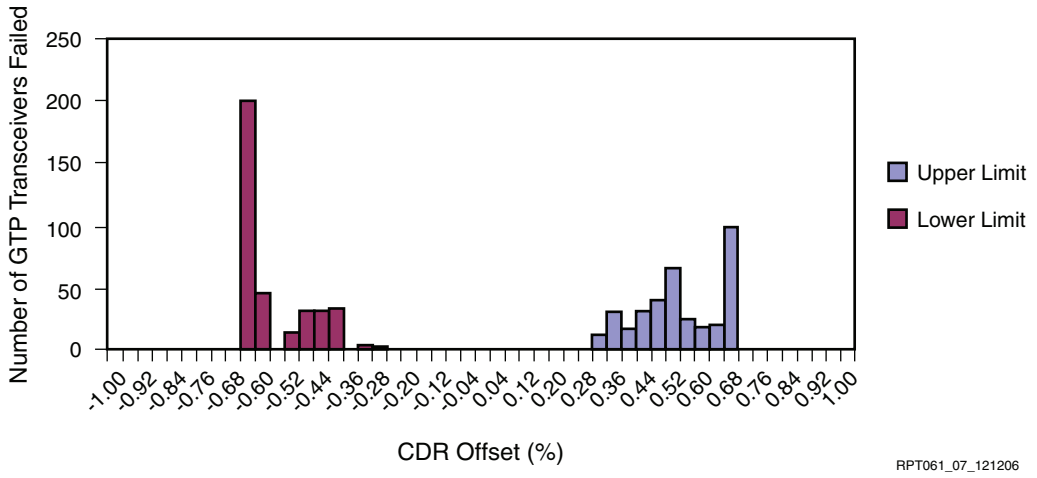

Figure 7: **Receiver PPM CDR Offset Test Results**

Table 7: **Receiver Baud Rate Test**

Reference Clock	Input Baud Rate		Test Results
	Min	Max	
125 MHz	1250 MHz – 100 ppm	1250 MHz + 100 ppm	±2700 ppm at 2.5 Gb/s

Receiver Input Sensitivity

The receiver differential amplitude test measures the minimum differential voltage amplitude between the positive and negative receiver pins with error free operation of the GTP receivers for the duration of the 0.5s test period.

The input signals are driven from a 100Ω impedance. The purpose of the test is to measure the performance of the receiver over the minimum input signal levels.

Test Setup

A variable input voltage is applied to the DUT RX from the Agilent ParBERT pattern generator, and a BER test is performed. RX input sensitivity is defined as the last passing voltage where the error detector starts to see errors.

Operating Conditions, Configurations, and Setup

Table 8 shows configurations of the TX and RX blocks.

Table 8: **GTP Transceiver Block Configurations**

TX Block	Mode/Configuration	RX Block	Mode/Configuration
Fabric Interface	10 bits	Fabric Interface	10 bits
8B/10B Encode	Disabled	8B/10B Encode	Disabled
Internal DATAWIDTH	10 bits	Internal DATAWIDTH	10 bits

Equipment Setup

The High Volume Characterization (HVC) system is used to collect the data. Table 9 lists the setup parameters for the pattern generator and the analyzer. A PRBS31 pattern is used to measure the input sensitivity. From the point of view of Gigabit Ethernet specifications, this represents a tougher test pattern on the receiver than the 8B/10B encoded data patterns.

Table 9: **HVC ParBERT Setup**

Pattern Generator Setup	Value	Analyzer Setup	Value
Output Level	START = 400 mV, STOP = 0 mV, STEP = 15 mV	Test Length	0.5s
Pattern	PRBS31	Pattern	PRBS31
Data Rate	1.250 Gb/s	Data Rate	1.250 Gb/s

Board Setup and Clock Connections

The Virtex-5 FF1136 HVC test fixture provides connections from the HVC to the DUT.

Receiver Input Sensitivity Specifications

Table 10 shows the receiver differential amplitude test limits.

Table 10: **Receiver Differential Amplitude Specification**

Differential Amplitude		Comments
Min	Max	
370	2000	mV peak-to-peak (INF 8074)
400	2000	mV peak-to-peak (1000-Base-CX)

Test Results

The characterization data for the receiver input sensitivity is shown in Figure 8 and summarized in Table 12. Table 11 lists the test details.

Table 11: **Receiver Input Sensitivity Test Details**

Test Type	Description
Test Case	RX sensitivity, differential peak-peak, in mV
Test Conditions	V_{CC} = NOM, ±5%, Temperature = –40°C to 100°C (I-Grade)
Method	RX input voltage is programmed from 400 mV to 0 mV in 15 mV steps, until the error detector sees an error.
Data Rates Tested	1.25 Gb/s
Pattern	PRBS31

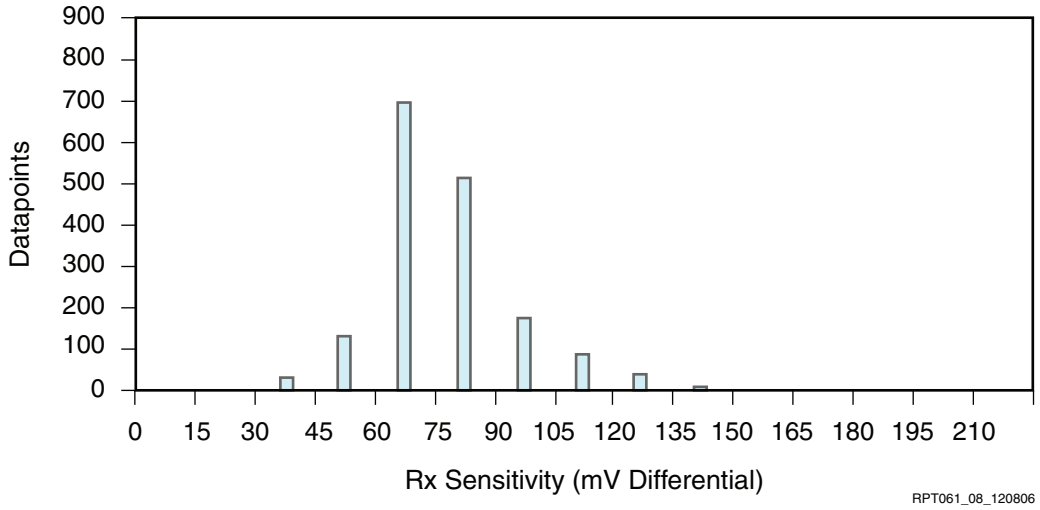

Figure 8: **Receiver Sensitivity**

Table 12: **Receiver Sensitivity Summary**

Min	Max	Mean	Median	Standard Deviation	Units
30	135	70	60	18	ps

Transmitter Electrical Tests

Test Setup

Eye closure measurements of the transmitter output are performed by the Bath Tub Curve (BTC) method, in which the random jitter component is extrapolated to 10^{-12} BER to measure the transmitter's total output jitter (TJ).

Test Equipment

Characterization of the XC5VLX50T-FF1136 GTP transceiver was performed using HVC hardware. The HVC system uses a 12-channel, 13.5 Gb/s ParBERT with integrated signal generators, power supplies, and a removable test fixture interface. Temperature control was achieved through forced air cooling and heating using a Thermonics unit. The system was developed for volume characterization of Virtex-4 MGTs and Virtex-5 GTP transceivers.

A Virtex-5 GTP test fixture was developed for the FF1136 package, which can be used for both XC5VLX50T and XC5VLX110T devices. Twelve GTP channels can be characterized in a single pass.

Board Setup and Clock Connections

The device is configured using JTAG. Power is supplied from eight programmable power supplies through connectors on the side of the fixture.

High-speed connections from the device to the ParBERT are made through SMP and SMA coaxial connectors. Blind-mate connectors are used to permit quick removal of the test fixture. A low-profile, high-speed socket from Altanova, as shown in Figure 9, was used to collect the data.

Two pairs of MGTCLKs are used to clock the six GTP_DUAL tiles in two groups of three GTP_DUAL tiles.

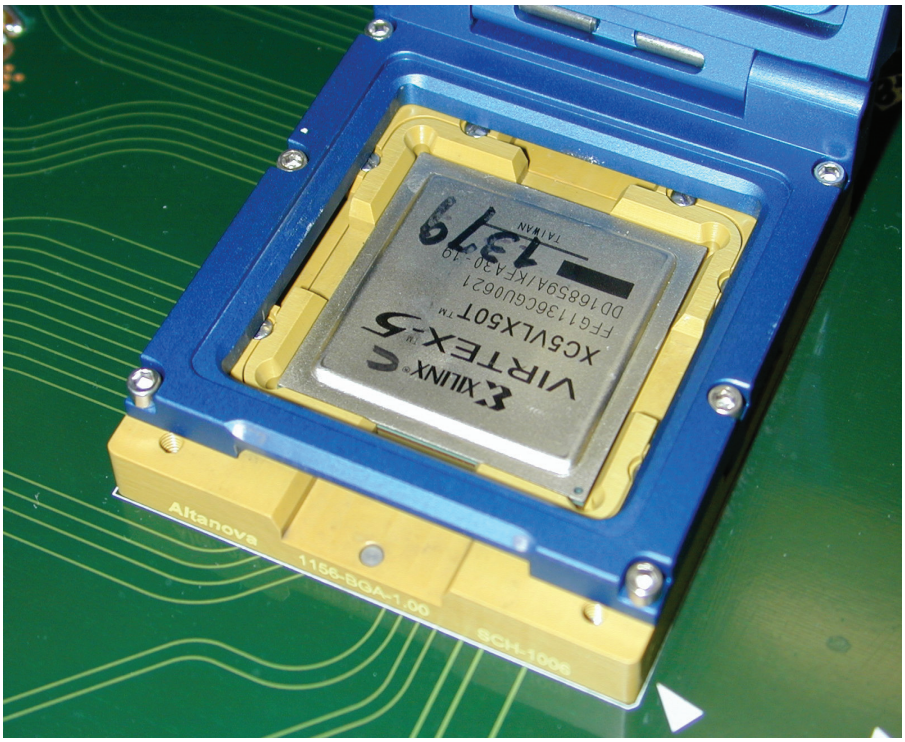

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Figure 9: **FF1136 Low-Profile High-Speed Socket**

Test Conditions

The tests were performed at –40°C, 0°C, and 100°C at nominal and V_{CC} (±5%) values. Table 13 lists the nominal voltages for the power supplies.

Table 13: **Power Supply Voltage Ranges**

Supply	Use	Nominal Voltage
V_{CCINT}	FPGA Logic main supply and GTP PCS	1.00V
V_{CCAUX}	FPGA Logic AUX supply, low noise	2.50V
V_{CCIO}	Fabric I/O supply	2.50V
MGTAVCC	GTP main supply	1.00V
MGTAVCCPLL	GTP supply for PLLs, low noise	1.20V
MGTVTTX	GTP TX supply	1.20V
MGTVTRX	GTP RX supply	1.20V
MGTVTTRXC	GTP RX *always on* supply used to maintain termination resistor calibration when GTP transceiver is powered down	1.20V

1. *All* supply voltages were adjusted together.
2. All GTP supplies use L/C passive filtering. See the *Virtex-5 RocketIO GTP Transceiver User Guide* for details.

Test Details

Five pieces each of the typical, slow, and fast corner material were characterized using HVC over voltage and temperature corners. All 12 GTP transceivers on each unit were tested.

The configuration designs use FPGA logic loopback in single-byte mode with both TXUSRCLK/2 and RXUSRCLK/2 clocked from TXOUTCLK. The configuration provides connections to GTP_RESET, CDR_RESET, and the DRP interface. For all test cases, the RX is configured for termination to GND with the RX front-end using internal AC coupling.

The data flow through the GTP transceiver is shown in Figure 10. Serial data to the RX is provided by the Agilent ParBERT pattern generator. This data is converted to 8-bit or 10-bit data at the PMA deserializer and passed through the PCS. The RX parallel data port is connected to the TX parallel data port in the FPGA logic. The 8-bit or 10-bit parallel data is then sent through the TX PCS and converted back to serial data at the TX PMA. The TX serial data is connected to the ParBERT data analyzer.

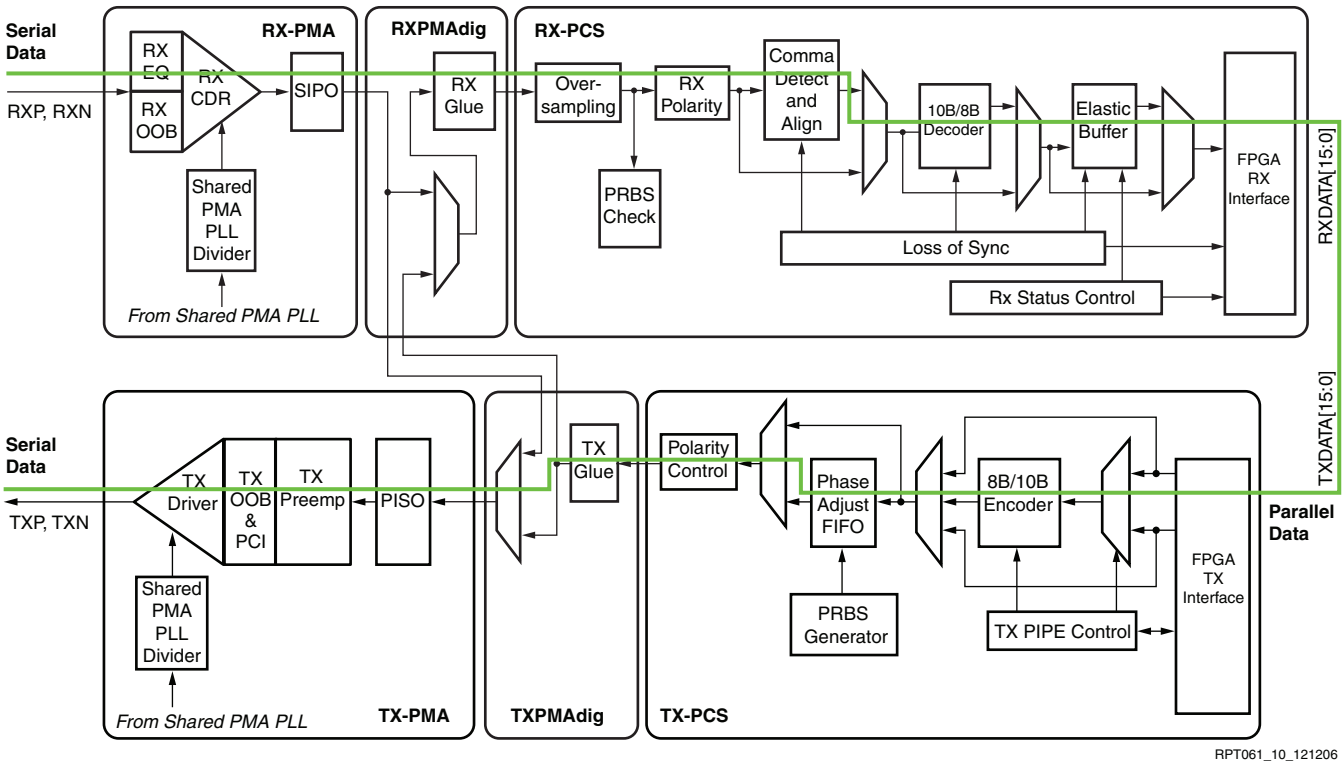

Figure 10: **Data Flow through the GTP Transceiver**

1000BASE-CX Transmitter Specifications

Table 14 shows the 1000BASE-CX transmitter specifications. Figure 11 shows the transmitter output mask and Table 15 lists the parameters. Figure 12 shows the jitter output eye at 1.25 Gb/s

Table 14: **1000BASE-CX Transmitter Specifications**

Description	Value	Units
Type	(P) ECL	
Data rate	1000	Mb/s
Clock tolerance	±100	ppm
Nominal signalling speed	1250	MBd
Rise/Fall time (20% - 80%)		
Maximum	327	ps
Minimum	85	ps

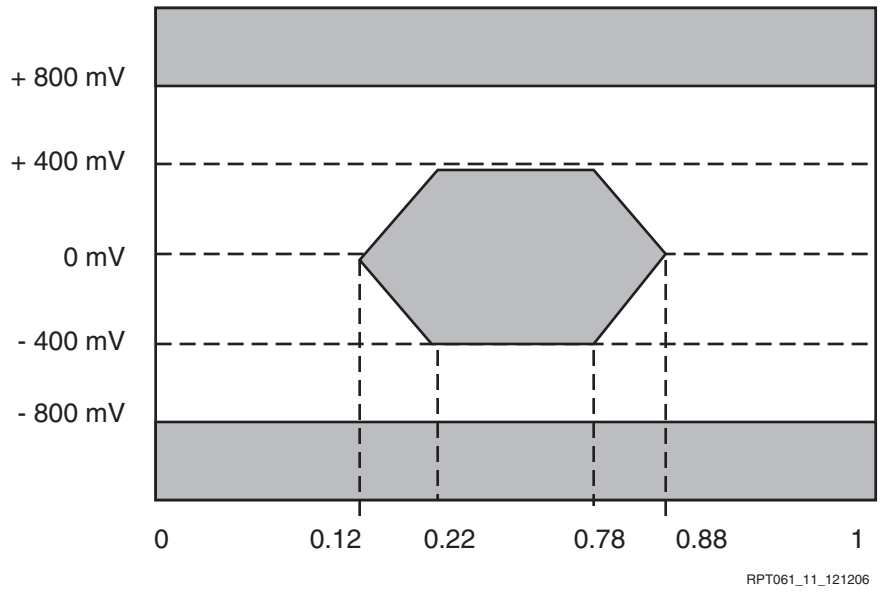

Figure 11: **Transmitter Output Mask**

Table 15: **1000BASE-CX Transmitter Mask Parameters – Jitter**

Line Rate	Maximum Jitter Specification	Comments
1250 Mb/s	0.1UI	Deterministic Jitter
	0.24UI	Total Jitter

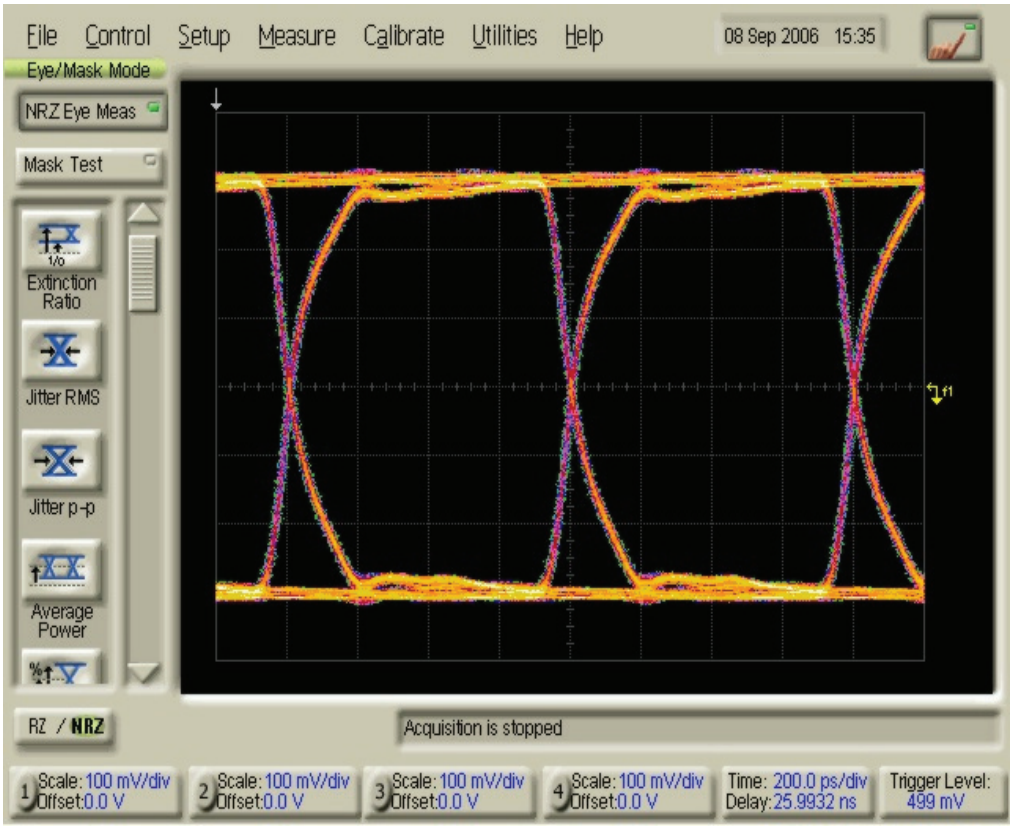

Figure 12: **Transmitter Output Eye at 1.25 Gb/s**

Jitter Generation, Rise/Fall Time, and Amplitude Tests

When directly measuring the eye, the output signals are driven into a 100Ω impedance. The purpose of the test is to match the output eye against the mask shown in Figure 11. The test also measures the rise/fall times of the individual outputs between 20% to 80% of their output points. These measurements are taken at the input to the connector.

Jitter Generation Test Results

Jitter Generation at 1.25 Gb/s

Table 16 summarizes the test conditions for jitter measured at 1.25 Gb/s. Table 17 summarizes the test results at 1.25 Gb/s shown in Figure 13.

Table 16: **Test Conditions for Jitter at 1.25 Gb/s (I-Grade)**

Condition	Description
Test Case	Eye Width in UI (Unit Interval)
Conditions	V_{CC} = NOM, ±5%; Temperature = -40°C to 100°C (I-Grade)
Method	BTC method. Eye Step = 0.01 UI, and number of bits collected = 10^8. A BER test is performed at each step in the eye, and the BER rate is calculated. The Dual Dirac method is used to extrapolate the eye opening at BER = 10^{-12}.
Configuration/Standard	Data Rate = 1.25 Gb/s, REFCLK=125 MHz
Pattern	PRBS7, 500 mV p-p

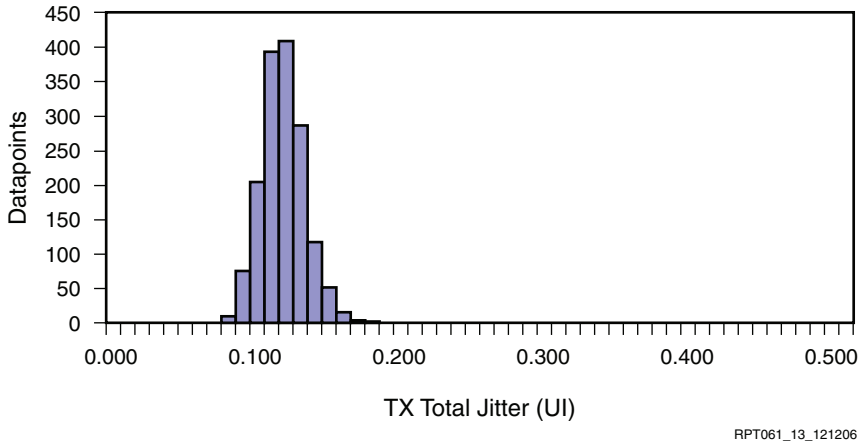

Figure 13: **XC5VLX50T TX Jitter 1.25 Gb/s (Reference Clock = 125 MHz) I-grade**

Table 17: **Transmitter Jitter Summary**

Min	Max	Mean	Median	Standard Deviation	Units
0.084	0.186	0.123	0.121	0.014	ps

Transmitter Rise and Fall Times Test Results

The GTP TX output rise and fall time measurements are made as a function of the MGTAVTTTX voltage supply. In these tests, the data rate is 2.5 Gb/s, REFCLK = 250 MHz, and the operating temperature was –40°C, 0°C, and 100°C. The resulting trends are plotted in the data plots shown in the following figures. The rise and fall times measured at 2.5 Gb/s is a typical representation of GTP behavior at 1.25 Gb/s.

Figure 14 and Figure 15 show the histogram distribution of the rise time of the XCV5LX50T TX side output at a 2.5 Gb/s data rate, with a `00001111` data pattern, and MGTAVTTTX equal to 1.2V ± 5%. Table 18 summarizes the transmitter rise time.

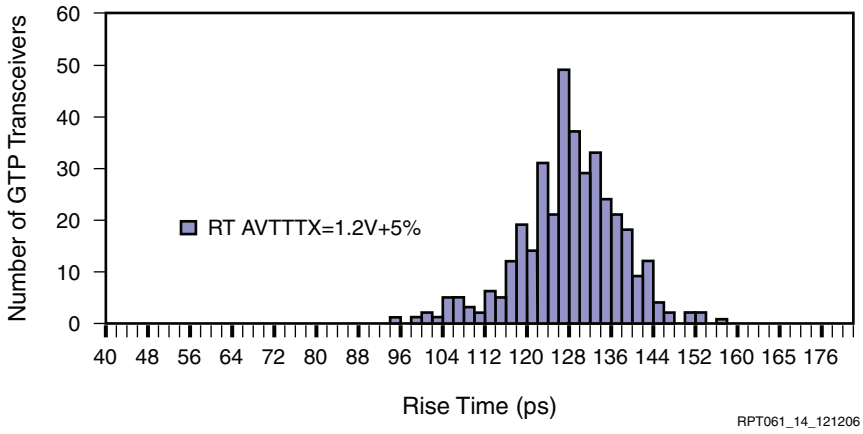

Figure 14: **XCV5LX50T Rise Time at AVTTTX = 1.26V**

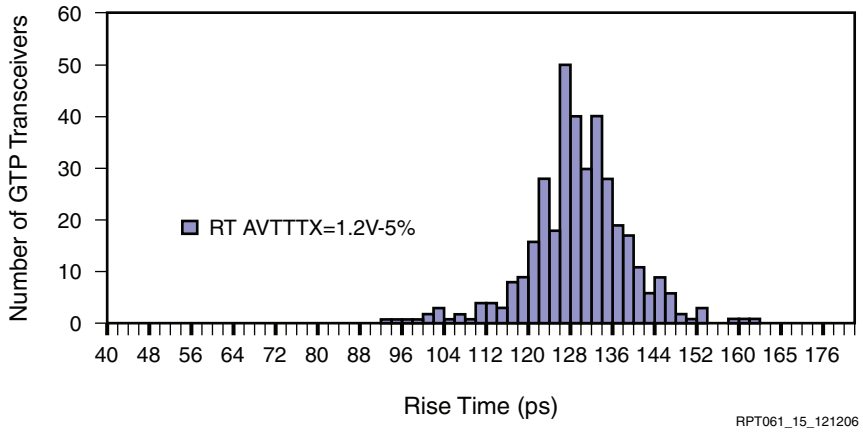

Figure 15: **XCV5LX50T Rise Time at AVTTTX = 1.14V**

Table 18: **Transmitter Rise Time Summary**

Min	Max	Mean	Median	Standard Deviation	Units
92	162	126	127	9.43	ps

Figure 16 and Figure 17 show the histogram distribution of the fall time of the XCV5LX50T TX side output at a 2.5 Gb/s data rate, with a `00001111` data pattern, and MGTAVTTTX equal to 1.2V ± 5%. Table 19 summarizes the transmitter fall time.

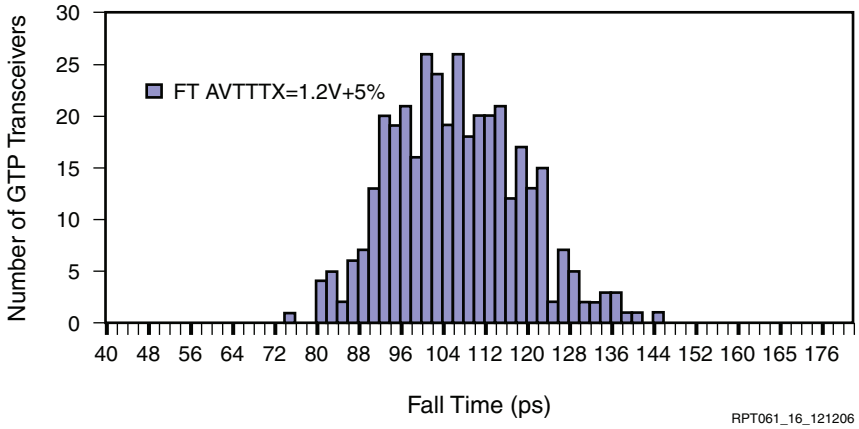

Figure 16: **XCV5LX50T Fall Time at AVTTTX = 1.26V**

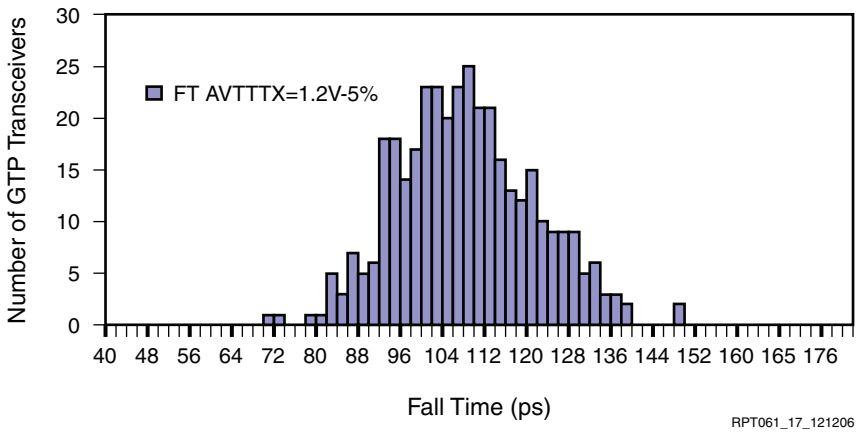

Figure 17: **XCV5LX50T Fall Time at AVTTTX = 1.14V**

Table 19: **Transmitter Fall Time Summary**

Min	Max	Mean	Median	Standard Deviation	Units
70	148	105	105	12.29	ps

Transmitter Differential Amplitude Test Results

The transmitter differential amplitudes measures the differential voltage amplitude between the positive and negative GTP transceiver pins when the transmit eye is fully open.

The bench setup was used to measure the output amplitudes for the programmable voltage control settings. Data was measured at TX data rate of 2.5 Gb/s with a `00001111` pattern. This is a typical representation of GTP behavior at 1.25 Gb/s operation.

MGTAVTTTX Trend

Figure 18 shows the transmitter output supply voltage trend for the GTP_DUAL transmitters at a 2.5 Gb/s data rate with a `00001111` data pattern. As shown in the figure, the TX average peak-to-peak differential output voltage decreases whenever TXDIFFCTRL setting increases.

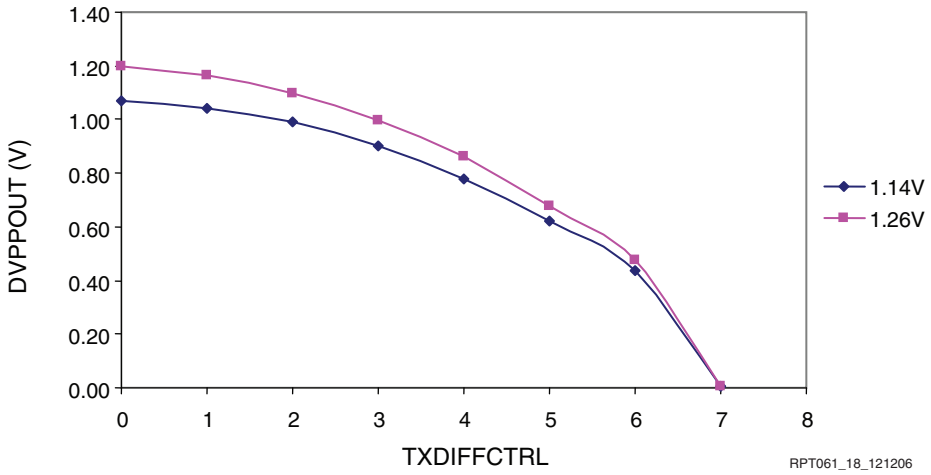

Figure 18: **XCV5LX50T MGTAVTTTX Trend at 2.5 Gb/s with REFCLK = 250 MHz**

Temperature Trend

Figure 19 shows the temperature trend at a 2.5 Gb/s data rate with a `00001111` data pattern. As shown in the figure, the temperature does not have significant effects on the TX average peak-to-peak differential output voltage.

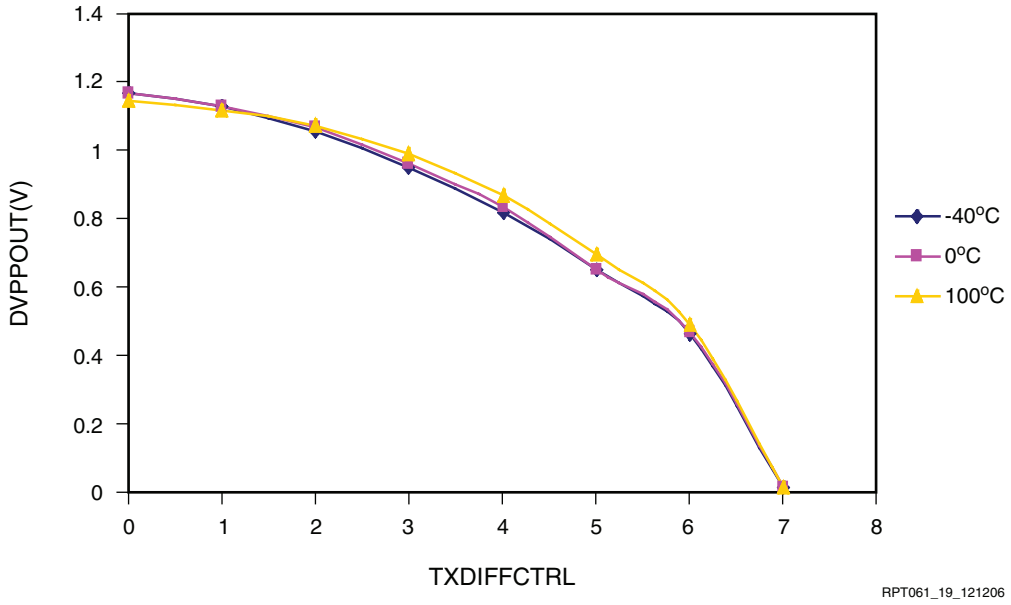

Figure 19: **XCV5LX50T Temperature Trend at 2.5 Gb/s with REFCLK = 250 MHz**

References

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