Virtex-5 XAUI Protocol Standard

Characterization Test Report

RPT062 (v1.0) December 12, 2006

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/12/06	1.0	Initial Xilinx release.

Virtex-5 XAUI Protocol Standard

Introduction

Virtex™-5 system connectivity technology delivers the lowest power solutions for building high-speed, high-bandwidth connections between devices, boards, and boxes. The RocketIO™ GTP transceiver design and proven SelectIO™ parallel I/O technologies enable flexible bridging between emerging serial standards and existing parallel standards. The features of the Virtex-5 GTP transceivers include:

- Current Mode Logic (CML) drivers/buffers with configurable termination, voltage swing, and coupling.
- Programmable transmit pre-emphasis and receive equalization for optimal signal integrity.
- Line rates from 500 Mb/s to 3.2 Gb/s with optional 5x over-sampling to bring the low-end down to 100 Mb/s.
- Optional built-in PCS features, such as 8B/10B encoding/decoding, comma alignment, channel bonding, and clock correction.
- Fixed latency modes for minimized, deterministic datapath latency.
- Out-of-band signaling support (specifically designed to address the requirements of PCI Express® and Serial ATA protocols).
- Built-in pseudo-random bitstream (PRBS) generation/checking logic for easier bit-error rate checking.
- A configuration wizard provided in the CORE Generator™ tool and a bit error rate tester (IBERT) integrated into the ChipScope™ Pro tools for easy implementation of GTP transceiver interfaces.

This document presents the GTP transceiver physical layer (PHY) electrical performance against the 10 Gb Attachment Unit Interface (XAUI) specifications across process, voltage, and temperature conditions. GTP transmitter and receiver electrical characteristics were measured using a combination of lab bench setups and a High Volume Characterization (HVC) system. The methods used to characterize the transceiver are based on the standards specifications and also follow the best-practice methods for some parameters.

Background

The 10 Gb Attachment Unit Interface (XAUI) is defined in the 10G Ethernet specification (IEEE 802.3-2005 clause 47). In addition XAUI is used as a generic chip-to-chip and backplane interface by many equipment providers. The XAUI is primarily intended as a point-to-point interface of up to approximately 50 cm between integrated circuits using controlled impedance traces on low-cost printed-circuit boards (PCBs).

The following sections describe the tests performed to show the basic operation and inter-workings of the interface. The system diagram, shown in Figure 1, has the XAUI interface highlighted. This document refers to testing at the TX output pins and the RX input pins. It is expected that in many implementations a backplane interconnect will exist between the TX and RX devices.

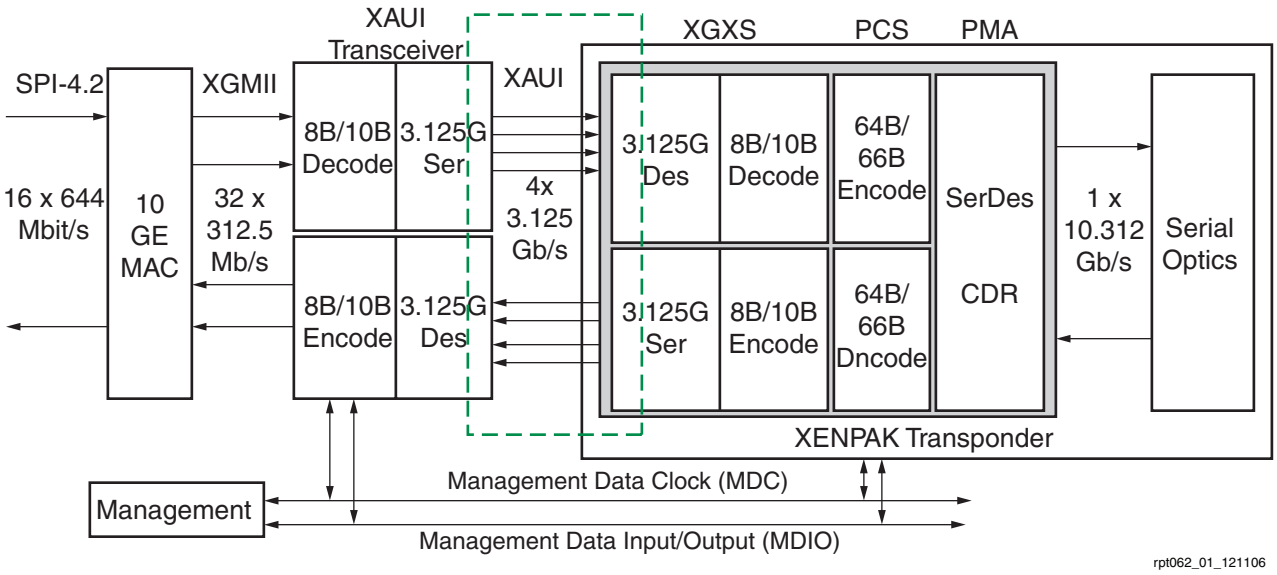

Figure 1: **XAUI and XGXS Relationships**

Test Equipment

Both bench and ATE based test equipment was used to characterize the GTP transceivers. Bench setups were used for the majority of the RX jitter and TX amplitude measurements. The ATE setup was based on a multi-channel ParBERT and was used for TX jitter and general characterization.

Test Conditions

Table 1 shows the operating supply voltages and Table 2 shows the operating temperatures.

Table 1: **Operating Supply Voltages**

Condition	MGTAVCC	MGTAVCCPLL	MGTAVTTRX	MGTAVTTTX	Units
V_{MIN}	0.95	1.14V	1.14V	1.14V	V
V_{NOM}	1.0	1.20V	1.20V	1.20V	V
V_{MAX}	1.05	1.26V	1.26V	1.26V	V

Notes:

1. Other FPGA voltages remain at nominal values.
2. Some tests performed at ±10% V_{CC}.

Table 2: **Operating Temperatures**

Condition	Temperature (Case for Bench Measurements)
T_{MAX}	100°C
T_{ROOM}	25°C(1)
T_{MIN}	–40°C

Notes:

1. Some tests performed at 0°C.

The devices chosen for characterization cover the process corner material. The number of devices varies. A minimum of two devices each were used from slow, typical, and fast process corners. The HVC system uses a larger sample size with five devices from each corner and 12 GTP transceivers tested per device across voltage and temperature specifications.

Summary of Results

Table 3 is a summary table of the XAUI specification requirements and the test results for the Virtex-5 GTP transceiver.

Table 3: **Summary of XAUI Test Results**

	XAUI Specifications		Virtex-5 GTP Test Results		Units	Compliant?	Comments
	Min	Max	Min	Max			
TX Specifications							
TX Deterministic Jitter (DJ)		0.17		0.16	UI	Yes	
TX Total Jitter (TJ)		0.35		0.32	UI	Yes	
Output Amplitude(1)	800	1600	900	1100	mV p-p differential	Yes	Measured at TXCTRL = 3. Output levels are programmable.
Rise Time(1)	60	130	92	162	ps	No	
Fall Time(1)	60	130	70	148	ps	No	
TX Differential Return Loss		3		7	dB	Yes	Measured within the range of 0 to 2.5 GHz. See Figure 22.
RX Specifications							
RX Deterministic Jitter (DJ)	0.37		0.35		UI	Yes	Additional SJ was added for compliance testing
RX Sinusoidal Jitter (SJ)	0.10		0.196		UI	Yes	
RX Total Jitter (TJ)	0.65		0.746		UI	Yes	
RX Input Sensitivity	200	1600	135		mV p-p differential	Yes	
RX Differential Return Loss	10		8		dB	No	Measured within the range of 0 to 2.5 GHz. See Figure 9.
RX Common Mode Return Loss	6		8		dB	Yes	Measured within the range of 0 to 2.5 GHz. See Figure 10.

Notes:

1. These tests were performed at 2.5 Gb/s.

Receiver Electrical Tests

Lab Board Setup

An ML523 evaluation board, with an Oztek socket hosting FF1136 package, is used to test the Virtex-5 devices. The Xilinx GUI-based XBERT platform is used for DRP loadings. A Chipscope Pro analyzer is used to configure the part.

XAUI Receiver Specifications

Receiver characteristics are summarized in Table 4. To test for receiver jitter tolerance, confirm that the receiver can operate with the worst case signal input jitter.

Table 4: **Receiver Characteristics**

Parameter	Value	Units
Baud rate tolerance	3.125 ±100	GBd ppm
Unit interval (UI) nominal	320	ps
Receiver coupling	AC	
Return loss(1)		
Differential	10	dB
Common mode	6	dB
Jitter amplitude tolerance(2)	0.65	UI_{p-p}

Notes:

1. Relative to 100 Ω differential and 25 Ω common mode. See"Receiver Return Loss" for input impedance details.
2. See "Total Jitter Tolerance" for jitter tolerance details.

Total Jitter Tolerance

Jitter tolerance measurements at a 3.125 Gb/s data rate are performed based on the 10 Gigabit Ethernet XAUI interface jitter tolerance test methodology. In this measurement, all three required jitter components—deterministic jitter (DJ), random jitter (RJ), and sinusoidal jitter (SJ)—are added to the input datapath. Based on channel calibration, DJ and RJ jitter components are fixed to introduce 0.55 UI of total jitter, and the SJ modulation is added and swept as a function of frequency to the failure point. The sinusoidal jitter tolerance mask specification is shown in Figure 2.

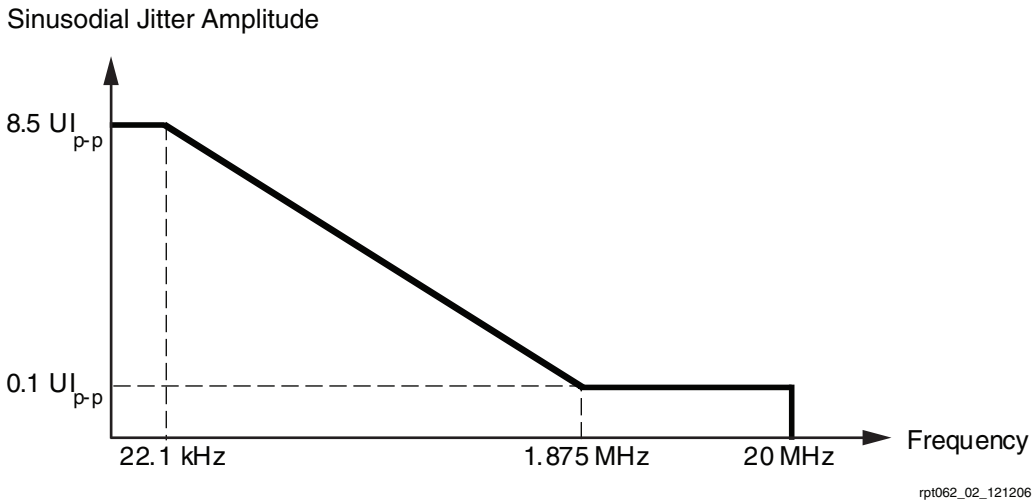

Figure 2: **Single-Tone Sinusoidal Jitter Mask**

The input signals are driven from a 100Ω impedance, known-good source generating a CJPAT test pattern. The purpose of the test is to feed in a jittery signal which meets the jitter mask shown in Figure 3 and measure the receiver's lock status, stability, and data BER. The receiver must be AC coupled, and the input is measured at the pin of the receiver. The receiver mask parameters are shown in Table 5.

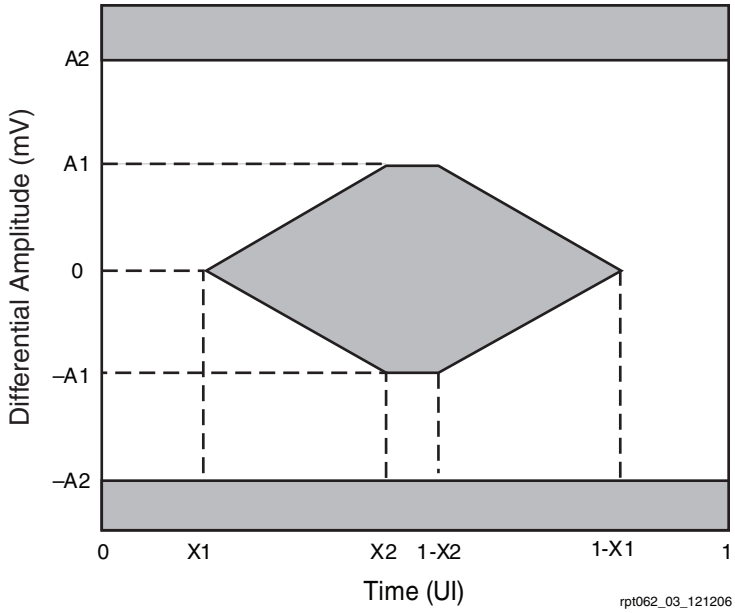

Figure 3: **RX Eye Diagram**

Table 5: **Receiver Mask Parameters**

Parameter	Value	Units
X1	0.275	UI
X2	0.400	UI
A1	100	mV
A2	800	mV

DJ and RJ Components

The DJ component is generated by passing the CJPAT test pattern through 30 inches of Tyco FR4 XAUI backplane with two HMZd backplane connectors. The RJ component from the NoiseCom random noise source is added to the pattern generator clock source using a power splitter. With these two jitter sources in place, the jitter decomposition measurement is made using the Agilent DCA-J scope, as shown in Figure 4. To compute the total jitter in this measurement at 10^{-12} BER, the scope math function multiplies the RJ rms value by 14 and adds it to the DJ number. Because the Tyco 30-inch backplane introduces about 0.35 UI of DJ, the random noise source is calibrated to add another 0.20 UI of peak-to-peak RJ for a total of 0.55 UI of DJ + RJ component.

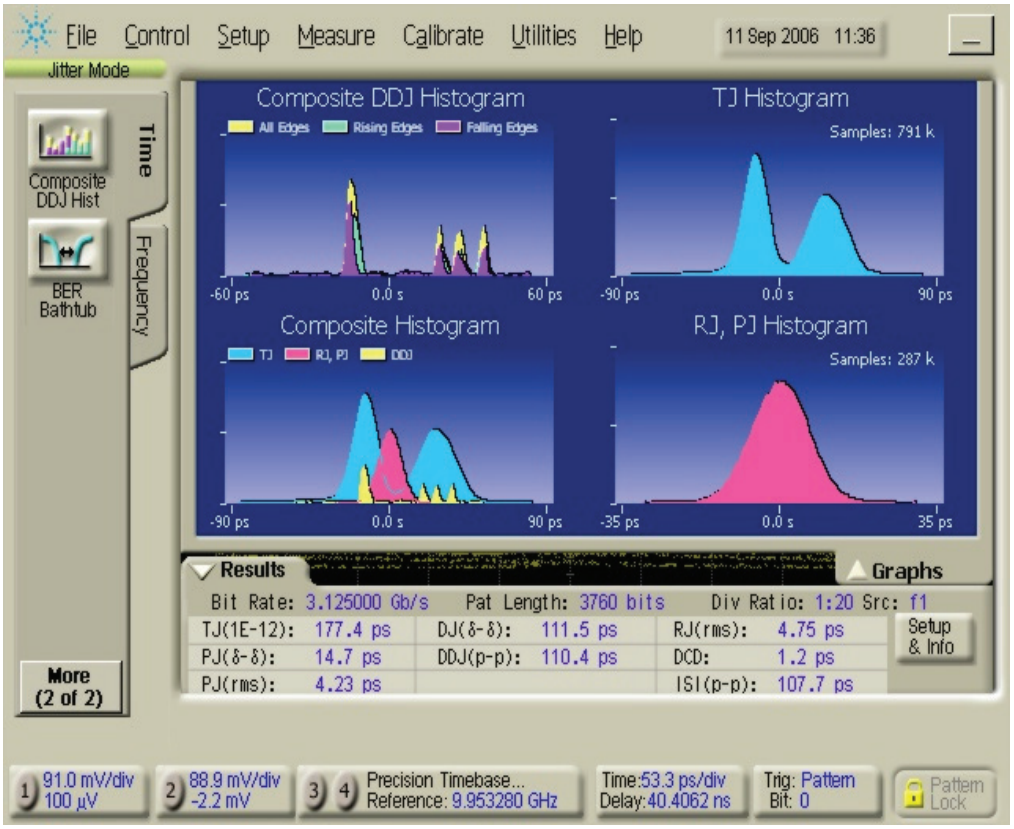

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Figure 4: **Jitter Decomposition at 3.125 Gb/s over a 30-inch Tyco Backplane**

SJ Component

With fixed DJ and RJ components in place, the sinusoidal jitter modulation is added and swept as a function of frequency to the point where the device starts to fail. Figure 5 shows a typical sinusoidal jitter tolerance sweep measurement on top of the present DJ and RJ components. The 10 MHz SJ modulation point in Figure 5 is the equipment maximum and not the worst case.

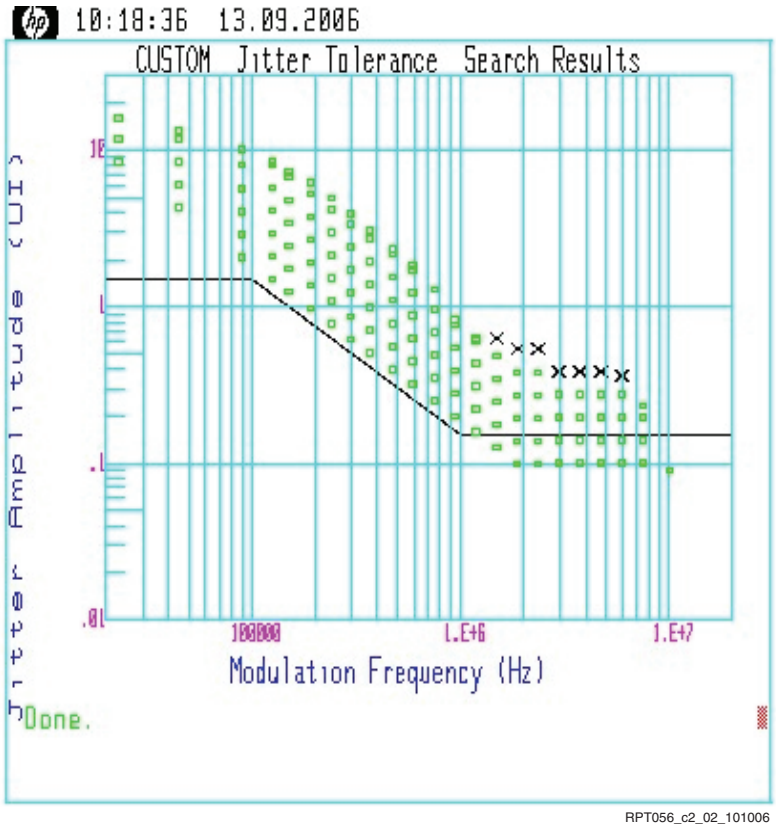

Figure 5: **Sinusoidal Jitter**

Jitter Tolerance Test Setup

Jitter tolerance measurements at a 3.125 Gb/s data rate using a backplane, external random noise source, and sinusoidal modulation are performed using the test setup as shown in Figure 6.

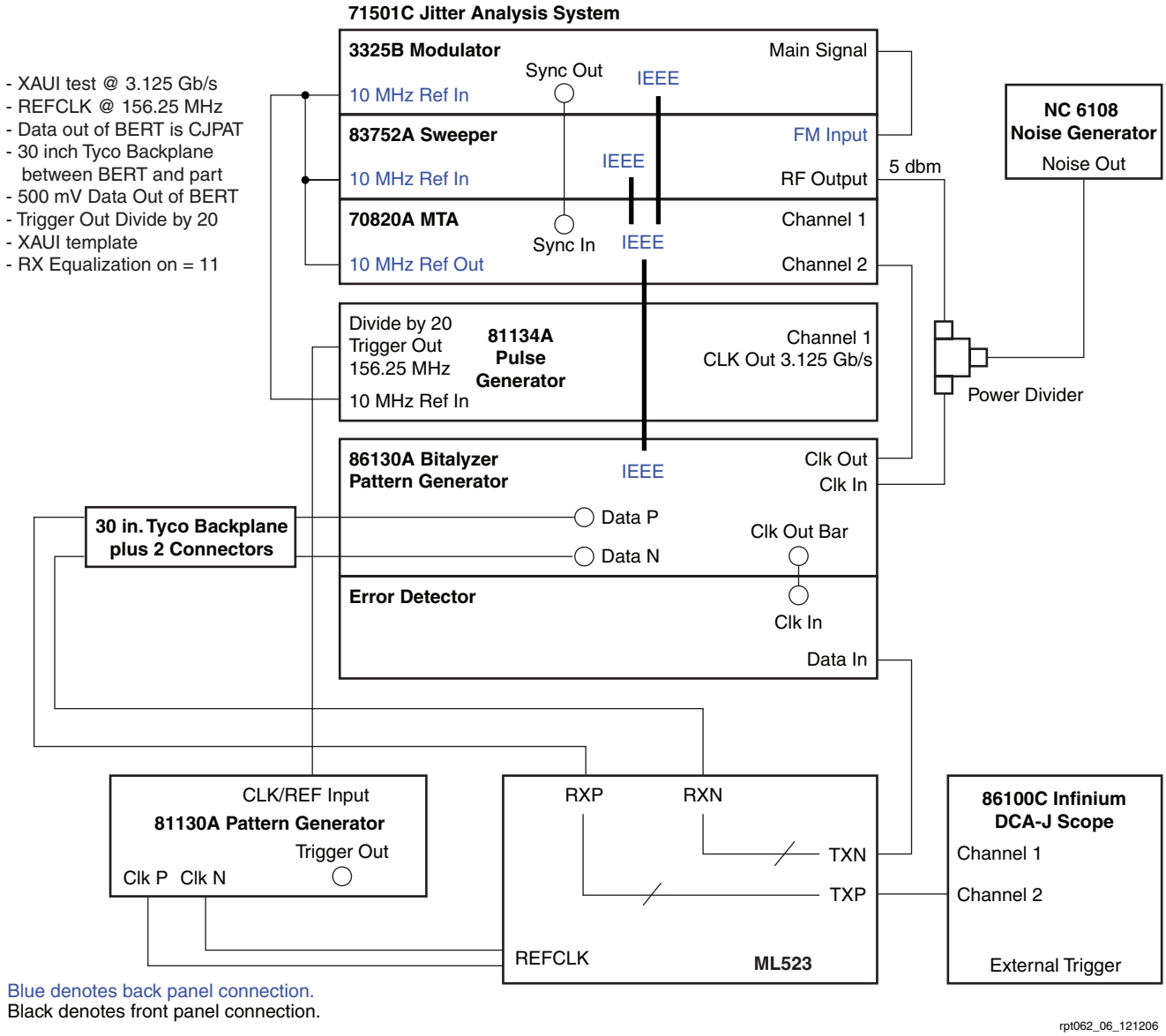

Figure 6: **XAUI RX Test Setup**

Jitter Tolerance Test Results

Table 6 shows the minimum tolerance results for each test case. These results were based on a data rate of 3.125 Gb/s, REFCLK = 156.25 MHz, f_{VCO} = 1.5625 Gb/s, RX_EQ = 11, a CJPAT pattern, and a Tyco 30-inch backplane. The DJ is 0.350 UI, and the RJ is 0.200 UI. The sinusoidal jitter (SJ) tolerance is measured as the modulation frequency is swept, and the minimum SJ tolerance point is recorded. The decomposed DJ and RJ values are added to SJ for total jitter tolerance results.

Table 6: **Total Jitter Tolerance Test Conditions and Results at 3.125 Gb/s**

Device	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	Jitter Tolerance	
						SJ (UI)	TJ (UI)
Typ-1	0.9	1.08	1.08	1.08	100	0.384	0.934
	1	1.2	1.2	1.2	25	0.384	0.934
	1.1	1.32	1.32	1.32	–40	0.384	0.934
Typ-2	0.9	1.08	1.08	1.08	100	0.274	0.824
	1	1.2	1.2	1.2	25	0.274	0.824
	1.1	1.32	1.32	1.32	–40	0.196	0.746
Typ-3	0.9	1.08	1.08	1.08	100	0.384	0.934
	1	1.2	1.2	1.2	25	0.384	0.934
	1.1	1.32	1.32	1.32	–40	0.384	0.934
Typ-4	0.9	1.08	1.08	1.08	100	0.274	0.824
	1	1.2	1.2	1.2	25	0.274	0.824
	1.1	1.32	1.32	1.32	–40	0.274	0.824
Typ-5	0.9	1.08	1.08	1.08	100	0.384	0.934
	1	1.2	1.2	1.2	25	0.384	0.934
	1.1	1.32	1.32	1.32	–40	0.274	0.824
Typ-6	0.9	1.08	1.08	1.08	100	0.274	0.824
	1	1.2	1.2	1.2	25	0.274	0.824
	1.1	1.32	1.32	1.32	–40	0.274	0.824
Typ-7	0.9	1.08	1.08	1.08	100	0.274	0.824
	1	1.2	1.2	1.2	25	0.274	0.824
	1.1	1.32	1.32	1.32	–40	0.274	0.824
FF-1	0.9	1.08	1.08	1.08	100	0.196	0.746
	1	1.2	1.2	1.2	25	0.384	0.934
	1.1	1.32	1.32	1.32	–40	0.274	0.824

Table 6: **Total Jitter Tolerance Test Conditions and Results at 3.125 Gb/s *(Continued)***

Device	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	Jitter Tolerance	
						SJ (UI)	TJ (UI)
FF-2	0.9	1.08	1.08	1.08	100	0.274	0.824
	1	1.2	1.2	1.2	25	0.196	0.746
	1.1	1.32	1.32	1.32	–40	0.196	0.746
SS-1	0.9	1.08	1.08	1.08	100	0.274	0.824
	1	1.2	1.2	1.2	25	0.274	0.824
	1.1	1.32	1.32	1.32	–40	0.196	0.746
SS-2	0.9	1.08	1.08	1.08	100	0.196	0.746
	1	1.2	1.2	1.2	25	0.274	0.824
	1.1	1.32	1.32	1.32	–40	0.274	0.824

The bars in the histogram plot in Figure 7 show the number of GTP test condition instances at each total jitter tolerance value across process, temperature, and voltage corners for a BER of 10^{-12}. In Figure 7, Average (UI) = 0.840, and Standard Deviation = 0.065.

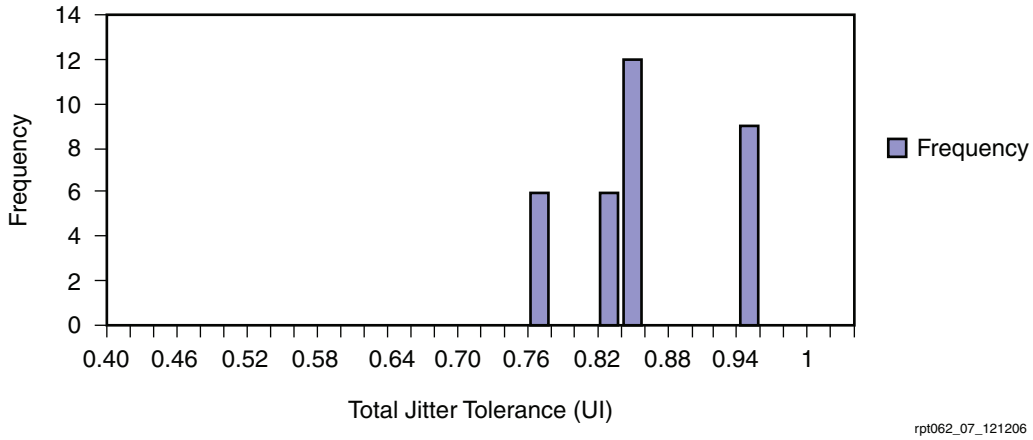

Figure 7: **Total Jitter Tolerance at 3.125 Gb/s**

Receiver Input Sensitivity

The receiver differential amplitude test measures the minimum differential voltage amplitude between the positive and negative receiver pins with error free operation of the GTP receivers for the duration of the 0.5s test period. The input signals are to be driven from a 100Ω impedance, known-good source. The test measures the BER with a minimum input signal per Table 5.

Test Setup

A variable input voltage is applied to the DUT RX from the Agilent ParBERT pattern generator, and a BER test is performed. RX input sensitivity is defined as the last passing voltage where the error detector starts to see errors.

Operating Conditions, Configurations, and Setup

Table 7 shows configurations of the TX and RX blocks.

Table 7: **GTP Transceiver Block Configurations**

TX Block	Mode/Configuration	RX Block	Mode/Configuration
Fabric Interface	10 bits	Fabric Interface	10 bits
8B/10B Encode	Disabled	8B/10B Encode	Disabled
Internal DATAWIDTH	10 bits	Internal DATAWIDTH	10 bits

Equipment Setup

The High Volume Characterization (HVC) system is used to collect the data. Table 8 lists the setup parameters for the pattern generator and the analyzer. A PRBS31 pattern is used to measure the input sensitivity. From the point of view of XAUI specifications, this represents a tougher test pattern on the receiver than the 8B/10B encoded data patterns.

Table 8: **HVC ParBERT Setup**

Pattern Generator Setup	Value	Analyzer Setup	Value
Output Level	START = 400 mV, STOP = 0 mV, STEP = 15 mV	Test Length	0.5s
Pattern	PRBS31	Pattern	PRBS31
Data Rate	3.125 Gb/s	Data Rate	3.125 Gb/s

Board Setup and Clock Connections

The Virtex-5 FF1136 HVC test fixture provides connections from the HVC to the DUT.

Receiver Differential Amplitude Specification

Table 9 shows the receiver differential amplitude test limits.

Table 9: **Receiver Differential Amplitude Specification**

Differential Amplitude		Comments
Min	Max	
200	1600	mV peak-to-peak

Test Results

Table 10 lists the test details. The characterization data for the receiver input sensitivity is summarized in the histogram shown in Figure 8 and summarized in Table 11.

Table 10: **Receiver Input Sensitivity Test Details**

Test Type	Description
Test Case	RX sensitivity, differential peak-peak, in mV
Test Conditions	V_{CC} = NOM, ±5%, Temperature = –40°C to 100°C (I-Grade)
Method	RX input voltage is programmed from 400 mV to 0 mV in 15 mV steps, until the error detector sees an error.
Data Rates Tested	3.125 Gb/s
Pattern	PRBS31
Observation	Reported value is differential (peak-peak)

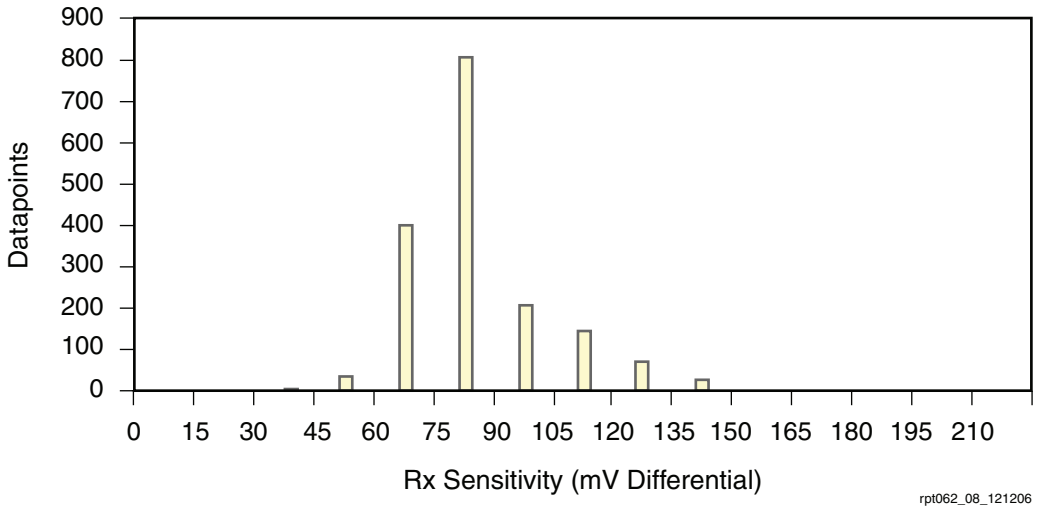

Figure 8: **Receiver Sensitivity**

Table 11: **3.125 Gb/s Receiver Sensitivity Summary**

Min	Max	Mean	Median	Standard Deviation	Units
45	135	78	75	18	mV

Receiver Return Loss

The receiver input should have a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to 2.5 GHz. This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100Ω for differential return loss and 25Ω for common mode.

The frequency domain return loss measurements (Figure 9 and Figure 10) were made using the UNH inter-operability lab guidelines. The four traces represent different GTP receivers with varying PCB trace lengths. The common mode return loss is within the requirements of the XAUI specifications. The return loss measurements based on the UNH inter-operability labs testing show a differential return loss of 8 dB at 2.5 GHz.

Higher return loss values (more positive) increase the amount of reflections back to the transmitter resulting in more inter-symbol interference (ISI). The GTP receiver equalization circuits can mitigate the effects of eye closure due to the reflection. The UNH inter-operability lab testing showed no increase in receiver BER due to the higher receiver differential return loss.

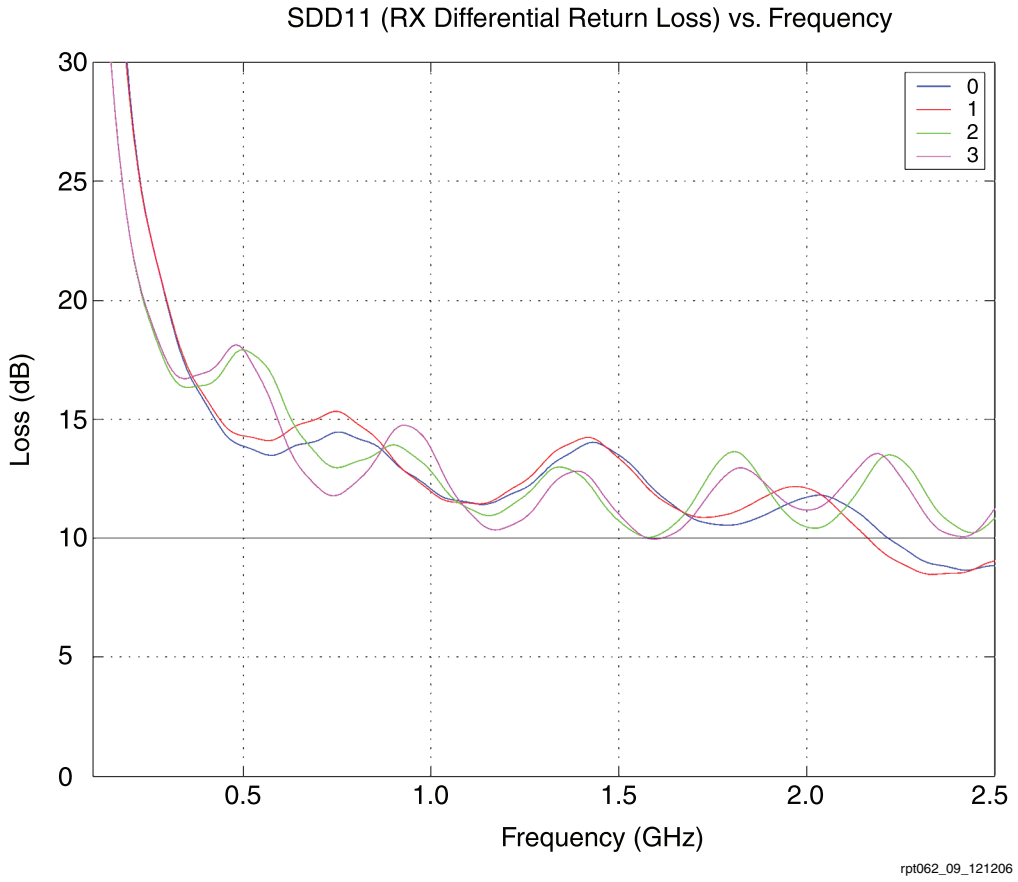

Figure 9: **SDD11 (RX Differential Return Loss) vs. Frequency**

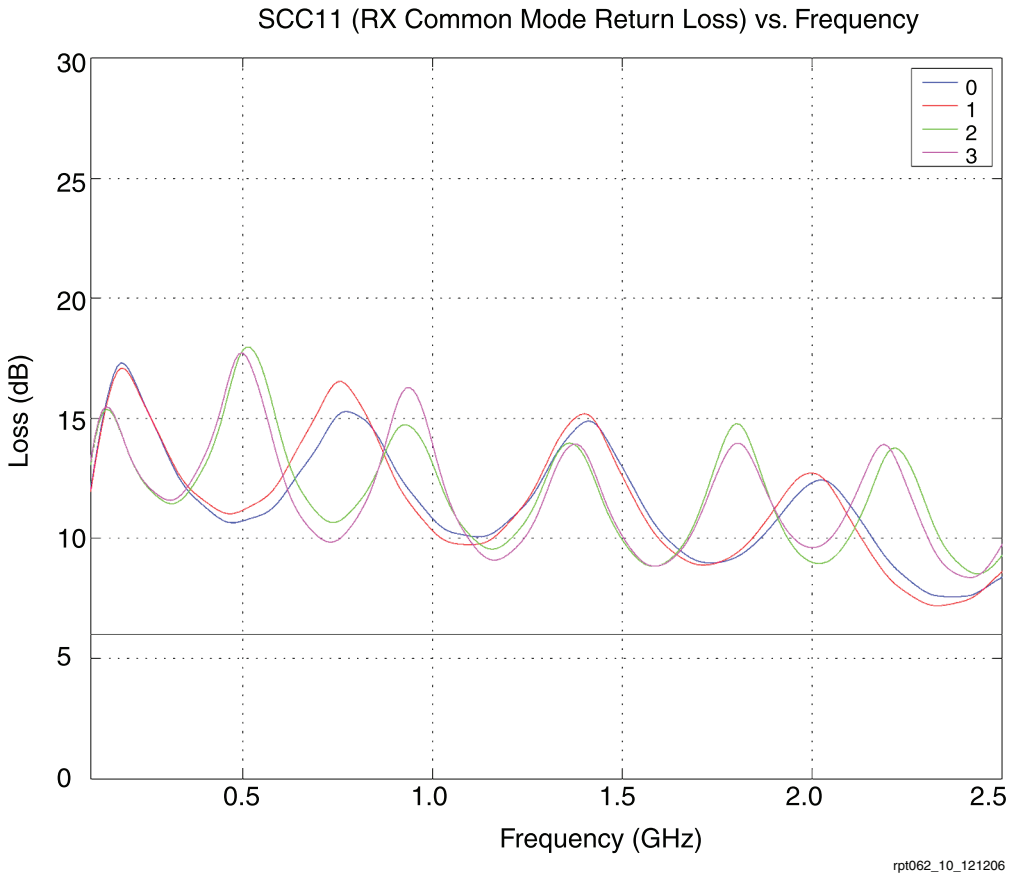

Figure 10: **SCC11 (RX Common Mode Return Loss) vs. Frequency**

Transmitter Electrical Tests

Jitter Generation, Rise/Fall Times, and Amplitude Tests

This document specifies compliance to the near-end eye template and jitter requirements. Transmit near-end jitter is measured at the driver output when terminated into the load. The eye templates is given in Figure 11 and Table 13.

Transmitter Specifications

The XAUI driver characteristics are summarized in Table 12 and Table 13. Figure 11 shows the driver template.

Table 12: **Driver Characteristics**

Parameter	Value	Units
Baud rate tolerance	3.125 GBd ± 100 ppm	GBd ppm
Unit interval nominal	320	ps
Differential amplitude (INF-8074 [Ref 1])	800 – 1600	mV_{P-P}
Differential output return loss minimum	[See Figure 22]	dB
Output jitter		
Near-end maximums		
Total jitter	± 0.175 peak from the mean	UI
Deterministic jitter	± 0.085 peak from the mean	UI

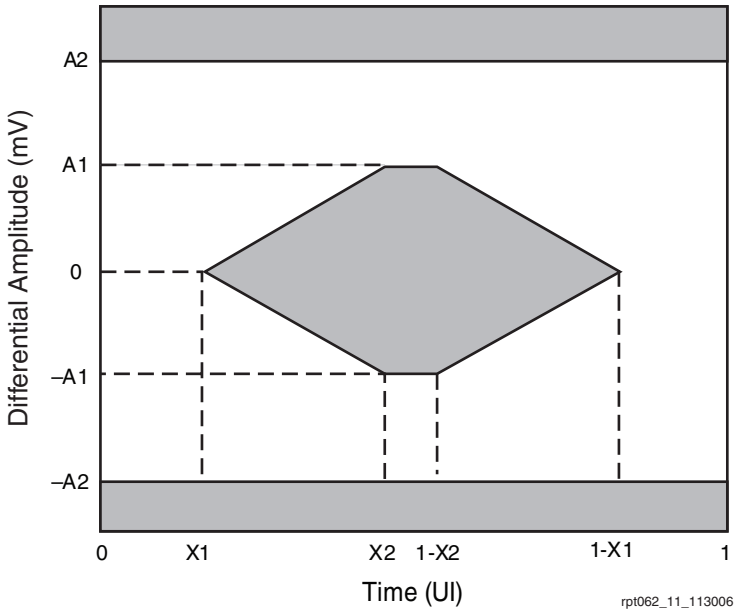

Figure 11: **Driver Template**

Table 13: **Driver Template Intervals**

Symbol	Values	Units
X1	0.175	UI
X2	0.390	UI
A1	400	mV
A2	800	mV

Jitter Generation Test Setup

Eye closure measurements of the transmitter output are performed by the Bath Tub Curve (BTC) method, in which the random jitter component is extrapolated to 10^{-12} BER to measure the transmitter's total output jitter (TJ).

Test Equipment

Characterization of the XC5VLX50T-FF1136 GTP transceiver was performed using HVC hardware. The HVC system uses a 12-channel, 13.5 Gb/s ParBERT with integrated signal generators, power supplies, and a removable test fixture interface. Temperature control was achieved through forced air cooling and heating using a Thermonics unit. The system was developed for volume characterization of Virtex-4 MGTs and Virtex-5 GTP transceivers.

A Virtex-5 GTP test fixture was developed for the FF1136 package, which can be used for both XC5VLX50T and XC5VLX110T devices. Twelve GTP channels can be characterized in a single pass.

Board Setup and Clock Connections

The device is configured using JTAG. Power is supplied from eight programmable power supplies through connectors on the side of the fixture.

High-speed connections from the device to the ParBERT are made through SMP and SMA coaxial connectors. Blind-mate connectors are used to permit quick removal of the test fixture. A low-profile, high-speed socket from Altanova, as shown in Figure 12, was used to collect the data.

Two pairs of MGTCLKs are used to clock the six GTP_DUAL tiles in two groups of three GTP transceivers.

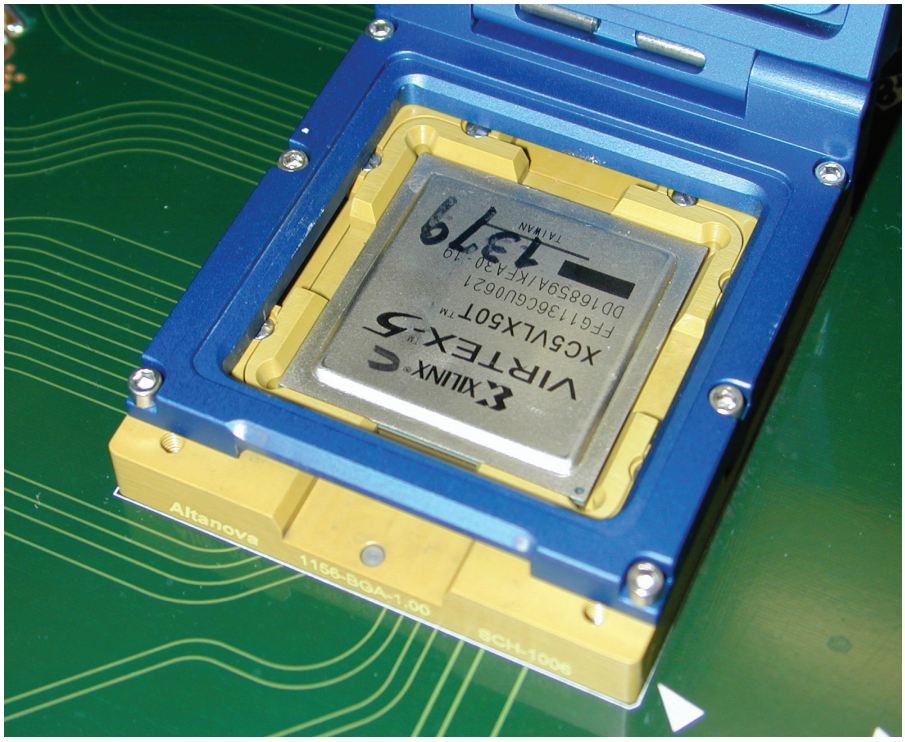

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Figure 12: **FF1136 Low-Profile High-Speed Socket**

Test Conditions

The tests were performed at –40°C, 0°C, and 100°C at nominal and V_{CC} (±5%) values.

Table 14 lists the nominal voltages for the power supplies.

Table 14: **Power Supply Voltage Ranges**

Supply	Use	Nominal Voltage
V_{CCINT}	FPGA Logic main supply and GTP PCS	1.00V
V_{CCAUX}	FPGA Logic AUX supply, low noise	2.50V
V_{CCIO}	Fabric I/O supply	2.50V
MGTAVCC	GTP main supply	1.00V
MGTAVCCPLL	GTP supply for PLLs, low noise	1.20V
MGTVTTX	GTP TX supply	1.20V
MGTVTRX	GTP RX supply	1.20V
MGTVTTRXC	GTP RX *always on* supply used to maintain termination resistor calibration when GTP transceiver is powered down	1.20V

1. *All* supply voltages were adjusted together.
2. All GTP supplies use L/C passive filtering. See the *Virtex-5 RocketIO GTP Transceiver User Guide* for details.

Test Details

Five pieces each of the typical, slow, and fast corner material were characterized using HVC over voltage and temperature corners. All 12 GTP transceivers on each unit were tested.

The configuration designs use FPGA logic loopback in single-byte mode with both TXUSRCLK/2 and RXUSRCLK/2 clocked from TXOUTCLK. The configuration provides connections to GTP_RESET, CDR_RESET, and the DRP interface. For all test cases, the RX is configured for termination to GND with the RX front-end using internal AC coupling.

The data flow through the GTP transceiver is shown in Figure 13. Serial data to the RX is provided by the Agilent ParBERT pattern generator. This data is converted to 8-bit or 10-bit data at the PMA deserializer and passed through the PCS. The RX parallel data port is connected to the TX parallel data port in the FPGA logic. The 8-bit or 10-bit parallel data is then sent through the TX PCS and converted back to serial data at the TX PMA. The TX serial data is connected to the ParBERT data analyzer.

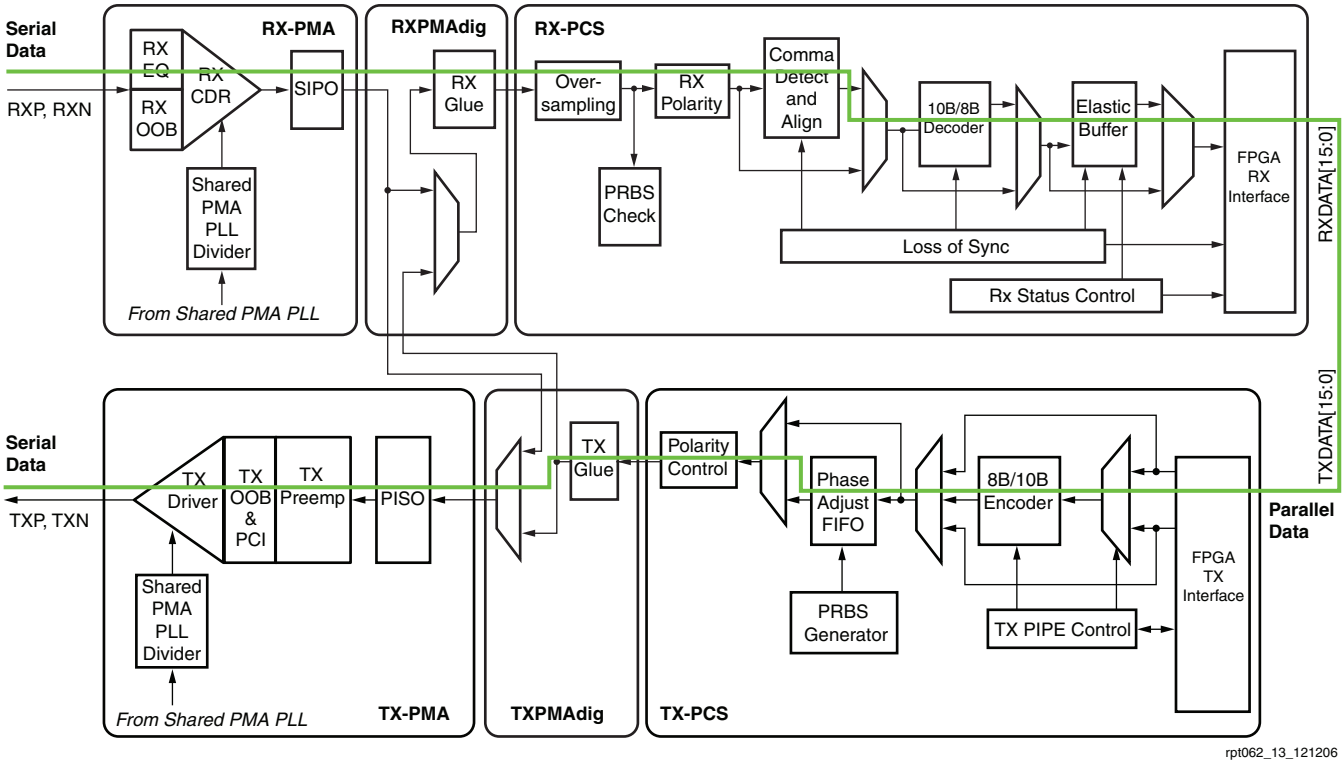

Figure 13: **Data Flow Through the GTP Transceiver**

Jitter Generation Test Results at 3.125 Gb/s

Table 15 summarizes the test conditions for jitter generation measured at 3.125 Gb/s (I-Grade). PRBS7 data pattern is used for output jitter measurements instead of the required CJPAT test pattern. The GTP transmitter behavior is similar for PRBS7 and CJPAT. The measured output jitter was not filtered and represents a pessimistic broadband jitter.

Table 15: **Test Conditions for Jitter Generation at 3.125 Gb/s**

Condition	Description
Test Case	Eye Width in UI (Unit Interval)
Conditions	V_{CC} = NOM, ±5%; Temperature = –40°C to +100°C (I-Grade)
Method	BTC method. Eye Step = 0.005 UI, and number of bits collected = 10^8. A BER test is performed at each step in the eye, and the BER rate is calculated. Dual Dirac method is used to extrapolate the eye opening at BER = 10^{-12}. BTC functional call reports TJ (Total Jitter = 1-eye opening) and estimate for RJ.
Configuration/Standard	DATARATE = 3.125 Gb/s, MGTCLK = 156.25 MHz, Target STD = XAUI. PLL = N/M/P = 10/1/1.
Pattern	PRBS7, 500 mV p-p
Specification	TJ $\leq$ 0.35 UI (EW $\geq$ 0.65 UI)
Results, RJ (p-p)/DJ	RJ=0.155 UI/DJ=0.075 UI

The test results at 3.125 Gb/s (I-Grade) are shown in Figure 14 and summarized in Table 16.

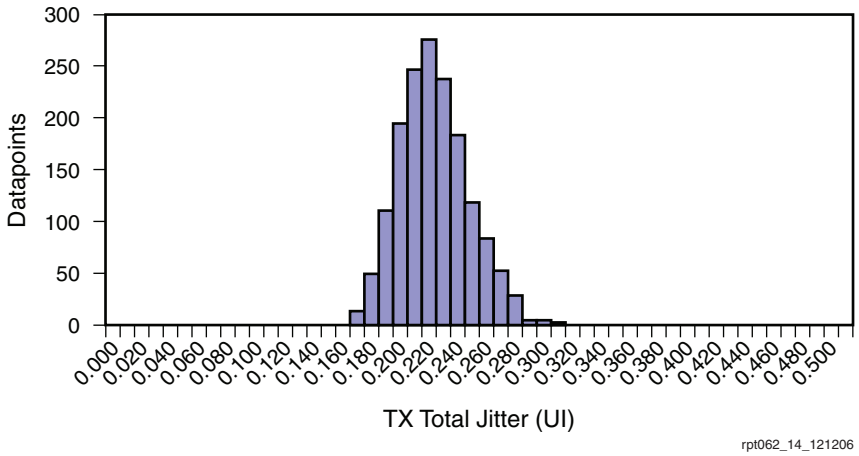

Figure 14: **Jitter Generation Test Results at 3.125 Gb/s**

Table 16: **Transmitter Jitter Generation Test Results Summary**

Type of Jitter	Min	Max	Mean	Median	Standard Deviation	Units
TJ	0.156	0.32	0.229	0.229	0.024	UI
RJ	0.102	0.270	0.155	0.154	0.018	UI
DJ	0(1)	0.16	0.07	0.07	0.02	UI

Notes:

1. Minimum results specified within measurement equipment resolution.

Figure 15 shows the transmitter output eye diagram.

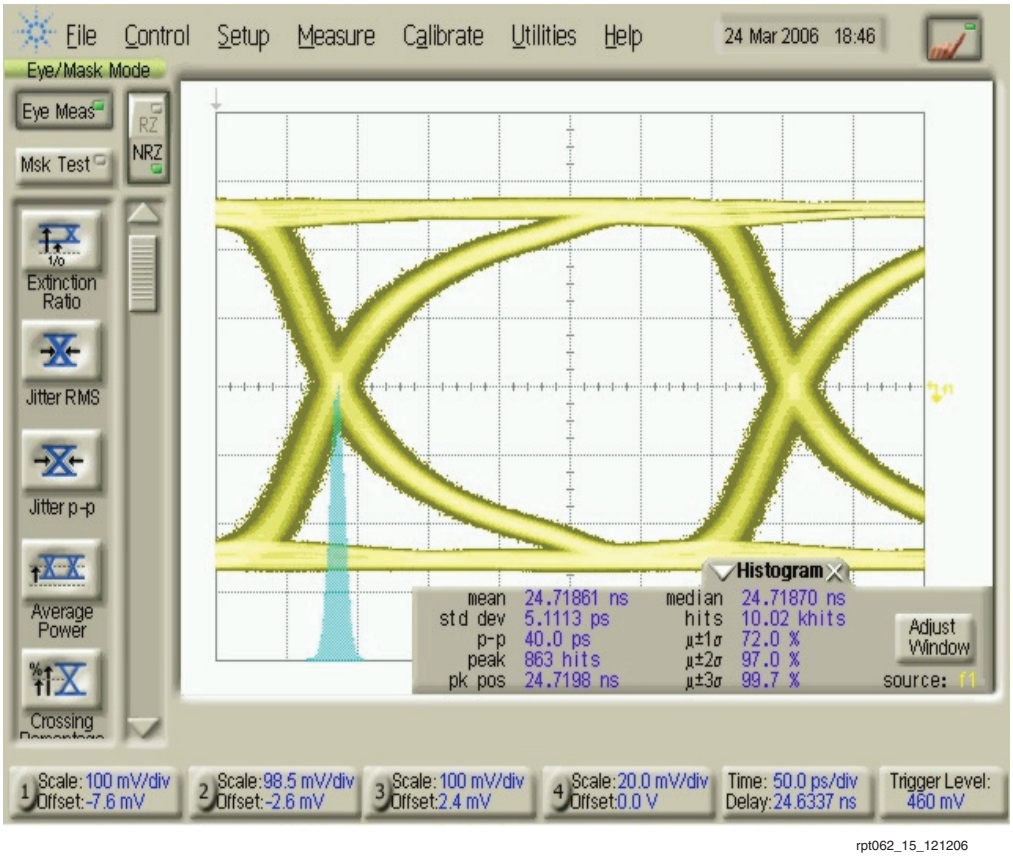

Figure 15: **Transmitter Output Eye at 3.125 Gb/s**

Transmitter Rise and Fall Times Test Results

The GTP TX output rise and fall time measurements are made as a function of the MGTAVTTTX voltage supply. In these tests, the data rate is 2.5 Gb/s, REFCLK = 250 MHz, and the operating temperature was –40°C, 0°C, and 100°C. The resulting trends are plotted in the data plots shown in the following figures. The rise and fall times measured at 2.5 Gb/s is a typical representation of GTP behavior at 3.125 Gb/s. Table 17 shows the XAUI specifications for rise and fall times.

Table 17: **Transmitter Rise and Fall Time Specifications**

Line Rate	Rise/Fall Time Specification (ps)	
	Min	Max
T_r	60	130
T_f	60	130

Figure 16 and Figure 17 show the histogram distribution of the rise time of the XCV5LX50T TX side output at a 2.5 Gb/s data rate, with a `00001111` data pattern, and MGTAVTTTX equal to 1.2V ± 5%. Table 18 summarizes the transmitter rise time.

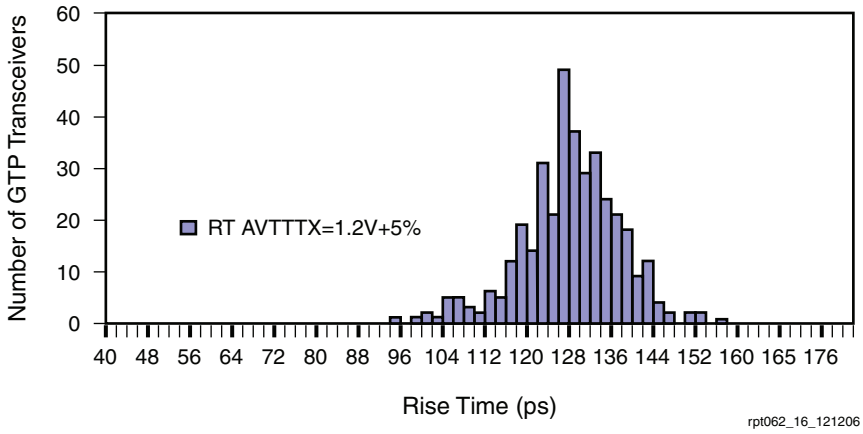

Figure 16: **XCV5LX50T Rise Time at MGTAVTTTX = 1.26V**

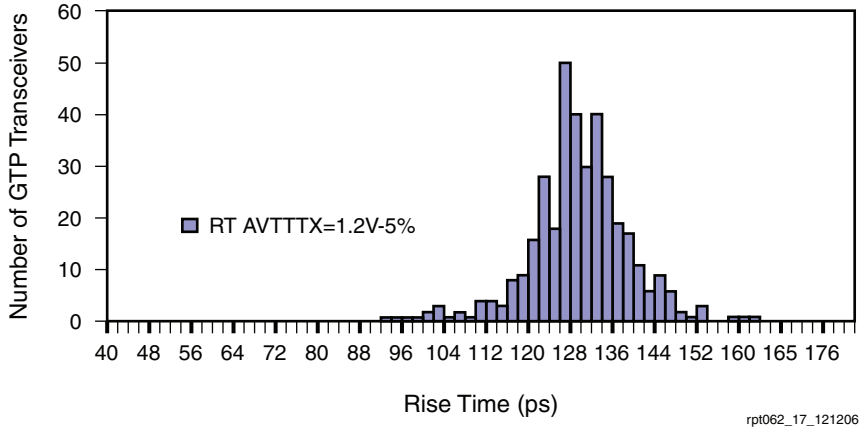

Figure 17: **XCV5LX50T Rise Time at MGTAVTTTX = 1.14V**

Table 18: **Transmitter Rise Time Summary**

Min	Max	Mean	Median	Standard Deviation	Units
92	162	126	127	9.43	ps

Figure 18 and Figure 19 show the histogram distribution of the fall time of the XCV5LX50T TX side output at a 2.5 Gb/s data rate, with a `00001111` data pattern, and MGTAVTTTX equal to 1.2V ± 5%. Table 19 summarizes the transmitter fall time.

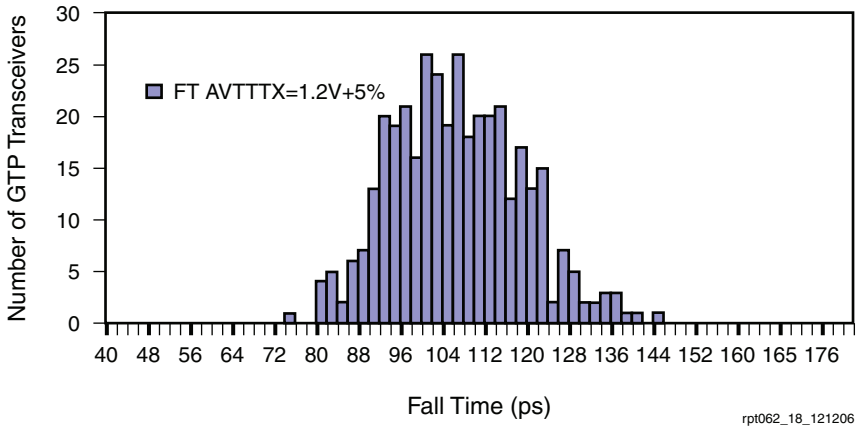

Figure 18: **XCV5LX50T Fall Time at MGTAVTTTX = 1.26V**

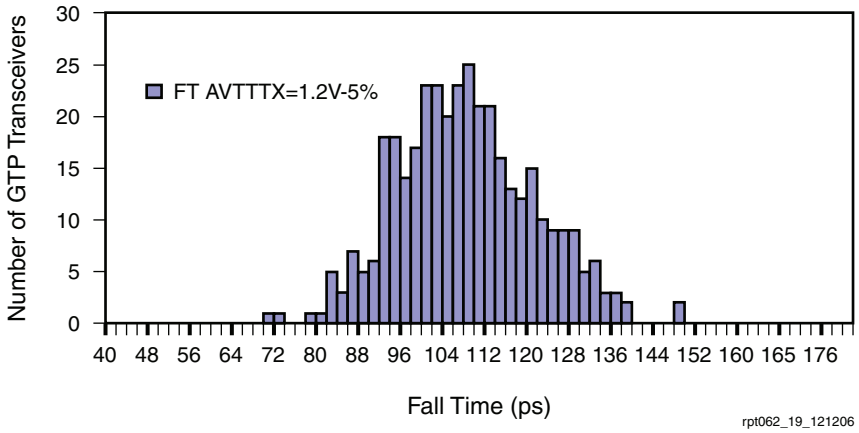

Figure 19: **XCV5LX50T Fall Time at MGTAVTTTX = 1.14V**

Table 19: **Transmitter Fall Time Summary**

Min	Max	Mean	Median	Standard Deviation	Units
70	148	105	105	12.29	ps

The GTP transmitter does not comply with the maximum rise and fall times of the XAUI specification. The UNH inter-operability lab testing and the XAUI receiver mask compliance testing showed no impact due to the worst case rise/fall times.

Transmitter Differential Amplitude Test Results

The transmitter differential amplitudes measures the differential voltage amplitude between the positive and negative GTP transceiver pins when the transmit eye is fully open. See Table 12, page 19 for amplitude limits.

The bench setup was used to measure the output amplitudes for the programmable voltage control settings. Data was measured at TX data rate of 2.5 Gb/s with a `00001111` pattern. This is a typical representation of GTP behavior at 3.125 Gb/s operation.

MGTAVTTTX Trend

Figure 20 shows the transmitter output supply voltage trend for the GTP_DUAL transmitters at a 2.5 Gb/s data rate with a `00001111` data pattern. The TX average peak-to-peak differential output voltage decreases whenever TXDIFFCTRL setting increases.

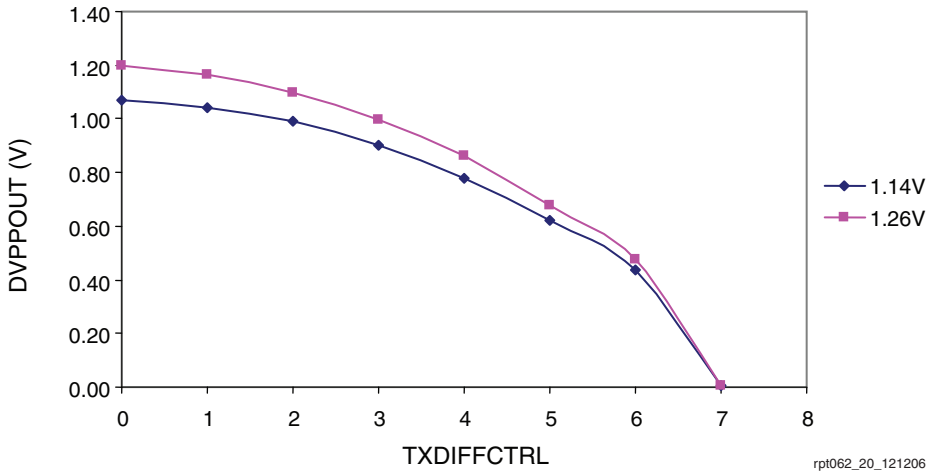

Figure 20: **XCV5LX50T MGTAVTTTX Trend at 2.5 Gb/s with REFCLK = 250 MHz**

Temperature Trend

Figure 21 shows the temperature trend at a 2.5 Gb/s data rate with a `00001111` data pattern. The temperature does not have significant effects on the TX average peak-to-peak differential output voltage.

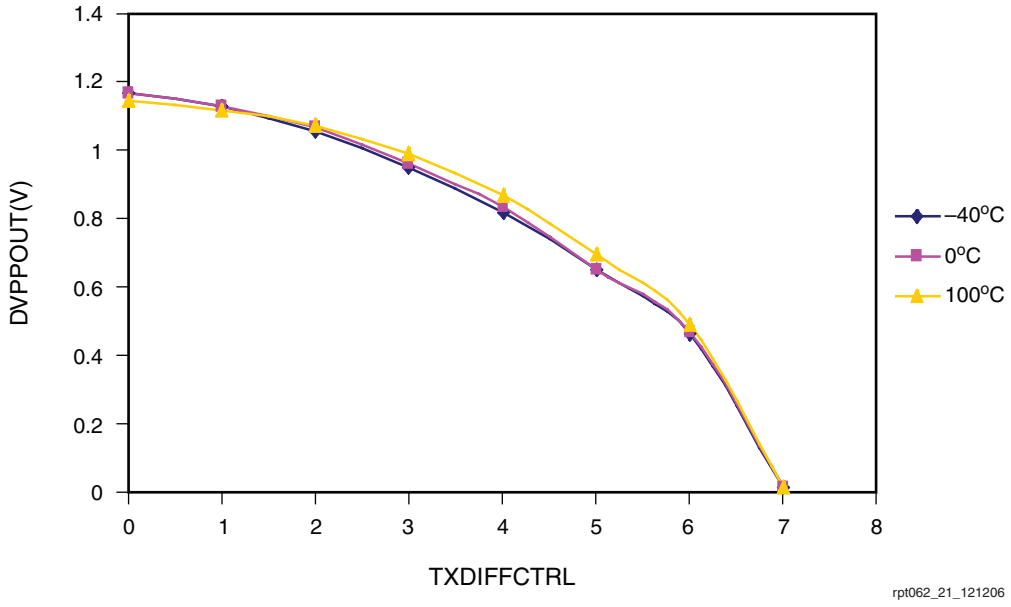

Figure 21: **XCV5LX50T Temperature Trend at 2.5 Gb/s with REFCLK = 250 MHz**

Transmitter Return Loss

For frequencies from 100 MHz to 2.5 GHz, the differential return loss of the driver must exceed the limits shown in Figure 22. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

The frequency domain return loss measurements (Figure 22 and Figure 23) were made using the UNH inter-operability lab guidelines. The four traces represent different GTP receivers with varying PCB trace lengths. The return loss measurements based on the UNH inter-operability labs testing show that the differential and common mode return loss are within the requirements of the XAUI specifications.

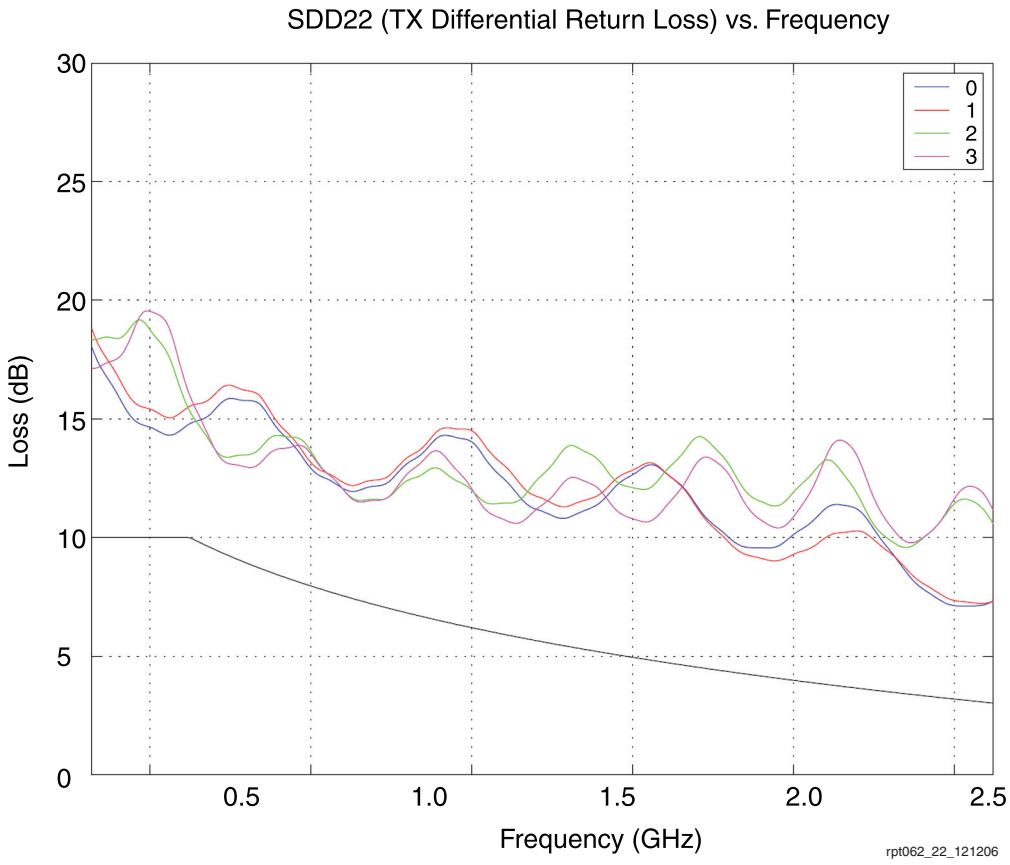

Figure 22: **SDD22 (TX Differential Return Loss) vs. Frequency**

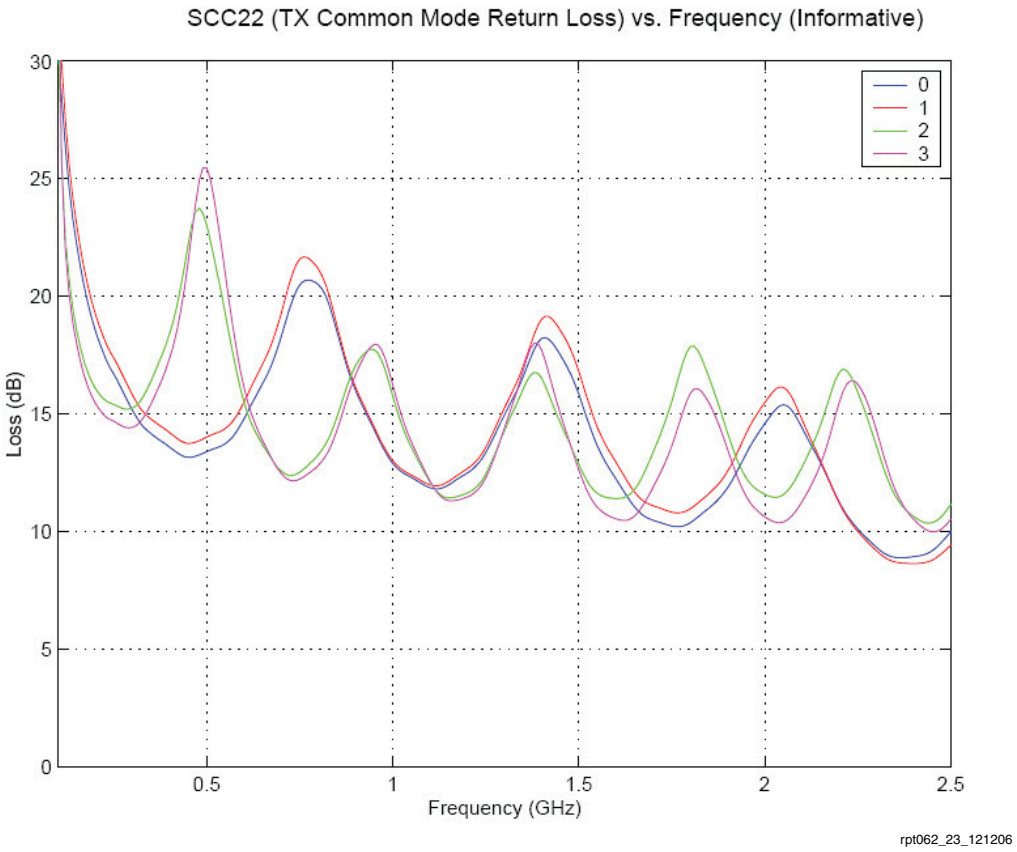

Figure 23: **TX Common Mode Return Loss vs. Frequency**

References

1. INF 8074: ftp://ftp.seagate.com/sff/INF-8074.PDF.
2. IEEE: 10 Gb Attachment Unit Interface (XAUI) 10G Ethernet specification (IEEE 802.3-2005 clause 47).
3. FC-PH-2: http://www.t11.org/ftp/t11/member/fc/ph-2/fc-ph-2_74.pdf.
4. MJSQ: Methodologies for Jitter and Signal Quality Specification (FC-MJSQ) ANSI/INCITS TR-35-2004 can be purchased from INCITS at www.INCITS.org. A draft version can be downloaded from http://www.schelto.com/t11_2/FC-MJSQ%20r14.pdf.