Virtex-5 OC-48 Protocol Standard

Characterization Test Report

RPT063 (v1.0.1) December 13, 2006

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/08/06	1.0	Initial Xilinx Confidential release.
12/13/06	1.0.1	Release to Xilinx website under license agreement.

Virtex-5 OC-48 Protocol Standard

Introduction

Virtex™-5 system connectivity technology delivers the lowest power solutions for building high-speed, high-bandwidth connections between devices, boards, and boxes. The RocketIO™ GTP transceiver design and proven SelectIO™ parallel I/O technologies enable flexible bridging between emerging serial standards and existing parallel standards. The features of the Virtex-5 GTP transceivers include:

- Current Mode Logic (CML) drivers/buffers with configurable termination, voltage swing, and coupling.
- Programmable transmit pre-emphasis and receive equalization for optimal signal integrity.
- Line rates from 500 Mb/s to 3.2 Gb/s with optional 5x over-sampling to bring the low-end down to 100 Mb/s.
- Optional built-in PCS features, such as 8B/10B encoding/decoding, comma alignment, channel bonding, and clock correction.
- Fixed latency modes for minimized, deterministic datapath latency.
- Out-of-band signaling support (specifically designed to address the requirements of PCI Express® and Serial ATA protocols).
- Built-in pseudo-random bitstream (PRBS) generation/checking logic for easier bit-error rate checking.
- A configuration wizard provided in the CORE Generator™ tool and a bit error rate tester (IBERT) integrated into the ChipScope™ Pro tools for easy implementation of GTP transceiver interfaces.

This document presents the GTP transceiver electrical performance against the OC-48 specifications across process, voltage, and temperature conditions. GTP transmitter and receiver electrical characteristics were measured using a lab bench test setup.The methods used to characterize the transceiver are based on the standards specifications and also follow the best-practice methods for some parameters.

OC-48/STS-48/STM-16 Background

SONET and SDH are a set of related standards for synchronous data transmission over fiber optic networks. SONET links are traditionally used in the Telecommunication industry. The applicable test specifications are found in GR-253, ITU-T G.783, and ITU-T G.957. The specifications are written for optical signals so a reference optical device is used in the test setup.

Lab Board Setup

The lab board setup consists of the following equipment:

- The Xilinx ML523 Evaluation board with Oztek socket for the FF1136 package is used to test devices.
- The Xilinx GUI-based XBERT platform is used for DRP loading.
- The Xilinx ChipScope Pro Analyzer is used to configure the part.

Test Conditions

The conditions for voltage and temperature used to test the OC-84 jitter generation are listed in Table 1 and Table 2.

Table 1: **OC-48 Jitter Generation Testing Operating Supply Voltages**

Condition	MGTAVCC	MGTAVCCPLL	MGTAVTTRX	MGTAVTTTX
V_{MIN}	0.95V	1.14V	1.14V	1.14V
V_{NOM}	1.0V	1.20V	1.20V	1.20V
V_{MAX}	1.05V	1.26V	1.26V	1.26V

Notes:

1. Other FPGA voltages stay at their nominal values.
2. Some tests performed at V_{NOM} ±10%.

Table 2: **OC-48 Jitter Generation Testing Operating Temperatures**

Condition	Temperature (Case, for Bench Measurements)
T_{MAX}	100°C
T_{ROOM}	25°C
T_{MIN}	–40°C

The devices chosen for characterization cover the process corner material. The number of devices varies. A total of 10 devices were tested covering the slow, typical, and fast process corners across voltage and temperature.

Summary of Test Results

Figure 3 is a summary table of the SONET OC-48 specification requirements and the test results across process, voltage, and temperature for the Virtex-5 GTP transceiver.

Table 3: **Summary of OC-48 Test Results**

	OC-48 Specifications		Virtex-5 GTP Test Results		Units	Compliant?	Comments
	Min	Max	Min	Max			
TX Specifications							
Jitter Generation		0.01		0.010	UI rms	Yes(1)	155 MHz reference clock
		0.01		0.0074	UI rms	Yes	311 MHz reference clock
Jitter Generation Peak-to-Peak		0.10		0.108	UI	Yes(2)	155 MHz reference clock
		0.10		0.074	UI	Yes	311 MHz reference clock
RX Specifications(3)							
RX SJ Jitter Tolerance	0.15		0.412		UI	Yes	
RX Run Length Tolerance				256			

Notes:

1. Conditional compliance — marginal performance. Refer to Table 6, page 12 and Figure 8, page 14.
2. Conditional compliance — marginal performance. Refer to Table 6, page 12 and Figure 7, page 14.
3. All RX tests using a 155.52 MHz reference clock.

Receiver Tests

OC-48 jitter tolerance tests measure the GTP RX CDR's ability to tolerate input jitter and recover the data stream error free. The input data is jittered using a sinusoidal signal and swept across frequency and amplitude until a failure is observed.

Test Setup

Sinusoidal jitter (SJ) tolerance measurements at 2.48832 Gb/s, the OC-48 data rate, are performed using the test setup as shown in Figure 1.

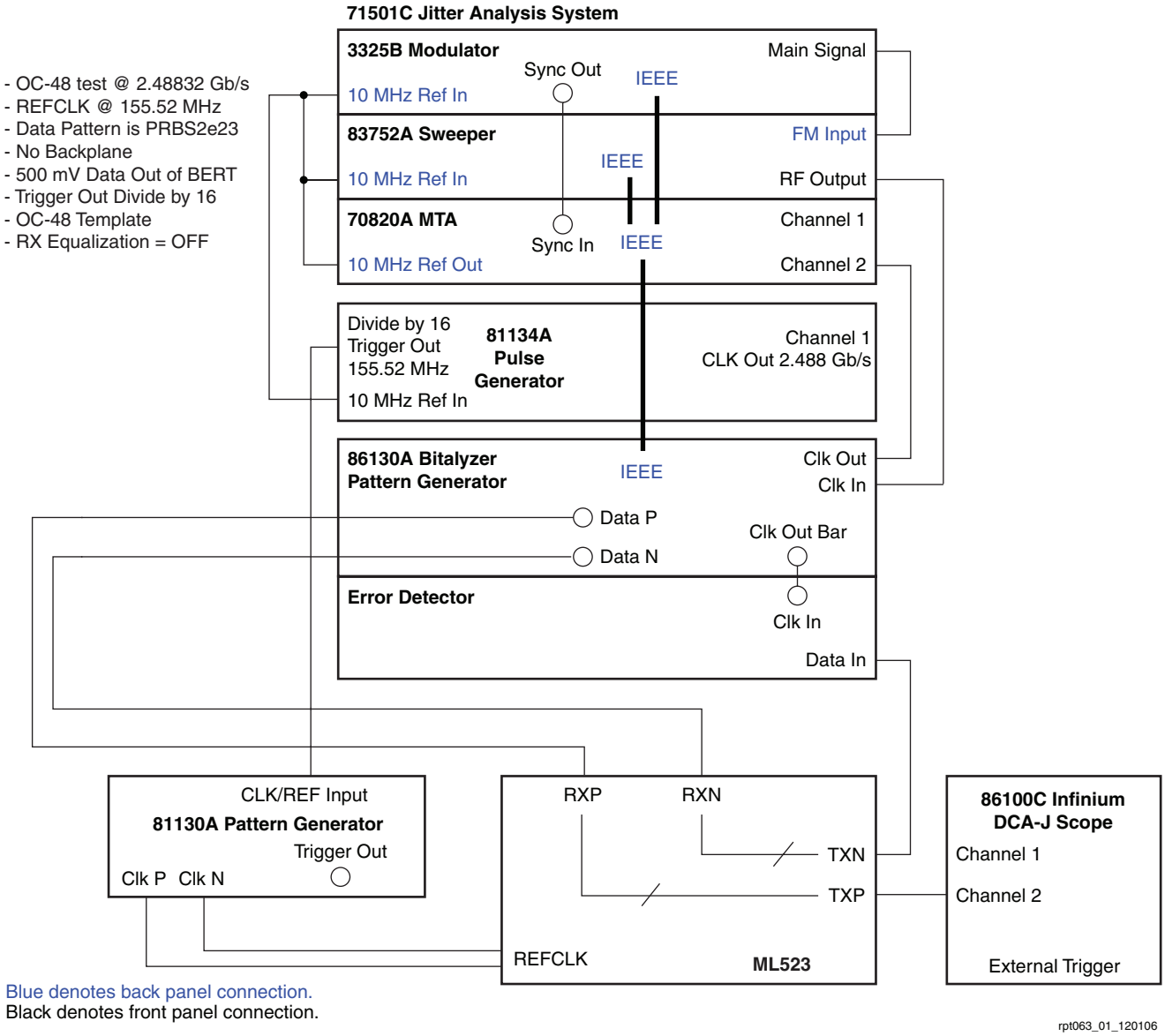

Figure 1: **OC-48 Sinusoidal Jitter Tolerance Setup**

Jitter Tolerance Test Specifications

SONET defines a jitter tolerance mask that specifies the magnitude of jitter in unit intervals across modulation frequency. For example, at modulation frequencies above 1 MHz, the receiver should tolerate at least 0.15 UI of input jitter.

In Figure 2, the circles indicate a pass and the crosses a failure. The test setup sweeps the jitter amplitude until a failure is encountered. Each test point is performed for 2s of error free operation. Figure 2 shows a typical sinusoidal jitter tolerance sweep measurement at the bench.

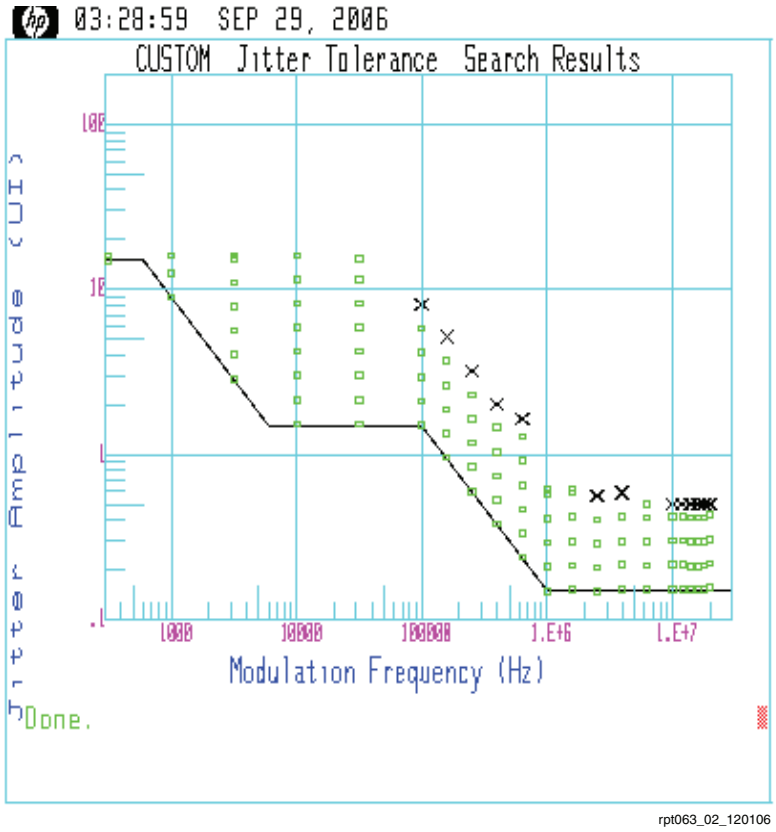

Figure 2: **Typical Sinusoidal Jitter Tolerance Sweep Measurement**

Test Results

Sinusoidal Jitter Tolerance at 2.48832 Gb/s

Table 4 shows the minimum tolerance results for each test case. These results were based on a data rate of 2.48832 Gb/s, REFCLK = 155.52 MHz, f_{VCO} = 1.24416 Gb/s, RX_EQ = OFF, a 2^{23}–1 pattern, and no backplane. The bars in the histogram plot in Figure 3 show the number of GTP test condition instances at each sinusoidal jitter tolerance value across corners.

Table 4: **Sinusoidal Jitter Tolerance Test Conditions and Results**

Device	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	Sinusoidal Jitter Tolerance (UI)
Typ-1	0.9	1.08	1.08	1.08	100	0.492
	1	1.2	1.2	1.2	25	0.492
	1.1	1.32	1.32	1.32	–40	0.492
Typ-2	0.9	1.08	1.08	1.08	100	0.538
	1	1.2	1.2	1.2	25	0.538
	1.1	1.32	1.32	1.32	–40	0.538
SS-1	0.9	1.08	1.08	1.08	100	0.412
	1	1.2	1.2	1.2	25	0.448
	1.1	1.32	1.32	1.32	–40	0.448
SS-2	0.9	1.08	1.08	1.08	100	0.448
	1	1.2	1.2	1.2	25	0.448
	1.1	1.32	1.32	1.32	–40	0.448
FF-1	0.9	1.08	1.08	1.08	100	0.412
	1	1.2	1.2	1.2	25	0.492
	1.1	1.32	1.32	1.32	–40	0.412
FF-2	0.9	1.08	1.08	1.08	100	0.412
	1	1.2	1.2	1.2	25	0.412
	1.1	1.32	1.32	1.32	–40	0.412

In Figure 3, Average (UI) = 0.461, and Standard Deviation = 0.047.

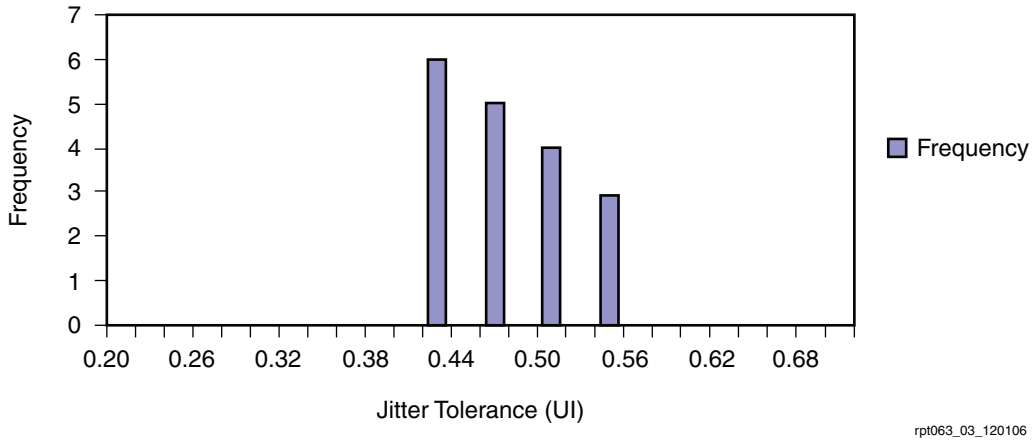

Figure 3: **Sinusoidal Jitter Tolerance at 2.48832 Gb/s**

Receiver Maximum Run Length

Test Description

The Clock and Data Recovery (CDR) unit in a serial transceiver relies on data edges to recover the clock used to re-time the input data. High performance receivers are capable of tolerating long strings of 1s or 0s while still maintaining phase lock to the input. The receiver run length test measures the maximum run length tolerance of a GTP transceiver. RX was stressed with increasing Consecutive Identical Digits (CID) run lengths until an error was detected. The input data stream used for this test at 2.48832 Gb/s is shown. The pattern is then repeated while increasing the string of consecutive identical digits until a failure is observed.

PRBS31 (15 kb)	All 1s (Run Length)	PRBS31 (15 kb)	All 0s (Run Length)	PAD

The PAD section of the pattern is required for the ParBERT to put the pattern on a memory boundary.

Test Results

Figure 4 shows the CID pattern run length. GTP receivers exhibit a run length tolerance of 256 CIDs with the stress pattern.

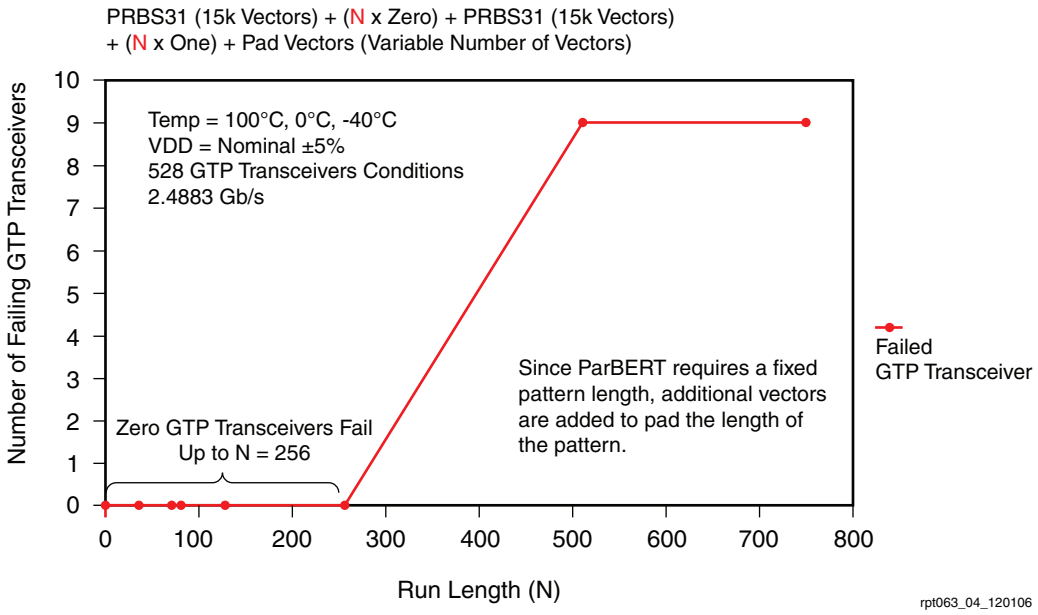

Figure 4: **CID Pattern Run Length Testing Results**

Transmitter Tests

Jitter Generation Measurements

Test Setup

GTP transmitter output jitter is measured at the OC-48 data rates using the Agilent OmniBER 725 (Figure 5). The GTP transceiver output is connected to the OmniBER through Finisar 1310 nm optical module (FTRJ 1310-1), and therefore includes the jitter contributions from the optical module. The SONET framed data (PRBS2e23) is generated and checked by the Agilent OmniBER at its optical interface.

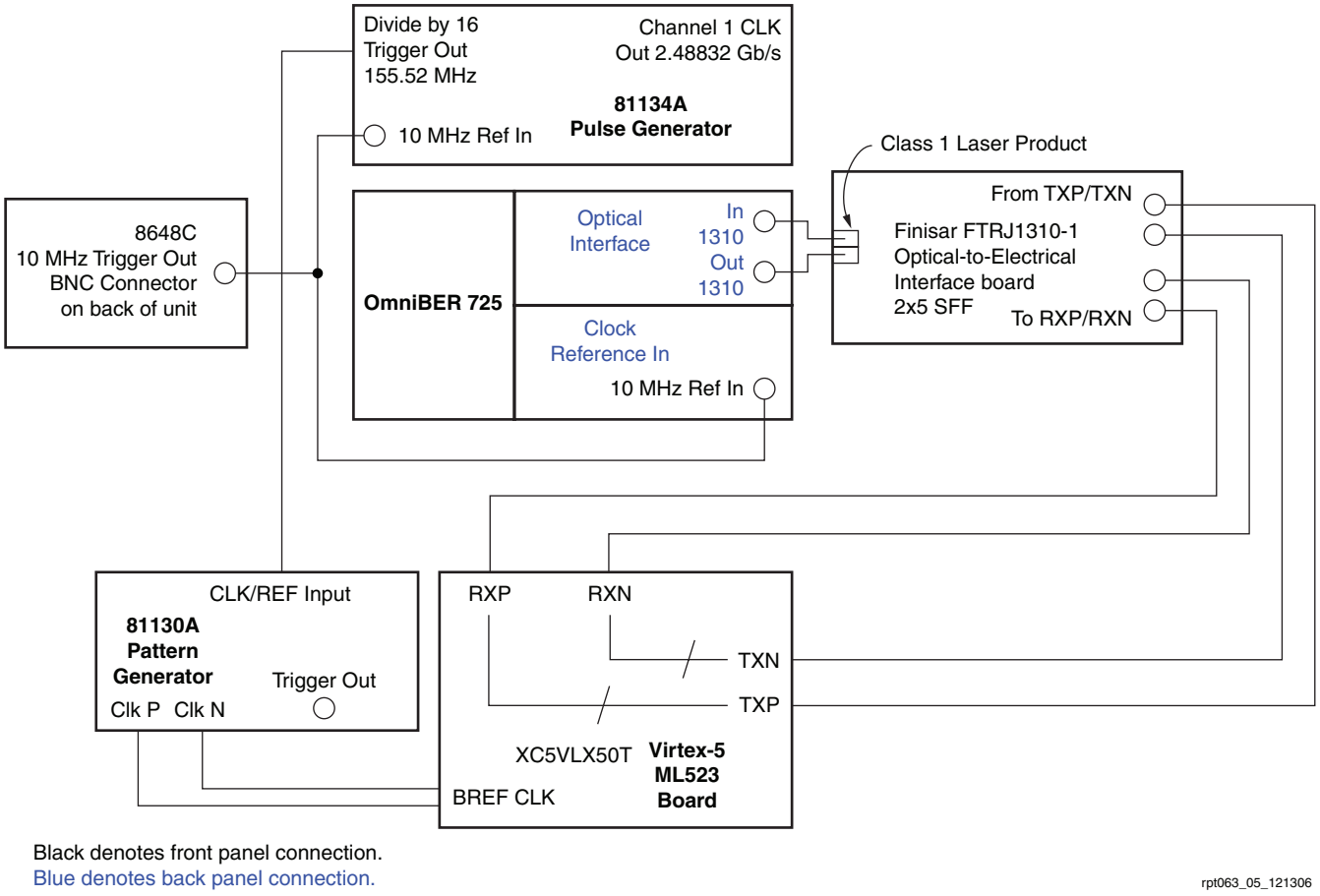

Figure 5: **OC-48 Jitter Using Agilent OmniBER 725**

Test Details

As shown in the "Test Setup" section, the Agilent OmniBER 725 transmits PRBS23 SONET framed payloads to the GTP transceivers in the Virtex-5 device through the Finisar FTRJ 1310 optical module at OC-48 data rates. The GTP loops back the received data from its fabric interface and transmits back to the OmniBER through the Finisar optical module. The OmniBER measures the peak-to-peak and rms jitter on the data received back from the GTP transceiver. The OmniBER is set to filter input data with a 12-kHz high-pass filter and a 20-MHz low-pass filter. Data is recorded for 10 devices and across process, temperature, and voltage combinations. A measurement screen shot from the OmniBER (see Figure 6) shows the measurement settings used on the OmniBER.

Figure 6: **Measurement Screen Shot from the OmniBER**

OC-48 Jitter Generation Specification

Jitter Generation is defined as the amount of jitter present at the OC-N/STS-N output of a SONET network element in the absence of applied jitter. Table 5 shows the requirements for jitter generation at different transmission rates. Two jitter parameters are defined as:

- Jitter peak-to-peak is the maximum measured jitter amplitude.
- Jitter rms is the root mean square (rms) value of the jitter signal that provides and indication of the jitter power.

Table 5: **Sonet Requirements for Jitter Generation**

OC-N/STS-N Level	f_1 (kHz)	f_2 (MHz)	Limit (UI_{rms})	Limit (UI_{P-P})
1	12	0.4	< 0.01	< 0.10
3	12	1.3	< 0.01	< 0.10
12	12	5	< 0.01	< 0.10
48	12	20	< 0.01	< 0.10
48(B)	12	20	< 0.01	< 0.10

These specifications apply to network elements (i.e., to the whole system) and therefore, compliance of individual components alone does not guarantee that the system will meet the SONET requirements for jitter generation. Interface between components and board layout must be carefully considered to minimize jitter generation.

At OC-48, the jitter generation specification requires less than 100 mUI_{P-P} and less than 10 mUI_{rms} when measured using a 12 kHz high-pass filter and a 20 MHz low-pass filter.

Test Results

Test conditions and test results for the OC-48 peak-to-peak and rms jitter generation tests are shown in Table 6 and Table 7 with adjoining histograms. These jitter tests are done over process, temperature, and voltage and include the jitter component contributed by the optical module.

OC-48 Peak-to-Peak and RMS Jitter Generation Results (REFCLK – 155.52 MHz)

Table 6 shows the results for the OC-48 peak-to-peak and RMS jitter generation tests at 155.52 MHz. These tests use a data rate of 2.48832 Gb/s, REFCLK equal to 155.52 MHz, and an OC-48 pattern.

Table 6: **OC-48 Peak-to-Peak and RMS Jitter Generation Results (REFCLK = 155.52 MHz)**

Device	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	Jitter Generation	
						Pk-Pk (UI)	rms (UI)
Typ-1	0.9	1.08	1.08	1.08	100	0.096	0.008
	1	1.2	1.2	1.2	25	0.088	0.008
	1.1	1.32	1.32	1.32	–40	0.078	0.007
Typ-2	0.9	1.08	1.08	1.08	100	0.089	0.008
	1	1.2	1.2	1.2	25	0.086	0.008
	1.1	1.32	1.32	1.32	–40	0.073	0.007

Table 6: **OC-48 Peak-to-Peak and RMS Jitter Generation Results (REFCLK = 155.52 MHz) *(Continued)***

Device	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	Jitter Generation	
						Pk-Pk (UI)	rms (UI)
Typ-3	0.9	1.08	1.08	1.08	100	0.091	0.009
	1	1.2	1.2	1.2	25	0.084	0.008
	1.1	1.32	1.32	1.32	–40	0.077	0.007
Typ-4	0.9	1.08	1.08	1.08	100	0.097	0.008
	1	1.2	1.2	1.2	25	0.084	0.008
	1.1	1.32	1.32	1.32	–40	0.075	0.007
Typ-5	0.9	1.08	1.08	1.08	100	0.097	0.009
	1	1.2	1.2	1.2	25	0.085	0.008
	1.1	1.32	1.32	1.32	–40	0.082	0.008
Typ-6	0.9	1.08	1.08	1.08	100	0.096	0.009
	1	1.2	1.2	1.2	25	0.087	0.008
	1.1	1.32	1.32	1.32	–40	0.083	0.008
SS-1	0.9	1.08	1.08	1.08	100	0.097	0.009
	1	1.2	1.2	1.2	25	0.084	0.008
	1.1	1.32	1.32	1.32	–40	0.077	0.007
SS-2	0.9	1.08	1.08	1.08	100	0.092	0.009
	1	1.2	1.2	1.2	25	0.084	0.008
	1.1	1.32	1.32	1.32	–40	0.077	0.007
FF-1	0.9	1.08	1.08	1.08	100	0.108	0.01
	1	1.2	1.2	1.2	25	0.091	0.008
	1.1	1.32	1.32	1.32	–40	0.082	0.008
FF-2	0.9	1.08	1.08	1.08	100	0.108	0.01
	1	1.2	1.2	1.2	25	0.094	0.009
	1.1	1.32	1.32	1.32	–40	0.095	0.008

In Figure 7, Average (pk-pk) = 0.08, and Standard Deviation (pk-pk) = 0.00089.

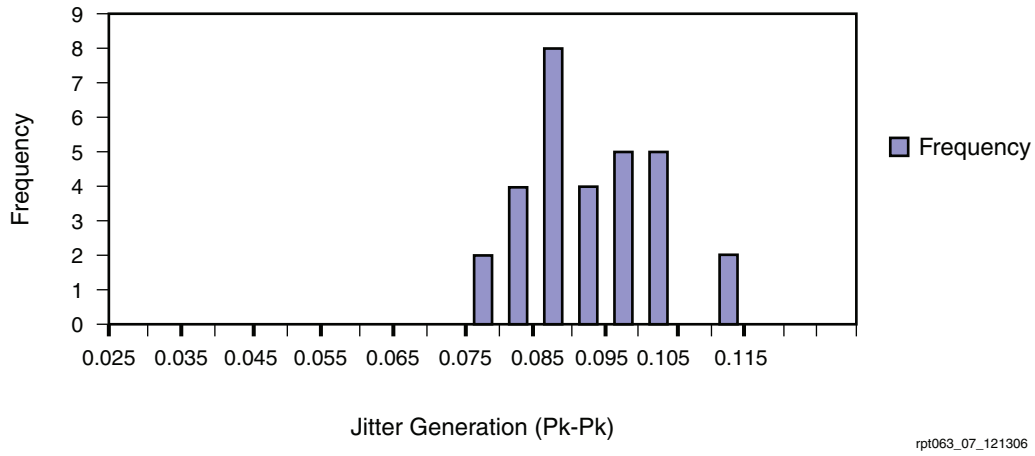

Figure 7: **OC48 Jitter Generation (pk-pk) at 155.52 MHz**

In Figure 8, Average (rms) = 0.0081, and Standard Deviation (rms) = 0.00082.

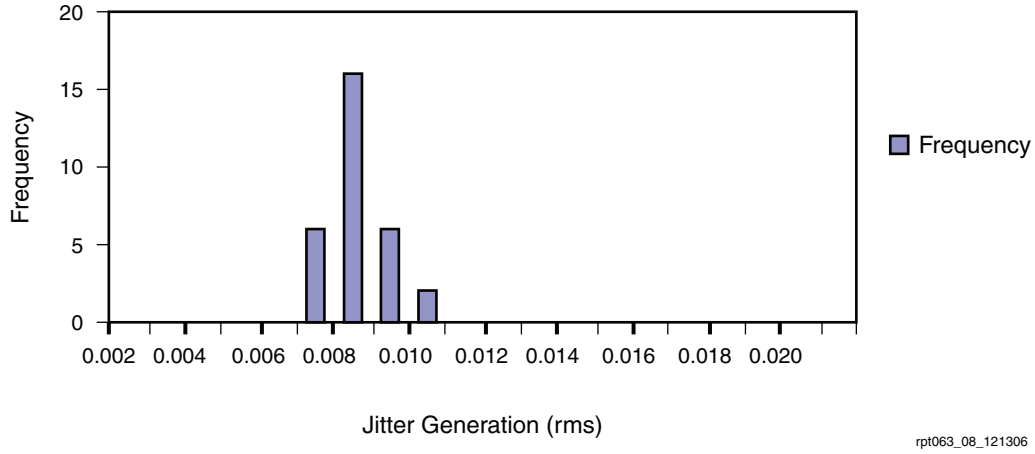

Figure 8: **OC48 Jitter Generation (rms) at 155.52 MHz**

OC-48 Peak-to-Peak and RMS Jitter Generation Results (REFCLK – 311.04 MHz)

Table 7 shows the results for the OC-48 peak-to-peak and RMS jitter generation tests at 311.04 MHz. These tests use a data rate of 2.48832 Gb/s, REFCLK equal to 311.04 MHz, and an OC-48 pattern.

Table 7: **OC-48 Peak-to-Peak and RMS Jitter Generation Results (REFCLK = 311.04 MHz)**

Device	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	Jitter Generation	
						Pk-Pk (UI)	rms (UI)
Typ-1	0.9	1.08	1.08	1.08	100	0.07	0.007
	1	1.2	1.2	1.2	25	0.066	0.007
	1.1	1.32	1.32	1.32	–40	0.062	0.007
Typ-2	0.9	1.08	1.08	1.08	100	0.071	0.008
	1	1.2	1.2	1.2	25	0.067	0.007
	1.1	1.32	1.32	1.32	–40	0.064	0.007
Typ-3	0.9	1.08	1.08	1.08	100	0.07	0.008
	1	1.2	1.2	1.2	25	0.07	0.007
	1.1	1.32	1.32	1.32	–40	0.064	0.007
Typ-4	0.9	1.08	1.08	1.08	100	0.071	0.008
	1	1.2	1.2	1.2	25	0.065	0.007
	1.1	1.32	1.32	1.32	–40	0.065	0.007
Typ-5	0.9	1.08	1.08	1.08	100	0.073	0.008
	1	1.2	1.2	1.2	25	0.072	0.008
	1.1	1.32	1.32	1.32	–40	0.067	0.007
Typ-6	0.9	1.08	1.08	1.08	100	0.073	0.007
	1	1.2	1.2	1.2	25	0.067	0.007
	1.1	1.32	1.32	1.32	–40	0.067	0.007
SS-1	0.9	1.08	1.08	1.08	100	0.072	0.008
	1	1.2	1.2	1.2	25	0.069	0.007
	1.1	1.32	1.32	1.32	–40	0.062	0.007
SS-2	0.9	1.08	1.08	1.08	100	0.07	0.008
	1	1.2	1.2	1.2	25	0.067	0.007
	1.1	1.32	1.32	1.32	–40	0.061	0.007
FF-1	0.9	1.08	1.08	1.08	100	0.074	0.008
	1	1.2	1.2	1.2	25	0.069	0.007
	1.1	1.32	1.32	1.32	–40	0.062	0.007

Table 7: **OC-48 Peak-to-Peak and RMS Jitter Generation Results (REFCLK = 311.04 MHz) *(Continued)***

Device	MGTAVCC (V)	MGTAVCCPLL (V)	MGTAVTTTX (V)	MGTAVTTRX (V)	Temperature (°C)	Jitter Generation	
						Pk-Pk (UI)	rms (UI)
FF-2	0.9	1.08	1.08	1.08	100	0.07	0.008
	1	1.2	1.2	1.2	25	0.067	0.007
	1.1	1.32	1.32	1.32	–40	0.063	0.007

In Figure 9, Average (pk-pk) = 0.068, and Standard Deviation (pk-pk) = 0.0037.

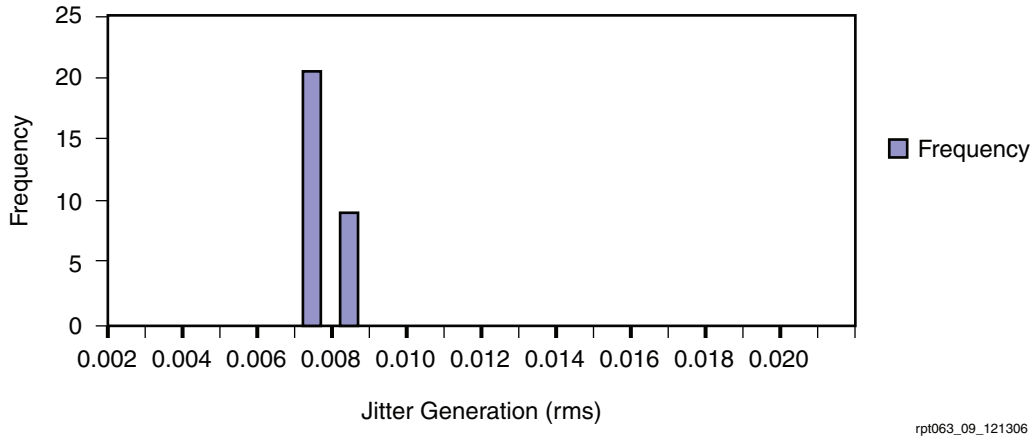

Figure 9: **OC-48 Jitter Generation (pk-pk) at 311.04 MHz**

In Figure 10, Average (rms) = 0.0073, and Standard Deviation (rms) = 0.00047.

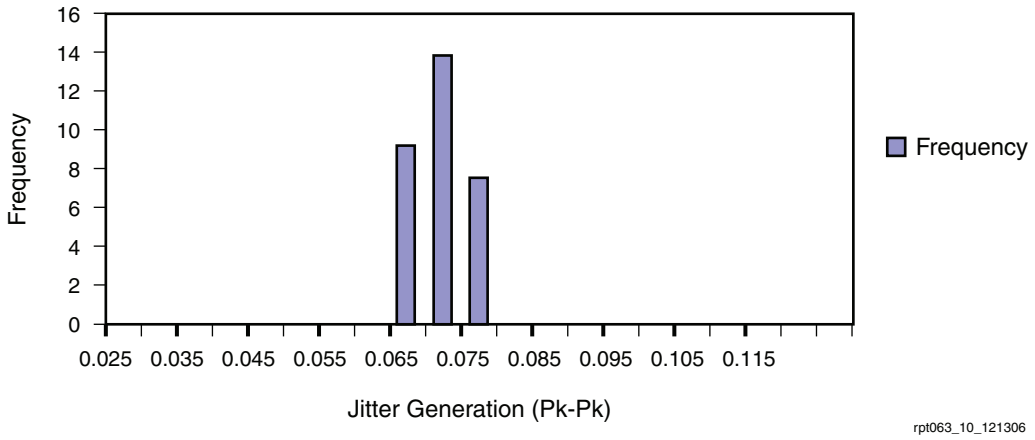

Figure 10: **OC-48 Jitter Generation (rms) at 311.04 MHz**