Namics Under-fill

Qualification Report

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/24/07	1.0	Initial Xilinx release.
08/27/07	1.0.1	Typos in Table 1 and Table 2.

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Namics Under-fill Qualification Report

Overview

This report summarizes the reliability testing results that were obtained to qualify Namics under-fill material that will be used in SPIL's Flip-Chip package assembly.

Qualification Objective

The objective of this qualification is to qualify Namics under-fill material for the flip-chip packages that are already in production.

Reliability Test Conditions and Results

The qualification vehicles were selected from several different product families as well as several different package sizes and pin counts for reliability tests. Table 1 provides a summary of the qualification.

Test	Conditions	Test Vehicle	Lot Qty	Cum Device- Hr/Cyc	# of Failures	
TC-B ⁽¹⁾	-55 to +125°C, 1000 cyc	XC4VLX200/FFG1513	3	102,000	0	
		XC4VLX160/FFG1513	3	112,000	0	
		XC4VLX25/SFG363	1	101,000	0	
		XC2VP70/FFG1517	3	155,000	0	
		XC2VP100/FFG1704	1	69,000	0	
		XC2V8000/FFG1152	3	127,000	0	
		XC2V6000/FFG1152	3	125,000	0	
TC-G ⁽¹⁾	-40 to +125°C, 1000 cyc	XC2V6000/FFG1517	3	132,000	0	
THB ⁽¹⁾	85°C, 85%RH, V _{DDMAX}	XC5VLX50T/FFG1136	3	142,000	0	
TH ⁽¹⁾	85°C, 85%RH	XC5VLX50T/FFG1136	3	142,000	0	

Table 1: Reliability Test Conditions and Results



Table 1:	Reliability Test Conditions and Results	(Continued)
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Test	Conditions	Test Vehicle	Lot Qty	Cum Device- Hr/Cyc	# of Failures
HTS ⁽²⁾	T _A =150°C	XC5VLX50T/FFG1136	3	144,000	0

Notes:

1. Package level-4 preconditioning performed prior to THB, TH, and TC-B tests.

2. Reflow (3X) applied to HTS samples prior to the stress test.

Based on the data gathered to date, Namics under-fill has demonstrated a satisfactory result meeting qualification requirements for releasing to SPIL's production assembly.

Qualification Data

Table 2:	Qualification Data						
Test	Conditions	Rel #	Device	Package	Samples	Duration	Fail Qty
TC-B ⁽¹⁾	-55°C/+125°C	192907	XC4VLX200	FFG1513	36	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	193007	XC4VLX200	FFG1513	35	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	193107	XC4VLX200	FFG1513	31	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	193207	XC4VLX160	FFG1513	33	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	193307	XC4VLX160	FFG1513	37	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	193407	XC4VLX160	FFG1513	42	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	204507	XC2VP70	FFG1517	47	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	204607	XC2VP70	FFG1517	50	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	204707	XC2VP70	FFG1517	58	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	204807	XC2V8000	FFG1152	43	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	204907	XC2V8000	FFG1152	44	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	205007	XC2V8000	FFG1152	40	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	205107	XC2V6000	FFG1152	43	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	205207	XC2V6000	FFG1152	38	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	205307	XC2V6000	FFG1152	44	1,000 cycs	0
TC-G ⁽¹⁾	-40°C/+125°C	205407	XC2V6000	FFG1517	40	1,000 cycs	0
TC-G ⁽¹⁾	-40°C/+125°C	205507	XC2V6000	FFG1517	44	1,000 cycs	0

Test	Conditions	Rel #	Device	Package	Samples	Duration	Fail Qty
TC-G ⁽¹⁾	-40°C/+125°C	205607	XC2V6000	FFG1517	48	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	212207	XC4VLX25	SFG363	101	1,000 cycs	0
TC-B ⁽¹⁾	-55°C/+125°C	224907	XC2VP100	FFG1704	69	1,000 cycs	0
THB ⁽¹⁾	85°C, 85%RH, Bias, V _{CCMAX}	175707	XC5VLX50T	FFG1136	43	1,000 hrs	0
TH ⁽¹⁾	85°C, 85%RH	175807	XC5VLX50T	FFG1136	44	1,000 hrs	0
HTS ⁽²⁾	$T_A = 150^{\circ}C$	175907	XC5VLX50T	FFG1136	45	1,000 hrs	0
THB ⁽¹⁾	85ºC, 85%RH, Bias, V _{CCMAX}	189307	XC5VLX50T	FFG1136	49	1,000 hrs	0
TH ⁽¹⁾	85°C, 85%RH	189407	XC5VLX50T	FFG1136	49	1,000 hrs	0
HTS ⁽²⁾	$T_{\rm A} = 150^{\circ}{\rm C}$	189507	XC5VLX50T	FFG1136	50	1,000 hrs	0
THB ⁽¹⁾	85°C, 85%RH, Bias, V _{CCMAX}	190607	XC5VLX50T	FFG1136	50	1,000 hrs	0
TH ⁽¹⁾	85°C, 85%RH	190707	XC5VLX50T	FFG1136	49	1,000 hrs	0
HTS ⁽²⁾	$T_{\rm A} = 150^{\rm o}C$	190807	XC5VLX50T	FFG1136	49	1,000 hrs	0

Notes:

1. Package level-4 preconditioning performed prior to THB, TH, and TC-B tests.

2. Reflow (3X) applied to HTS samples prior to the stress test.

