Qualification of Additional Substrate Material Set from Fujitsu Technologies

Qualification Report

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/31/07	1.0	Initial Xilinx release.

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Overview

This report summarizes the reliability testing results that were performed to qualify the Fujitsu package substrate that will be used in Flip-Chip package assembly.

Qualification Objective

The objective of this qualification is to qualify the Fujitsu package substrate for the Flip-Chip packages that are already in production.

Reliability Test Conditions and Results

Table 1 provides a summary of reliability testing results, the environmental stress conditions, and the qualification vehicle information.

Based on the data gathered to date, the Fujitsu package substrate has demonstrated a satisfactory result and meets qualification requirements for releasing to Flip-Chip package production assembly.

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Table 1: **Reliability Test Conditions and Results**

Test	Conditions	Test Vehicle	Lot Qty	Cum Device-Hr/Cyc	# of Failures
TC-B(1)	-55 to +125°C	XC4VFX60/FF1152	1	77,000	0
		XC4VFX60/FF672	1	80,000	0
		XC4VLX160/FF1148	1	43,000	0
		XC2VP50/FF1152	2	70,000	0
		XC2VP50/FF1517	2	68,000	0
		XC2VP40/FF1152	2	68,000	0
		XC2VP20/FF896	2	70,000	0
		XC2VP20/FF1152	2	70,000	0
		XC2VP30/FF896	2	70,000	0
		XC2VP30/FF1152	2	70,000	0
THB(1)	85°C, 85%RH, Bias, V_{CCMAX}	XC4VFX20/FF672	1	67,000	0
TH(1)	85°C, 85%RH, No bias	XC4VFX20/FF672	1	77,000	0
HTS	150°C	XC4VFX20/FF672	1	77,000	0

Note:

1. Package level-4 preconditioning with Lead-free reflow temperature performed prior to THB, TH, and TC-B tests.

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Qualification Data

Table 2: **Qualification Data**

Test	Conditions	Rel #	Device	Package	Samples	Duration	Fail Qty
TC-B(1)	-55°C/+125°C	2005	XC4VFX60	FF1152	77	1,000 cycs	0
TC-B(1)	-55°C/+125°C	3105	XC4VFX60	FF672	80	1,000 cycs	0
TC-B(1)	-55°C/+125°C	20805	XC4VLX160	FF1148	43	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120088	XC2VP50	FF1152	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120089	XC2VP50	FF1152	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120366	XC2VP50	FF1517	33	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120367	XC2VP50	FF1517	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120368	XC2VP40	FF1152	33	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120369	XC2VP40	FF1152	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120370	XC2VP20	FF896	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120371	XC2VP20	FF896	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120372	XC2VP20	FF1152	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120373	XC2VP20	FF1152	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120374	XC2VP30	FF896	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120375	XC2VP30	FF896	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120381	XC2VP30	FF1152	35	1,000 cycs	0
TC-B(1)	-55°C/+125°C	L6120382	XC2VP30	FF1152	35	1,000 cycs	0
THB(1)	85°C, 85%RH, Bias, V_{CCMAX}	9405	XC4VFX20	FF672	67	1,000 hrs	0
TH(1)	85°C, 85%RH	11105	XC4VFX20	FF672	77	1,000 hrs	0
HTS	T_A = 150°C	11205	XC4VFX20	FF672	77	1,000 hrs	0

Note:

1. Package level-4 preconditioning with Lead-free reflow temperature performed prior to THB, TH, and TC-B tests.

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