Spartan-3A/3AN Starter Kit Board Schematic

(Annotated)

21-AUG-2007

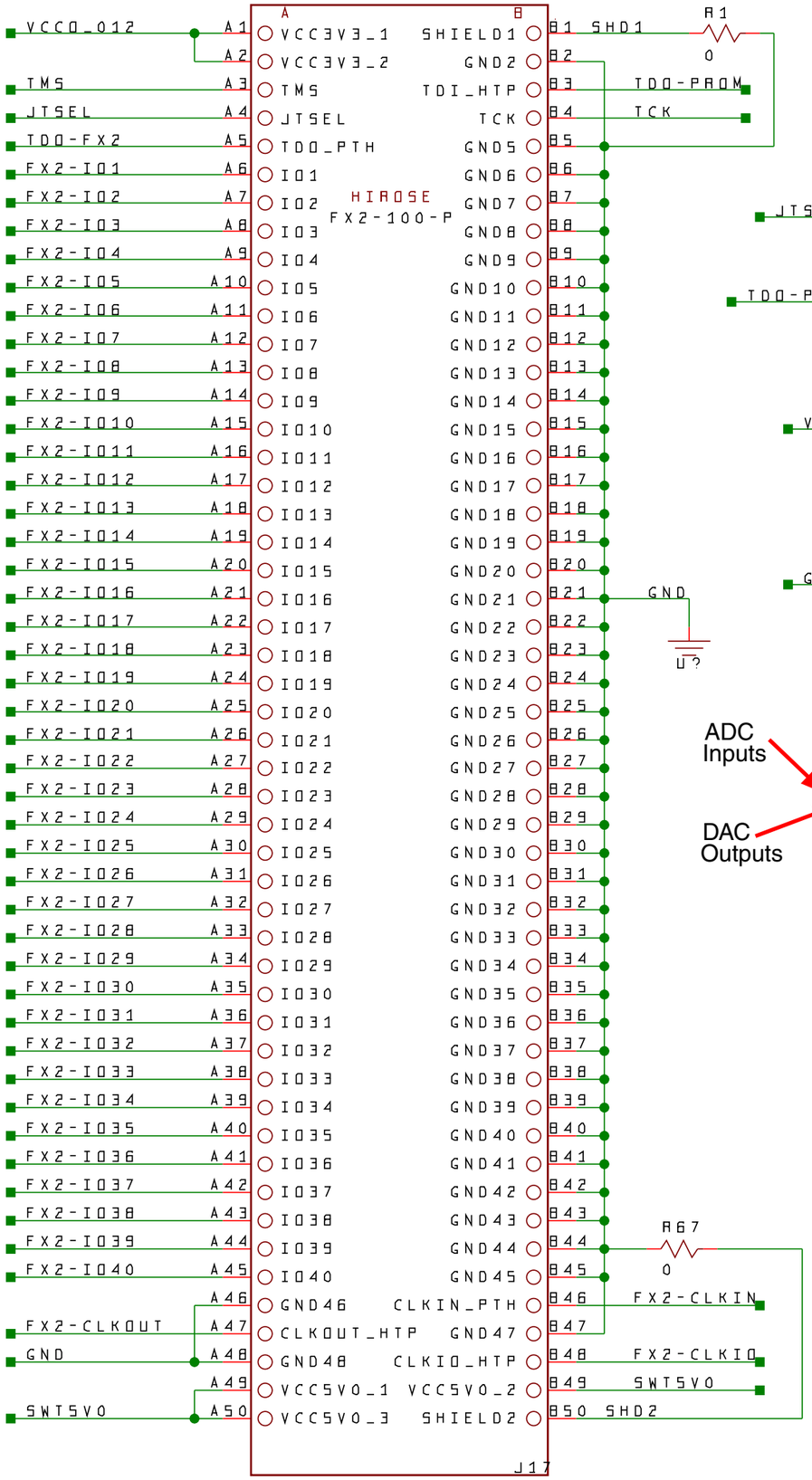
For additional information …

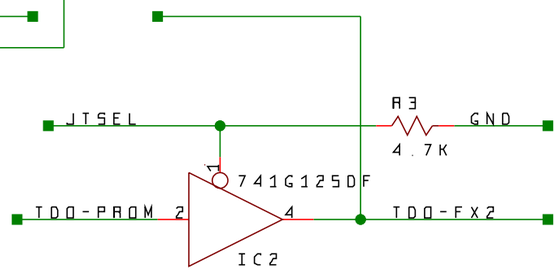
www.xilinx.com/s3astarter

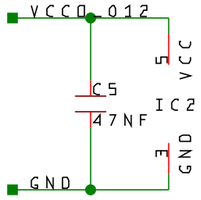
See UG334: Spartan-3A/3AN Starter Kit User Guide for further information on each board feature

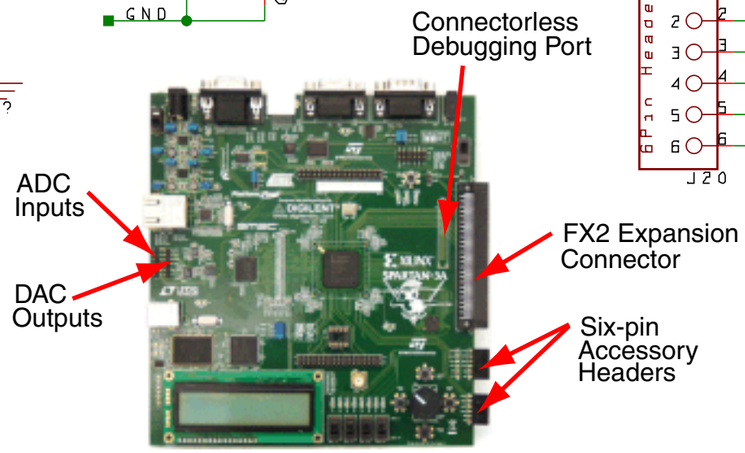
XILINX®

Hirose FX2 100-pin Expansion Connector

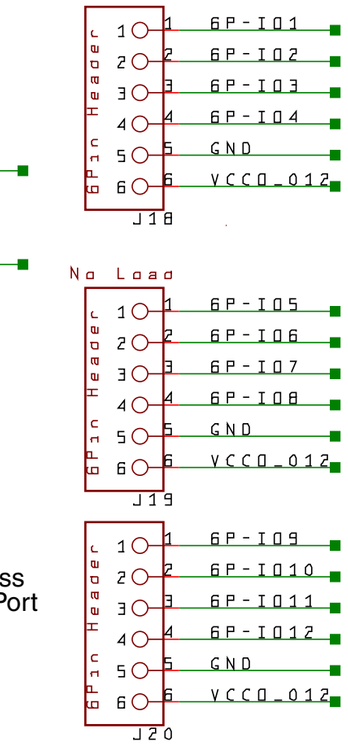




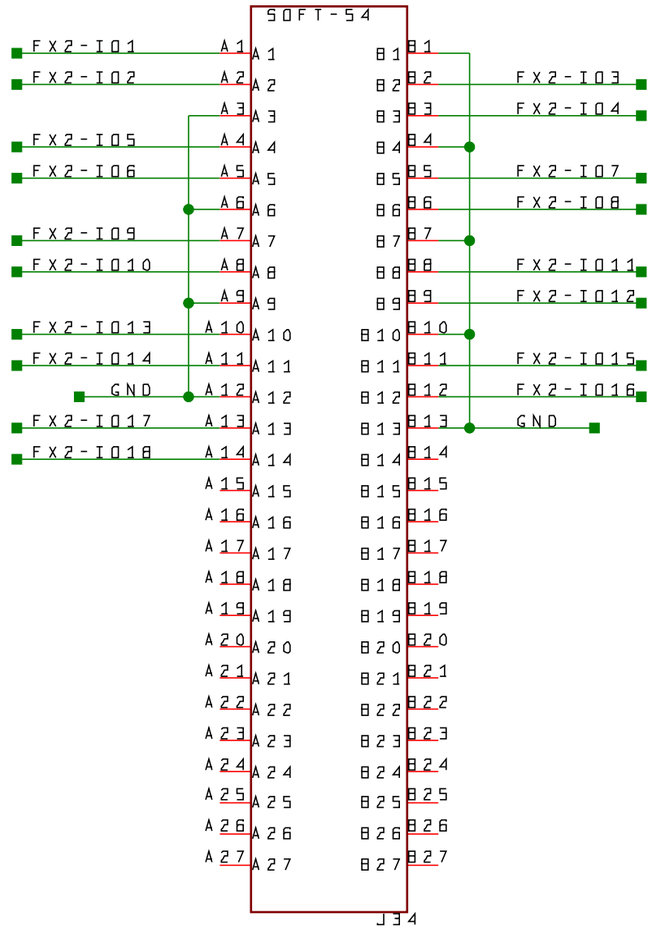




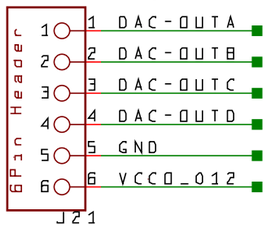
Six-pin Accesory Headers



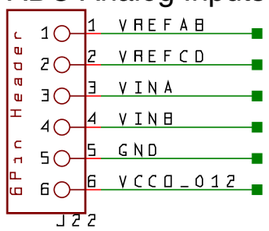
Connectorless Debugging Port Landing Pads



DAC Analog Outputs



ADC Analog Inputs



JTAG Scan Chain

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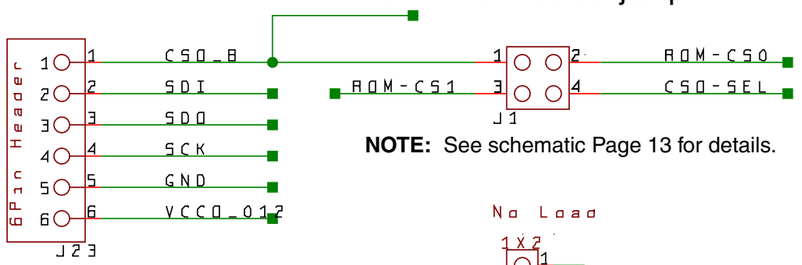
TITLE: **Spartan-3A/3AN Starter Kit Board**

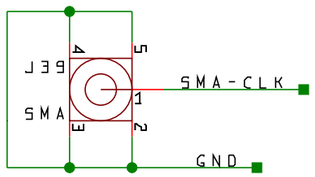
DESCRIPTION: FX2 Expansion Connector, 6-pin Headers	ENGINEER: CC
Copyright 2006	AUTHOR: GMA
SHEET 2 of 17	DOC# 500-112
REVISION: C	DATE: 12-13-2006_16:57

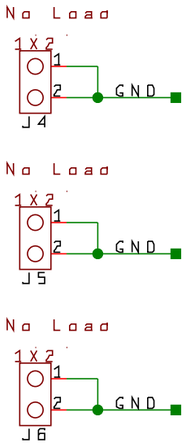
SPI PROM select jumpers



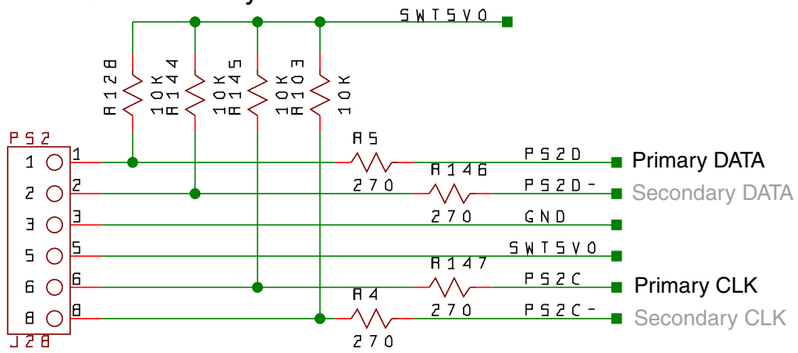
NOTE: See schematic Page 13 for details.

Clock Input/Output SMA connector



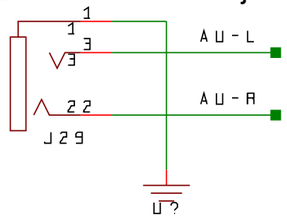


PS/2 Mouse/Keyboard connector

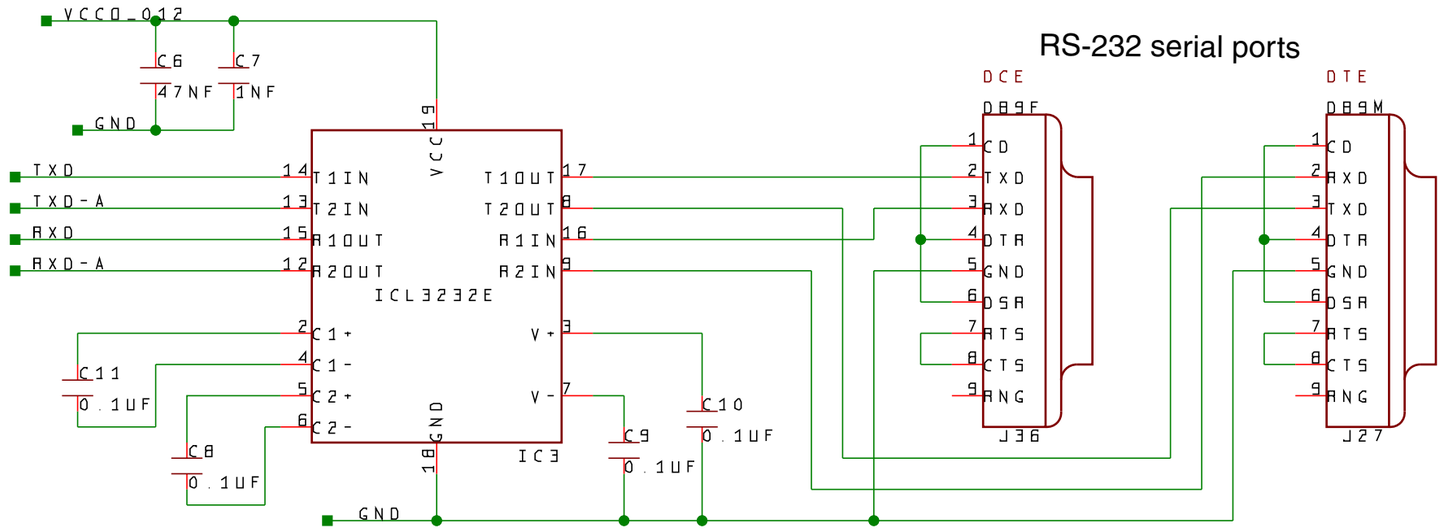


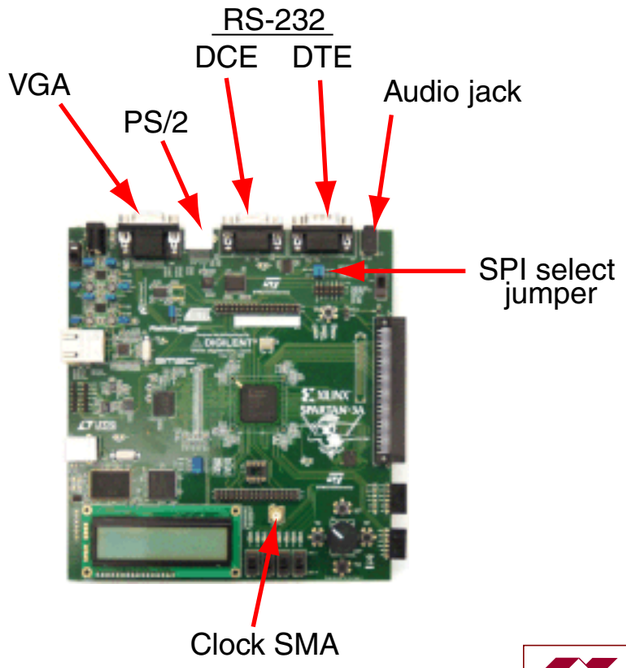
The PS/2 connector has primary and secondary connections to the FPGA. The secondary connections are available by attaching an external Y-splitter cable.

Stereo Audio mini jack

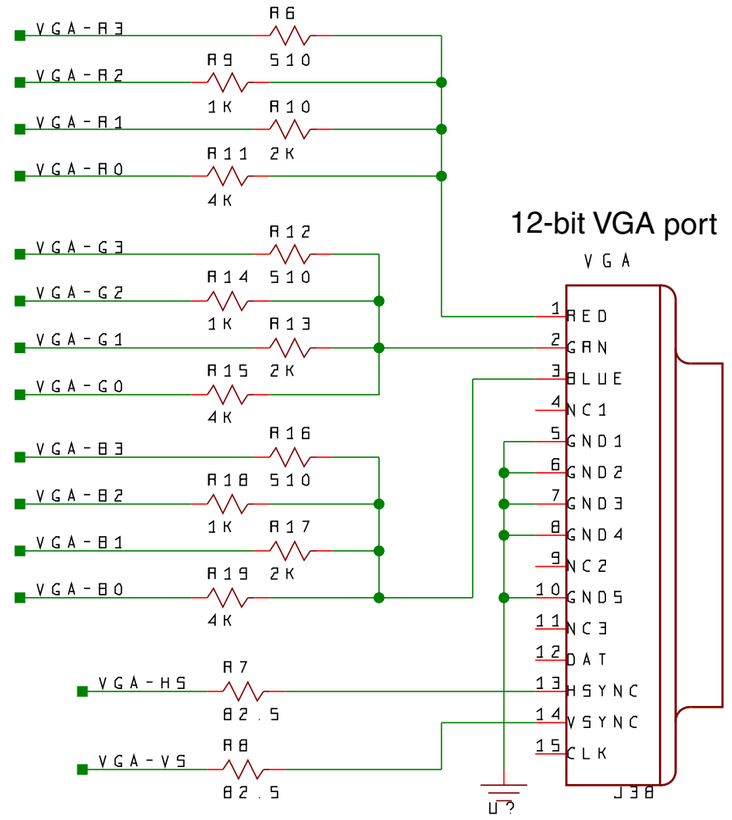


RS-232 serial ports





12-bit VGA port



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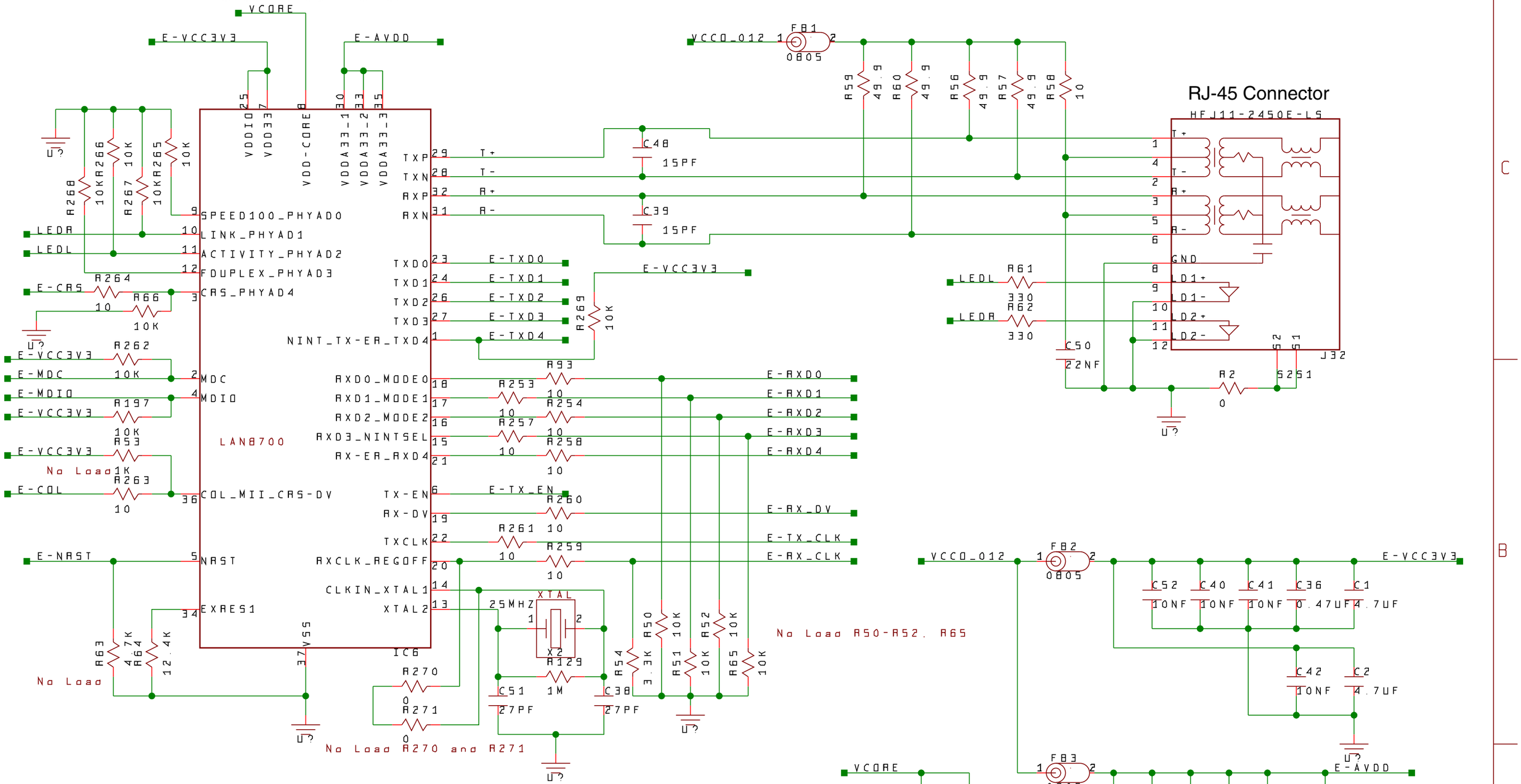
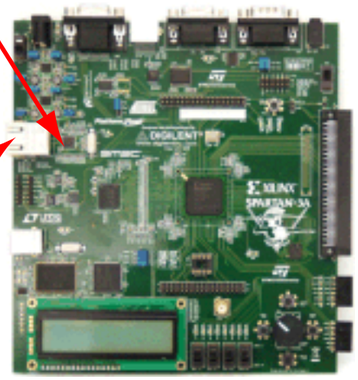
TITLE: **Spartan-3A/3AN Starter Kit Board**	
DESCRIPTION: RS-232, VGA, Audio ports, SMA connector Copyright 2006	ENGINEER: CC AUTHOR: GMA
SHEET 3 of 17 · DOC# 500-112 · REVISION C	DATE: 12-13-2006_16:57

LAN8700 10/100 Ethernet PHY



LAN8700 10/100 Ethernet PHY



RJ-45 Connector

smsc® SUCCESS BY DESIGN

www.smsc.com/main/catalog/lan8700.html

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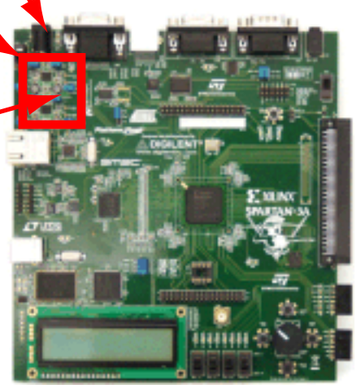
TITLE	Spartan-3A/3AN Starter Kit Board
DESCRIPTION	10/100 Ethernet PHY, magnetics
Copyright 2006	
ENGINEER	CC
AUTHOR	GMA
SHEET 4 of 17	DOC# 500-112
REVISION	C
DATE	12-13-2006_16:57

PWR-COAX
VCC5V0
J35
SW5
POWER SWITCH
J14
No Load
POWER
LED
R251 390
R69 1K
SW15V0
C230 C231 10UF 10UF
C57 C55 C56 1UF 1UF 1UF
LP3906SQ
AVDD ENSW1 ENSW2 ENLDO1 ENLDO2 EN_T
VIN1 VIN2 VINLDO1 VINLDO2 VINLDO12
SW1 FB1 SW2 FB2 LDO1 LDO2 SDA SCL SYNC
GND_SW1 GND_SW2 GND_L GND_C PAD
IC19
NP04SZ L1 2.2UH
NP04SZ L2 2.2UH
R198 10K R199 10K
VCC0_012
I2C Interface
REG1-SDA
REG1-SCL
No Load R273, R274 and C49, C201, C202
C49 13PF
R272 280K
R273 200K
C202 3.1PF
R275 1.1M
R274 200K
C201 18PF
C232 10UF
C233 10UF
C234 0.47UF
C235 0.47UF
VCCINT 1.2V
FPGA core supply (1.2V)
VCC0_012
FPGA I/O Banks 0, 1, 2 (3.3V)
Bank 0
Bank 1
Bank 2
FPGA
VCCAUX
3.3/2.5/2.0V
FPGA auxiliary supply (3.3V)
USB1V8
Embedded USB / JTAG Programmer (1.8V)
Bank 3
FPGA
R69 1K
SW15V0
C229 C245 10UF 10UF
C54 C53 C4 1UF 1UF 1UF
LP3906SQ
AVDD ENSW1 ENSW2 ENLDO1 ENLDO2 EN_T
VIN1 VIN2 VINLDO1 VINLDO2 VINLDO12
SW1 FB1 SW2 FB2 LDO1 LDO2 SDA SCL SYNC
GND_SW1 GND_SW2 GND_L GND_C PAD
IC18
NP04SZ L3 2.2UH
NP04SZ L4 2.2UH
R200 10K R201 10K
VCC0_012
I2C Interface
REG2-SDA
REG2-SCL
No Load R276, R278 and C203-C204
C203 22PF
R277 160K
R276 200K
C204 6.8PF
R279 520K
R278 200K
C227 10UF
C226 10UF
C246 0.47UF
C247 0.47UF
DDR0V9 0.9V
DDR2 SDRAM Termination (0.9V)
DDR1V8 1.8V
DDR2 SDRAM Device, FPGA I/O Bank 3 (1.8V)
DAC-REF_CD 1V-3.3V
DAC Reference Voltage (3.3V)
VREF1V8
R116 1.8V 200
VREF0V9 0.9V
R117 200
DDR2 SDRAM Voltage Ref. (0.9V)

Wall power adapter input
Power switch
Voltage regulators



National Semiconductor
www.national.com/pf/LP/LP3906.html

Resistors R272, R275, R277, R279 must be 0 ohm if external feedback networks are removed

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TITLE: Spartan-3A/3AN Starter Kit Board

DESCRIPTION	ENGINEER	AUTHOR	DATE
Voltage regulators Copyright 2006	CC	GMA	12-13-2006_16:56

SHEET	DOC#	REVISION
5 of 17	500-112	C

JTAG Header

FPGA Configuration Control

SUSPEND slide switch

PROG_B jumper

PROG_B pushbutton

DONE LED

Platform Flash Enable (Jumper J46)

Platform Flash PROM

FPGA Mode Select jumper (Jumper J26)

Platform Flash Enable Jumper (Jumper J46)

DISABLE

Enable only during configuration

Enable Always

Second 4 Mbit Platform Flash PROM is not mounted

Master Serial

Also enable Platform Flash PROM using Jumper J46

JTAG

Disable Platform Flash PROM by removing Jumper J46

Master SPI

Master BPI

(Spartan-3AN only) Master Internal SPI

Platform Flash PROM

Platform Flash Enable Jumper (Jumper J46)

JTAG Header

SUSPEND switch

PROG_B pushbutton

DONE LED

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TITLE: **Spartan-3A/3AN Starter Kit Board**

DESCRIPTION: Configuration, Mode pins, Platform Flash PROM
SUSPEND pin, JTAG header

ENGINEER: CC

AUTHOR: GMA

SHEET 6 of 17

DOC# 500-112

REVISION C

DATE 12-13-2006_16:56

FPGA: XC3S700A/AN-4FGG484C(E

BANK 1

NF-BYTE	Y21	IO_L01N_1_LDC2	G22	NF-A15	IO_L30N_1_A15
NF-WE	AA22	IO_L01P_1_HDC	H22	NF-A14	IO_L30P_1_A14
NF-CE0	W20	IO_L02N_1_LDC0	K18	FX2-IO31	IO_L32N_1
NF-OE	W19	IO_L02P_1_LDC1	K17	FX2-IO32	IO_L32P_1
NF-A1	T18	IO_L03N_1_A1	H20	NF-A17	IO_L33N_1_A17
NF-A0	T17	IO_L03P_1_A0	H21	NF-A16	IO_L33P_1_A16
LD7	W21	IO_L05N_1	F21	NF-A19	IO_L34N_1_A19
LD6	Y22	IO_L05P_1	F22	NF-A18	IO_L34P_1_A18
LD5	V20	IO_L06N_1	G20	FX2-IO27	IO_L36N_1
LD4	V19	IO_L06P_1	G19	FX2-IO28	IO_L36P_1
NF-D10	V22	IO_L07N_1	H19	FX2-IO29	IO_L37N_1
NF-D9	W22	IO_L07P_1	J18	FX2-IO30	IO_L37P_1
NF-D11	U21	IO_L09N_1	F20	FX2-IO25	IO_L38N_1
NF-D12	U22	IO_L09P_1	E20	FX2-IO26	IO_L38P_1
LD3	U19	IO_L10N_1	F18	FX2-IO23	IO_L40N_1
LD2	U20	IO_L10P_1	F19	FX2-IO24	IO_L40P_1
NF-D13	T22	IO_L11N_1	D22	FX2-IO21	IO_L41N_1
NF-D8	T20	IO_L11P_1	E22	FX2-IO22	IO_L41P_1
LD1	T19	IO_L13N_1	D20	FX2-IO19	IO_L42N_1
LD0	R20	IO_L13P_1	D21	FX2-IO20	IO_L42P_1
NF-RP	R22	IO_L14N_1	C21	NF-A21	IO_L44N_1_A21
NF-D14	R21	IO_L14P_1	C22	NF-A20	IO_L44P_1_A20
NF-STS	P22	IO_L15N_1_VREF_1	B21		IO_L45N_1_A23
FX2-IO40	P20	IO_L15P_1	B22		IO_L45P_1_A22
NF-A3	P18	IO_L17N_1_A3	G17		IO_L46N_1_A25
NF-A2	R19	IO_L17P_1_A2	G18		IO_L46P_1_A24
NF-A5	N21	IO_L18N_1_A5	R16		IP_L04N_1_VREF_1
NF-A4	N22	IO_L18P_1_A4	R15		IP_L04P_1
NF-A7	N19	IO_L19N_1_A7	P16		IP_L08N_1
NF-A6	N20	IO_L19P_1_A6	P15		IP_L08P_1
NF-A9	N17	IO_L20N_1_A9	R18		IP_L12N_1_VREF_1
NF-A8	N18	IO_L20P_1_A8	R17		IP_L12P_1
FX2-CLKOUT	L22	IO_L21N_1_RHCLK1	N16		IP_L16N_1_VREF_1
FX2-CLKIN	M22	IO_L21P_1_RHCLK0	N15		IP_L16P_1
FX2-IO39	L20	IO_L22N_1_TRDY1_RHCLK3	M16		IP_L23N_1
FX2-CLKIO	L21	IO_L22P_1_RHCLK2	M17		IP_L23P_1
FX2-IO37	M20	IO_L24N_1_RHCLK5	L16		IP_L27N_1
FX2-IO38	M18	IO_L24P_1_RHCLK4	M15		IP_L27P_1_VREF_1
FX2-IO33	K19	IO_L25N_1_RHCLK7	K16		IP_L31N_1
FX2-IO34	K20	IO_L25P_1_IRDY1_RHCLK6	L15		IP_L31P_1
NF-A11	J22	IO_L26N_1_A11	K15		IP_L35N_1
NF-A10	K22	IO_L26P_1_A10	K14		IP_L35P_1_VREF_1
FX2-IO35	L19	IO_L28N_1	H18		IP_L39N_1
FX2-IO36	L18	IO_L28P_1	H17		IP_L39P_1
NF-A13	J20	IO_L29N_1_A13	J15		IP_L43N_1_VREF_1
NF-A12	J21	IO_L29P_1_A12	J16		IP_L43P_1
			H15		IP_L47N_1
			H16		IP_L47P_1_VREF_1

IC1

FPGA Bank 1

VCCO_012

C69 0.1UF — IC13 SG8002 (VDD, OE, GND, OUT) — CLK_50MHZ — GCLK5

50 MHz Oscillator

C70 0.1UF — IC14 OSC (VDD, OE, GND, OUT) — CLK_AUX — GCLK2

Auxiliary Oscillator Socket

FPGA: XC3S700A/AN-4FGG484C(ES)

BANK 0

FX2-IO17	D18	IO_L01N_0	C9	VGA-B3	IO_L24N_0_VREF_0
FX2-IO18	E17	IO_L01P_0	B9	VGA-B2	IO_L24P_0
FX2-IO15	C19	IO_L02N_0	C8	VGA-B3	IO_L25N_0
FX2-IO16	D19	IO_L02P_0_VREF_0	B8	VGA-B2	IO_L25P_0
FX2-IO13	A20	IO_L03N_0	A6	R2-	IO_L26N_0
FX2-IO14	B20	IO_L03P_0	A7	R2+	IO_L26P_0
TXD	F15	IO_L04N_0	C7	VGA-B0	IO_L27N_0
TXD-A	E15	IO_L04P_0	D7	VGA-B1	IO_L27P_0
FX2-IO9	A18	IO_L05N_0	A5	R1-	IO_L28N_0
FX2-IO10	C18	IO_L05P_0	B6	R1+	IO_L28P_0
FX2-IO11	A19	IO_L06N_0	D6	VGA-G3	IO_L29N_0
FX2-IO12	B19	IO_L06P_0_VREF_0	C6	VGA-G2	IO_L29P_0
	C17	IO_L07N_0	D8	E-TX_EN	IO_L30N_0
	D17	IO_L07P_0	E9		IO_L30P_0
	C16	IO_L08N_0	B4	R0-	IO_L31N_0
AD-SDO	D16	IO_L08P_0	A4	R0+	IO_L31P_0
NF-WP	E14	IO_L09N_0	D5	VGA-G1	IO_L32N_0
ROM-WP	C14	IO_L09P_0	C5	VGA-G0	IO_L32P_0
FX2-IO7	A17	IO_L10N_0	B3	VGA-R1	IO_L33N_0
FX2-IO8	B17	IO_L10P_0	A3	VGA-R0	IO_L33P_0
ROM-RST	C15	IO_L11N_0	F8	E-TXD0	IO_L34N_0
E-NRST	D15	IO_L11P_0	E7	E-TXD1	IO_L34P_0
FX2-IO5	A15	IO_L12N_0_VREF_0	E6	E-TXD2	IO_L35N_0
FX2-IO6	A16	IO_L12P_0	F7	E-TXD3	IO_L35P_0
FX2-IO3	A14	IO_L13N_0	B2	E-TXD4	IO_L36P_0_VREF_0
FX2-IO4	B15	IO_L13P_0	E8		IP1
REG1-SCL	E13	IO_L14N_0	E16	RXD	IP2
REG2-SDA	F13	IO_L14P_0	F10		IP3
ROM-W	C13	IO_L15N_0	F12		IP4
REG1-SDA	D13	IO_L15P_0	F16	RXD-A	IP5
FX2-IO1	A13	IO_L16N_0	G9	E-RXD2	IP6
FX2-IO2	B13	IO_L16P_0	G10	E-RXD4	IP7
GCLK5	E12	IO_L17N_0_GCLK5	G11		IP8
E-RX_CLK	C12	IO_L17P_0_GCLK4	G12	E-COL	IP9
RCK-	A11	IO_L18N_0_GCLK7	G13		IP10
RCK+	A12	IO_L18P_0_GCLK6	G14		IP11
VGA-HS	C11	IO_L19N_0_GCLK9	G15		IP12
VGA-VS	B11	IO_L19P_0_GCLK8	G16		IP13
E-TX_CLK	E11	IO_L20N_0_GCLK11	H10	E-RX_DV	IP14
REG2-SCL	D11	IO_L20P_0_GCLK10	H13		IP15
R4-	C10	IO_L21N_0	H14		IP16
R4+	A10	IO_L21P_0	G7	E-RXD0	IP17_IREF
R3-	A8	IO_L22N_0	G8	E-RXD1	IP18_VREF_0
R3+	A9	IO_L22P_0	H9	E-RXD3	IP19_VREF_0
E-MDIO	E10	IO_L23N_0	H12	E-CRS	IP20_VREF_0
E-MDC	D10	IO_L23P_0			

IC1

FPGA Bank 0

XILINX®

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TITLE: **Spartan-3A/3AN Starter Kit Board**

DESCRIPTION: FPGA I/O Bank 0 and Bank 1, Clock Oscillators

ENGINEER: CC

AUTHOR: GMA

SHEET 7 of 17 | DOC# 500-112 | REVISION C | DATE 12-13-2006_16:56

FPGA: XC3S700A/AN-4FGG484C(ES)

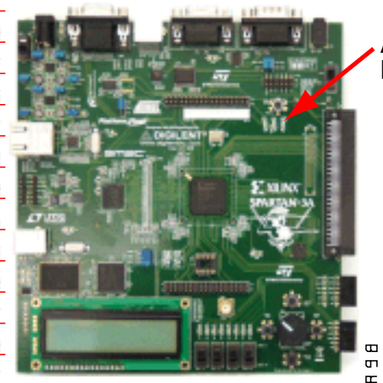
BANK 3

FPGA I/O Bank 3 is dedicated to the DDR2 SDRAM interface

	IO_L01N_3	D2	R2	SD-A0	
	IO_L01P_3	C1	R1	SD-A2	
	IO_L02N_3	C2	R4		
	IO_L02P_3	B1	R3	SD-BA1	
	IO_L03N_3	E4	T4	SD-A1	
	IO_L03P_3	D3	R5		
	IO_L05N_3	G5	T3	SD-A10	
	IO_L05P_3	G6	T1	VREFOV9	
	IO_L06N_3	E1	U2	SD-A4	
	IO_L06P_3	D1	U1	SD-A6	
SD-UDM	IO_L07N_3	E3	V3	SD-A13	
	IO_L07P_3	F4	V1	SD-A11	
SD-DQ9	IO_L08N_3	G4	U5		
SD-DQ15	IO_L08P_3	F3	T5		
SD-DQ11	IO_L09N_3	H6	U4	SD-A5	
SD-DQ12	IO_L09P_3	H5	U3	SD-A3	
SD-UDQS_N	IO_L10N_3	J5	W2	SD-A9	
SD-UDQS_P	IO_L10P_3	K6	W1	SD-A8	
SD-DQ13	IO_L12N_3	F1	W3	SD-A15	
SD-DQ8	IO_L12P_3	F2	V4	SD-A14	
SD-DQ10	IO_L13N_3	G1	Y2	SD-A12	
SD-DQ14	IO_L13P_3	G3	Y1	SD-A7	
SD-LDQP	IO_L14N_3	H3	AA2		
SD-LDQP	IO_L14P_3	H4	AA1		
SD-DQ0	IO_L16N_3	H1	J8	VREFOV9	
SD-DQ7	IO_L16P_3	H2	R6	VREFOV9	
VREFOV9	IO_L17N_3_VREF_3	J1	H7	VREFOV9	
SD-LDM	IO_L17P_3	J3	H8		
SD-DQ6	IO_L18N_3	K4	K8		
SD-DQ1	IO_L18P_3	K5	J7		
SD-LDQS_N	IO_L20N_3	K2	L8	VREFOV9	
SD-LDQS_P	IO_L20P_3	K3	K7		
SD-DQ3	IO_L21N_3_LHCLK1	L3	M8		
SD-DQ4	IO_L21P_3_LHCLK0	L5	L7		
SD-DQ5	IO_L22N_3_IRDY2_LHCLK3	L1	M6		
SD-DQ2	IO_L22P_3_LHCLK2	K1	M7		
SD-CK_N	IO_L24N_3_LHCLK5	M2	N9		
SD-CK_P	IO_L24P_3_LHCLK4	M1	N8		
SD-CAS	IO_L25N_3_LHCLK7	M4	N5		
SD-RAS	IO_L25P_3_TRDY2_LHCLK6	M3	N6		
SD-CKE	IO_L26N_3	N3	P8		
VREFOV9	IO_L26P_3_VREF_3	N1	N7		
	IO_L28N_3	P2	R8		
SD-ODT	IO_L28P_3	P1	P7		
SD-BA2	IO_L29N_3	P5	T6	VREFOV9	
SD-BA0	IO_L29P_3	P3	R7		
SD-WE	IO_L30N_3	N4			
SD-CS	IO_L30P_3	M5			
	IO_L36P_3_VREF_3				
	IP_L04N_3_VREF_3				
	IP_L15N_3_VREF_3				
	IP1_VREF_3				
	IP2_VREF_3				

IC1

Bank 3 FPGA



AWAKE LED

R98 680

LD13

SG-BGA-6007

NC 1 3 NC

NC 2 4 NC

J33

Ironwood Connector

interface

FPGA: XC3S700A/AN-4FGG484C(ES)

BANK 2

IO-	AA3	IO_L03N_2		IO_L26N_2_D3	U13	NF-D3
IO+	AB2	IO_L03P_2		IO_L27N_2	Y16	LCD-DB5
I1-	AA4	IO_L04N_2		IO_L27P_2	AB16	LCD-DB6
I1+	AB3	IO_L04P_2		IO_L28N_2_D1	Y17	NF-D1
CSO-SEL	Y5	IO_L05N_2		IO_L28P_2_D2	AA17	NF-D2
AMP-CS	W6	IO_L05P_2		IO_L29N_2	AB18	LCD-DB1
	AB5	IO_L06N_2		IO_L29P_2	AB17	LCD-DB2
LCD-E	AB4	IO_L06P_2		IO_L30N_2	V15	GP-IO10
AD-CONV	Y6	IO_L07N_2		IO_L30P_2	V14	GP-IO9
DAC-CS	W7	IO_L07P_2		IO_L31N_2	V16	GP-IO12
I2-	AB6	IO_L08N_2		IO_L31P_2	W16	GP-IO11
I2+	AA6	IO_L08P_2		IO_L32N_2	AA19	GP-IO3
	W9	IO_L09N_2_VS2		IO_L32P_2	AB19	GP-IO4
I3-	AB7	IO_L10N_2		IO_L33N_2	V17	GP-IO7
I3+	Y7	IO_L10P_2		IO_L33P_2	W18	GP-IO6
	Y8	IO_L11N_2_VS0		IO_L34N_2	W17	GP-IO8
	W8	IO_L11P_2_VS1		IO_L34P_2	Y18	GP-IO5
I4-	AB8	IO_L12N_2		IO_L35N_2	AA21	GP-IO1
I4+	AA8	IO_L12P_2		IO_L35P_2	AB21	GP-IO2
AU-L	Y10	IO_L13N_2		IP1	P12	
AU-R	V10	IO_L13P_2		IP2	R9	
NF-D6	AB9	IO_L14N_2_D6		IP3	R10	
NF-D7	Y9	IO_L14P_2_D7		IP4	R11	
TCK-	AB10	IO_L15N_2		IP5	T9	SW3
TCK+	AA10	IO_L15P_2		IP6	T13	ROT-A
NF-D4	AB11	IO_L16N_2_D4		IP7	T14	NORTH
NF-D5	Y11	IO_L16P_2_D5		*IP8	U7	
PS2D	V11	IO_L17N_2_GCLK13		IP9	U8	SW2
PS2C-	U11	IO_L17P_2_GCLK12		IP10	U10	SW1
PS2D-	Y12	IO_L18N_2_GCLK15		IP11	U15	WEST
PS2C	W12	IO_L18P_2_GCLK14		*IP12	U16	
LCD-DB3	AB12	IO_L19N_2_GCLK1		IP13	V7	DA-SDO
LCD-DB4	AA12	IO_L19P_2_GCLK0		IP14_VREF_2	R12	
SMA-CLK	U12	IO_L20N_2_GCLK3		IP15_VREF_2	R13	CENTER
GCLK2	V12	IO_L20P_2_GCLK2		IP16_VREF_2	R14	ROT-B
LCD-DB0	Y13	IO_L21N_2		IP17_VREF_2	T7	AMP-DO
DAC-CLR	AB13	IO_L21P_2		*IP18_VREF_2	T8	
	AA14	IO_L22P_2		IP19_VREF_2	T10	
LCD-RS	Y14	IO_L23N_2		IP20_VREF_2	T11	
LCD-R/W	W13	IO_L23P_2		IP21_VREF_2	T15	SOUTH
AWAKE	AB15	IO_L24P_2_AWAKE		IP22_VREF_2	T16	EAST
LCD-DB7	Y15	IO_L25N_2		IP23_VREF_2	V8	SW0
AMP-SHDN	W15	IO_L25P_2				

IC1

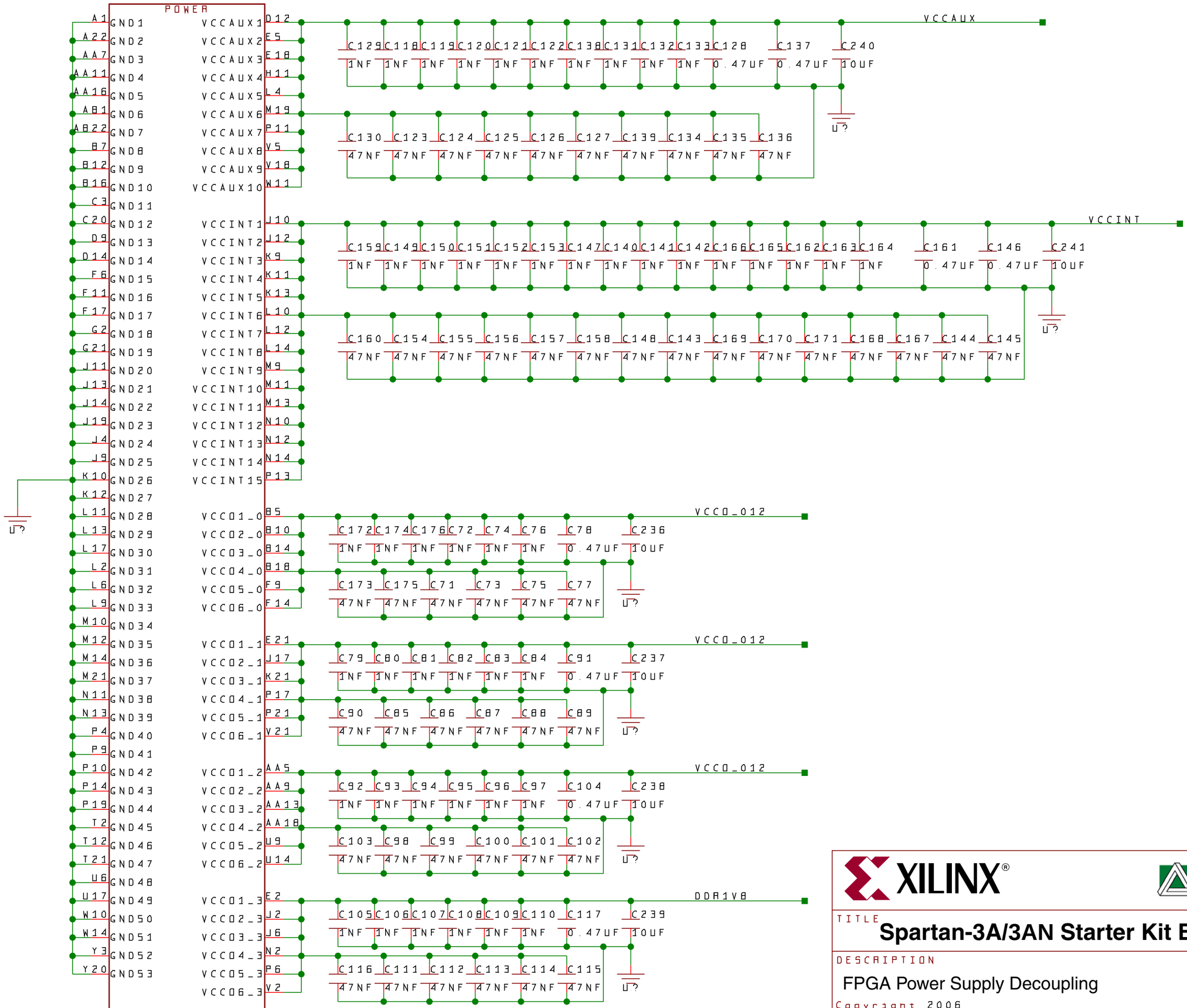
Bank 2 FPGA

* indicates NO CONNECT on the XC3S700A

XILINX®

DIGILENT™

TITLE: Spartan-3A/AN Starter Kit Board	
DESCRIPTION: FPGA I/O Bank 2 and Bank 3	ENGINEER: CC
Copyright 2006	AUTHOR: GMA
SHEET 8 of 17	DOC# 500-112
REVISION: C	DATE: 12-13-2006_16:56



XILINX®

DIGILENT™

TITLE: **Spartan-3A/3AN Starter Kit Board**

DESCRIPTION: FPGA Power Supply Decoupling

ENGINEER: CC

AUTHOR: GMA

SHEET 9 of 17

DOC# 500-112

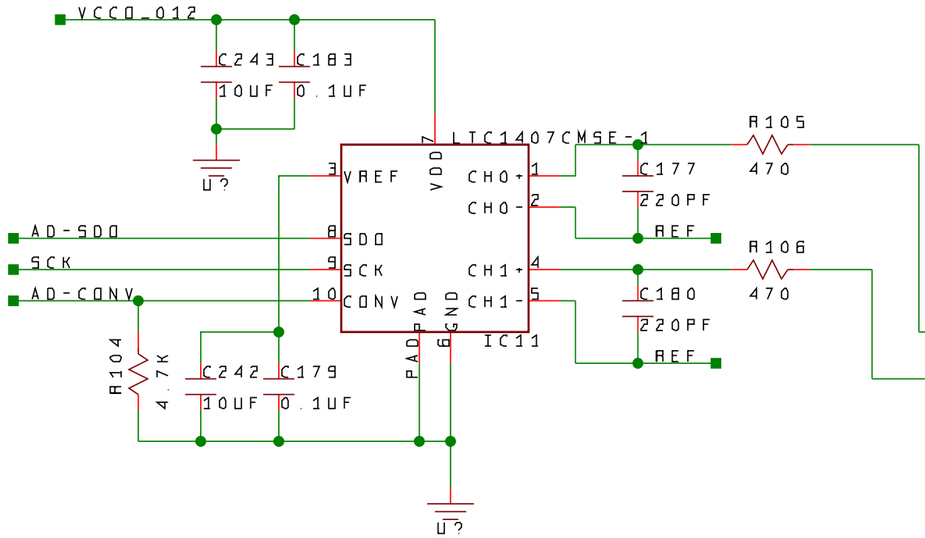
REVISION C

DATE 12-13-2006_16:56

Analog-to-Digital Converter (ADC)

LTC1407-1, two-channel, 12-bit resolution, serial

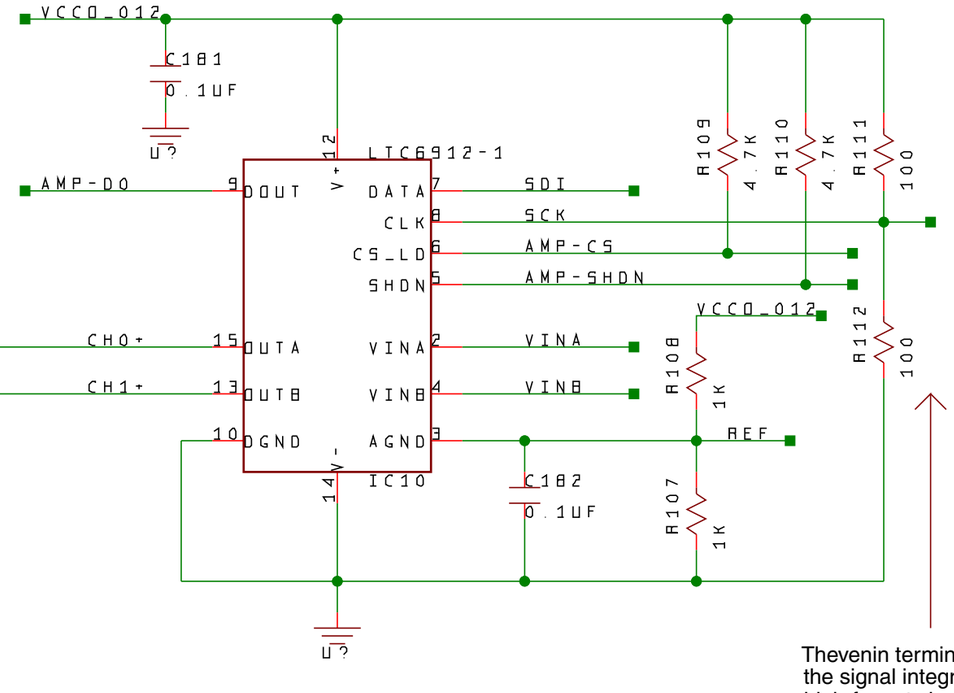
www.linear.com/pc/productDetail.do?navId=H0,C1,C1155,C1001,C1158,P2484



Programmable Gain Amplifier (AMP)

LTC6912-1, two-channel, serial

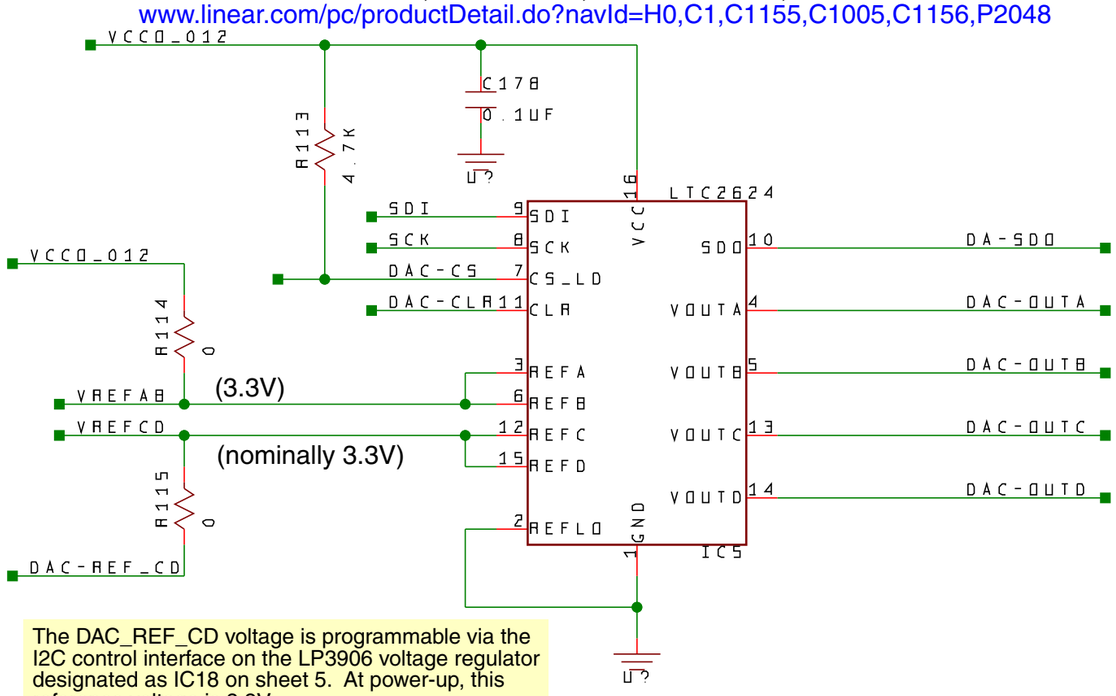
www.linear.com/pc/productDetail.do?navId=H0,C1,C1154,C1009,C1121,P7596



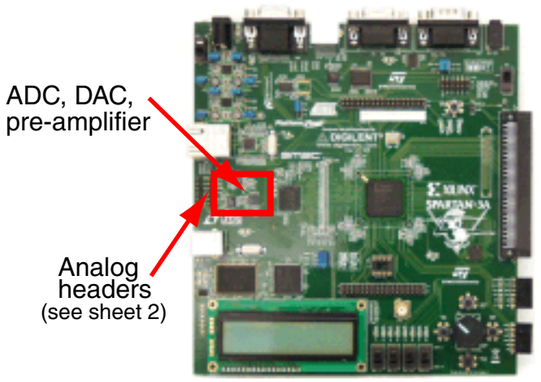
Digital-to-Analog Converter (DAC)

LTC2624, four-channel, 12-bit resolution, serial

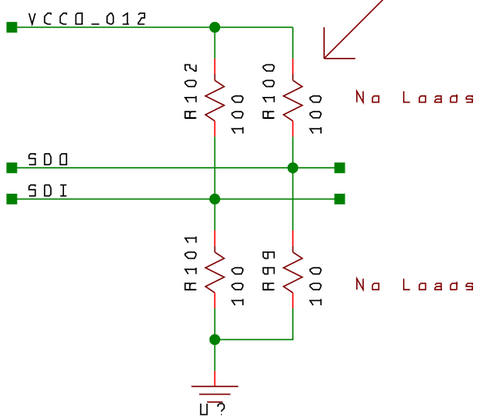
www.linear.com/pc/productDetail.do?navId=H0,C1,C1155,C1005,C1156,P2048



The DAC_REF_CD voltage is programmable via the I2C control interface on the LP3906 voltage regulator designated as IC18 on sheet 5. At power-up, this reference voltage is 3.3V.



Thevenin termination to improve the signal integrity on these high-fanout signals.



LINEAR TECHNOLOGY

www.linear.com

XILINX®

DIGILENT™

TITLE: Spartan-3A/3AN Starter Kit Board			
DESCRIPTION: ADC, DAC, and Pre-amplifier			ENGINEER: CC
Copyright 2006			AUTHOR: GMA
SHEET: 10 of 17	DOC#: 500-112	REVISION: C	DATE: 12-13-2006_16:56

DESIGN NOTE: The Revision C board has an inductor in this location. Shorting across this location improves high-frequency DDR2 SDRAM interface performance.

The Revision D board uses a 0Ω resistor.

0Ω FB5 0805

DDR1V8 1 2

DDR1V8_Q

C185 C186 C187 C188 C189 C190 C191 C192 C193 C194 47NF

C200 47NF

DDR1V8

C195 C196 C197 C198 C199 47NF

VREF0V9

C184 39PF

VDDQ9 VDDQ8 VDDQ7 VDDQ6 VDDQ5 VDDQ4 VDDQ3 VDDQ2 VDDQ1 VDDQ0 VDDL VDD4 VDD3 VDD2 VDD1 VDD0

J2 VREF

SD-A0	M8	A0
SD-A1	M3	A1
SD-A2	M7	A2
SD-A3	N2	A3
SD-A4	N8	A4
SD-A5	N3	A5
SD-A6	N7	A6
SD-A7	P2	A7
SD-A8	P8	A8
SD-A9	P3	A9
SD-A10	M2	A10
SD-A11	P7	A11
SD-A12	R2	A12
SD-A13	R8	A13_RFU
SD-A14	R3	A14_RFU
SD-A15	R7	A15_RFU
SD-BA0	L2	BA0
SD-BA1	L3	BA1
SD-BA2	L1	BA2_RFU
SD-CK_P	J8	CK
SD-CK_N	K8	CK#
SD-CKE	K2	CKE
SD-CS	L8	CS#
SD-RAS	K7	RAS#
SD-CAS	L7	CAS#
SD-WE	K3	WE#

32Mx16 DDR2 SDRAM

MT47H32M16CC-XX

DQ0	G8	SD-DQ0
DQ1	G2	SD-DQ1
DQ2	H7	SD-DQ2
DQ3	H3	SD-DQ3
DQ4	H1	SD-DQ4
DQ5	H9	SD-DQ5
DQ6	F1	SD-DQ6
DQ7	F9	SD-DQ7
DQ8	C8	SD-DQ8
DQ9	C2	SD-DQ9
DQ10	D7	SD-DQ10
DQ11	D3	SD-DQ11
DQ12	D1	SD-DQ12
DQ13	D9	SD-DQ13
DQ14	B1	SD-DQ14
DQ15	B9	SD-DQ15
UDQS	B7	SD-UDQS_P
LDQS	F7	SD-LDQS_P
UDQS#_NU	A8	SD-UDQS_N
LDQS#_NU	E8	SD-LDQS_N
LDM	F3	SD-LDM
UDM	B3	SD-UDM
ODT	K9	SD-ODT

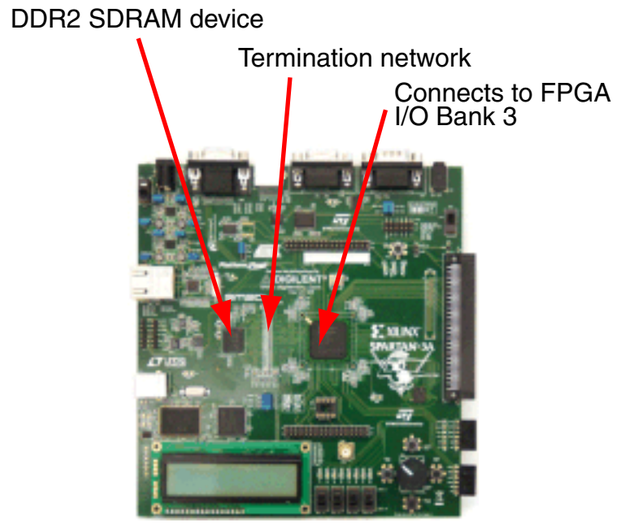
VSSQ9 VSSQ8 VSSQ7 VSSQ6 VSSQ5 VSSQ4 VSSQ3 VSSQ2 VSSQ1 VSSQ0 VSSDL VSS4 VSS3 VSS2 VSS1 VSS0

IC23

0Ω FB4 0805 DDRGND

DESIGN NOTE: The Revision C board has an inductor in this location. Shorting across this location improves high-frequency DDR2 SDRAM interface performance.

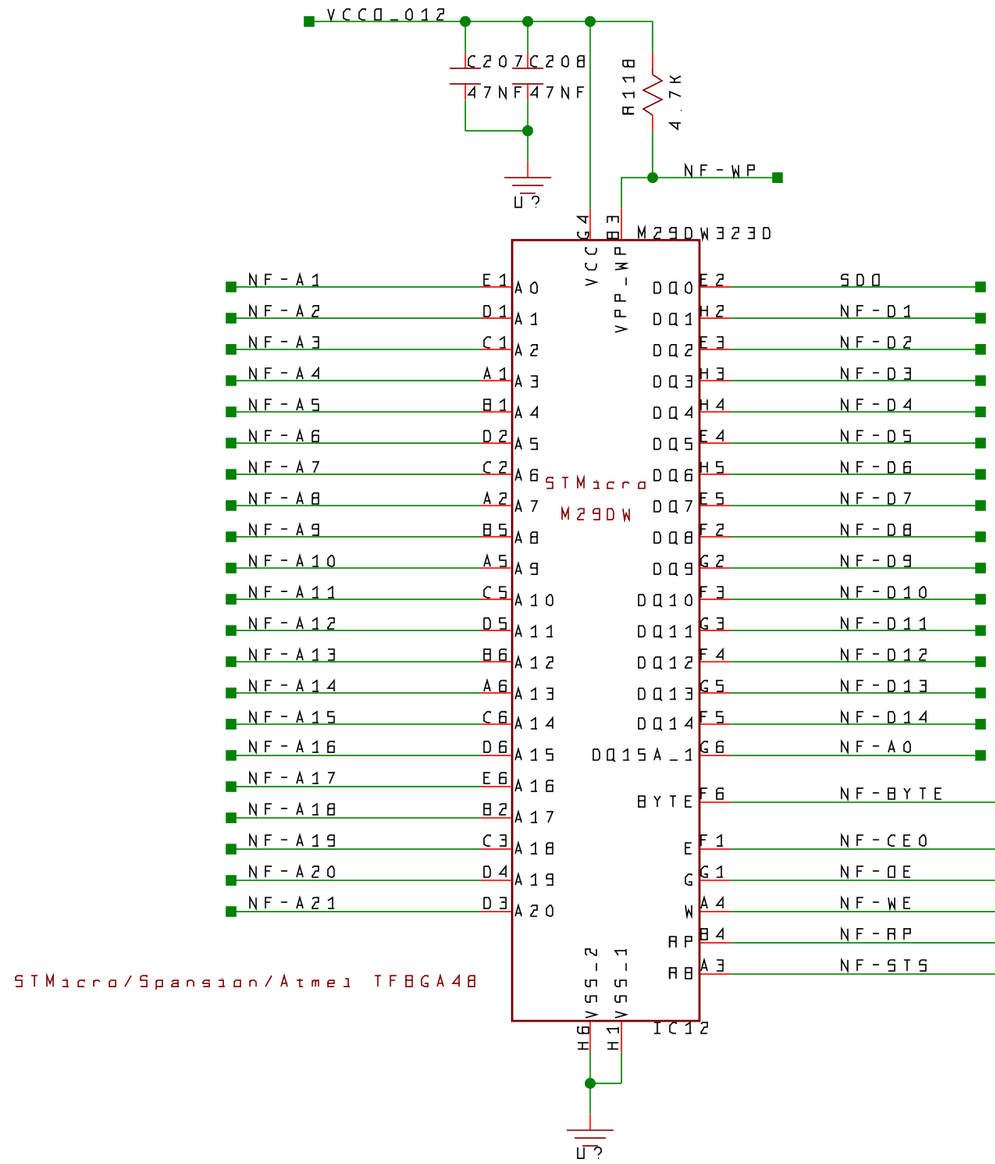
The Revision D board uses a 0Ω resistor.

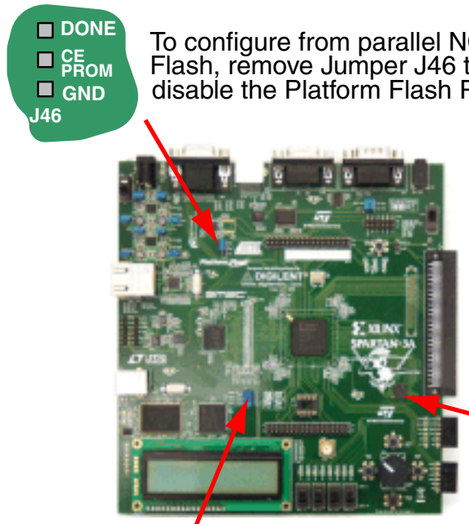


The DDR2 SDRAM interface has specific pin assignment and layout requirements to support the Xilinx Memory Interface Generator (MIG) software. See the "DDR SDRAM" chapter in UG334: Spartan-3A/3AN Starter Kit User Guide.

XILINX® DIGILENT™

TITLE: Spartan-3A/3AN Starter Kit Board			
DESCRIPTION: 32Mx16 DDR2 SDRAM Copyright 2006			ENGINEER: CC AUTHOR: GMA
SHEET 11 of 17	DOC# 500-112	REVISION C	DATE 12-13-2006_16:56





STMicroelectronics

www.st.com/stonline/products/families/memories/fl_nor_emb/fl_m29dw.htm

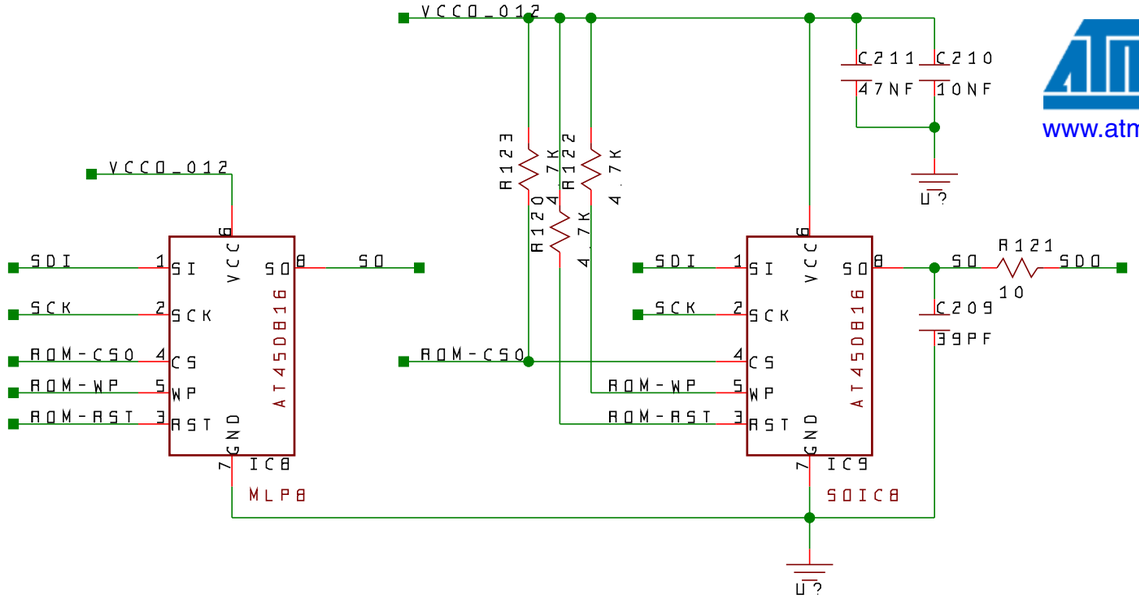
XILINX®

DIGILENT™

TITLE: **Spartan-3A/3AN Starter Kit Board**

DESCRIPTION: M29DW323DT x8/x16 Parallel NOR Flash Copyright 2006			ENGINEER: CC AUTHOR: GMA
SHEET: 12 of 17	DOC#: 500-112	REVISION: C	DATE: 12-13-2006_16:56

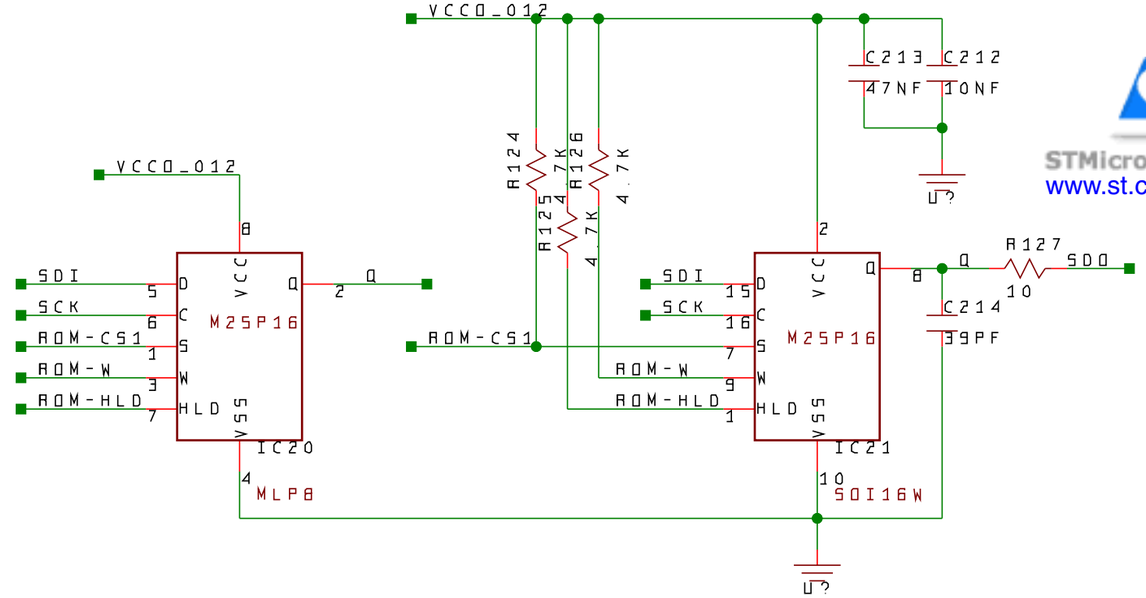
Atmel AT45DB161D 16 Mbit serial DataFlash® PROM



NOTE: Only one of these devices may be loaded at the same time.

www.atmel.com/products/DataFlash/

STMicroelectronics M25P16 16 Mbit SPI serial Flash PROM



NOTE: Only one of these devices may be loaded at the same time.

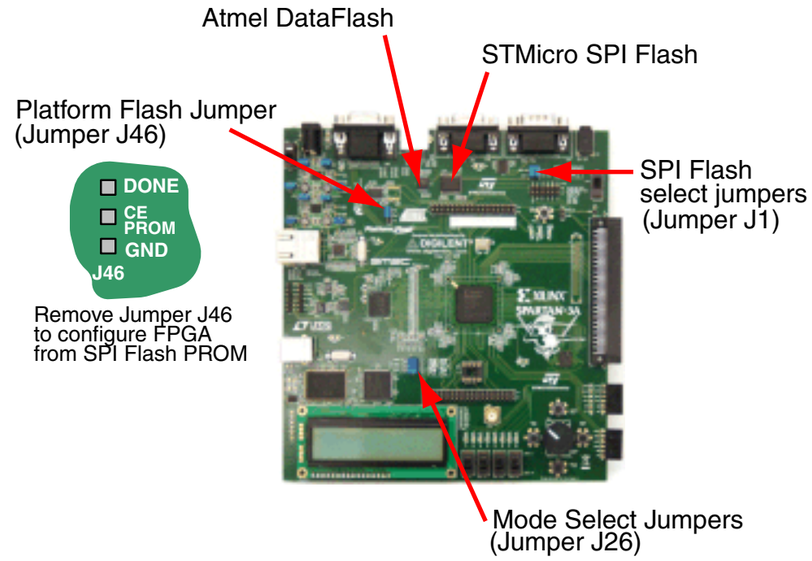
STMicroelectronics
www.st.com/stonline/products/families/memories/fl_ser/index.htm

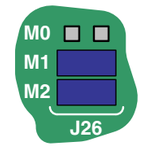
The Spartan-3A Starter Kit board supports multiple pad landings for each SPI Flash architecture. However, only one STMicro and one Atmel PROM are mounted on the board.

Jumper J1 defines which SPI Flash is used for SPI mode configuration and which is available using a second SPI slave select signal.

NOTE: Jumper J1 appears on schematic Page 3.

	Atmel	STMicro
Configure From:		
Atmel Select Signal:	SPI_SS_B	ALT_SS_B
STMicro Select Signal:	ALT_SS_B	SPI_SS_B





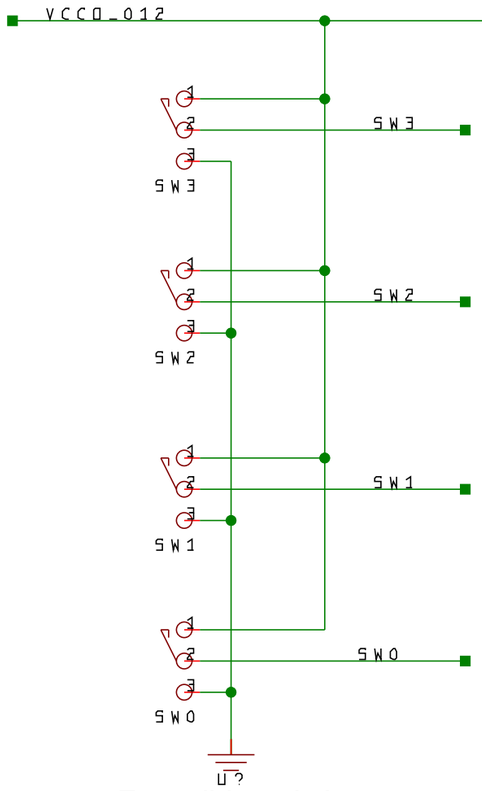
Master SPI Mode
M[2:0]=<0:0:1>

XILINX®

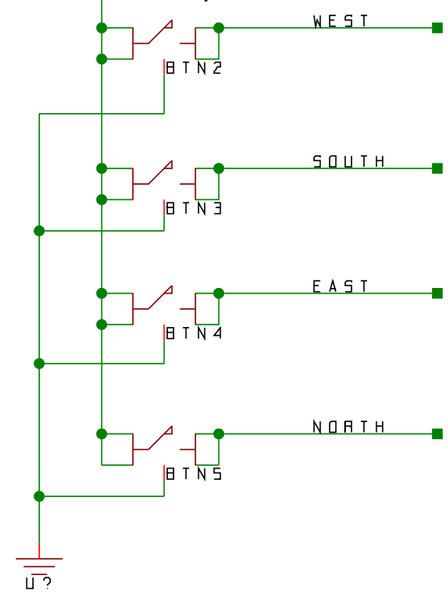
DIGILENT™

TITLE: **Spartan-3A/3AN Starter Kit Board**

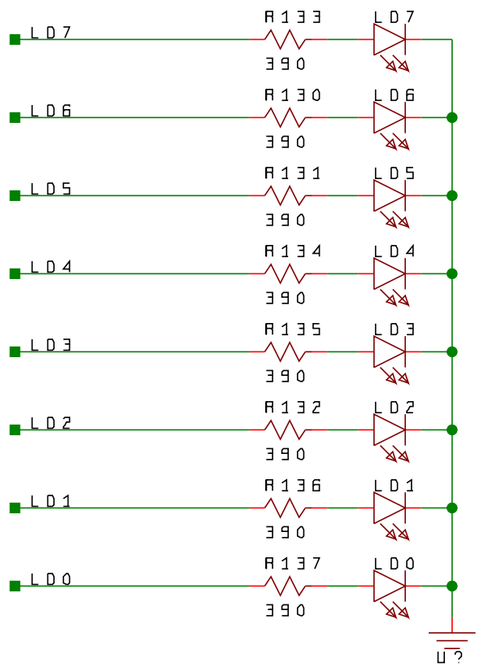
DESCRIPTION: STMicro SPI serial Flash, Atmel serial DataFlash			ENGINEER: CC
Copyright 2006			AUTHOR: GMA
SHEET 13 of 17	DOC# 500-112	REVISION C	DATE 12-13-2006_16:56



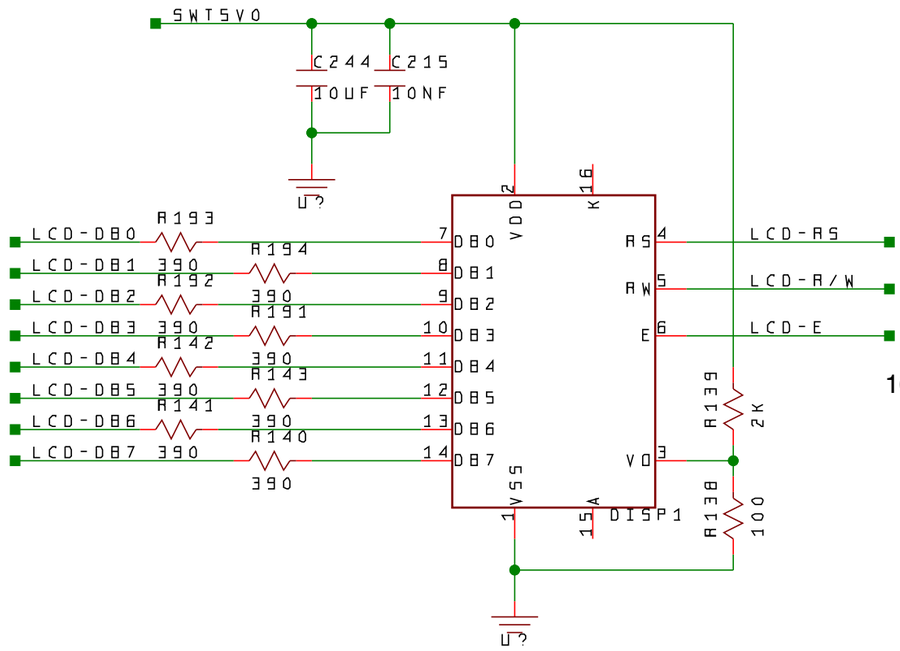
Four slide switches



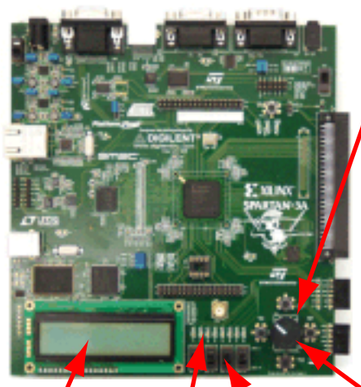
Four pushbutton switches



Eight discrete LEDs



16-character by 2-line LCD display



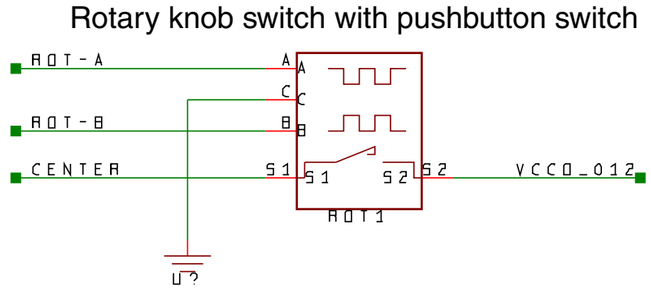
16x2 character LCD

Four pushbutton switches surround rotary knob

Eight discrete LEDs

Four slide switches

Rotary pushbutton switch



Rotary knob switch with pushbutton switch

XILINX®

DIGILENT™

TITLE
Spartan-3A/3AN Starter Kit Board

DESCRIPTION: Slide switches, Rotary knob, Character LCD, Pushbutton switches, discrete LEDs	ENGINEER: CC
Copyright 2006	AUTHOR: GMA
SHEET 14 of 17	DOC# 500-112
REVISION 0	DATE 12-13-2006_16:56

The DDR2 SDRAM interface has specific pin assignment and layout requirements to support the Xilinx Memory Interface Generator (MIG) software. See the “DDR SDRAM” chapter in UG334: Spartan-3A/3AN Starter Kit User Guide.

XILINX®

DIGILENT™

TITLE: Spartan-3A/3AN Starter Kit Board

DESCRIPTION: DDR2 SDRAM Termination Network (1 of 2)

ENGINEER: CC

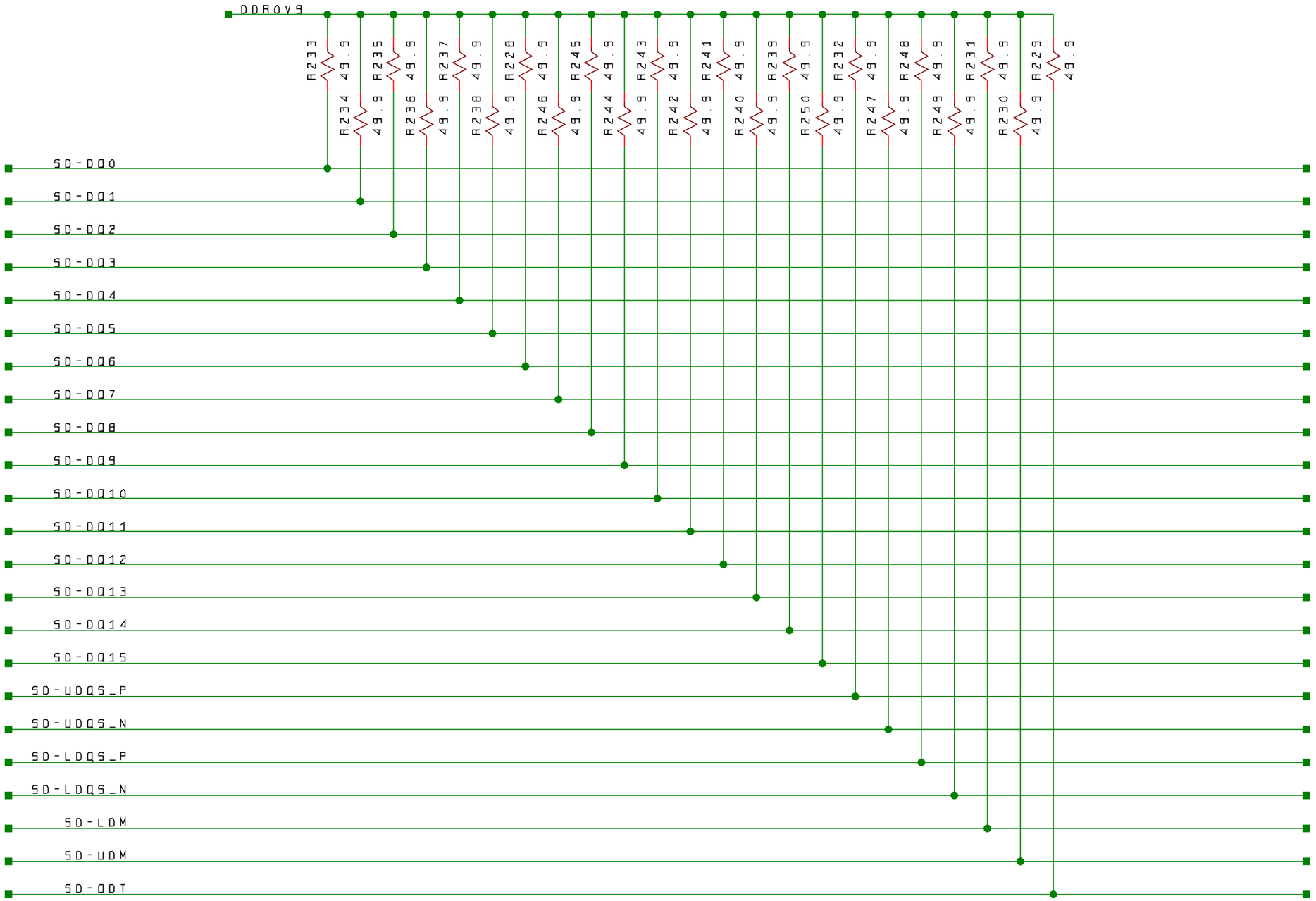
AUTHOR: GMA

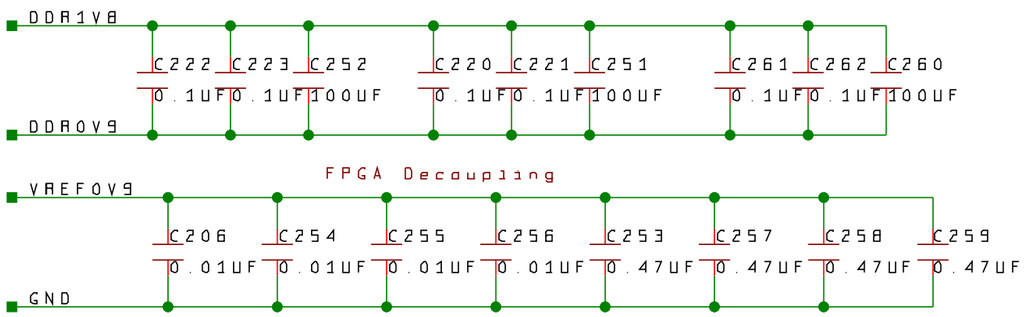
SHEET 15 of 17

DOC# 500-112

REVISION: B2

DATE: 12-13-2006_16:56





The DDR2 SDRAM interface has specific pin assignment and layout requirements to support the Xilinx Memory Interface Generator (MIG) software. See the “DDR SDRAM” chapter in UG334: Spartan-3A/3AN Starter Kit User Guide.

XILINX®

DIGILENT™

TITLE: **Spartan-3A/3AN Starter Kit Board**

DESCRIPTION: DDR2 SDRAM Termination Network (2 of 2)

ENGINEER: CC

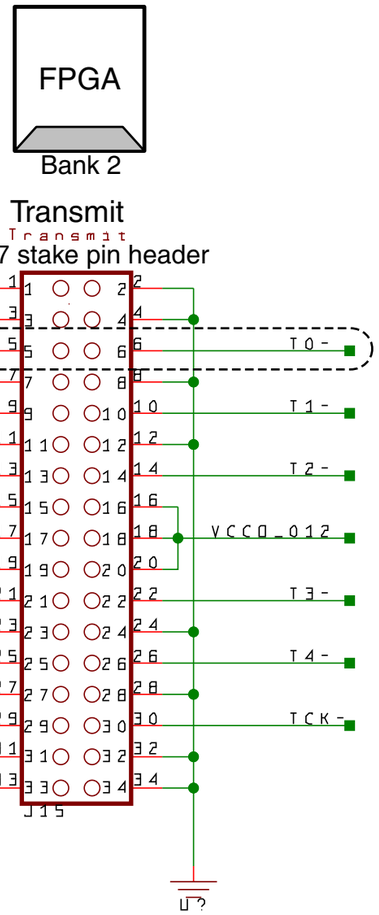
AUTHOR: GMA

SHEET 16 of 17

DOC# 500-112

REVISION B2

DATE 12-13-2006_16:56



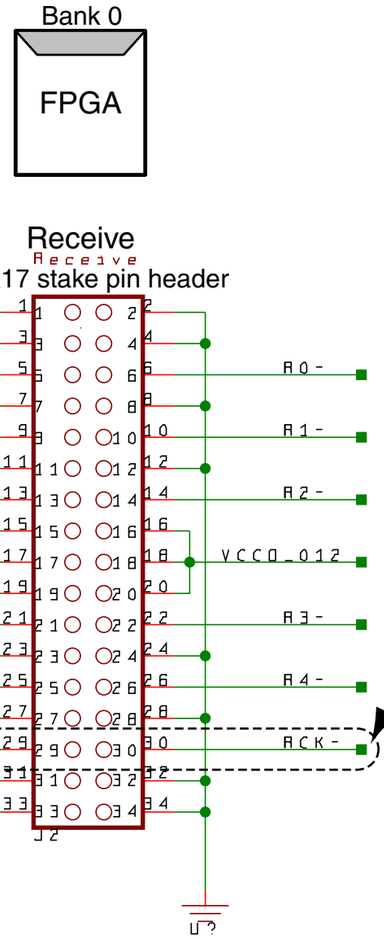
Transmit

2x17 stake pin header

Pairs of pins on the header form potential differential I/O pairs.

Optionally, each pin can be a single-ended I/O pin.

Each individual differential I/O pair is routed with matched 100-ohm impedance.



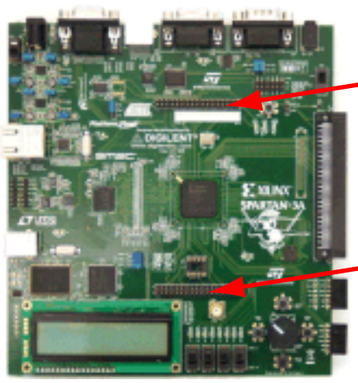
Receive

2x17 stake pin header

The receive clock differential pair feeds the GCLK6 and GCLK7 global clock inputs, which in turn connect to the top, right DCM labeled DCM_X2Y3

If using differential inputs, set the DIFF_TERM=TRUE constraint.
There are no external termination resistors provided on the board.

```
INST <I/O_BUFFER_INSTANTIATION_NAME> DIFF_TERM = "TRUE" ;
```



Recieve stake pins

Transmit stake pins

*NOTE: These signals are 100R Differential pairs and must be routed within 0.25"

XILINX®

DIGILENT™

TITLE: Spartan-3A/3AN Starter Kit Board

DESCRIPTION: Differential I/O Headers

ENGINEER: CC

AUTHOR: GMA

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DOC# 500-112

REVISION B2

DATE 12-13-2006_16:56