ML410 Embedded Development Platform

User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/06/06	1.0	Initial Xilinx release.
02/10/06	1.1	Corrected pinouts in Table 2-20, page 53.
05/26/06	1.2	Corrected pinouts in Table 2-5, page 33 and Table 2-21, page 54. Expanded "PCI Express" section.
09/25/06	1.2.1	Updated PHY address in Table 2-7, page 38 and Table 2-9, page 41. Miscellaneous typographical edits.
10/26/06	1.3	Updated "Clock Generation," page 26, "Serial ATA," page 73, and "High-Speed I/O," page 84 for RoHS-compliant revision E boards. Added Appendix A, "Board Revisions."
11/01/06	1.4	Corrected Table 2-19, page 51.
12/22/06	1.5	Added note to "RocketIO Transceivers," page 17. Added board revision details to Table A-1, page 97.
03/06/07	1.6	Updated Table 2-19, page 51 and Table A-1, page 97.
04/06/07	1.6.1	Fixed typo in Figure 2-19, page 71.
09/28/07	1.7	Corrected pinouts in Table 2-15, page 46 for SYSACE_FPGA_CLK, SYSACE_MPD[15], SYSACE_MPCE, and SYSACE_MPWE signals.
03/05/08	1.7.1	Fixed typo in Table 2-8, page 40. Updated trademark statements and copyright date.
12/11/08	1.7.2	Minor edits to Table A-1, page 97. Removed support for unbuffered DIMMs.

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About This Guide

This manual accompanies the ML410 series of Embedded Development Platforms and contains information about the ML410 hardware and software tools.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "Introduction to Virtex-4, ISE, and EDK," provides an overview of the hardware and software features
- Chapter 2, "ML410 Embedded Development Platform," provides an overview of the embedded development platform and details the components and features of the ML410 board
- Appendix A, "Board Revisions" details the differences between board revisions in the ML410 series
- Appendix B, "References"

Additional Resources

To find additional documentation, see the Xilinx® website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

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Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** `[`*`option_name`*`]` *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr =`**`{`**`on`**`|`**`off`**`}`
Vertical bar |	Separates items in a list of choices	**`lowpwr =`**`{`**`on`**`|`**`off`**`}`

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis **...**	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.

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Convention	Meaning or Use	Example
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Platform FPGA User Guide.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 1

Introduction to Virtex-4, ISE, and EDK

Virtex-4 FPGAs

Virtex®-4 domain-optimized FPGAs provide an ideal mix of features and the greatest choice of devices of any FPGA product line on the market today, with a column-based architecture unique to the programmable logic industry. Virtex-4 FPGAs contain three platforms: LX, FX, and SX. Choice and feature combinations are offered for all complex applications. A wide array of hard-IP core blocks complete the system solution. These cores include the PowerPC® processors (with a new APU interface), Tri-Mode Ethernet MACs, 622 Mb/s to 6.5 Gb/s serial transceivers, dedicated DSP slices, high-speed clock management circuitry, and source-synchronous interface blocks. The basic Virtex-4 building blocks allow migration of existing Virtex series designs. Virtex-4 devices are produced by a state-of-the-art 90 nm copper process, using 300 mm (12 inch) wafer technology. Combining a wide variety of flexible features, the Virtex-4 family enhances programmable logic design capabilities and is a powerful alternative to ASIC technology.

Summary of Virtex-4 FX Features

The Virtex-4 family has an impressive collection of both programmable logic and hard IP, historically the domain of ASICs. The Virtex-4 FX FPGAs used on ML410 platforms are high-performance, full-featured solutions for embedded platform applications.

- Xesium™ clock technology
  - Digital clock manager (DCM) blocks
  - Additional phase-matched clock dividers (PMCD)
  - Differential global clocks
- XtremeDSP™ slice
  - 18 x 18, two's complement, signed multiplier
  - Optional pipeline stages
  - Built-in accumulator (48-bits) and adder/subtracter
- Smart RAM memory hierarchy
  - Distributed RAM
  - Dual-port 18 Kb RAM blocks
    - Optional pipeline stages
    - Optional programmable FIFO logic - Automatically remaps RAM signals as FIFO signals
  - High-speed memory interface support: DDR and DDR2
- SDRAM, QDR II, RLDRAM II, and FCRAM II SelectIO technology
  - 1.5V to 3.3V I/O operation

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- Built-in ChipSync™ source-synchronous technology
- Digitally-controlled impedance (DCI) active termination
- Fine grained I/O banking (configuration in one bank)

- Flexible logic resources
- Secure Chip AES bitstream encryption
- 90 nm copper CMOS process
- 1.2V core voltage
- Flip-Chip packaging
- RocketIO™ 622 Mb/s to 6.5 Gb/s multi-gigabit transceivers (MGT)
- IBM PowerPC RISC processor core
  - PowerPC 405 (PPC405) core
  - Auxiliary processor unit interface (user coprocessor)
- Multiple Tri-Mode Ethernet MACs

Table 1-1: **Virtex-4 FX Family Members**

Device	XC4VFX12	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140
Logic Cells	12,312	19,224	41,904	56,880	94,896	142,128
PPC405	1	1	2	2	2	2
MGTs	N/A	8	12	16	20	24
Block RAM (Kb)	648	1,224	2,592	4,176	6,768	9,936
XtremeDSP Multipliers	32	32	48	128	160	192

PowerPC™ 405 Core

- 32-bit Harvard architecture core
- Five-stage execution pipeline
- Integrated 16 KB level 1 instruction cache and 16 KB level 1 data cache
  - Integrated level 1 cache parity generation and checking
- CoreConnect™ bus architecture
- Efficient, high-performance on-chip memory (OCM) interface to block RAM
- PLB synchronization logic (enables non-integer CPU-to-PLB clock ratios)
- Auxiliary Processor Unit (APU) interface and integrated APU controller
  - Optimized FPGA-based coprocessor connection
  - Automatic decode of PowerPC floating-point instructions
  - Allows custom instructions (decode for up to eight instructions)
  - Extremely efficient microcontroller-style interfacing

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RocketIO Transceivers

- Full-duplex serial transceiver (SERDES) capable of running 622 Mb/s - 6.5 Gb/s

  Note: Only Revision E boards support 6.5 Gb/s. See Appendix A, "Board Revisions" for more details.
- Full clock and data recovery
- 32-bit or 40-bit datapath support
- Optional 8B/10B, 64B/66B, or FPGA-based encode/decode
- Integrated FIFO/elastic buffer
- Support for channel bonding
- Embedded 32-bit CRC generation/checking
- Integrated comma-detect or programmable A1/A2, A1A1/A2A2 detection
- Programmable pre-emphasis (AKA transmitter equalization)
- Programmable receiver equalization
- Embedded support for:
  - Out of band (OOB) signaling: Serial ATA
  - Beaconing and electrical idle: PCI Express®
- On-chip bypassable AC coupling for receiver

ISE Foundation

ISE Foundation is the industry's most complete programmable logic design environment. With ISE Foundation, you have everything you need to target today's most advanced CPLDs and FPGAs, including the new Virtex-4 family of FPGAs. ISE Foundation includes the industry's most advanced timing driven implementation tools available for programmable logic design, along with design entry, synthesis and verification capabilities. With its ultra-fast runtimes, an average 40% faster than the nearest competitive FPGA offering, ProActive Timing Closure technologies, and seamless integration with the industry's most advanced verification products, ISE Foundation offers a great design environment in which to create a complete programmable logic design solution.

Foundation Features

Design Entry

ISE greatly improves time-to-market, productivity, and design quality with robust design entry features. ISE provides support for today's most popular methods for design capture including HDL and schematic entry, integration of IP cores, and robust support for reuse of your own IP.

ISE's architecture wizards allow easy access to device features like the DCM and multi-gigabit I/O technology.

ISE also includes a tool called PACE (Pinout Area Constraint Editor) that includes a front-end pin assignment editor, a design hierarchy browser, and an area constraint editor. By using PACE, designers are able to observe and describe information regarding the connectivity and resource requirements of a design, resource layout of a target FPGA, and the mapping of the design onto the FPGA via location/area.

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This rich mixture of design entry capabilities provides the easiest to use design environment available today for your logic design.

Synthesis

Synthesis is one of the most essential steps in your design methodology. It takes your conceptual Hardware Description Language (HDL) design definition and generates the logical or physical representation for the targeted silicon device.

A state-of-the-art synthesis engine is required to produce highly optimized results with a fast compile and turnaround time. To meet this requirement, the synthesis engine needs to be tightly integrated with the physical implementation tool and have the ability to proactively meet the design timing requirements by driving the placement in the physical device. In addition, cross probing between the physical design report and the HDL design code further improves the turnaround time.

Xilinx ISE provides the seamless integration with the leading synthesis engines from Mentor Graphics, Synopsys, and Synplicity. You can use the synthesis engine of our choice. In addition, ISE includes Xilinx proprietary synthesis technology, XST. You have options to use multiple synthesis engines to obtain the best-optimized result of your programmable logic design.

Implementation and Configuration

Programmable logic design implementation assigns the logic created during design entry and synthesis into specific physical resources of the target device.

The term “place and route” has historically been used to describe the implementation process for FPGA devices and “fitting” has been used for CPLDs. Implementation is followed by device configuration, where a bitstream is generated from the physical place and route information and downloaded into the target programmable logic device.

To ensure designers get their product to market quickly, Xilinx ISE software provides several key technologies required for design implementation:

- Ultra-fast runtimes enable multiple “turns” per day
- ProActive™ Timing Closure drives high-performance results
- Timing-driven place and route combined with pushbutton ease
- Incremental Design

Board-Level Integration

Xilinx understands the critical issues such as complex board layout, signal integrity, high-speed bus interface, high-performance I/O bandwidth, and electromagnetic interference for system-level designers.

To ease the system level designers' challenge, ISE provides support to all Xilinx leading FPGA technologies:

- System IO
- XCITE
- Digital clock management for system timing
- EMI control management for electromagnetic interference

To ensure that your programmable logic design works in the context of your entire system, Xilinx provides complete pin configurations, packaging information, tips on signal integration, and various simulation models for your board-level verification including:

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- IBIS models
- HSPICE models
- STAMP models

Embedded Development Kit

The Embedded Development Kit (EDK) is a series of software tools for designing embedded processor systems on programmable logic and supports the IBM PowerPC hard processor core and the MicroBlaze™ soft processor core. This pre-configured kit includes the Platform Studio Tool Suite.

EDK Components

The Embedded Development Kit is distributed as a single media installable CD image.

The components of the Xilinx EDK are:

- Hardware IP for the Xilinx embedded processors and its peripherals
- Drivers, libraries, and a microkernel for embedded software development
- Platform Studio tools
- Software Development Kit (Eclipse-based IDE)
- GNU compiler and debugger for C development for MicroBlaze and PowerPC
- Documentation
- Sample projects

Platform Studio Features

The Xilinx Platform Studio (XPS) is a graphical user interface technology that integrates all of the processes from design entry to design debug and verification. XPS streamlines development with the embedded features of the Xilinx Virtex-4 FX family of devices, featuring the industry's only immersed dual PowerPC processors and innovative Auxiliary Processor Unit (APU) controller for accelerating processing functions.

XPS automates the configuration of user-defined hardware co-processing modules used to replace application-specific software algorithms. These hardware accelerator functions operate as extensions to the PowerPC 405 processor, thereby offloading the CPU from demanding computational tasks. Utilizing the direct processor-FPGA coupling presented by the APU controller and its high throughput interfaces, flexible design partitioning with synchronization of hardware and software is greatly simplified and overall system performance is improved. The suite also includes system profiling and analysis tools to help optimize performance and target design functions for acceleration in FPGA hardware.

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Chapter 2

ML410 Embedded Development Platform

Overview

The ML410 series of Embedded Development Platforms offer designers a versatile Virtex-4 FX platform for rapid prototyping and system verification. In addition to the more than 30,000 logic cells, over 2,400 kb of block RAM, dual IBM PowerPC 405 (PPC405) processors, and RocketIO transceivers available in the FPGA, the ML410 provides an onboard Ethernet MAC PHY, DDR memory, multiple PCI bus slots, and standard front panel interface ports within an ATX form factor motherboard. An integrated System ACE™ CompactFlash (CF) controller is deployed to perform board bring-up and to load applications from the CompactFlash card.

The ML410 website contains up-to-date documentation and files, including tutorials, device data sheets, reference designs, and utilities. The EDK *Processor IP User Guide* [Ref 2] should be reviewed as well as the data sheets corresponding to the devices listed in "Detailed Description."

The setup and quickstart documentation highlights the functionality of the ML410, using the applications contained on the CompactFlash card. The reference designs were produced using the Xilinx Embedded Development Kit (EDK), ISE, and Answer Browser solution records. Tutorials, in coordination with Xilinx documentation for EDK, ISE, and the Answer Browser, describe how the reference designs and applications were produced. These tutorials can be used to re-create the provided applications and also as a basis for the development of new designs. Xilinx EDK provides for the development of basic board-specific systems, beginning with Base System Builder (BSB), to highly customized systems that leverage the flexibility of Xilinx Platform Studio (XPS) and the EDK intellectual property (IP).

Features

The list below is a superset of features in the ML410 series. Appendix A, "Board Revisions" describes the differences between the ML410-P and ML410 model boards.

- ATX form factor motherboard and ATX-compliant power supply
- 32-bit component DDR memory and 64-bit DDR2 DIMM*
- 512 MB CompactFlash (CF) card and System ACE CF controller for configuration*
- Two onboard 10/100/1000 Ethernet PHYs with RJ-45 connectors
- PCI Express interface and MIC2592B PCI Express power controller
- Two UARTs with RS-232 connectors
- VGA graphics interface

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- LEDs, LCD*, and switches
- 32/33 PCI subsystem
  - Two 3.3V slots and two 5V slots
  - ALi South Bridge SuperIO controller
    - PS/2 mouse and keyboard connectors
    - 3.5mm headphone and microphone connectors
    - Two USB peripheral ports and one parallel port
    - General purpose I/O (GPIO)
    - Flash memory interface
- Two serial ATA connectors
- Xilinx Personality Module (XPM) interface for access to:
  - RocketIO transceivers
  - SPI4.2
  - GPIO
  - Power
- JTAG and trace debug ports
- Encryption battery
- Fan controller
- Onboard power regulators for all necessary voltages
- IIC/SMBus interface*
  - LTC1694 SMBus accelerator
  - RTC8566 Real Time Clock (RTC)
  - 64 kb 24LC64 EEPROM
  - LM87 voltage/temp monitor
  - DDR2 DIMM SPD EEPROM
- SPI EEPROM*
- High-speed I/O through RocketIO transceivers

Note: * Compatible with EDK supported IP and software drivers

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Block Diagram

Figure 2-1 shows a high-level block diagram of the ML410 and its peripherals.

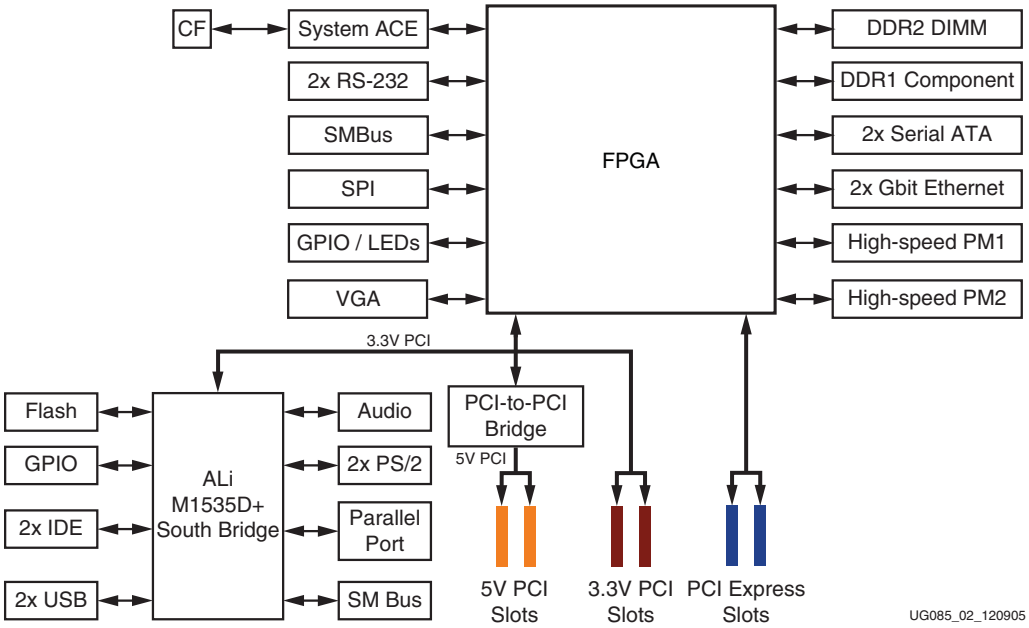

Figure 2-1: **ML410 High-Level Block Diagram**

Related Xilinx Documents

Prior to using the ML410 Embedded Development Platform, users should be familiar with Xilinx resources. See Appendix B, "References" for direct links to Xilinx documentation. See the following locations for additional documentation on Xilinx tools and solutions:

- EDK: www.xilinx.com/edk
- ISE: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Virtex-4 FPGAs: www.xilinx.com/virtex-4

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Detailed Description

The ML410, shown in Figure 2-2, is an example of the ML410 series described in this user guide.

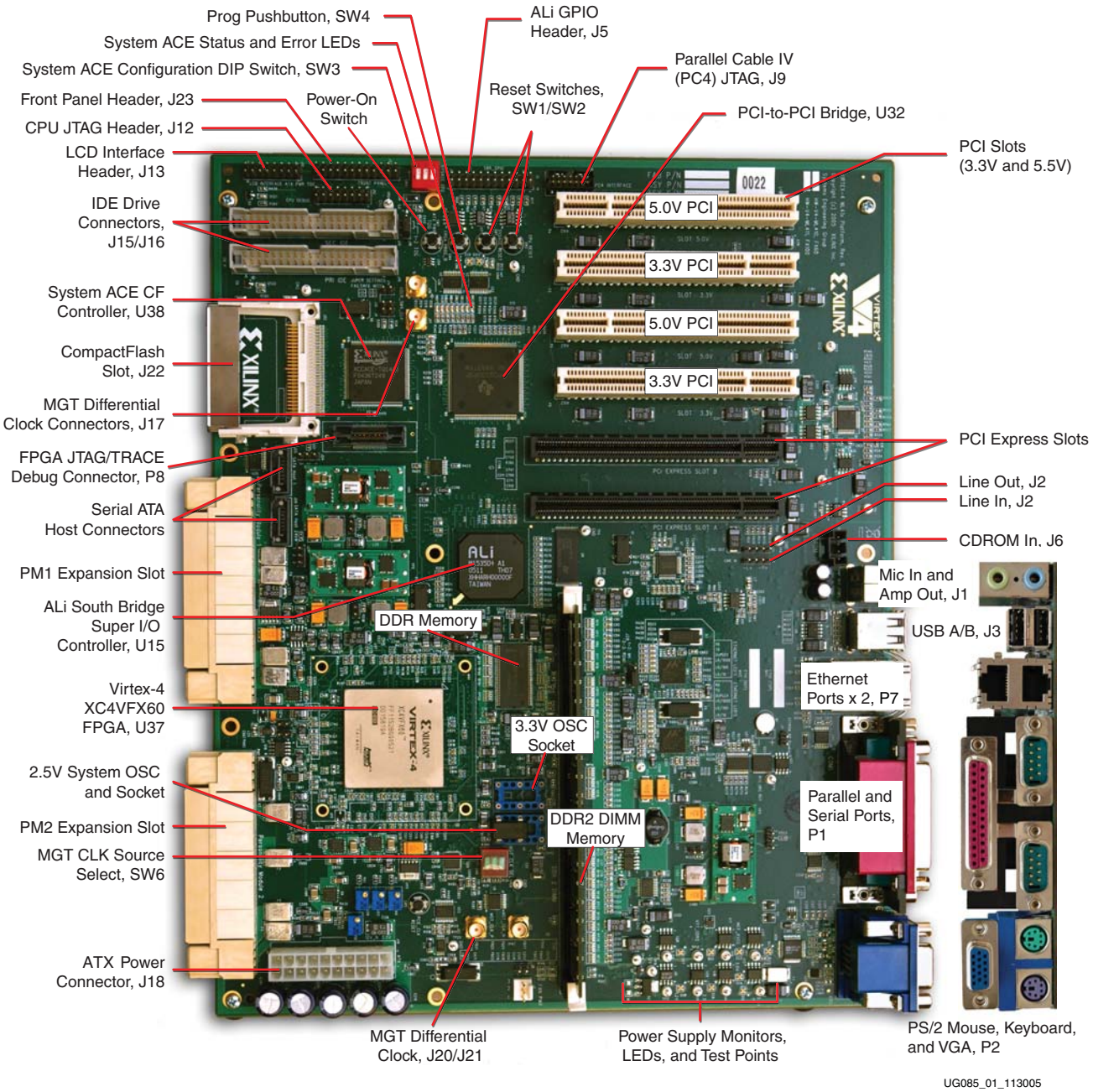

Figure 2-2: **ML410 Board and Front Panel Detail**

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Configuration

ML410 platforms support configuration in JTAG mode only. Configuration can be accomplished by using a Xilinx download cable (such as Parallel Cable IV or Platform Cable USB) or by using the onboard System ACE CompactFlash solution. See "System ACE CF Controller," page 44.

I/O Voltage Rails

The FPGA requires different banking voltages that are set based on the I/O voltage interface requirements of each device directly connected to the FPGA. The Virtex-4 FPGA I/O can be configured to use different I/O standards such as SSTL18 as required on the DDR2 DIMM interface. See the *Virtex-4 Data Sheet* [Ref 3] for more information regarding I/O standards.

The voltage applied to the FPGA I/O banks used by the ML410 platforms is summarized in Table 2-1.

Table 2-1: **I/O Voltage Rail of FPGA Banks**

FPGA Bank	I/O Voltage Rail	Description
1	2.5V	PCI Express controls and DDR1
2	2.5V	LCD and SPI
3	2.5V	Clocks and miscellaneous signals
4	2.5V	Clocks and miscellaneous signals
5	2.5V	DDR
6	3.0V	VGA, PHY, and both UARTs
7	2.5V	PMIO, CPU debug, and ATD
8	2.5V	PMIO and trace port
9	1.8V	DDR2
10	3.0V	PCI
11	1.8V	DDR2
12	3.0V	System ACE, PMIO_3V, and LEDs **Note:** User selectable as 3.0V (default) or 2.5V. See schematic sheet 46 (R486–R488 and R489–R491).

Digitally Controlled Impedance (DCI)

Some FPGA banks can support the DCI feature in Virtex-4 FPGAs. Support for DCI is summarized in Table 2-2.

Table 2-2: **DCI Capability of FPGA Bank**

FPGA Bank	DCI Capability	FPGA Bank	DCI Capability
1	Not supported.	7	Yes, 49.9Ω resistors are installed.
2	Not supported.	8	Yes, 49.9Ω resistors are installed.
3	Not supported.	9	Yes, 49.9Ω resistors are installed.

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Table 2-2: **DCI Capability of FPGA Bank *(Cont'd)***

FPGA Bank	DCI Capability	FPGA Bank	DCI Capability
4	Not supported	10	Not supported.
5	Yes, 49.9Ω resistors are installed.	11	Yes, 49.9Ω resistors are installed.
6	Yes, 49.9Ω resistors are installed.	12	Yes, 49.9Ω resistors are installed.

Clock Generation

ML410 boards are equipped with two crystal oscillator sockets (X6 and X10) each wired for standard LVTTL-type oscillators. Both sockets accept half- and full-size oscillators. See the reference design documentation on the ML410 website for examples of how to set up the clocks on ML410 boards.

X6 is populated with a 100 MHz oscillator that provides the system clock. This system clock is typically used to generate multiple other clocks with varying frequencies and phases within the FPGA fabric by using the Virtex-4 DCMs. The FPGA also generates and drives clocks required by the DDR memory, DDR2 DIMM memory, and PCI bus interfaces. If required, a second user clock can be brought into the FPGA by installing a second oscillator in the X10 socket.

High-precision clock signals can be supplied to the FPGA using differential clock signals brought in through 50Ω SMA connectors. A single-ended clock can be connected to USER_SMA_CLK_P. Two additional single-ended clocks can be supplied through the XPM connectors. Furthermore, ML410 boards are equipped with several high-precision clocks for driving the high-speed RocketIO transceivers (not available on ML410-P model boards). These clocks can also be used to drive the global clock nets of the FPGA. See the *Virtex-4 Data Sheet* [Ref 3] for details.

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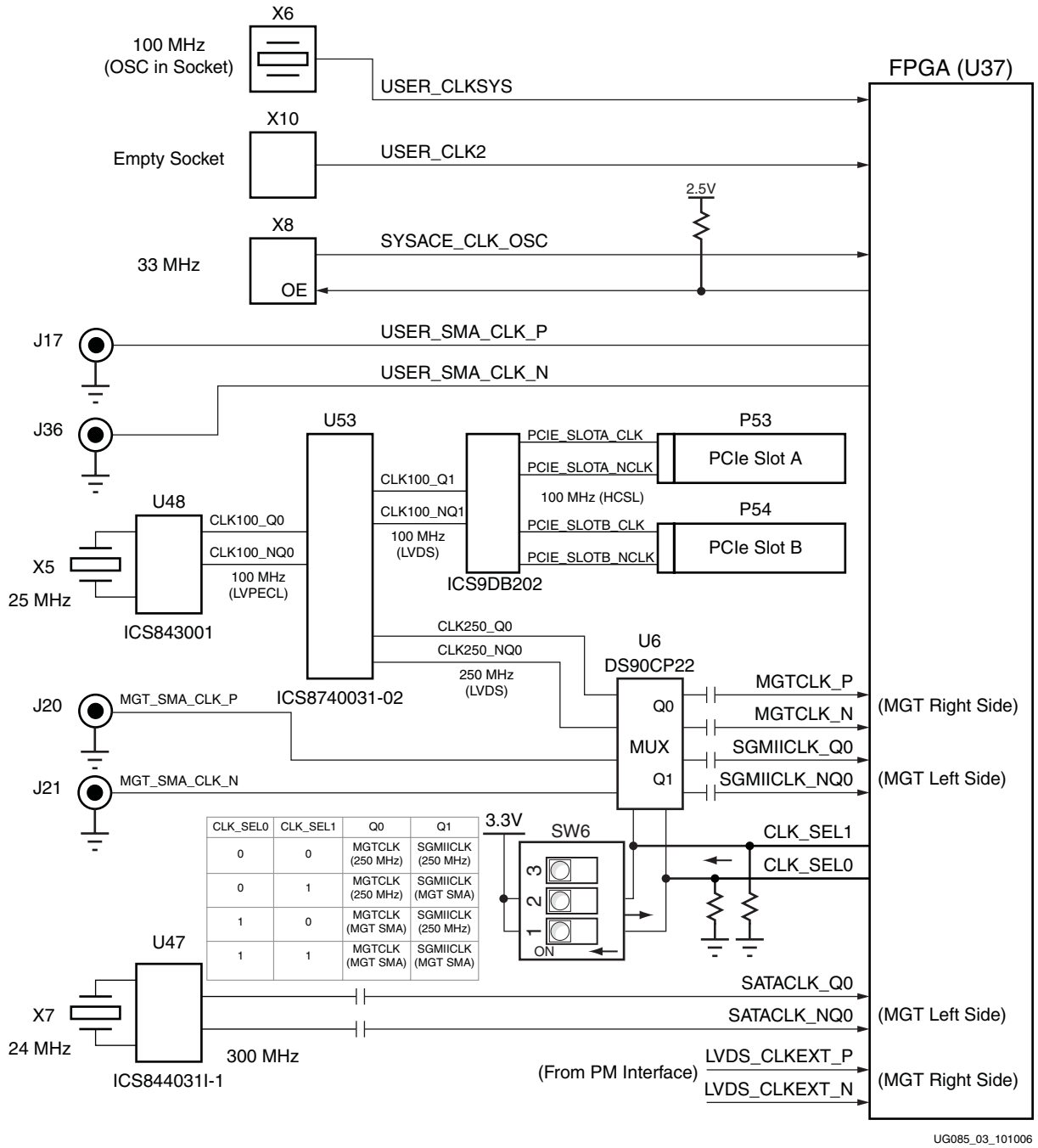
Figure 2-3 is an example of the clock distribution for the ML410 board. For clocking on earlier revisions of the ML410 platform, see Appendix A, "Board Revisions."



CLK_SEL0	CLK_SEL1	Q0	Q1
0	0	MGTCLK (250 MHz)	SGMIICLK (250 MHz)
0	1	MGTCLK (250 MHz)	SGMIICLK (MGT SMA)
1	0	MGTCLK (MGT SMA)	SGMIICLK (250 MHz)
1	1	MGTCLK (MGT SMA)	SGMIICLK (MGT SMA)

Figure 2-3: **ML410 Clock Distribution**

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Table 2-3 shows the ML410 clock connections.

Table 2-3: **Clock Connections**

Schematic Net Name	Clock Source	FPGA Pin (U37)	Description
USER_CLKSYS	X6	J16	100 MHz socketed user clock oscillator (2.5V).
USER_CLK2	X10	L15	Socket for user-supplied clock oscillator (3.3V)(1).
USER_SMA_CLK_N	J36	AG18	100Ω differential SMA connections that can be used as a differential pair clock.
USER_SMA_CLK_P	J17	AF18	100Ω differential SMA connections that can be used as a differential pair clock. J17 can be used single ended at 50Ω.
PM_CLK_TOP	PM1.F9	K16	Personality module clock (top) (2.5V)(1).
PM_CLK_BOT	PM2.F10	AD21	Personality module clock (bottom) (2.5V)(1).
LVDS_CLKEXT_P	PM1.F12	J1	LVDS pair (2.5V)(1) (2). Frequency is user-defined.
LVDS_CLKEXT_N	PM1.F11	K1	LVDS pair (2.5V)(1)(2). Frequency is user-defined.
SGMIICLK_Q0	(Selectable)	M34	SMA or onboard 250 MHz clock source selectable through SW6(2).
SGMIICLK_NQ0	(Selectable)	N34	SMA or onboard 250 MHz clock source selectable through SW6(2).
MGTCLK_P_110	(Selectable)	AP3	SMA or onboard 250 MHz clock source selectable through SW6(2).
MGTCLK_N_110	(Selectable)	AP4	SMA or onboard 250 MHz clock source selectable through SW6(2).
SATACLK_Q0	(Selectable)	AP29	300 MHz Serial ATA clock(2).
SATACLK_NQ0	(Selectable)	AP28	300 MHz Serial ATA clock(2).

Notes:

1. See "High-Speed I/O," page 84.
2. These clocks are differential pairs through the RocketIO transceivers and are not available on ML410-P boards. See Figure 2-3, page 27.

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DDR and DDR2 Memory

ML410 platforms have two types of double data rate (DDR) memory, two component DDRs and a DDR2 SDRAM DIMM. The two memory systems are independent and enable users to build independent systems.

DDR Component Memory

The board contains 64 MB of DDR SDRAM (U42 and U43). Each chip is 16 bits wide and together form a 32-bit data bus. All DDR SDRAM signals are terminated through 47Ω resistors to a 1.25V VTT reference voltage. The board is designed for matched length traces across all DDR control and data signals except clocks.

DDR Component Clock Signal

The DDR component clock signals are broadcast from the FPGA as a single differential pair that drives both DDR chips. The delay on the clock trace is designed to match the delay of the other DDR control and data signals. The DDR component clock is also fed back to the FPGA to allow for clock deskew using Virtex-4 DCMs. The board is designed so that the DDR clock signal reaches the FPGA clock feedback pin at the same time it arrives at the DDR components. Figure 2-4 is a block diagram of the DDR component interface.

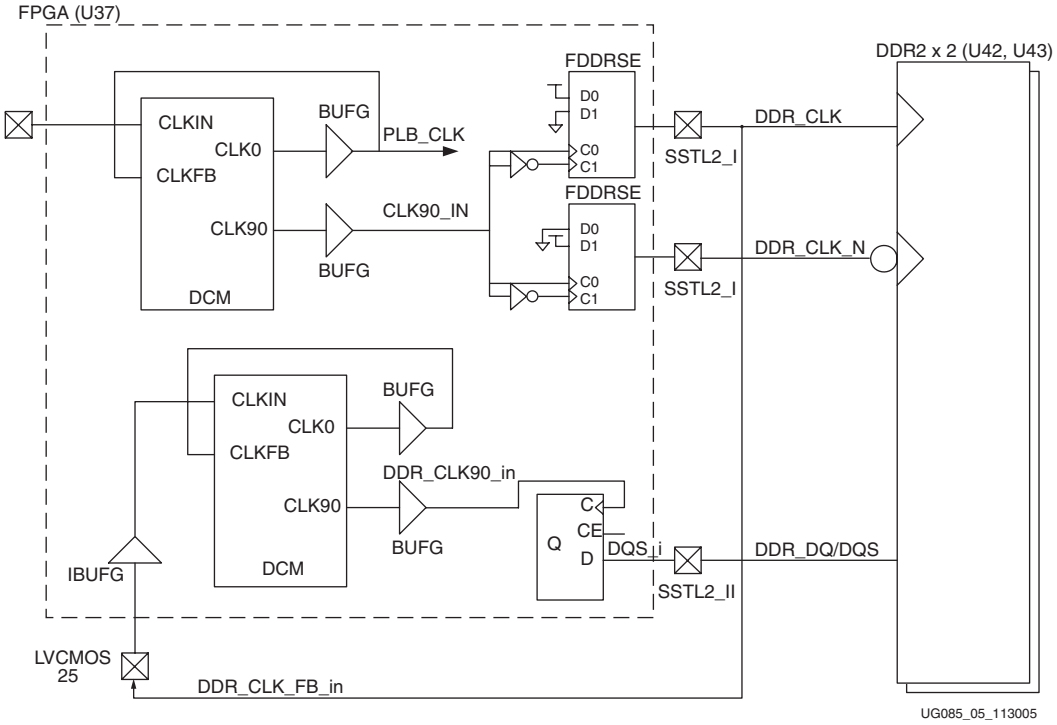

Figure 2-4: **DDR Component Block Diagram**

DDR Component Signaling

The FPGA DDR interface uses SSTL2 signaling. All signals are controlled impedance and are SSTL2 terminated.

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Table 2-4 lists the connections from the FPGA to the DDR interface. Note that the DDR1_DQ signal names do not correlate as the FPGA uses IBM notation, big endian, while the DDR components use Intel notation, little endian.

Table 2-4: **Connections from FPGA to DDR1 SDRAMs (U42 and U43)**

UCF Signal Name	XC4FX60 Pin (U37)	Schematic Signal Name	DDR1 SDRAM (U42)	DDR1 SDRAM (U43)
DDR1_WE_N	E27	DDR1_WE_N	21	21
DDR1_RAS_N	D27	DDR1_RAS_N	23	23
DDR1_CAS_N	D26	DDR1_CAS_N	22	22
DDR1_DQS[0]	F20	DDR1_DQS[0]	16	-
DDR1_DQS[1]	G20	DDR1_DQS[1]	51	-
DDR1_DQS[2]	G25	DDR1_DQS[2]	-	16
DDR1_DQS[3]	F25	DDR1_DQS[3]	-	51
DDR1_DM[0]	F21	DDR1_DM[0]	20	-
DDR1_DM[1]	G22	DDR1_DM[1]	47	-
DDR1_DM[2]	E23	DDR1_DM[2]	-	20
DDR1_DM[3]	G23	DDR1_DM[3]	-	47
DDR1_DQ[0]	E17	DDR1_D[0]	2	-
DDR1_DQ[1]	E18	DDR1_D[1]	4	-
DDR1_DQ[2]	F18	DDR1_D[2]	5	-
DDR1_DQ[3]	G18	DDR1_D[3]	7	-
DDR1_DQ[4]	F19	DDR1_D[4]	8	-
DDR1_DQ[5]	E19	DDR1_D[5]	10	-
DDR1_DQ[6]	D21	DDR1_D[6]	11	-
DDR1_DQ[7]	E21	DDR1_D[7]	13	-
DDR1_DQ[8]	G21	DDR1_D[8]	54	-
DDR1_DQ[9]	H20	DDR1_D[9]	56	-
DDR1_DQ[10]	J20	DDR1_D[10]	57	-
DDR1_DQ[11]	J21	DDR1_D[11]	59	-
DDR1_DQ[12]	K21	DDR1_D[12]	60	-
DDR1_DQ[13]	L21	DDR1_D[13]	62	-
DDR1_DQ[14]	J22	DDR1_D[14]	63	-
DDR1_DQ[15]	H22	DDR1_D[15]	65	-
DDR1_DQ[16]	C22	DDR1_D[16]	-	2
DDR1_DQ[17]	C23	DDR1_D[17]	-	4

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Table 2-4: **Connections from FPGA to DDR1 SDRAMs (U42 and U43) *(Cont'd)***

UCF Signal Name	XC4FX60 Pin (U37)	Schematic Signal Name	DDR1 SDRAM (U42)	DDR1 SDRAM (U43)
DDR1_DQ[18]	C24	DDR1_D[18]	-	5
DDR1_DQ[19]	C25	DDR1_D[19]	-	7
DDR1_DQ[20]	D22	DDR1_D[20]	-	8
DDR1_DQ[21]	D24	DDR1_D[21]	-	10
DDR1_DQ[22]	D25	DDR1_D[22]	-	11
DDR1_DQ[23]	C28	DDR1_D[23]	-	13
DDR1_DQ[24]	F23	DDR1_D[24]	-	54
DDR1_DQ[25]	F24	DDR1_D[25]	-	56
DDR1_DQ[26]	F26	DDR1_D[26]	-	57
DDR1_DQ[27]	G26	DDR1_D[27]	-	59
DDR1_DQ[28]	H25	DDR1_D[28]	-	60
DDR1_DQ[29]	H24	DDR1_D[29]	-	62
DDR1_DQ[30]	E24	DDR1_D[30]	-	63
DDR1_DQ[31]	E22	DDR1_D[31]	-	65
DDR1_CS_N	C27	DDR1_CS_N	24	24
DDR1_CKE	H14	DDR1_CKE	44	44
DDR1_LOOP	E26	-	-	-
DDR1_LOOP	G17	-	-	-
DDR1_CK1_P	F28	DDR1_CK1_P	45	45
DDR1_CK1_N	E28	DDR1_CK1_N	46	46
DDR1_CLK_FB	K18	DDR1_CLK_FB	-	-
DDR1_BA[0]	J25	DDR1_BA[0]	26	26
DDR1_BA[1]	J26	DDR1_BA[1]	27	27
DDR1_A[0]	P24	DDR1_A[0]	29	29
DDR1_A[1]	P22	DDR1_A[1]	30	30
DDR1_A[2]	N22	DDR1_A[2]	31	31
DDR1_A[3]	N23	DDR1_A[3]	32	32
DDR1_A[4]	N24	DDR1_A[4]	35	35
DDR1_A[5]	M23	DDR1_A[5]	36	36
DDR1_A[6]	L24	DDR1_A[6]	37	37
DDR1_A[7]	L25	DDR1_A[7]	38	38
DDR1_A[8]	L26	DDR1_A[8]	39	39

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Table 2-4: **Connections from FPGA to DDR1 SDRAMs (U42 and U43) *(Cont'd)***

UCF Signal Name	XC4FX60 Pin (U37)	Schematic Signal Name	DDR1 SDRAM (U42)	DDR1 SDRAM (U43)
DDR1_A[9]	K23	DDR1_A[9]	40	40
DDR1_A[10]	K24	DDR1_A[10]	28	28
DDR1_A[11]	K26	DDR1_A[11]	41	41
DDR1_A[12]	J24	DDR1_A[12]	42	42
DDR1_A[13]	E16	DDR1_A[13]	17	17

DDR2 SDRAM DIMM

The DDR2 DIMM is a standard 240-pin DIMM socket, supporting standard computer DDR2 memory.

ML410 platforms are shipped with a single-rank registered 256 MB PC2-3200 DDR2-400 Dual Inline Memory Module (DIMM). The DDR2 DIMM is commercially available from Wintec Industries as part number WID32M72R8 (-5 speed grade). The DDR2 DIMM uses nine 32M x 8 DDR2 SDRAM devices with 14-row address lines, 10-column address lines, and two bank address lines. Read and write access is programmable in burst lengths of 4 or 8. The memory module inputs and outputs are compatible with SSTL18 signaling. Serial Presence Detect (SPD) using an SMBus interface to the DDR DIMM is also supported. See the "IIC/SMBus Interface" section for more details on accessing the DIMM module's SPD EEPROM.

The DDR2 DIMM memory interface includes a 64-bit wide datapath to the DDR2 DIMM, thus ECC is not supported.

DDR2 Memory Expansion

The DDR2 interface is very flexible and can accommodate different DDR2 memory requirements, such as increased memory size. The DDR2 interface core delivered with EDK supports registered DRR2 memory interfaces. Please review the EDK *Processor IP User Guide* [Ref 2] when migrating to a different DDR2 DIMM.

DDR2 Clock Signal

The DDR2 clock signal is broadcast from the FPGA as a single differential pair that drives a clock fan-out chip, which then drives the DDR2 DIMM. The clock fan-out chip provides support for registered DIMMs. The delay on the clock trace is designed to match the delay of the other DDR2 control and data signals. The DDR2 clock is also fed back to the FPGA to allow for clock deskew using Virtex-4 DCMs. The board is designed so that the DDR2 clock signal reaches the FPGA clock feedback pin at the same time as it arrives at the DDR2 DIMM.

DDR2 Signaling

All DDR2 SDRAM signals are terminated through 47Ω resistors to a 0.9V VTT reference voltage. The board is designed for matched length traces across all DDR2 control and data signals, except clocks. The FPGA DDR2 interface supports SSTL18 signaling. All DDR2 signals are controlled impedance and are SSTL18 terminated.

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Table 2-5 describes all the signals associated with DDR2 DIMM component memories. Note that the DDR2_DQ signal names do not correlate because the FPGA uses IBM notation, big endian, while the DDR2 DIMM uses Intel notation, little endian.

Table 2-5: **Connections from FPGA to DDR2 DIMM Interface (P48)**

UCF Signal Name	XC4FX60 Pin (U37)	Schematic Signal Name	DDR2 DIMM (P48)
DDR2_WE_N	T31	DDR2_WE_N	73
DDR2_CAS_N	R31	DDR2_CAS_N	74
DDR2_RAS_N	R32	DDR2_RAS_N	192
DDR2_RST_N	AA26	DDR2_RST_N	18
DDR2_ODT	AA25	DDR2_ODT	195
DDR2_LOOP (Bank 9)	M26	-	-
DDR2_LOOP (Bank 11)	AB26	-	-
DDR2_DQSn[0]	E29	DDR2_DQS[00]	6
DDR2_DQS[0]	F29	DDR2_DQS[00]	7
DDR2_DQSn[1]	J29	DDR2_DQSn[01]	15
DDR2_DQS[1]	K29	DDR2_DQS[01]	16
DDR2_DQSn[2]	P26	DDR2_DQSn[02]	27
DDR2_DQS[2]	P27	DDR2_DQS[02]	28
DDR2_DQSn[3]	N32	DDR2_DQSn[03]	36
DDR2_DQS[3]	P32	DDR2_DQS[03]	37
DDR2_DQSn[4]	V27	DDR2_DQSn[04]	83
DDR2_DQS[4]	W27	DDR2_DQS[04]	84
DDR2_DQSn[5]	W30	DDR2_DQSn[05]	92
DDR2_DQS[5]	W31	DDR2_DQS[05]	93
DDR2_DQSn[6]	AH32	DDR2_DQSn[06]	104
DDR2_DQS[6]	AG32	DDR2_DQS[06]	105
DDR2_DQSn[7]	AE31	DDR2_DQSn[07]	113
DDR2_DQS[7]	AE32	DDR2_DQS[07]	114
DDR2_A[0]	H28	DDR2_A[00]	188
DDR2_A[1]	K28	DDR2_A[01]	183
DDR2_A[2]	L28	DDR2_A[02]	63
DDR2_A[3]	M25	DDR2_A[03]	182
DDR2_A[4]	Y24	DDR2_A[04]	61
DDR2_A[5]	N27	DDR2_A[05]	60
DDR2_A[6]	AD26	DDR2_A[06]	180

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Table 2-5: **Connections from FPGA to DDR2 DIMM Interface (P48) *(Cont'd)***

UCF Signal Name	XC4FX60 Pin (U37)	Schematic Signal Name	DDR2 DIMM (P48)
DDR2_A[7]	AC25	DDR2_A[07]	58
DDR2_A[8]	R26	DDR2_A[08]	179
DDR2_A[9]	R28	DDR2_A[09]	177
DDR2_A[10]	T26	DDR2_A[10]	70
DDR2_A[11]	T28	DDR2_A[11]	57
DDR2_A[12]	U27	DDR2_A[12]	176
DDR2_A[13]	AA28	DDR2_A[13]	196
DDR2_BA[0]	V28	DDR2_BA[0]	71
DDR2_BA[1]	W26	DDR2_BA[1]	190
DDR2_CK0	H30	DDR2_CK0	185
DDR2_CK0_N	H29	DDR2_CK0_N	186
DDR2_CS0_N	AJ30	DDR2_CS0_N	193
DDR2_CKE0	AJ31	DDR2_CKE0	52
DDR2_DM[0]	AH30	DDR2_DQM[00]	125
DDR2_DM[1]	M31	DDR2_DQM[01]	134
DDR2_DM[2]	T30	DDR2_DQM[02]	146
DDR2_DM[3]	U28	DDR2_DQM[03]	155
DDR2_DM[4]	AJ32	DDR2_DQM[04]	202
DDR2_DM[5]	AG31	DDR2_DQM[05]	211
DDR2_DM[6]	AG30	DDR2_DQM[06]	223
DDR2_DM[7]	AF29	DDR2_DQM[07]	232
DDR2_DQ[0]	C32	DDR2_DQ[00]	3
DDR2_DQ[1]	D32	DDR2_DQ[01]	4
DDR2_DQ[2]	E32	DDR2_DQ[02]	9
DDR2_DQ[3]	G32	DDR2_DQ[03]	10
DDR2_DQ[4]	H32	DDR2_DQ[04]	121
DDR2_DQ[5]	J32	DDR2_DQ[05]	122
DDR2_DQ[6]	K32	DDR2_DQ[06]	128
DDR2_DQ[7]	M32	DDR2_DQ[07]	129
DDR2_DQ[8]	N28	DDR2_DQ[08]	12
DDR2_DQ[9]	D31	DDR2_DQ[09]	13
DDR2_DQ[10]	E31	DDR2_DQ[10]	21

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Table 2-5: **Connections from FPGA to DDR2 DIMM Interface (P48) *(Cont'd)***

UCF Signal Name	XC4FX60 Pin (U37)	Schematic Signal Name	DDR2 DIMM (P48)
DDR2_DQ[11]	F31	DDR2_DQ[11]	22
DDR2_DQ[12]	G31	DDR2_DQ[12]	131
DDR2_DQ[13]	J31	DDR2_DQ[13]	132
DDR2_DQ[14]	K31	DDR2_DQ[14]	140
DDR2_DQ[15]	L31	DDR2_DQ[15]	141
DDR2_DQ[16]	C30	DDR2_DQ[16]	16
DDR2_DQ[17]	D30	DDR2_DQ[17]	17
DDR2_DQ[18]	F30	DDR2_DQ[18]	30
DDR2_DQ[19]	G30	DDR2_DQ[19]	31
DDR2_DQ[20]	Y28	DDR2_DQ[20]	143
DDR2_DQ[21]	Y27	DDR2_DQ[21]	144
DDR2_DQ[22]	L30	DDR2_DQ[22]	149
DDR2_DQ[23]	M30	DDR2_DQ[23]	150
DDR2_DQ[24]	N30	DDR2_DQ[24]	33
DDR2_DQ[25]	C29	DDR2_DQ[25]	34
DDR2_DQ[26]	D29	DDR2_DQ[26]	39
DDR2_DQ[27]	J30	DDR2_DQ[27]	40
DDR2_DQ[28]	L29	DDR2_DQ[28]	152
DDR2_DQ[29]	N29	DDR2_DQ[29]	153
DDR2_DQ[30]	P29	DDR2_DQ[30]	158
DDR2_DQ[31]	R29	DDR2_DQ[31]	159
DDR2_DQ[32]	T29	DDR2_DQ[32]	80
DDR2_DQ[33]	U32	DDR2_DQ[33]	81
DDR2_DQ[34]	V32	DDR2_DQ[34]	86
DDR2_DQ[35]	W32	DDR2_DQ[35]	87
DDR2_DQ[36]	Y32	DDR2_DQ[36]	199
DDR2_DQ[37]	AB32	DDR2_DQ[37]	200
DDR2_DQ[38]	AC32	DDR2_DQ[38]	205
DDR2_DQ[39]	AD32	DDR2_DQ[39]	206
DDR2_DQ[40]	AB27	DDR2_DQ[40]	89
DDR2_DQ[41]	U31	DDR2_DQ[41]	90
DDR2_DQ[42]	W25	DDR2_DQ[42]	95

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Table 2-5: **Connections from FPGA to DDR2 DIMM Interface (P48) *(Cont'd)***

UCF Signal Name	XC4FX60 Pin (U37)	Schematic Signal Name	DDR2 DIMM (P48)
DDR2_DQ[43]	Y31	DDR2_DQ[43]	96
DDR2_DQ[44]	AA31	DDR2_DQ[44]	208
DDR2_DQ[45]	AB31	DDR2_DQ[45]	209
DDR2_DQ[46]	AD31	DDR2_DQ[46]	214
DDR2_DQ[47]	AB28	DDR2_DQ[47]	215
DDR2_DQ[48]	AF31	DDR2_DQ[48]	98
DDR2_DQ[49]	U30	DDR2_DQ[49]	99
DDR2_DQ[50]	V30	DDR2_DQ[50]	107
DDR2_DQ[51]	Y26	DDR2_DQ[51]	108
DDR2_DQ[52]	AA30	DDR2_DQ[52]	217
DDR2_DQ[53]	AB30	DDR2_DQ[53]	218
DDR2_DQ[54]	AC30	DDR2_DQ[54]	226
DDR2_DQ[55]	AD30	DDR2_DQ[55]	227
DDR2_DQ[56]	AF30	DDR2_DQ[56]	110
DDR2_DQ[57]	V29	DDR2_DQ[57]	111
DDR2_DQ[58]	W29	DDR2_DQ[58]	116
DDR2_DQ[59]	Y29	DDR2_DQ[59]	117
DDR2_DQ[60]	AA29	DDR2_DQ[60]	229
DDR2_DQ[61]	AC29	DDR2_DQ[61]	230
DDR2_DQ[62]	AD29	DDR2_DQ[62]	235
DDR2_DQ[63]	AE29	DDR2_DQ[63]	236

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Figure 2-5 is a block diagram of the DDR2 DIMM interface.

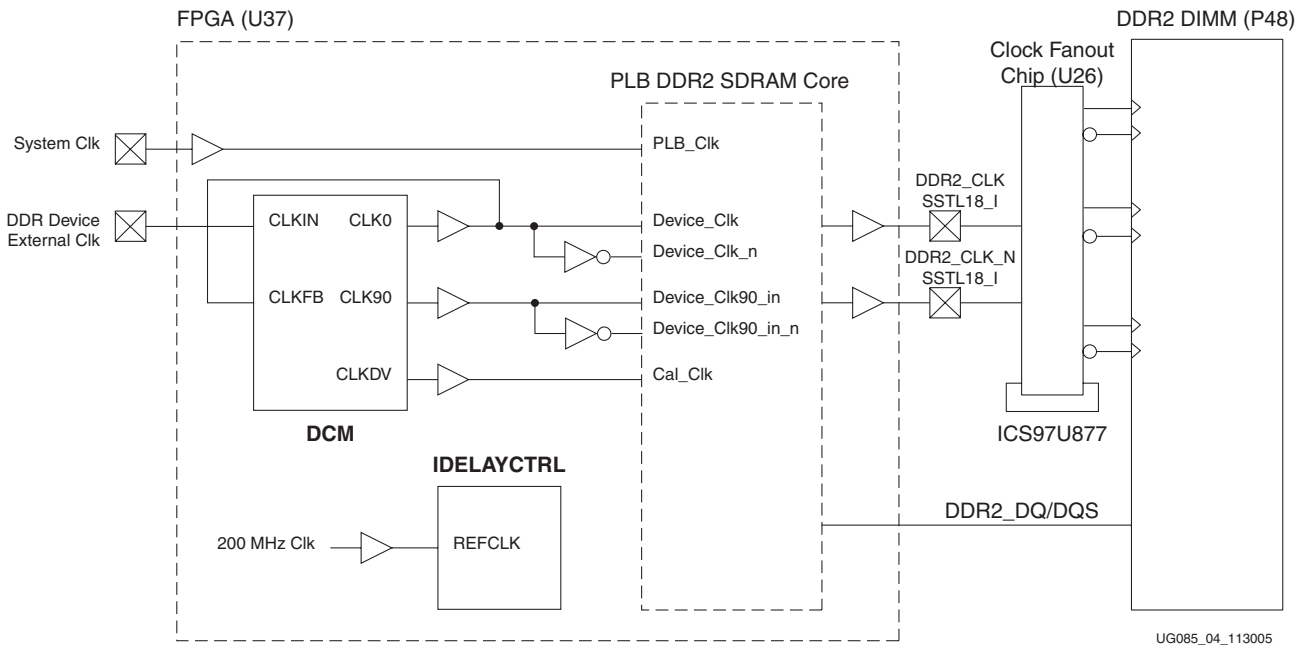

Figure 2-5: **DDR2 DIMM Block Diagram**

Tri-Mode (10/100/1000 Mb/s) Ethernet PHY

ML410 platforms feature two Ethernet PHYs that support MII, RGMII, and SGMII interfaces, as shown in Table 2-6. The Marvell Alaska PHY devices (88E1111) operate at 10/100/1000 Mb/s and are connected to a Halo HFJ21-1G01SE Dual RJ-45 connector with built-in magnetics (see Table 2-6). The PHY devices have independent MDIO and MDC controls and individual 25 MHz clock crystals.

Table 2-6: **Marvell Alaska PHY Configurations**

PHY	Interface	10BASE-T	100BASE-T	1000BASE-T
PHY0	MII	x	x (Full-duplex only)	-
	RGMII	x	x	x (Full-duplex only)
PHY1(1)	SGMII	x	x	x

Notes:

1. SGMII is not supported on the ML410-P. The ML410-P only supports one MII/RGMII PHY.

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PHY0: MII/RGMII

PHY0 (U60) is configured at power-on or reset to the default settings shown in Table 2-7. PHY0 is configurable to MII, or RGMII modes through the J28 jumper settings, as shown in Figure 2-6. These settings can be overwritten through software.

Table 2-7: **PHY0 (U60) Configuration Settings for MII/RGMII**

PHY Configuration	Power On Settings
5-bit PHY address (1)	`0b00111`
Interrupt polarity	Active-Low
MDC/MDIO interface	Enabled
Auto-negotiate	Slave (operational at 10/100/1000 Mb/s)
MDI crossover	Enabled
Fibre/copper auto-select	Disabled
Energy detect	Disabled
MAC pause	Disabled

Notes:

1. PHY address is `0b00000` for Rev. C and earlier boards.

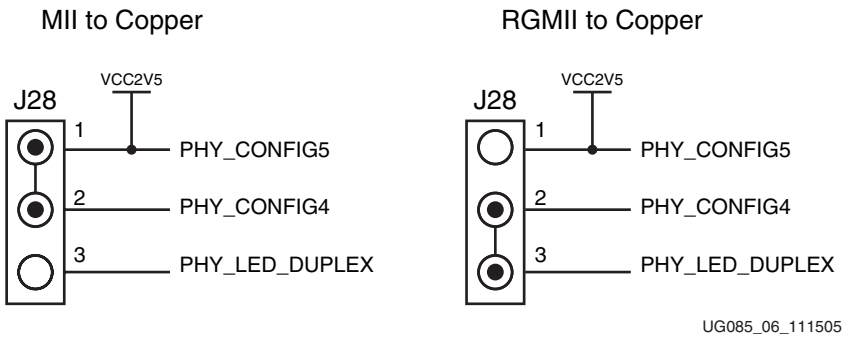

Figure 2-6: **PHY0 Jumper (J28) Settings**

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Figure 2-7 and Figure 2-8 show the MII and RMII interfaces. Functional differences are shown in bold text to indicate the behavior of the signals on each interface.

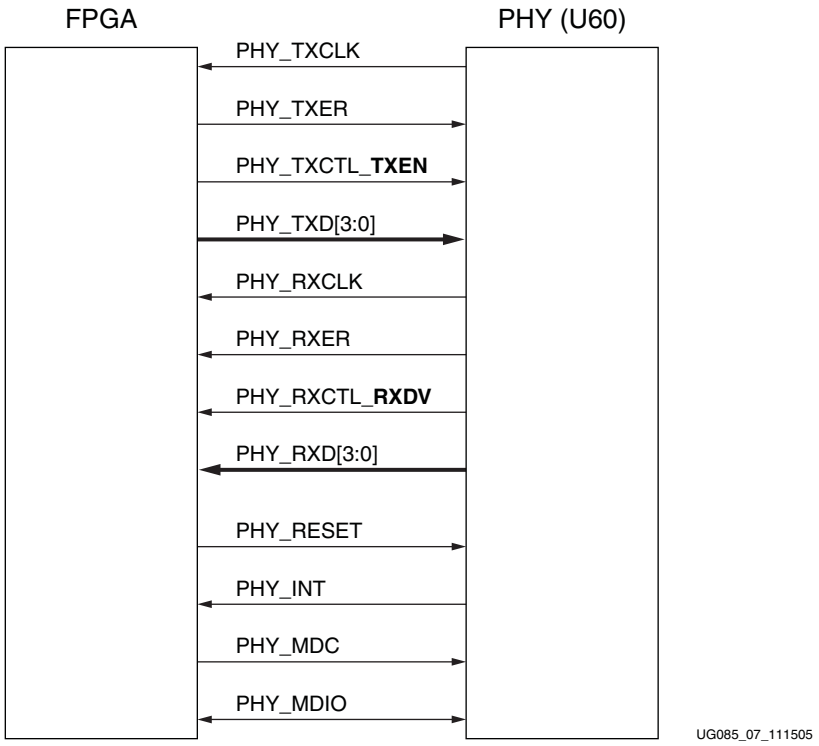

Figure 2-7: **MII Interface**

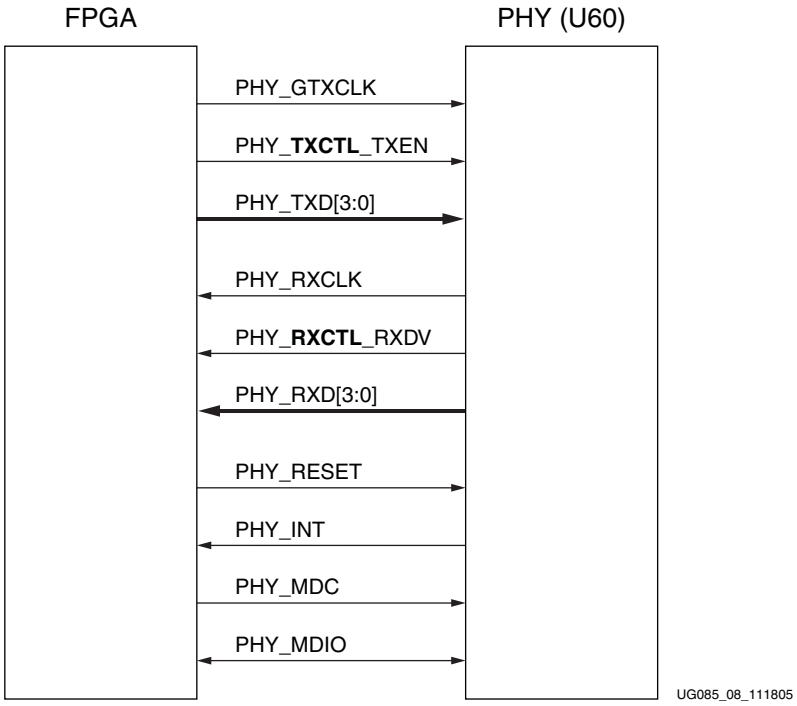

Figure 2-8: **RGMII Interface**

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Table 2-8 shows the MII/RGMII interface for PHY0.

Table 2-8: **PHY0 MII/RGMII Interface**

Signal Name	FPGA Pin (U37)	MII	RGMII	Description
PHY_TXCLK	J14	x		MII transmit clock
PHY_RXC_RXCLK	K19	x	x	Receive clock
PHY_GTXCLK	J19		x	RGMII transmit clock
PHY_TXD3	K9	x	x	Transmit data bits
PHY_TXD2	K11	x	x	
PHY_TXD1	K12	x	x	
PHY_TXD0	K13	x	x	
PHY_TXER	L14	x		Transmit controls
PHY_TXCTL_TXEN (1)	L11	x	x	
PHY_RXD3	J9	x	x	Receive data bits
PHY_RXD2	J10	x	x	
PHY_RXD1	J11	x	x	
PHY_RXD0	J12	x	x	
PHY_RXER	H18	x		Receive control signals
PHY_RXCTL_RXDV (2)	H12	x	x	
PHY_INT	M11	x	x	PHY0 interrupt
PHY_RESET	M12	x	x	PHY0 reset
PHY_MDIO	L13	x	x	PHY0 management data input/output
PHY_MDC	M13	x	x	PHY0 management data clock

Notes:

1. PHY_TXCTL_TXEN is a dual-purpose pin. In MII mode, it is TXEN. In RGMII mode, it is TXCTL.
2. PHY_RXCTL_RXDV is a dual-purpose pin. In MII mode, it is RXDV. In RGMII mode, it is RXCTL.

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PHY1: SGMII

Table 2-9 shows the default configuration settings for PHY1 (U61). PHY1 is fixed to SGMII mode only. It connects directly to the RocketIO transceiver so it is not software selectable.

Table 2-9: **PHY1 (U61) Configuration Settings for SGMII**

PHY Configuration	Power On settings
5-bit PHY address (1)	`0b00111`
Interrupt polarity	Active-Low
MDC/MDIO interface	Enabled
Auto-negotiate	Slave (operational at 10/100/1000 Mb/s)
MDI crossover	Enabled
Fibre/copper auto-select	Disabled
Energy detect	Disabled
MAC pause	Disabled

Notes:

1. PHY address is `0b00000` for Rev. C and earlier boards.

Table 2-10 shows the SGMII interface for PHY1.

Table 2-10: **PHY1 SGMII Interface**

Signal Name	FPGA Pin (U37)	Description
SGMIICLK_QO	M34	Clocks
SGMIICLK_NQO	N34	
RXPPADB_102	J34	Receive data (MGT)
RXNPADB_102	K34	
TXPPADB_102	F34	Transmit data (MGT)
TXNPADB_102	G34	
PHY_INT_SGMII	K17	PHY0 interrupt
PHY_RESET_SGMII	J17	PHY0 reset

Table 2-11 shows the MDIO interface for PHY1.

Table 2-11: **PHY1 MDIO Interface**

Signal Name	FPGA Pin (U37)	Description
PHY1_MDIO	AE19	PHY1 management data input/output
PHY1_MDC	AD19	PHY1 management data clock

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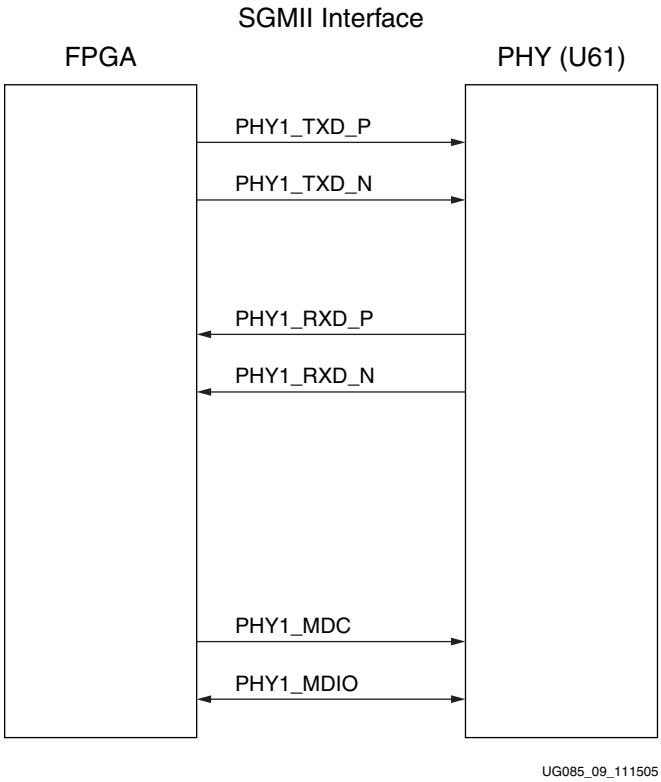

Figure 2-9: **SGMII Interface**

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RS-232 Ports

Two RS-232 ports, shown in Figure 2-10, are connected to the FPGA (U37) through independent MAX3232 transceivers (U7 and U46). The FPGA RS-232 ports are wired as DTE and meet the *EIA/TIA-574* standard. The ports are accessible via two DB9M connectors integrated on the P1 connector assembly.

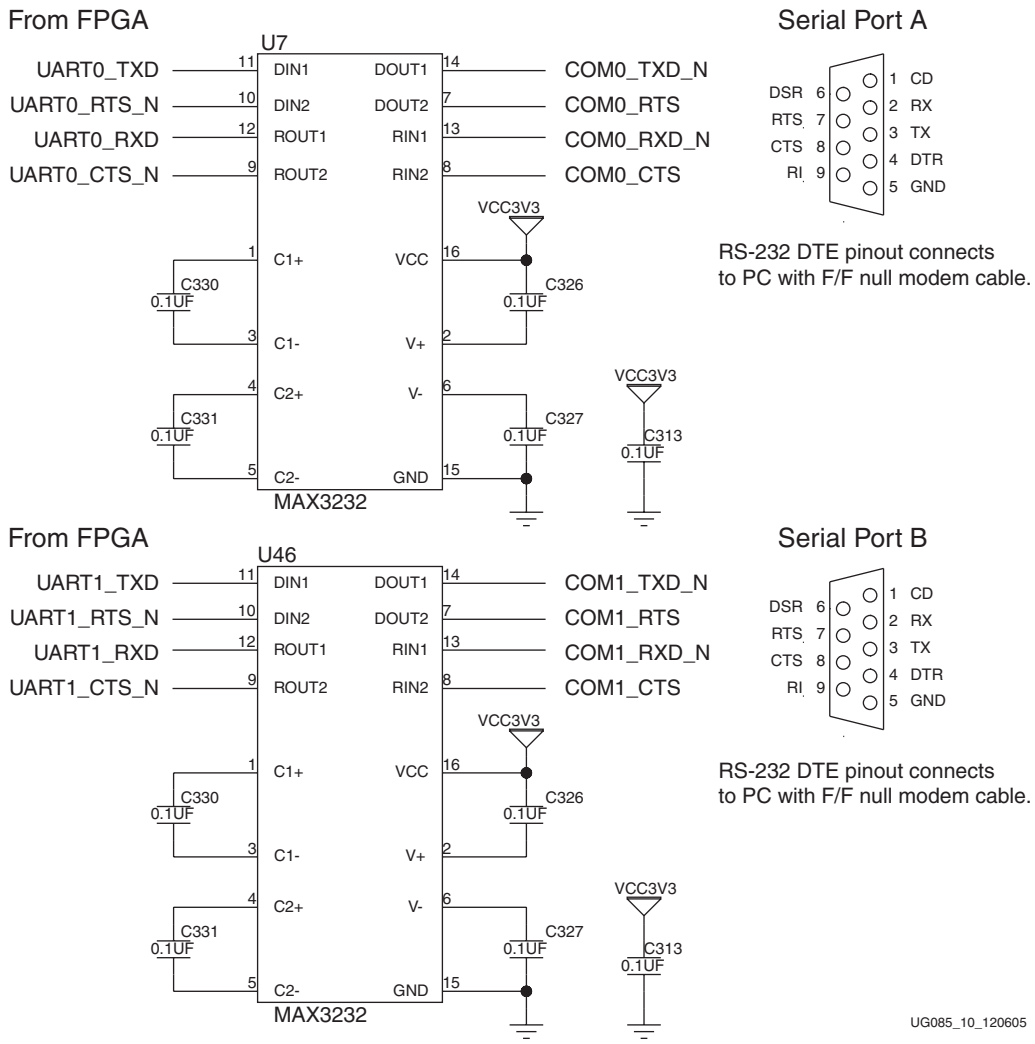

Figure 2-10: **FPGA UART and RS-232 Connectivity**

Table 2-12 and Table 2-13, page 44 show the RS-232 connections to the FPGA for UART0 and UART1.

Table 2-12: **FPGA RS-232 Connections for UART0**

Signal Name	FPGA Pin (U37)
UART0_CTS_N	G6
UART0_RTS_N	F6
UART0_RXD	E6
UART0_TXD	D6

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Table 2-13: **FPGA RS-232 Connections for UART1**

Signal Name	FPGA Pin (U37)
UART1_CTS_N	E14
UART1_RTS_N	D16
UART1_RXD	D15
UART1_TXD	D14

System ACE CF Controller

Introduction to JTAG

JTAG (Joint Test Action Group) is a simple interface that provides for many uses. On ML410 platforms, the primary uses include configuration of the FPGA, debugging software (similar to the CPU debug interface), and debugging hardware using the ChipScope™ Integrated Logic Analyzer (ILA).

The Virtex-4 family is fully compliant with the *IEEE Standard 1149.1 Test Access Port and Boundary-Scan Architecture* and includes all mandatory elements defined in the standard. These elements include the Test Access Port (TAP), the TAP controller, the instruction register, the instruction decoder, the Boundary-Scan register, and the bypass register. The Virtex-4 family also supports some optional instructions; the 32-bit identification register, and a configuration register in full compliance with the standard.

Introduction to the System ACE Configuration Solution

The Xilinx System ACE CompactFlash (CF) configuration controller allows a Type I or Type II CompactFlash card to program the FPGA through the JTAG port. Both hardware and software data can be downloaded through the JTAG port. The System ACE controller supports up to eight configuration images on a single CompactFlash card. The configuration address switches allow the user to choose which of the eight configuration images to use.

System ACE error and status LEDs indicate the operational state of the System ACE controller:

- A blinking red error LED indicates that no CompactFlash card is present
- A solid red error LED indicates an error condition during configuration
- A blinking green status LED indicates a configuration operation is ongoing
- A solid green status LED indicates a successful download

Every time a CompactFlash card is inserted into the System ACE socket, a configuration operation is initiated. Pressing the System ACE reset button re-programs the FPGA.

The board also features a System ACE *failsafe* mode. In this mode, if the System ACE controller detects a failed configuration attempt, it automatically reboots back to a predefined configuration image. The failsafe mode is enabled by inserting two jumpers across J4 and J10 (in horizontal or vertical orientation).

> ***Caution!*** Use caution when inserting a CompactFlash card with exposed metallic surfaces. Improper insertion can cause a short with the traces or components on the board.

The System ACE MPU port is connected to the FPGA. This connection allows the FPGA to use the System ACE controller to reconfigure the system or access the CompactFlash card

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as a generic FAT file system. The data bus for the System ACE MPU port is shared with the USB controller. See "Non-Volatile Storage through the MPU Interface," page 46.

Board Bring-Up through the JTAG Interface

The System ACE CF controller is located between the JTAG connector and the FPGA, and passes the JTAG signals back and forth between the two. During configuration, the System ACE CF controller has full control of the JTAG signals. Figure 2-11 shows the connections between the JTAG connector, System ACE CF controller, and the FPGA. The CPU JTAG header (J12) is used to access the JTAG interface when J27 is jumpered. See "JTAG Source Select (J27)," page 79.

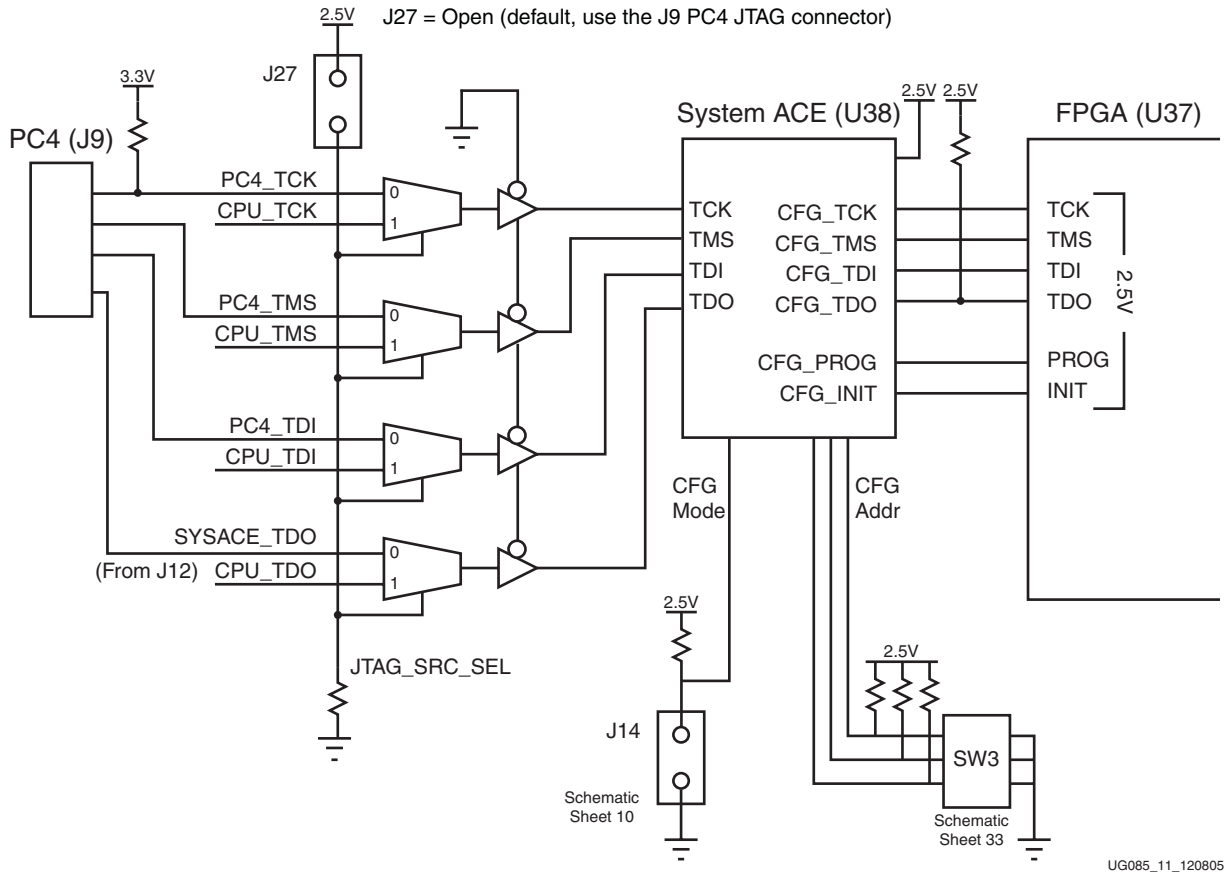

Figure 2-11: **JTAG Connections to the FPGA and System ACE CF Controller**

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The pinout shown in Figure 2-12 is compatible with the Parallel Cable IV (PC4) JTAG programming solution. The J9 header is used when programming the FPGA by way of the PC4 download cable.

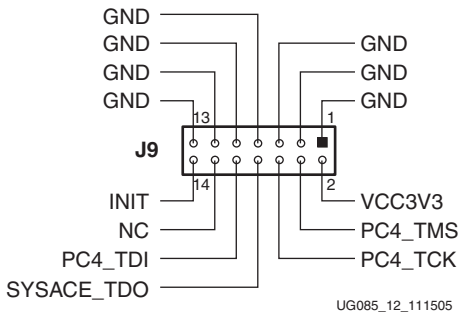

Figure 2-12: **PC4 JTAG Connector Pinout (J9)**

The JTAG configuration port on the System ACE CF controller is connected directly to the JTAG interface of the FPGA, as shown in Table 2-14.

Table 2-14: **JTAG Connection from System ACE CF to FPGA**

Signal Name	System ACE Pin (U38)	FPGA Pin (U37)
FPGA_TCK	80	AA14
FPGA_TDO	81	W17
FPGA_TDI	82	AA15
FPGA_TMS	85	Y14

Non-Volatile Storage through the MPU Interface

In addition to programming the FPGA and storing bitstreams, the System ACE CF controller can be used to facilitate general-use, non-volatile storage. The System ACE CF controller provides an MPU interface for allowing a microprocessor to access the CompactFlash memory, enabling the use of the CompactFlash card as a file system. The System ACE MPU interface is capable of supporting 16-bit or 8-bit modes of operation because all 16 data lines are wired to the FPGA.

Table 2-15 shows the connection between the System ACE MPU interface and the FPGA.

Table 2-15: **System ACE MPU Connection from FPGA to Controller**

UCF Signal Name	FPGA Pin (U37)	Schematic Signal Name	System ACE Pin (U38)
SYSACE_FPGA_CLK	AF16	SYSACE_FPGA_CLK	93
SYSACE_CLK_OE	AD4	SYSACE_CLK_OE	77
SYSACE_MPA[0]	AE6	SYSACE_MPA[00]	70
SYSACE_MPA[1]	AE4	SYSACE_MPA[01]	69
SYSACE_MPA[2]	AE3	SYSACE_MPA[02]	68
SYSACE_MPA[3]	AF6	SYSACE_MPA[03]	67
SYSACE_MPA[4]	AF5	SYSACE_MPA[04]	45

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Table 2-15: **System ACE MPU Connection from FPGA to Controller *(Cont'd)***

UCF Signal Name	FPGA Pin (U37)	Schematic Signal Name	System ACE Pin (U38)
SYSACE_MPA[5]	AF4	SYSACE_MPA[05]	44
SYSACE_MPA[6]	AF3	SYSACE_MPA[06]	43
SYSACE_MPD[0]	AG6	SYSACE_MPD[00]	66
SYSACE_MPD[1]	AG5	SYSACE_MPD[01]	65
SYSACE_MPD[2]	AG3	SYSACE_MPD[02]	63
SYSACE_MPD[3]	AH5	SYSACE_MPD[03]	62
SYSACE_MPD[4]	AH4	SYSACE_MPD[04]	61
SYSACE_MPD[5]	AH3	SYSACE_MPD[05]	60
SYSACE_MPD[6]	AJ6	SYSACE_MPD[06]	59
SYSACE_MPD[7]	AJ5	SYSACE_MPD[07]	58
SYSACE_MPD[8]	AJ4	SYSACE_MPD[08]	56
SYSACE_MPD[9]	AK6	SYSACE_MPD[09]	53
SYSACE_MPD[10]	AK4	SYSACE_MPD[10]	52
SYSACE_MPD[11]	AK3	SYSACE_MPD[11]	51
SYSACE_MPD[12]	AL6	SYSACE_MPD[12]	50
SYSACE_MPD[13]	AL5	SYSACE_MPD[13]	49
SYSACE_MPD[14]	AL4	SYSACE_MPD[14]	48
SYSACE_MPD[15]	AA3	SYSACE_MPD[15]	47
SYSACE_MPOE	AM5	SYSACE_MPOE	77
SYSACE_MPCE	AB6	SYSACE_MPCE	42
SYSACE_MPWE	AB3	SYSACE_MPWE	76
SYSACE_MPIRQ	AM6	SYSACE_MPIRQ	41

GPIO LEDs and LCD

ML410 platforms provide direct GPIO access to eight LEDs for general purpose use, and provide indirect access to a 16-pin connector (J13) that interfaces the FPGA to a 2-line by 16-character LCD display, AND491GST. A simple register interface handles access to the FPGA's GPIO signals.

The user also has indirect access to additional GPIO capability by way of the PCI bus through the GPIO header (J5) connected to the ALi M1535D+ South Bridge. See the "ALi South Bridge Interface, M1535D+ (U15)" section for more details on programming and controlling the ALi M1535D+ GPIO port.

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Figure 2-13 shows the connectivity of the ML410 LEDs and LCD.

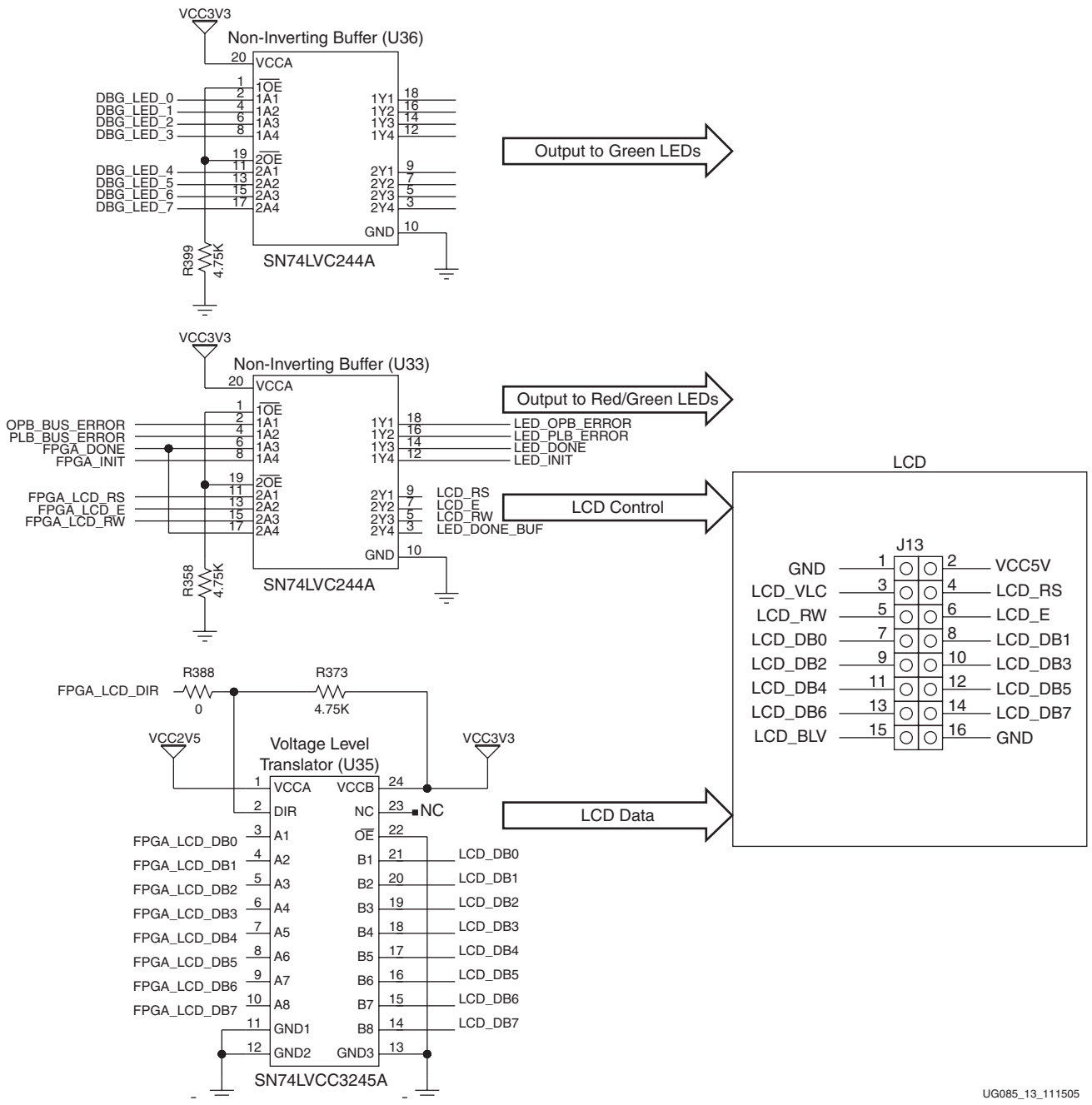

Figure 2-13: **LEDs and LCD Connectivity**

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GPIO LED Interface

All LEDs connected to the GPIO lines illuminate green when driven with a logic 0 and extinguish with a logic 1. Table 2-16 shows the connections for the GPIO LEDs from the FPGA to the non-inverting buffer (U36).

Table 2-16: **GPIO LED Connection from FPGA to U36**

UCF Signal Name	FPGA Pin (U37)	Schematic Signal Name	LVC244 Buffer (U36)	LED
DBG_LED_0	AF19	DBG_LED_0	2	DS20
DBG_LED_1	AD5	DBG_LED_1	4	DS19
DBG_LED_2	AD6	DBG_LED_2	6	DS18
DBG_LED_3	AD7	DBG_LED_3	8	DS17
DBG_LED_4	AB8	DBG_LED_4	11	DS16
DBG_LED_5	AC7	DBG_LED_5	13	DS15
DBG_LED_6	AC9	DBG_LED_6	15	DS14
DBG_LED_7	AC10	DBG_LED_7	17	DS13

GPIO LCD Interface

The GPIO LCD interface has eight input/output signals used as data and three output-only signals used as control. The data signals are controlled by the logic level of the FPGA_LCD_DIR signal. A logic 1 on FPGA_LCD_DIR configures the LVCC3245 to drive the J13 header, while a logic 0 on FPGA_LCD_DIR configures the LVCC3245 to drive the FPGA.

Table 2-17 shows the data bus signals on the GPIO LCD interface from the FPGA to U35.

Table 2-17: **GPIO LCD Data Signals from FPGA to U35**

UCF Signal Name	FPGA Pin (U37)	Schematic Signal Name	LVCC3245 Translator (U35)	LCD I/F (J13)
FPGA_LCD_DB0	AJ21	FPGA_LCD_DB0	3	7
FPGA_LCD_DB1	AG21	FPGA_LCD_DB1	4	8
FPGA_LCD_DB2	AJ20	FPGA_LCD_DB2	5	9
FPGA_LCD_DB3	AH20	FPGA_LCD_DB3	6	10
FPGA_LCD_DB4	AG20	FPGA_LCD_DB4	7	11
FPGA_LCD_DB5	AK19	FPGA_LCD_DB5	8	12
FPGA_LCD_DB6	AJ19	FPGA_LCD_DB6	9	13
FPGA_LCD_DB7	AH19	FPGA_LCD_DB7	10	14
FPGA_LCD_DIR	AK18	FPGA_LCD_DIR	2	-

The control signals allow the user to read/write the LCD character display in conjunction with the eight LCD data signals defined in Table 2-17. See the AND491GST LCD display data sheet located on the ML410 documentation CD for more information.

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Table 2-18 shows the control signal connections for the GPIO LCD from the FPGA to U33.

Table 2-18: **GPIO LCD Control Signals from FPGA to U33**

UCF Signal Name	FPGA Pin (U37)	Schematic Signal Name	LVC244 Buffer (U33)	LCD I/F (J13)
FPGA_LCD_E	AH18	FPGA_LCD_E	13	6
FPGA_LCD_RS	AK17	FPGA_LCD_RS	11	4
FPGA_LCD_RW	AJ17	FPGA_LCD_RW	15	5

CPU Debugging Interfaces

ML410 platforms include two optional CPU debugging interfaces: the combined FPGA JTAG/TRACE (P8) mictor connector and the CPU JTAG header (J12). These connectors can be used in conjunction with third party tools, or in some cases with the Xilinx Parallel Cable IV, to debug software as it runs on the processor. The P8 mictor connector supports the Agilent ATC2 core that can be mapped using the ChipScope Pro CORE Generator™ software. See www.xilinx.com/chipscope for more information.

The PPC405 CPU core includes dedicated debug resources that support a variety of debug modes for debugging during hardware and software development. These debug resources include:

- Internal debug mode for use by ROM monitors and software debuggers
- External debug mode for use by JTAG debuggers
- Debug wait mode, which allows the servicing of interrupts while the processor appears to be stopped
- Real-time trace mode, which supports event triggering for real-time tracing

Debug modes and events are controlled using debug registers in the processor. The debug registers are accessed through either software running on the processor or through the JTAG port. The debug modes, events, controls, and interfaces provide a powerful combination of debug resources for hardware and software development tools. The JTAG port interface supports the attachment of external debug tools, such as the ChipScope Integrated Logic Analyzer, a tool providing logic analyzer capabilities for signals inside an FPGA, without the need for expensive external instrumentation. Using the JTAG test access port, a debug tool can single-step the processor and examine the internal processor state to facilitate software debugging. This capability complies with the *IEEE 1149.1 Standard* for vendor-specific extensions and is, therefore, compatible with standard JTAG hardware for Boundary-Scan system testing. See the *PowerPC 405 Processor Block Reference Guide* [Ref 1].

CPU Debug Description

External-debug mode can be used to alter normal program execution. It provides the ability to debug both system hardware and software. External-debug mode supports setting of multiple breakpoints, as well as monitoring processor status. Access to processor debugging resources is available through the CPU JTAG port (J12) providing the appropriate connections to the FPGA fabric are in place.

The PPC405 JTAG debug port in the FPGA complies with *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary Scan Architecture*. This standard describes a method for accessing internal chip resources using a four-signal or five-signal interface. The PPC405 JTAG Debug port supports scan-based board testing and is further enhanced to

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support the attachment of debug tools. These enhancements comply with the IEEE 1149.1 specifications for vendor-specific extensions and are compatible with standard JTAG hardware for boundary-scan system testing.

The PPC405 JTAG debug port supports the four required JTAG signals: TCK, TMS, TDI, and TDO. It also implements the optional TRST signal. The frequency of the JTAG clock signal can range from 0 MHz (DC) to one-half of the processor clock frequency. The JTAG debug port logic is reset at the same time the system is reset, using TRST. When TRST is asserted, the JTAG TAP controller returns to the test-logic reset state. See the *PowerPC 405 Processor Block Reference Guide* [Ref 1] for more information on the JTAG debug port signals.

Figure 2-14 shows a 38-pin Mictor connector that combines the CPU Trace and the CPU Debug interfaces for high-speed, controlled-impedance signaling. For more information on starting and stopping the processor, single-stepping instruction execution on the trace-debug capabilities, how trace-debug works, and how to connect an external trace tool, see the *RISCWatch Debugger User's Guide*.

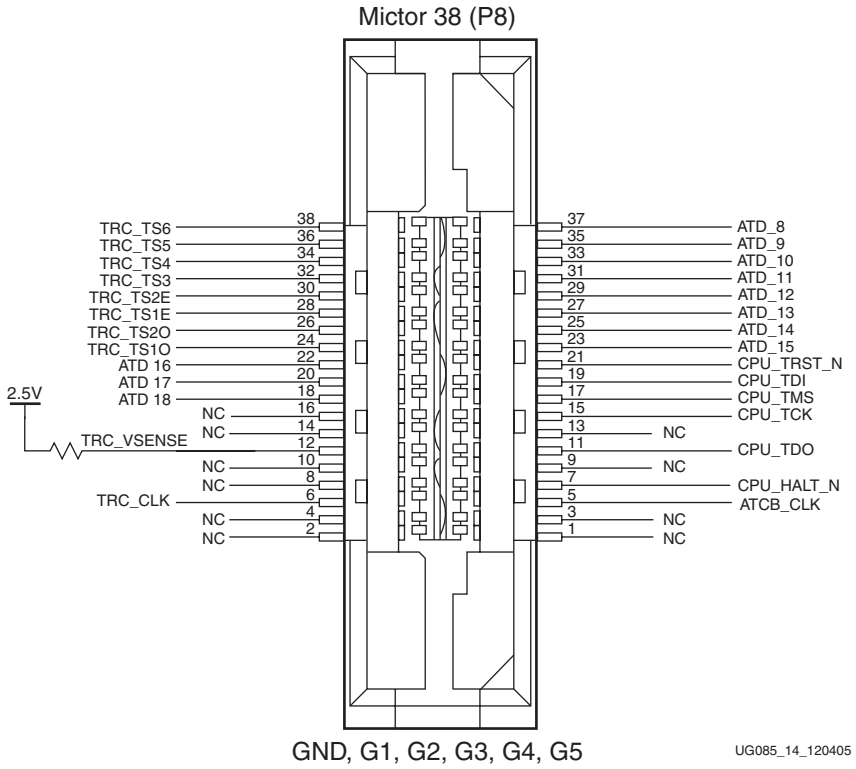

Figure 2-14: **Combined Trace/Debug Connector Pinout**

Table 2-19 shows the CPU trace/debug connections from P8 to the FPGA.

Table 2-19: **CPU Trace/Debug Connection to FPGA**

Pin Name	FPGA Pin (U37)	Connector Pin (P8)
-	NC	1
-	NC	2
-	NC	3
-	NC	4

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Table 2-19: **CPU Trace/Debug Connection to FPGA *(Cont'd)***

Pin Name	FPGA Pin (U37)	Connector Pin (P8)
ATCB_CLK	AL8	5
TRC_CLK	AK8	6
CPU_HALT_N	AH17	7
-	NC	8
-	NC	9
-	NC	10
CPU_TDO	AM8	11
TRC_VSENSE	-	12
-	NC	13
-	NC	14
CPU_TCK	AJ27	15
-	NC	16
CPU_TMS	AM7	17
ATD_18	AH13	18
CPU_TDI	AK29	19
ATD_17	AJ11	20
CPU_TRST_N	AH27	21
ATD_16	AK7	22
ATD_15	AK21	23
TRC_TS1O	AH7	24
ATD_14	AH24	25
TRC_TS2O	AG10	26
ATD_13	AK11	27
TRC_TS1E	AH8	28
ATD_12	AL21	29
TRC_TS2E	AG11	30
ATD_11	AJ24	31
TRC_TS3	AF11	32
ATD_10	AJ29	33
TRC_TS4	AF10	34
ATD_9	AG13	35
TRC_TS5	AD12	36

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Table 2-19: **CPU Trace/Debug Connection to FPGA *(Cont'd)***

Pin Name	FPGA Pin (U37)	Connector Pin (P8)
ATD_8	AJ7	37
TRC_TS6	AE12	38

CPU JTAG Header Pinout

Figure 2-15 shows J12, the 16-pin header that can be used to debug the software operating in the CPU with debug tools such as Parallel Cable IV or third party tools. Refer to the *PowerPC 405 Processor Block Reference Guide* [Ref 1] for more information on the JTAG debug port signals.

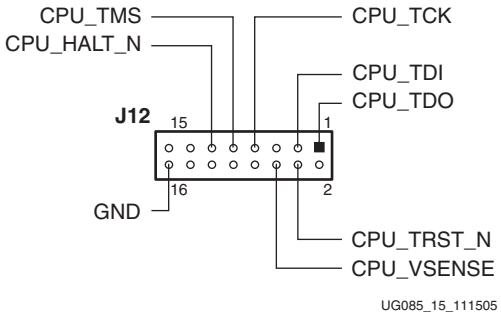

Figure 2-15: **CPU JTAG Header (J12)**

CPU JTAG Connection to FPGA

The connection between the CPU JTAG header (J12) and the FPGA are shown in Table 2-20. These are attached to the PPC405 JTAG debug resources using normal FPGA routing resources. The JTAG debug resources are not hard-wired to particular pins and are available for attachment in the FPGA fabric, making it possible to route these signals to the preferred FPGA pins.

Table 2-20: **CPU JTAG Connection to FPGA**

Pin Name	FPGA Pin (U37)	Connector Pin (J12)
CPU_TDO	AM8	1
CPU_TDI	AK29	3
CPU_TRST_N	AH27	4
CPU_TCK	AJ27	7
CPU_TMS	AM7	9
CPU_HALT_N	AH17	11

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VGA Output

A VGA DB15HD connector (P2) is present on ML410 platforms to support an external video monitor. The VGA circuitry utilizes a 140 MHz, 24-bit color video DAC (Analog Devices ADV7125KST140). Table 2-21 shows the connections between the FPGA and the DAC.

Note: The VGA connector does not support plug and play protocol via ID0/ID1 pins.

Table 2-21: **Connections from FPGA to DAC**

Signal Name	FPGA Pin (U37)	Description
VGA_R0	F10	Red pixel data outputs
VGA_R1	F11	
VGA_R2	G10	
VGA_R3	G11	
VGA_R4	G12	
VGA_R5	H9	
VGA_R6	C5	
VGA_R7	H8	
VGA_G0	E8	Green pixel data outputs
VGA_G1	E9	
VGA_G2	E11	
VGA_G3	E12	
VGA_G4	E13	
VGA_G5	F8	
VGA_G6	D4	
VGA_G7	D5	
VGA_B0	G8	Blue pixel data outputs
VGA_B1	C13	
VGA_B2	D9	
VGA_B3	D10	
VGA_B4	D11	
VGA_B5	D12	
VGA_B6	C3	
VGA_B7	C4	
VGA_HSYNC	F9	Horizontal sync
VGA_VSYNC	H10	Vertical sync
VGA_CLK	C12	Video clock

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PCI Express

ML410 platforms that are equipped with PCI Express host connectors (P53 and P54) are capable of supporting PCI Express cores. Power distribution is handled by a MIC2959B dual-slot PCI Express hot-plug controller (Figure 2-16) that also provides comprehensive system protection and fault isolation. The MIC2959B controls the power delivered through MOSFETs to the Slot A (P53) and Slot B (P54) PCI Express connectors. The MIC2592B also incorporates an SMBus interface that provides control for and status of each PCI Express slot.

Although two 16x PCI Express connectors are mounted on ML410 platforms, not all 16 lanes are wired for use. Refer to Appendix A, "Board Revisions" for a summary of features and devices available on each board.

The PCI Express interface supports MGTs operating at 2.5 Gb/s. Power is activated to the PCI Express slots only when the proper MIC2959B IIC commands are delivered to the MIC2959B at address `0x8E` over the IIC interface. For more on IIC, see "IIC/SMBus Interface," page 69. For details on the power controller, see the *MIC2959B data sheet* at www.micrel.com. For more on clocking, see "Clock Generation," page 26.

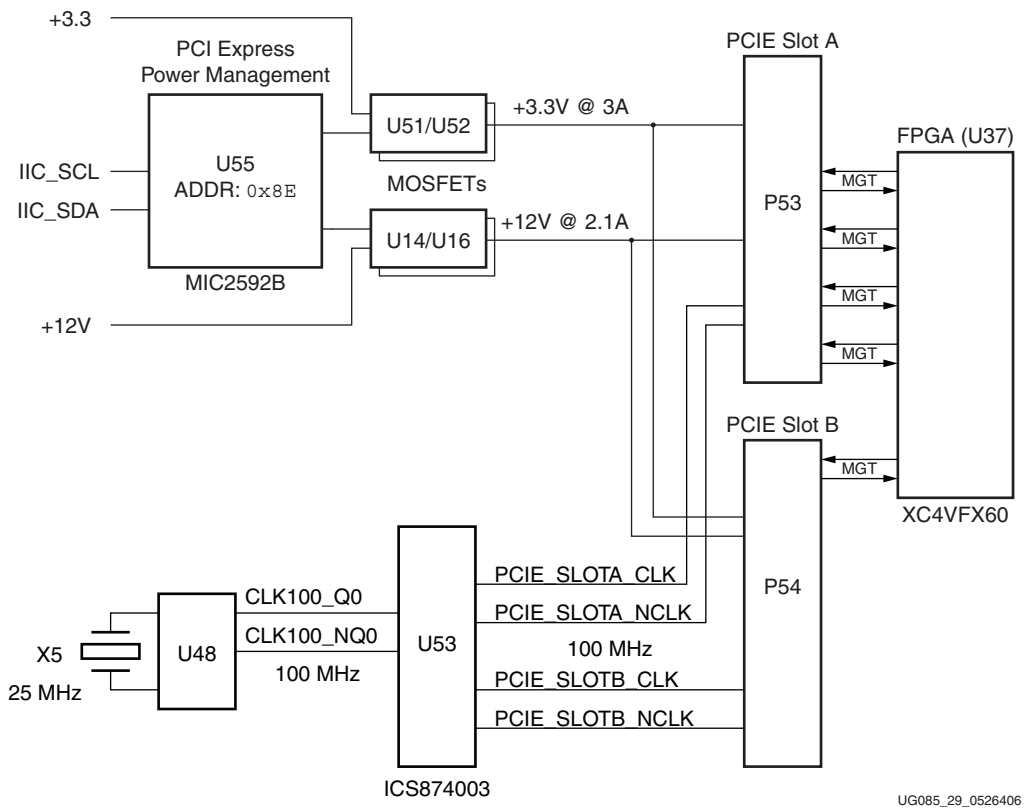

Figure 2-16: **PCI Express Power Management and Clocking**

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Table 2-22 and Table 2-23, page 57 detail the connections between the FPGA and the PCI Express connectors.

Table 2-22: **Connections from FPGA to PCI Express Slot A**

Net Name	FPGA Pin (U37)	Connector Pin (P53)
RXPPADA_103	R34	16
RXNPADA_103	T34	17
RXPPADB_103	AC34	21
RXNPADB_103	AD34	22
TXPPADA_103	V34	96
TXNPADA_103	W34	106
TXPPADB_103	Y34	101
TXNPADB_103	AA34	102
RXPPADA_105	AF34	25
RXNPADA_105	AG34	26
RXPPADB_105	AP32	29
RXNPADB_105	AP31	30
TXPPADA_105	AJ34	105
TXNPADA_105	AK34	106
TXPPADB_105	AL34	109
TXNPADB_105	AM34	110
PCIE_SLOTA_PRSNT2#	F15	130
PCIE_SLOTA_PWRGD#	H13	11
PCIE_SLOTA_WAKE#	F13	93

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Table 2-23: **Connections from FPGA to PCI Express Slot B**

Net Name	FPGA Pin (U37)	Connector Pin (P54)
RXPPADA_101	A20	25
RXNPADA_101	A21	26
RXPPADB_101	A28	21
RXNPADB_101	A29	22
TXPPADA_101	A23	105
TXNPADA_101	A24	106
TXPPADB_101	A25	101
TXNPADB_101	A26	102
RXPPADA_102	A31	16
RXNPADA_102	A32	17
RXPPADB_114	A10	29
RXNPADB_114	A9	30
TXPPADA_102	D34	96
TXNPADA_102	E34	97
TXPPADB_114	A13	109
TXNPADB_114	A12	110
PCIE_SLOTB_PRSNT2#	F16	130
PCIE_SLOTB_PWRGD#	G13	11
PCIE_SLOTB_WAKE#	F14	93

PCI Bus

ML410 platforms provide the FPGA with access to two 33 MHz/32-bit PCI buses, a primary 3.3V PCI bus and a secondary 5V PCI bus. The FPGA is directly connected to the primary 3.3V PCI bus while the 5V PCI bus is connected to the primary PCI bus via a PCI-to-PCI bridge. Several PCI devices are available on the PCI buses as well as four PCI add-in card slots. All PCI bus signals driven by the FPGA comply with the I/O requirements specified in the *PCI Local Bus Specification, Revision 2.2* (see www.pcisig.com).

The majority of the ML410 features are accessed over the 33 MHz/32-bit PCI bus. The Virtex-4 PPC405 processors can access the primary PCI bus through the EDK PCI Host Bridge IP. All PCI configuration and control can be performed via a PCI Host Bridge implemented in the FPGA fabric. The primary PCI bus is wired so that the FPGA fabric must be used to provide PCI bus arbitration logic. EDK also provides PCI Arbiter IP. See the EDK *Processor IP User Guide* [Ref 2] for more information about the EDK IP mentioned in this section.

The FPGA is responsible generating the PCI RST signal as well as the PCI CLK signal. The FPGA fabric is used to generate several PCI clocks that drive each of the PCI devices/slots shown in Figure 2-17. All six PCI clock outputs are length matched. Because the FPGA

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generates all PCI clocks, the downstream PCI devices have no clock input prior to or during FPGA configuration; therefore, PCI Reset should be deasserted after the PCI CLK has stabilized. Please review the *PCI Local Bus Specification, Revision 2.2* for more information.

The onboard 33 MHz, 32-bit PCI bus is connected to fixed PCI devices that are part of the ML410. These fixed PCI devices are as follows:

- Texas Instruments, TI2250, PCI-to-PCI bridge
- ALi, M1535D+, PCI South Bridge

These devices are described in the following sections as well in their data sheets on the ML410 documentation CD.

In addition to the fixed PCI devices, there are four 33 MHz, 32-bit PCI slots available for use. For more information on the PCI slot pinouts, refer to the *PCI Local Bus Specification, Revision 2.2* and the ML410 schematics.

- Two 3.3V keyed PCI add-in card slots (P5 and P3)
- Two 5V keyed PCI add-in card slots (P6 and P4)

Figure 2-17 shows the connectivity of the PCI bus and PCI devices. For more information on the PCI slot pinouts, refer to the *PCI Local Bus Specification, Revision 2.2* or review the ML410 schematics.

Note: The 5V PCI slots differ from the 3.3V slots. See the *Important Instructions* sheet (PN 0402395) packaged with the ML410 kit before using Universal PCI add-in cards with ML410 platforms.

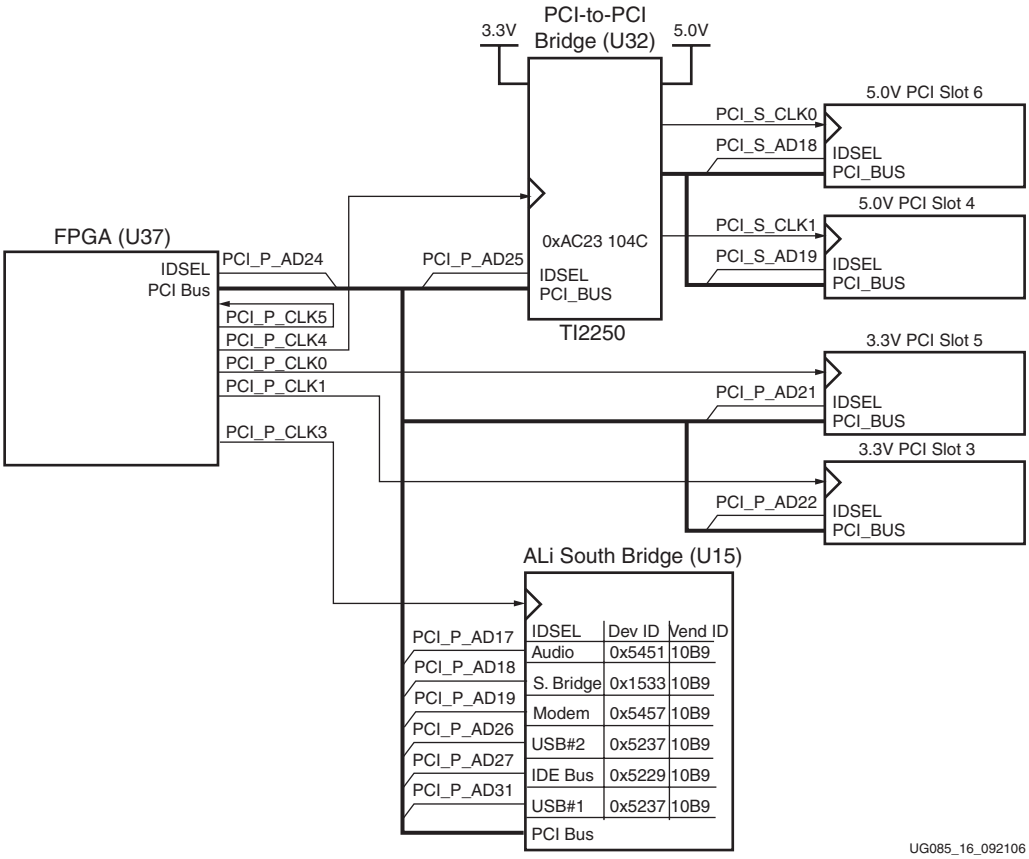

Figure 2-17: **PCI Bus and Device Connectivity**

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Table 2-24 shows the connections for the PCI controller.

Table 2-24: **PCI Controller Connections**

UCF Signal Name	FPGA Pin (U37)	Description
PCI_CLK0	V5	PCI_P_CLK0
PCI_CLK1	T11	PCI_P_CLK1
PCI_CLK3	U7	PCI_P_CLK3
PCI_CLK4	U3	PCI_P_CLK4
PCI_CLK5	U5	PCI_P_CLK5
PCI_CLK5_FB	H17	PCI_P_CLK5
PCI_INTA_N	P5	PCI Interrupt Signals
PCI_INTB_N	R8	
PCI_INTC_N	P9	
PCI_INTD_N	V4	
PCI_REQ0_N	T3	PCI Request Signals
PCI_REQ1_N	R7	
PCI_REQ2_N	T8	
PCI_REQ3_N	T9	
PCI_REQ4_N	R9	
PCI_GNT0_N	T4	PCI Grant Signals
PCI_GNT1_N	T5	
PCI_GNT2_N	U8	
PCI_GNT3_N	V3	
PCI_GNT4_N	T6	
PCI_CBE[0]	M5	PCI Byte-Enable Signals
PCI_CBE[1]	L6	
PCI_CBE[2]	R4	
PCI_CBE[3]	R6	
PCI_FRAME_N	N8	PCI Control Signals
PCI_IRDY_N	N5	
PCI_TRDY_N	M3	
PCI_STOP_N	P11	
PCI_DEVSEL_N	R3	
PCI_PERR_N	M6	
PCI_SERR_N	M7	
PCI_LOCK	P4	
PCI_IDSEL	N7	

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Table 2-24: **PCI Controller Connections *(Cont'd)***

UCF Signal Name	FPGA Pin (U37)	Description
PCI_AD[0]	L4	PCI Address/Data Lines
PCI_AD[1]	L5	
PCI_AD[2]	H3	
PCI_AD[3]	F4	
PCI_AD[4]	E3	
PCI_AD[5]	E4	
PCI_AD[6]	N3	
PCI_AD[7]	N4	
PCI_AD[8]	G5	
PCI_AD[9]	F3	
PCI_AD[10]	F5	
PCI_AD[11]	G3	
PCI_AD[12]	L9	
PCI_AD[13]	L10	
PCI_AD[14]	J4	
PCI_AD[15]	J5	
PCI_AD[16]	H4	
PCI_AD[17]	H5	
PCI_AD[18]	N9	
PCI_AD[19]	N10	
PCI_AD[20]	K3	
PCI_AD[21]	K4	
PCI_AD[22]	J6	
PCI_AD[23]	J7	
PCI_AD[24]	M8	
PCI_AD[25]	M10	
PCI_AD[26]	K8	
PCI_AD[27]	L3	
PCI_AD[28]	K6	
PCI_AD[29]	K7	
PCI_AD[30]	P6	
PCI_AD[31]	P7	
PCI_PAR	L8	PCI_P_PAR
PCI_RST_N	R11	PCI_P_RST_N

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Table 2-25 shows how the primary PCI bus interrupts are connected on ML410 platforms along with information for each device.

Table 2-25: **3.3V Primary PCI Bus Information**

Device Name	Dev. ID	Vend. ID	Bus	DEV	IDSEL	REQ	FPGA PCI CLK		PCI Interrupts on FPGA				
									A	B	C	D	ALI SBR
PCI Slot 5	N/A	N/A	0	5	AD21	0	0	PCI Device Interrupt	D	A	B	C	-
PCI Slot 3	N/A	N/A	0	6	AD22	1	1		C	D	A	B	-
U15, ALi SB	0x1533	0x10B9	0	2	AD18	3	3		-	-	-	-	(INT, NMI)
U15, ALi Pwr Mgt	0x7101	0x10B9	0	12	AD28	3	3		-	-	-	-	(INT, NMI)
U15, ALi IDE	0x5229	0x10B9	0	11	AD27	3	3		-	-	-	-	(INT, NMI)
U15, ALi Audio	0x5451	0x10B9	0	1	AD17	3	3		-	-	-	-	(INT, NMI)
U15, ALi Modem	0x5457	0x10B9	0	3	AD19	3	3		-	-	-	-	(INT, NMI)
U15, ALi USB#1	0x5237	0x10B9	0	15	AD31	3	3		-	-	-	-	(INT, NMI)
U15, ALi USB#2	0x5237	0x10B9	0	10	AD26	3	3		-	-	-	-	(INT, NMI)
U32, PCI-PCI Brg	0xAC23	0x104C	0	9	AD25	4	4		-	-	-	-	-
U37, FPGA	0x0410	0x10EE	0	8	AD24	Int.	5		-	-	-	-	-

Notes:

The PCI ALi South Bridge device uses a separate interrupt line that connects to the FPGA via schematic net SBR_INTR. Anytime an interrupt occurs within the ALi South Bridge, it generates an interrupt on schematic net SBR_INTR.

Table 2-26 shows how the secondary PCI bus interrupts are connected on ML410 platforms along with information for each device.

Table 2-26: **5V Secondary PCI Bus Information**

Device Name	Dev. ID	Vend. ID	Bus	DEV	IDSEL	REQ	Bridge CLK		PCI Interrupts on FPGA				
									A	B	C	D	ALI SBR
PCI Slot 6	N/A	N/A	1	2	AD18	0	0	PCI Dev. Intr.	B	C	D	A	-
PCI Slot 4	N/A	N/A	1	3	AD19	1	1		A	B	C	D	-
U32, PCI-PCI Brg	N/A	N/A	N/A	7	N/A	Int.	4		-	-	-	-	-

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ALi South Bridge Interface, M1535D+ (U15)

The ALi M1535D+ South Bridge Super I/O controller (Figure 2-18) augments the ML410 with many of the basic features found on legacy PCs. These basic PC features are only accessible over the PCI bus because this is the only way to access the ALI M1535D+. A brief description of the ALi M1535D+ features employed on ML410 platforms follows. Please review the ALi M1535D+ data sheet located on the ML410 documentation CD for more information.

ALi M1535D+ supports the following features:

- 1 parallel port
- 2 USB ports
- 2 IDE connectors
- GPIO
- SMBus interface
- AC'97 audio codec
- PS/2 keyboard and mouse

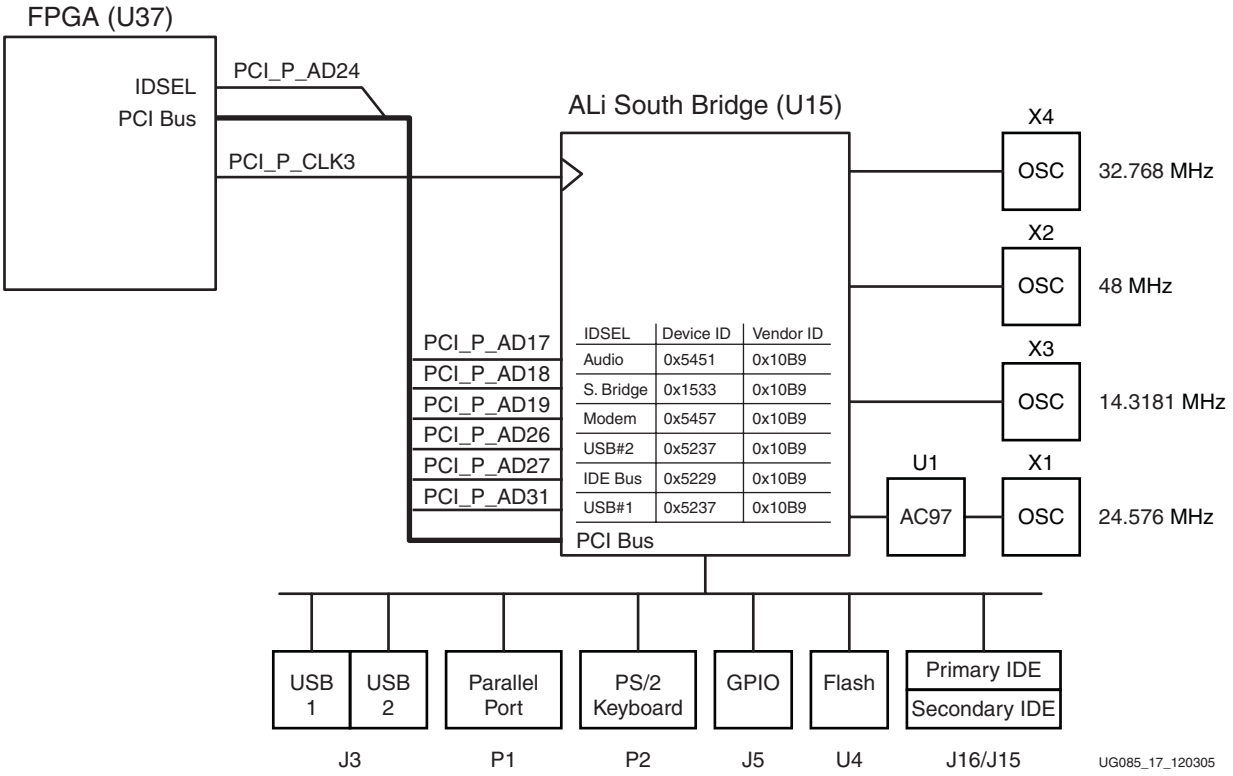

Figure 2-18: **ALi South Bridge Interface, M1535D+ (U15)**

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Parallel Port Interface Connector Assembly (P1)

The parallel port interface of the ALi South Bridge is connected to a 25-pin connector, female DB25, which is part of the P1 connector assembly. The ALi M1535D+ supports various parallel port modes such as *standard parallel port* (SPP), *enhanced parallel port* (EPP), and IEEE 1284 compatible ECP. The P1, female DB25, connector pinout is configured as per *IEEE Std. 1284-1994*.

Table 2-27 shows the ALi parallel port connections.

Table 2-27: **ALi South Bridge Parallel Port Connections**

Signal Name	DB25 Pin (P1)	Description
PP_STROBE_N	1	Strobe
PP_DATA0	2	Data Bit 0
PP_DATA1	3	Data Bit 1
PP_DATA2	4	Data Bit 2
PP_DATA3	5	Data Bit 3
PP_DATA4	6	Data Bit 4
PP_DATA5	7	Data Bit 5
PP_DATA6	8	Data Bit 6
PP_DATA7	9	Data Bit 7
PP_ACK_N	10	Acknowledge
PP_BUSY	11	Busy
PP_PEND	12	Paper End
PP_SELECT	13	Select
PP_AUTOFD_N	14	Autofeed
PP_ERROR_N	15	Error
PP_INIT_N	16	Initialize
PP_SLCTIN_N	17	Select In
GND	18, 19, 20, 21, 22, 23, 24, 25	Ground

USB Connector Assembly (J3)

The M1535D+ USB is an implementation of the *Universal Serial Bus Specification Version 1.0a* (see www.usb.org) that contains two PCI Host Controllers and an integrated Root Hub. The two USB connectors, A/B, are part of the J3 connector assembly and are USB Type-A plugs.

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Table 2-28 shows the ALi USB connections to the two USB Type-A plugs (J3).

Table 2-28: **ALi South Bridge Connections to USB Type-A**

Signal Name	A/B Pin (J3)	Description
USB_VCC	1	USB Power, 5V, MOSFET Isolated
USB0_DN/USB1_DN	2	USB Data -
USB0_DP/USB1_DP	3	USB Data +
GND	4	Ground

IDE Connectors (J15 and J16)

Supports a two-channel UltraDMA-133 IDE master controller independently connected to a primary 40-pin IDE connector (J16) and a secondary 40-pin IDE connector (J15).

Table 2-29 shows the ALi Primary and Secondary IDE connections.

Table 2-29: **ALi South Bridge IDE Connections**

IDE Primary Pin (J16)	Schematic Signal	IDE Secondary Pin (J15)	Schematic Signal
1	PIDE_RESET_N	1	SIDE_RESET_N
2	GND	2	GND
3	PIDE_D7	3	SIDE_D7
4	PIDE_D8	4	SIDE_D8
5	PIDE_D6	5	SIDE_D6
6	PIDE_D9	6	SIDE_D9
7	PIDE_D5	7	SIDE_D5
8	PIDE_D10	8	SIDE_D10
9	PIDE_D4	9	SIDE_D4
10	PIDE_D11	10	SIDE_D11
11	PIDE_D3	11	SIDE_D3
12	PIDE_D12	12	SIDE_D12
13	PIDE_D2	13	SIDE_D2
14	PIDE_D13	14	SIDE_D13
15	PIDE_D1	15	SIDE_D1
16	PIDE_D14	16	SIDE_D14
17	PIDE_D0	17	SIDE_D0
18	PIDE_D15	18	SIDE_D15
19	GND	19	GND
20	NC	20	NC
21	PIDE_DMARQ	21	SIDE_DMARQ

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Table 2-29: **ALi South Bridge IDE Connections *(Cont'd)***

IDE Primary Pin (J16)	Schematic Signal	IDE Secondary Pin (J15)	Schematic Signal
22	GND	22	GND
23	PIDE_DIOW_N	23	SIDE_DIOW_N
24	GND	24	GND
25	PIDE_DIOR	25	SIDE_DIOR
26	GND	26	GND
27	PIDE_IORDY	27	SIDE_IORDY
28	PIDE_CSEL	28	SIDE_CSEL
29	PIDE_DMACK_N	29	SIDE_DMACK_N
30	GND	30	GND
31	PIDE_INTRQ	31	SIDE_INTRQ
32	NC	32	NC
33	PIDE_A1	33	SIDE_A1
34	PIDE_PDIAG_N	34	SIDE_PDIAG_N
35	PIDE_A0	35	SIDE_A0
36	PIDE_A2	36	SIDE_A2
37	PIDE_CS1_N	37	SIDE_CS1_N
38	PIDE_CS3_N	38	SIDE_CS3_N
39	PIDE_DASP_N	39	SIDE_DASP_N
40	GND	40	GND

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GPIO Connector (J5)

There are 15 GPIO pins connecting the ALi M1535D+ to the 24-pin GPIO header (J5). These can be accessed through the ALi M1535D+ by way of the PCI bus. Table 2-30 shows the types and number of GPIO signals available to the user from the ALi South Bridge.

Table 2-30: **Type of GPIO Available on Header J5**

ALi GPIO Types	Number Available
Output	5
Input	4
Input/Output	6

Table 2-31 shows the connections from the ALi, M1535D+, GPIO signals available at the GPIO header (J5).

Table 2-31: **GPIO Connections on Header J5**

Schematic Net Name	GPIO Pin (J5)	M1535D+ (U15)	I/O Type
GPO_10	21	T3	Output
GPO_29	23	N17	Output
GPO_30	20	N18	Output
GPO_34	22	P18	Output
GPO_35	24	P19	Output
GPI_24	1	M17	Input
GPI_25	3	E9	Input
GPI_34	5	W7	Input
GPI_36	7	U8	Input
GPIO_0	9	Y3	Input/Output
GPIO_1	11	V4	Input/Output
GPIO_2	13	W4	Input/Output
GPIO_3	15	Y4	Input/Output
GPIO_22	17	U6	Input/Output
GPIO_23	19	U5	Input/Output

System Management Bus Controller

The SMBus host controller in the M1535D+ supports the ability to communicate with power-related devices using the SMBus protocol. It provides quick send byte/receive byte/ write byte/write word/read word/block read/block write command with clock synchronization function and 10-bit addressing ability. See "IIC/SMBus Interface," page 69 for more information regarding the devices that are connected to the SMBus.

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AC'97 Audio Interface

The ALi South Bridge Super I/O controller has a built-in audio interface that is combined with a standard audio codec (AC'97), LM4550. Available features include:

- AC'97 Codec 2.1 Specification compliant
- Codec variable sample rate support
- 32-voice hardware wave-table synthesis
- 32 independent DMA channels
- 3D positioning sound acceleration
- Legacy Sound Blaster compatible
- FM OPL3 emulation
- MIDI interpretation
- MIDI MPU-401 interface

ML410 platforms employ a National Semiconductor LM4550 audio codec (U1) combined with the ALi South Bridge AC'97 interface. This interface can be used to play and record audio. The LM4550 has left and right channel line inputs, left and right CD-ROM inputs, a microphone input, left and right channel line outputs, and an amplified headphone output suitable for driving an 8Ω load using the LM4880 (U2). The microphone input and right/left amplified outputs are easily accessible via two 2.5mm audio jacks on the J1 connector. The Line In and Line Out connections are accessible via two Berg headers (J2 and J31).

Table 2-32 describes the audio jacks available to the user on ML410 platforms.

Table 2-32: **Audio Jacks (J1, J2, and J31)**

Audio Jack	Signal Name	Description
J1 Top	AC_AMP_OUTR AC_AMP_OUTL	AC Amplified Output, right and left channels, driven by U2, LM4880
J1 Bottom	AC_MIC_IN	Microphone Input to U1, LM4550
J31	AC_LINE_OUTR AC_LINE_OUTL	AC Line Output, right and left channels, driven by U1, LM4550
J2	AC_LINE_INR AC_LINE_INL	AC Line Input, right and left channels, driven by U1, LM4550
J6	AC_CD_INR AC_CD_INL	AC CD Input, right and left channels, driven by U1, LM4550

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PS/2 Keyboard and Mouse Interface Connector (P2)

The ALi M1535D+ has a built-in PS2/AT keyboard and PS/2 mouse controller. The PS/2 keyboard and mouse ports are connected to the ALi M1535D+ through standard DIN connectors contained in the P2 connector assembly. In the event of a short circuit by the keyboard or mouse device, the 5V power provided to these devices is protected by a resettable fuse, F1.

Table 2-33 shows the PS/2 keyboard and mouse connections to the P2 connector assembly.

Table 2-33: **PS/2 Keyboard and Mouse**

Signal Name	PS2 Pin (P2)	Description
KDAT	1B	Keyboard data
KCLK	5B	Keyboard clock
MDAT	1C	Mouse data
MCLK	5C	Mouse clock
KVCC, MVCC	4B, 4C	Fuse protected power to keyboard and mouse

Flash ROM (U4)

The ALi South Bridge has a flash memory interface port that supports up to 4 Mb of flash memory. ML410 platforms provide connectivity to an AM29F040B 4 Mb (512 K x 8 bit) flash memory (U4) via the ALi M1535D+ ROM interface.

Table 2-34 shows the connections between the ALi M1535D+ (U15) ROM signals to the AM29F040B (U4) flash memory device.

Table 2-34: **ALi M1535D+ Flash Memory Interface**

Schematic Net Name	M1535D+ Pin (U15)	AM29F040B Pin (U4)	Description
ROM_WE_N	U14	7	Active-Low Write Enable
ROM_OE_N	T14	32	Active-Low Output Enable
ROM_D7	W19	29	Flash Data
ROM_D6	Y19	28	
ROM_D5	V20	27	
ROM_D4	W20	26	
ROM_D3	Y20	25	
ROM_D2	U18	23	
ROM_D1	U19	22	
ROM_D0	U20	21	
ROM_A18	T15	9	Flash Addresses
ROM_A17	U15	6	
ROM_A16	V15	10	
ROM_A15	W15	11	

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Table 2-34: **ALi M1535D+ Flash Memory Interface *(Cont'd)***

Schematic Net Name	M1535D+ Pin (U15)	AM29F040B Pin (U4)	Description
ROM_A14	T16	5	
ROM_A13	U16	4	
ROM_A12	V16	12	
ROM_A11	W16	1	
ROM_A10	Y16	31	
ROM_A9	R17	2	
ROM_A8	T17	3	
ROM_A7	U17	13	
ROM_A6	V17	14	
ROM_A5	W17	15	
ROM_A4	Y17	16	
ROM_A3	V18	17	
ROM_A2	W18	18	
ROM_A1	Y18	19	
ROM_A0	V19	20	

IIC/SMBus Interface

Introduction to IIC/SMBus

The Inter Integrated Circuit (IIC) bus provides the connection from the CPU to peripherals. It is a serial bus with a data signal, SDA, and a clock signal, SCL, both of which are bidirectional. The IIC/SMBus interface serves as an interface to one master device and multiple slave devices. The interface operates in the range of 100 kHz to 400 kHz.

The SMBus also provides connectivity from the CPU to peripherals. The SMBus is also a two wire serial bus through which simple power related devices can communicate with the rest of the system. SMBus uses IIC as its backbone. EDK provides IP that integrates the IIC interface with a microprocessor system. See the EDK *Processor IP User Guide* [Ref 2] for more details.

IIC/SMBus Signaling

The IIC bus data and clock signals operate as open-drain. By default, these signals are pulled High to 5V, although some devices support lower voltages. Either the master device or a slave device can drive either of the signals Low to transmit data or clock signals.

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IIC/SMBus on ML410 Platforms

Table 2-35 lists the function, part number, and addresses of the IIC devices on ML410 platforms. These devices include EEPROM, temperature sensors, power monitors, and a Real Time Clock.

Table 2-35: **IIC and SMBus Controller Connections**

UCF Signal Name	FPGA Pin (U37)	Schematic Signal Name
fpga_scl	E7	FPGA_SCL
fpga_sda	D7	FPGA_SDA
iic_irq_n	C9	IIC_IRQ_N
iic_therm_n(1)	C7	IIC_THERM_N

Notes:

1. This signal connects to U20 therm_l on the LM87. See data sheet for additional details.

Figure 2-19 shows a block diagram of the FPGA in relation to the SMBus accelerator and the IIC bus.

Note: Either the FPGA or the ALi M1535D+ can master the IIC bus, but not simultaneously.

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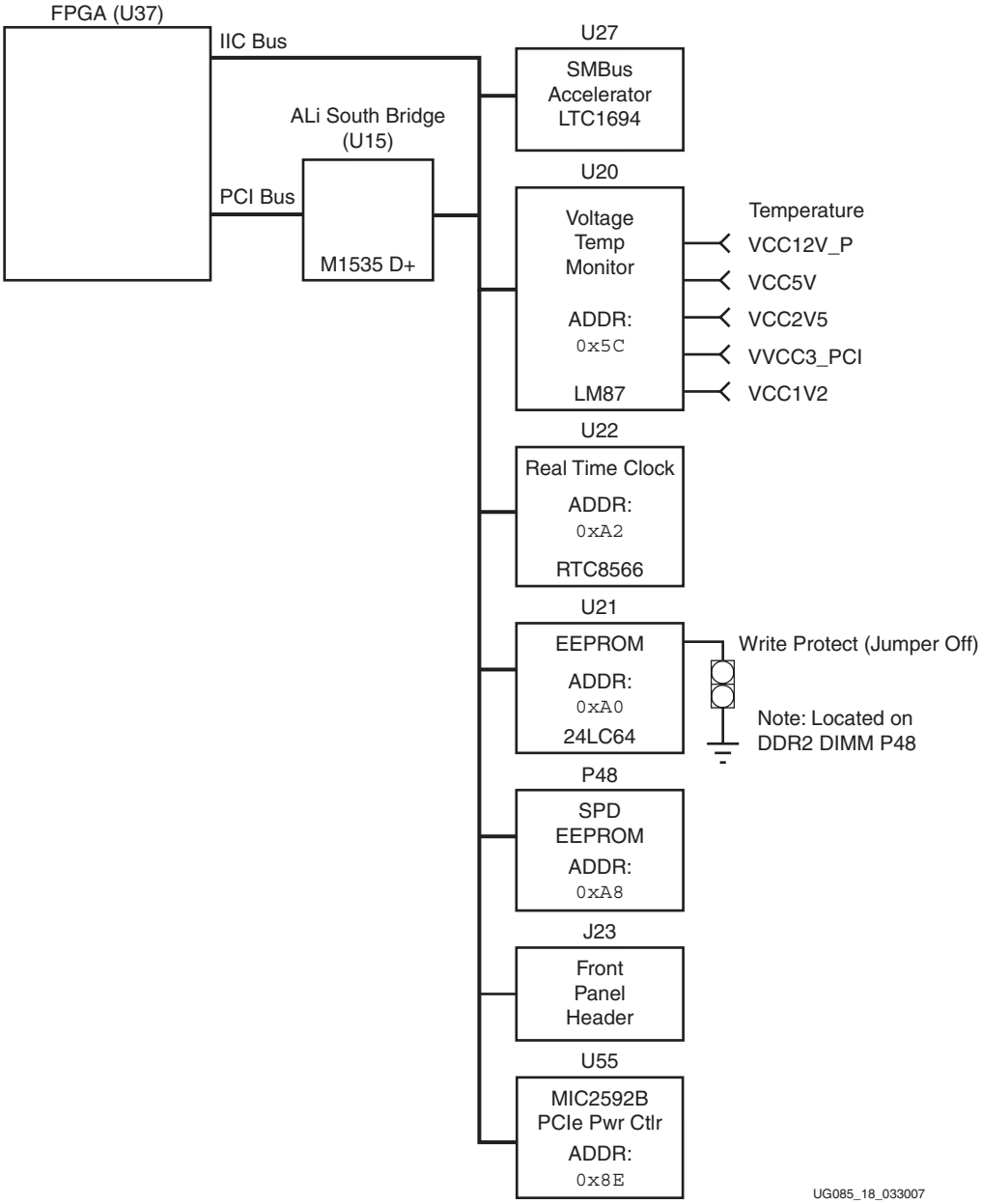

Figure 2-19: **IIC and SMBus Block Diagram**

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Table 2-36 lists the IIC devices and their associated addresses.

Table 2-36: **IIC Devices and Addresses**

Device	Reference Designator	Address	Description
LTC1694	U27	N/A	SMBus accelerator that ensures data integrity with multiple devices on the SMBus. Enhances data transmission speed and reliability under all specified SMBus loading conditions and is compatible with the IIC bus.
RTC8564	U22	0xA2	IIC bus interface Real Time Clock module along with an external rechargeable battery and charging circuit.
24LC64	U21	0xA0	64 kb electrically erasable PROM (EEPROM).
LM87	U20	0x5C	Voltage/temperature monitor.
MIC2592B	U55	0x8E	Dual-slot PCI Express power controller.
DDR2_DIMM	P48	0xA8 0x68	DDR2
Header	J23	N/A	Front panel header connectivity for expansion.

Notes:

1. The IIC bus can be controlled directly by the FPGA or indirectly by the ALi bridge over the FPGA PCI interface.

Serial Peripheral Interface

Serial Peripheral Interface™ (SPI) is a serial interface similar to the IIC bus interface. There are three primary differences: the SPI operates at a higher speed, there are separate transmit and receive data lines, and the device access is chip-select based instead of address based. EDK provides IP that integrates the SPI interface with a microprocessor system. See the EDK *Processor IP User Guide* [Ref 2] and the data sheet available on the ML410 documentation CD for more details.

SPI Signaling

There are four main signals used in the SPI interface; Clock, Data In, Data Out, and Chip Select. Signaling rates on the SPI bus range from 1 MHz to 3 MHz, roughly a factor of 10 faster than the IIC bus interface. SPI continues to differ from IIC using active drivers for driving the signal High and Low, while IIC only actively drives signals Low, relying on pull-up resistors to pull the signals High.

There are four basic signals on the SPI bus:

- **Master Out Slave In (MOSI):** A data line that supplies the output data from the master device that is shifted into a slave device
- **Master In Slave Out (MISO):** A data line that supplies the output data from a slave device that is shifted into the master device
- **Serial Clock (SCK):** A control line driven by the master device to regulate the flow of data and enable a master to transmit data at a variety of baud rates
  - The SCK line must cycle once for each data bit that is transmitted
- **Slave Select (SS):** A control line dedicated to a specific slave device that allows the master device to turn the slave device on and off

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SPI Addressing

The SPI does not use an addressed-based system like the IIC bus interface uses. Instead, devices are selected by dedicated Slave Select signals, comparable to a Chip Select signal. Each SPI slave device needs its own Slave Select signal driven from the SPI master. This increases the total pin count but decreases overhead and complexity, increasing the available bandwidth and decreasing bus contention.

ML410 platforms employ a 25LC640, 64 kb EEPROM SPI device. Figure 2-20 shows the FPGA and the EEPROM connected by the SPI bus.

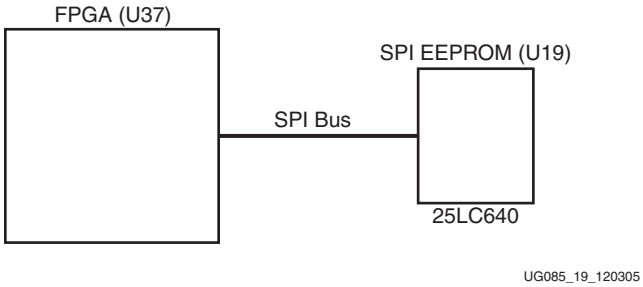

Figure 2-20: **SPI EEPROM Device Interface**

Table 2-37 shows the connections between the IIC/SMBus controller and the FPGA.

Table 2-37: **IIC and SMBus Controller Connections**

UCF Signal Name	FPGA Pin (U37)	Schematic Signal Name
SPI_DATA_OUT	AJ22	SPI_DATA_OUT
SPI_DATA_IN	AH22	SPI_DATA_IN
SPI_CLK	AF21	SPI_CLK
SPI_DATA_CS_N	AG22	SPI_DATA_CS_N

Serial ATA

ML410 platforms provide two Serial ATA (SATA) host port connections via J25 and J26. Each SATA host port connection provides AC-coupled connections to and from an MGT on the FPGA. A 300 MHz differential reference clock is provided for use with the SATA MGTs and logic used to support the SATA protocol. For more information, see the *Virtex-4 RocketIO MGT User Guide* [Ref 4].

Serial ATA Description

Serial ATA is the next generation of the ATA family of interfaces. Providing a higher throughput through a simpler and less expensive cable, Serial ATA maintains software compatibility with older ATA implementations.

FPGA to Serial ATA Connector

ML410 platforms that are equipped with RocketIO transceivers provide for operation as a Serial ATA host or device. The connection between the FPGA and the Serial ATA connector is fairly simple, involving only four wires per connector, as well as a few

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capacitors and resistors to AC-couple the signals. These connections are also shown in Table 2-38.

Table 2-38: **Connections Between FPGA and Serial ATA Connector (J25 and J26)**

Signal Name	FPGA Pin (U37)	Serial ATA Pin
RXNPADA	AP25	J26.3
RXPPADA	AP26	J26.2
TXNPADA	AP22	J26.5
TXPPADA	AP23	J26.6
RXNPADB	AP17	J25.3
RXPPADB	AP18	J25.2
TXNPADB	AP20	J25.5
TXPPADB	AP21	J25.6
SATACLK_Q0(1)	AP29	-
SATACLK_NQ0(1)	AP28	-

Notes:

1. 300 MHz

The Serial ATA connectors have different connections to the FPGA for transmit and receive differential pairs. The receive differential pair is connected by way of a 0.01µF capacitor to AC-couple the incoming signal to the FPGA. The transmit differential pair between the FPGA and the Serial ATA connector is connected by way of a 0Ω resistor. The resistor is a place holder to allow for AC-coupling if required at a future date.

Pushbuttons, Switches, Front Panel Interface, and Jumpers

Pushbuttons

System ACE Reset (SW1)

SW1 is a manual reset switch for the System ACE CF (U38) device. When SW1 is actuated, it drives the PB_SYSTEM_ACE_RESET signal Low, which causes the LTC1326 (U31) to generate a 100 µs active-Low pulse. The active-Low output from the LTC1326 drives the reset input of the System ACE CF controller (U38) through the SYSTEMACE_RESET_N signal. When the System ACE CF device is reset, it causes the FPGA to be reconfigured. The ACE file used to program the device is selected via SW3 DIP switch settings.

The front panel interface header (J23) can also drive the PB_SYSTEM_ACE_RESET signal. For more details on J23, see the "Front Panel Interface (J23)" section.

CPU Reset (SW2)

SW2 is a manual pushbutton reset switch for the PPC405 system implemented in the FPGA. To use this switch, the user must connect the PB_FPGA_CPU_RESET signal to the PPC405 system within the FPGA fabric. EDK provides IP to perform this task. See the EDK *Processor IP User Guide* [Ref 2] for more details.

If the SW2 switch is connected in the FPGA fabric, it drives the PB_FPGA_CPU_RESET signal Low when pushed, causing the LTC1326 (U30) to generate a 100 µs active-Low

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pulse. The active-Low output of the LTC1326 pin drives the FPGA_CPU_RESET_N signal connected to H7 on the FPGA.

In addition to resetting the CPU, SW2 can also perform a System ACE CF reset as described in "System ACE Reset (SW1)," page 74. This can be accomplished by simply holding down the SW2 pushbutton for longer than two seconds. This action performs a CPU reset followed by a System ACE CF reset. See the ML410 schematics and the LTC1236 data sheet on the ML410 documentation CD for more details.

The front panel interface header (J23) can also drive the PB_ FPGA_CPU_RESET signal. For more details on J23, please review the "Front Panel Interface (J23)" section.

FPGA Prog (SW4)

SW4 is a pushbutton switch for programming the FPGA.

PCI Express Clock Circuit Reset (SW5)

SW5 is a pushbutton switch that resets the PCI Express clock.

Power On/Off (SW7)

SW7 is a pushbutton power switch for the ATX power toggle circuit. Shorting pins 1 and 2 of jumper J19 allows the ATX power toggle circuit to control power on sequencing.

Switches

System ACE Configuration (SW3)

SW3 is a three position dual-inline package (DIP) switch that controls the three configuration address pins on the System ACE CF controller. The addresses, CFGADDR0, CFGADDR1, and CFGADDR2, are marked on SW3 as positions 1, 2, and 3 respectively. SW3 also has an ON indicator and directional arrow etched onto the plastic housing. An arrow appears on the board silkscreen, as well, to indicate the on position. When any of the three switches are moved to the ON position, the associated CFGADDR bit is set to a logic 0. When any of the three switches are moved opposite of the ON position (i.e., OFF), the associated CFGADDR bit is set to a logic 1 via a pull-up resistor.

Figure 2-21, page 76 shows the SW3 DIP switch connections to the System ACE device. One side of the DIP switch is tied to pull-up resistors that are connected to each of the CFGADDR lines while the other side of the DIP switch is connected to ground. The configuration address lines are also connected to the front panel interface. See the "Front Panel Interface (J23)" section for more details. This allows the user to manually select one of eight configurations stored on the CompactFlash card that is connected to the System ACE device. After the user makes a valid selection on SW3, the user can then depress pushbutton SW1 to command the System ACE device to reset and configure the FPGA using the configuration selected by DIP switch SW3. See the *System ACE CompactFlash Solution Data Sheet* [Ref 5] for more details.

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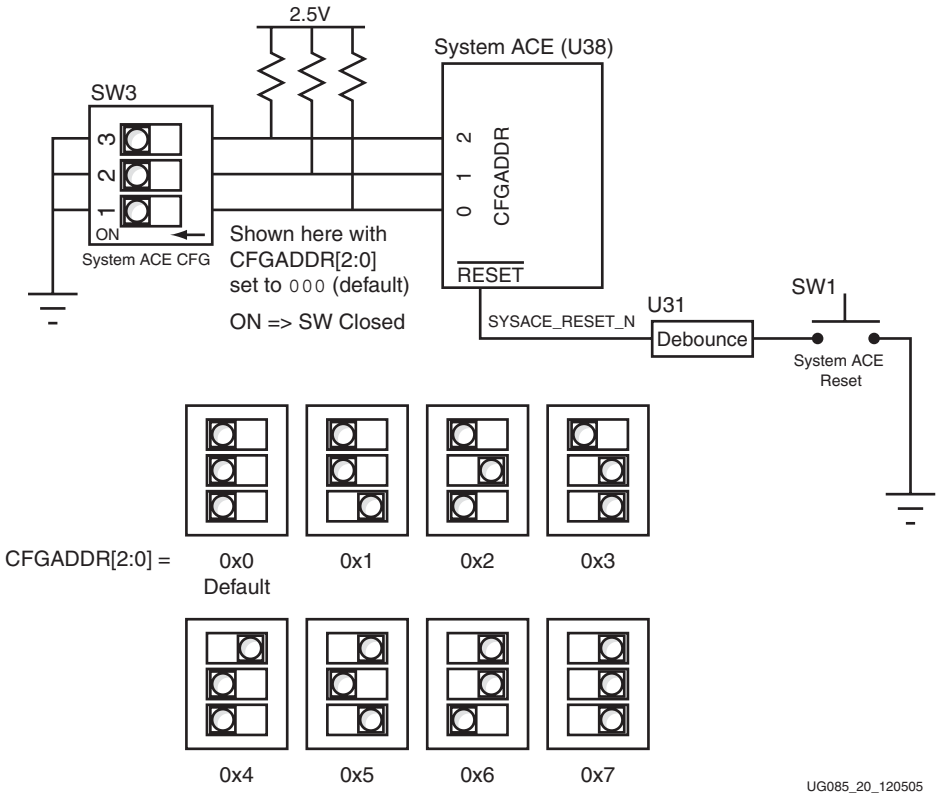

Figure 2-21: **SW3: System ACE Configuration Switch Detail**

MGT Clock Source Select (SW6)

SW6 is a three-position DIP switch that controls the select lines of the clock multiplexer at U6, as shown in Figure 2-3, page 27. When switches 1 and 2 are in the ON position, the associated SEL0 and SEL1 bits are set to a logic 1. When the switches are in the OFF position, the select lines are pulled down to ground (Logic 0). To control the select lines from the FPGA, switches 1 and 2 *must* be set to the open (OFF) position to prevent contention. Switch position 3 is not used. Table 2-39 shows the pinout for the select lines.

Table 2-39: **SW6 Output**

Signal Name	FPGA Pin (U37)	Description
CLK_SEL0	AG16	Select 0
CLK_SEL0	AG17	Select 1

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Table 2-40 shows the output combinations of the clock multiplexer.

Table 2-40: **Outputs of the Clock Multiplexer (U6)**

CLK_SEL0	CLK_SEL1	Q0	Q1
0	0	250 MHz MGTCLK sourced from X5	250 MHz SGMIICLK sourced from X5
0	1	250 MHz MGTCLK sourced from X5	SGMIICLK sourced from the MGT SMA connectors at J20 and J21
1	0	MGTCLK sourced from the MGT SMA connectors at J20 and J21	250 MHz SGMIICLK sourced from X5
1	1	MGTCLK sourced from the MGT SMA connectors at J20 and J21	SGMIICLK sourced from the MGT SMA connectors at J20 and J21

Front Panel Interface (J23)

The front panel interface connector (J23) is a 24-pin header that accepts a standard IDC 24 pin connector (0.1 inch pitch). J23 provides an optional means to control and gather status information from the ML410 if enclosed in a case similar to a desktop computer. The functionality listed below can easily be connected with a custom user-provided cable that connects to user logic designed to control and monitor the functionality available through the front panel interface.

The front panel interface provides the following control capability:

- Power ON | OFF the board
  - ML410 platforms are delivered with a jumper installed on J23
- Eight System ACE configuration selections
  - Connects to the three System ACE configuration address lines
- System ACE Reset
  - Active-Low input (pulsed)
- CPU Reset
  - Active-Low input (pulsed)

The front panel interface provides access to the following status information:

- FPGA configuration DONE output
- IDE disk access output
- ATX power output
- Two FPGA user-defined output signals
- ATX speaker output
- Keyboard inhibit input (active-Low)

Note: All front panel interface outputs, except for the speaker out, can drive LEDs.

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Table 2-41 shows the signals available at the front panel interface header (J23).

Table 2-41: **Front Panel Interface Connector (J23)**

J23 Pin	Schematic Signal	Description
1	SYACE_CFGA0	Used to select System ACE configuration, CFGADDR0
2	FPGA_LED_USER1	User defined function, connects to the FPGA, U37-G15, (2.5V bank)
3	SYACE_CFGA1	Used to select System ACE configuration, CFGADDR1
4	FPGA_LED_USER2	User defined function, connects to the FPGA, U37-G16, (2.5V bank)
5	SYACE_CFGA2	Used to select System ACE configuration, CFGADDR2
6	NC	No Connect
7	LED_DONE_R	Remote FPGA DONE indicator; tie this pin to anode of user's LED and cathode to ground
8	GND	Ground
9	ATX_PWRLED	ATX 3.3V power indicator; tie this pin to anode of user's LED and cathode to ground
10	ATX_SPKR	Used to drive user-provided ATX speaker
11	SCL	IIC bus
12	SCA	IIC bus
13	GND	Ground
14	GND	Ground
15	KBINH	Tie this pin to ground to activate Keyboard Inhibit (See ALi M1536D+ data sheet for more details)
16	VCC5V	5V ATX power available to user
17	ATX_IDELED_R	ATX IDE access indicator; tie this pin to anode of user's LED and cathode to ground
18	VCC5V	5V ATX power available to user
19	GND	Ground
20	ATX_PWR_TOG	ATX power toggle
21	PB_SYSACE_RESET	Used to reset System ACE when driven Low, as described in "System ACE Reset (SW1)"
22	GND	Ground
23	PB_FPGA_CPU_RESET	Used to reset CPU when driven Low, as described in "CPU Reset (SW2)"
24	GND	Ground

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Jumpers

Note: Pins should only be jumpered with the board powered off.

5V Fan (J8)

Table 2-42 shows the pinout of the 5V fan.

Table 2-42: **5V Fan BERG Header Connections**

J8 Pin	Description
1	+5V
2	Ground

Power Supply On (J19)

Jumper J19 selects the power supply options. Shorting pins 1 and 2 allows the ATX power toggle circuit to control power on sequencing achieved by toggling SW7. Shorting pins 2 and 3 allows the ATX power supply AC switch to control power-on sequencing of the board.

JTAG Source Select (J27)

The JTAG source select jumper (J27) enables the use of either the PC4 JTAG connector (J9) or the CPU JTAG (J12) *and* FPGA JTAG/TRACE (P8) to source the FPGA JTAG pins. This is available for third-party tool support. The multiplexing is performed by an external device, 74LVC157A (U39), as shown in Figure 2-11.

Note: To avoid contention after the FPGA is configured, this functionality should not be used if logic that also drives the CPU JTAG connector (J12) or the FPGA JTAG/TRACE connector (P8) is implemented.

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I/O Voltage Margining (J24, J29, and J37)

The voltage margins on the board can be adjusted by shorting the jumpers as shown in Table 2-43. Apply shorting jumpers only when the board is powered off. For more on voltage regulation, see "ATX Power Distribution and Voltage Regulation."

Table 2-43: **Voltage Margining Jumper Settings**

Voltage Regulator	Inhibit Jumper(1)	Margin Jumper	Description
VR1	J30	J34	To adjust the 2.5V supply: • Equal to or greater than –5% margining, short pins 1–2 on J34 • Equal to or greater than +5% margining, short pins 2–3 on J34 • No margining, leave pins open on J34
VR2	J34	J29	To adjust the 1.2V supply: • Equal to or greater than –5% margining, short pins 1–2 on J29 • Equal to or greater than +5% margining, short pins 2–3 • No margining, leave pins open
VR3	J35	J37	To adjust the 2.0V supply: • Equal to or greater than –5% margining, short pins 1–2 • Equal to or greater than +5% margining, short pins 2–3 • No margining, leave pins open

Notes:

1. Inhibit jumpers are open by default at nominal voltage.

ATX Power Distribution and Voltage Regulation

ML410 platforms are shipped with a commercially available 250W ATX power supply. All voltages required by the ML410 logic devices are derived from the 5V supply, except the ±12V supplies, as shown in Figure 2-22. The ATX power supply can be easily mounted in a standard ATX chassis along with the ML410 board.

The ATX power supply is a Sparkle Power Inc. model FSP250-60PLN. The *Sparkle User's Manual* is provided in the data sheet section on the ML410 documentation CD. The Sparkle power supply supports a full range input to automatically accommodate a wide range of voltage/frequency standards, such as 115V for North America, Japan, and others, and 230V for most European countries. See the *Sparkle User's Manual* for more information.

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The different logic devices used on the ML410 platforms require a variety of voltages. Voltage levels are derived from the 5V supply and regulated on the board as shown in Figure 2-22.

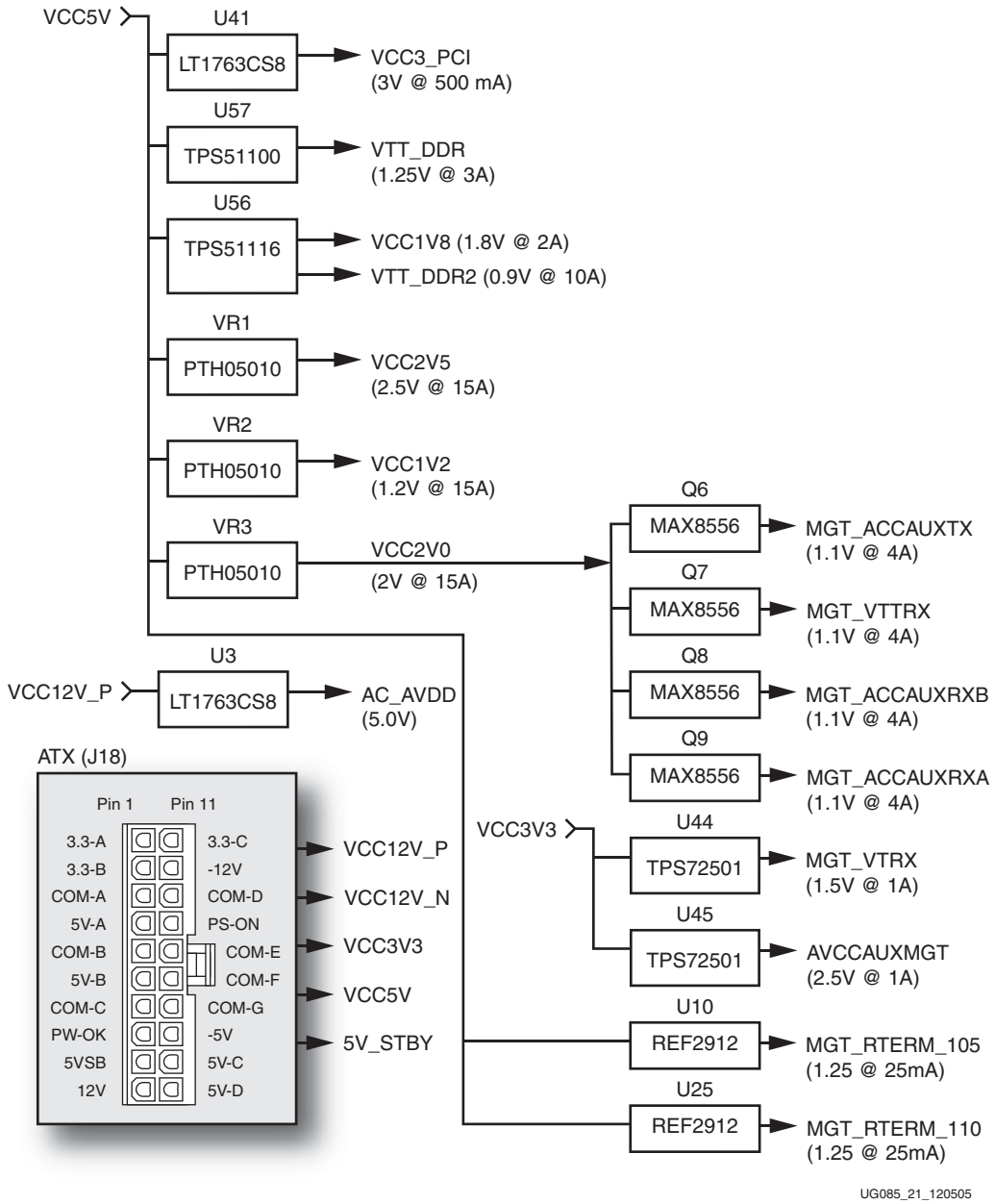

Figure 2-22: **ATX Power Distribution and Voltage Regulation**

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Voltage monitors connected to power indicator LEDs monitor the regulated power on the board (see Figure 2-23). The indicator LEDs illuminate red if a regulated supply voltage is out of spec, and illuminate green if the regulated supply voltage is nominal. Each regulated supply voltage has a corresponding test point located near its indicator LED. See the ML410 schematics and the associated data sheets for more information.

In addition to the voltage monitors, the ML410 employs a SMBus device, LM87, which samples several of the same supply voltages when accessed over the System Management Bus. See the "IIC/SMBus Interface" section for more information.

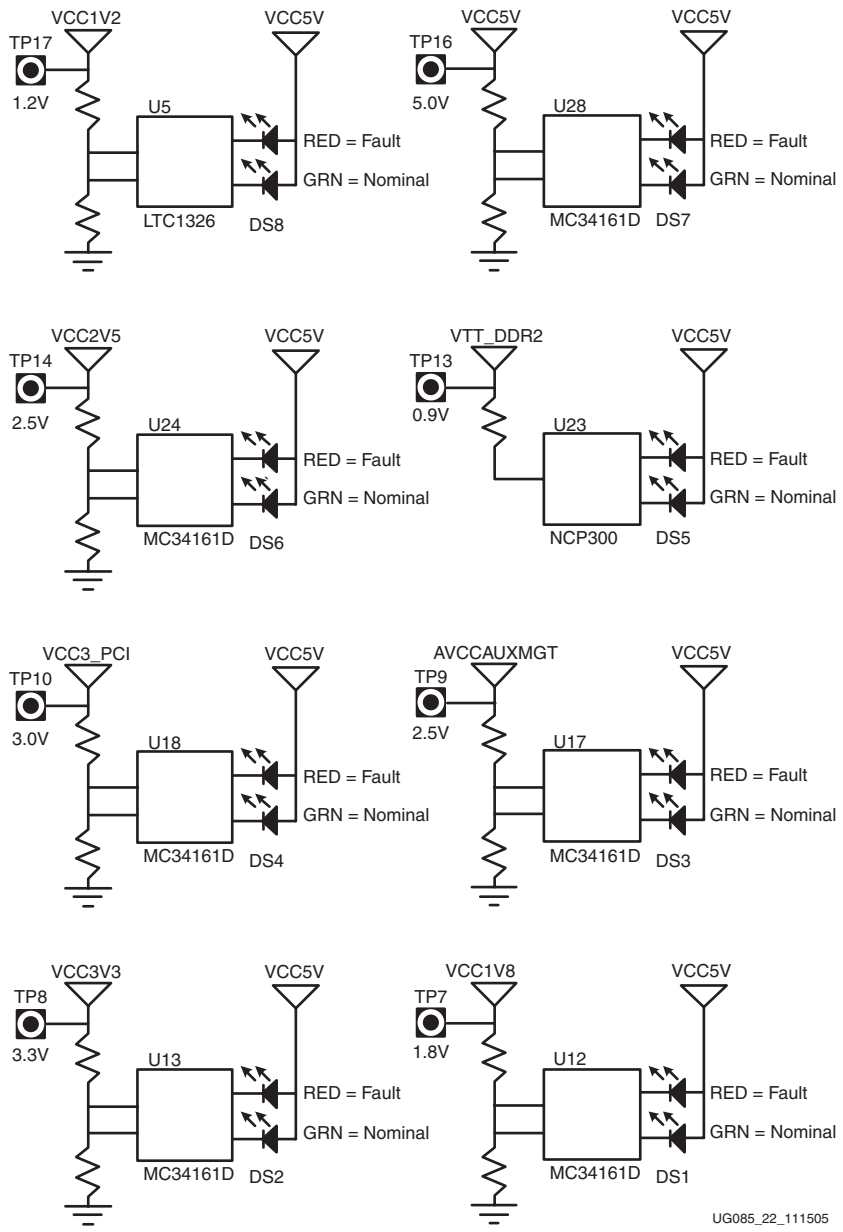

Figure 2-23: **Voltage Monitors**

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Table 2-44 shows the various voltage monitor information.

Table 2-44: **Voltage Monitor Information**

Schematic Net Name	Voltage	Test Point	Indicator LED(1)	Description
VCC1V2	1.2V	TP17	DS8	Regulated FPGA core voltage
VCC1V8	1.8V	TP7	DS1	Regulated DDR2 power
VCC2V5	2.5V	TP14	DS6	Regulated FPGA/board logic and DDR power
VCC3_PCI	3.0V	TP10	DS4	Regulated FPGA PCI bank 1-2 voltage
VCC3V3	3.3V	TP8	DS2	Regulated PCI and other logic
VCC5V	5V	TP16	DS7	From ATX power supply, all regulators derive power
VTT_DDR2	0.9V	TP13	DS5	Regulated DDR2 termination (SSTL18)
VTTDDR	1.25V			Regulated DDR termination (SSTL2)
AVCCAUXMGT	2.5V	TP9	DS3	Regulated MGT power
VCC12V_P	+12V	TP18	N/A	Direct from ATX power supply
VCC12V_N	–12V	TP19	N/A	Direct from ATX power supply

Notes:

1. Green LED = Voltage Nominal; Red LED = Voltage Fault

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High-Speed I/O

The ML410 platform's high-speed I/O is based on the RocketIO transceiver and LVDS capability of Virtex-4 FX FPGAs. Although revision E platforms provide access to the RocketIO MGTs, the ML410 series is only intended for embedded processor development, not MGT characterization. The ML42*x* series of Virtex-4 FX RocketIO characterization platforms is designed for characterizing MGTs.

The high-speed I/O signals on the FPGA are accessible through two personality module (PM) connectors, referred to as Personality Module 1 and Personality Module 2, on the ML410 platforms. The PM connectors are Tyco Z-Dok+ docking connectors. See the 1367550-5 data sheet at Tyco's website (www.z-dok.com).

The ML410 is the host board, functioning as the development platform for the Virtex-4 FX FPGA. The PM connectors on the ML410 platforms provide a means for extending the functionality of the board through high-speed I/O pins.

Figure 2-24 shows an example of a personality module connected to an embedded development platform (an ML310 in this example). The plug, located on the embedded development platform, is referred to as the *host board connector*; the receptacle, located on the personality module, is referred to as the *adapter board connector*.

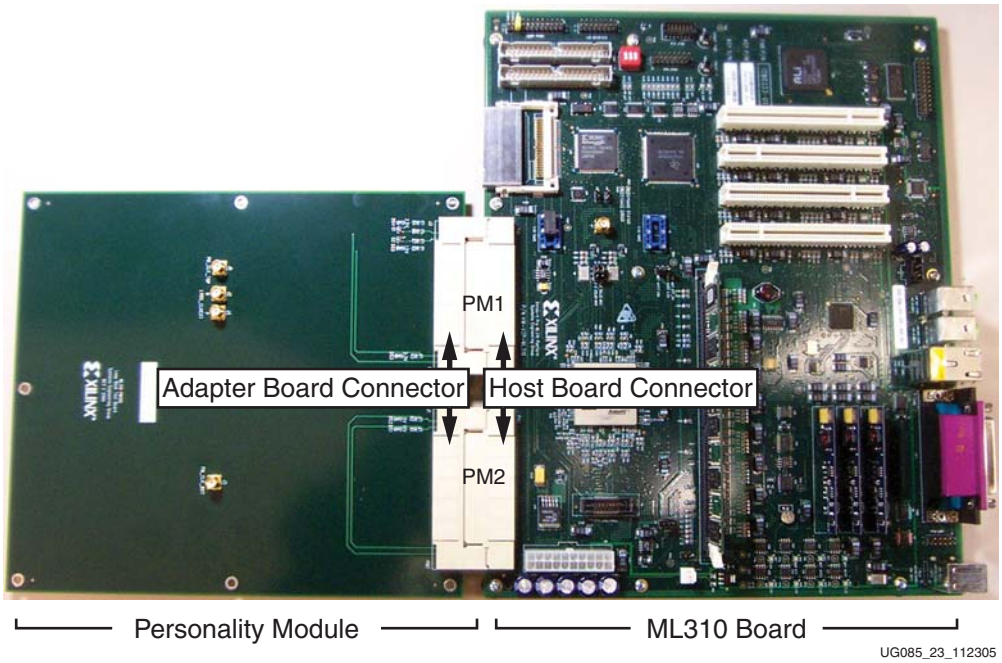

Figure 2-24: **Personality Module Connected to Embedded Development Platform**

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Personality Module Connectors

Figure 2-25 shows an edge view of the PM host board connectors.

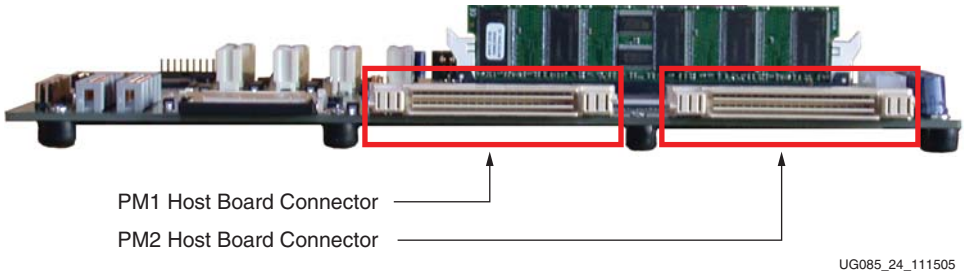

Figure 2-25: **Edge View of Host Board Connectors**

Each signal pair on the PM1 and PM2 host board connectors has a wide ground pin on the opposite side of the plastic divider, as shown in Figure 2-26. The signal pairs alternate from side to side along the length of the divider. All of the B and E pins are grounded on the ML410. The A, C, D, and F pins are signal pins.

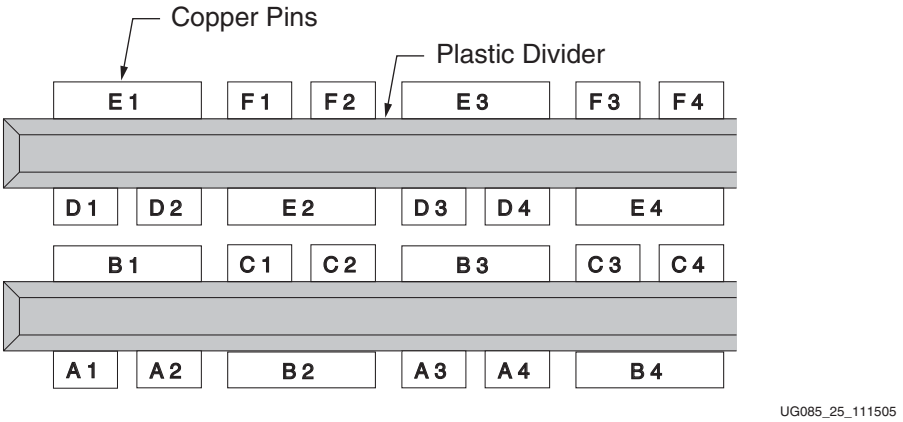

Figure 2-26: **Host Board Connector Pin Detail**

Z-Dok+ Connector Offsets

The Z-Dok+ connectors provide four rows of signals pairs. Each row has a particular propagation delay through a mated pair of connectors (Table 2-45).

Table 2-45: **Delay Offsets**

ZDOK+ Connector	Connector Propagation Delay	Physical Length
Row A	145.2 ps	830 mils
Row C	196.8 ps	1125 mils
Row D	213.3 ps	1219 mils
Row F	264.8 ps	1513 mils

Notes:

1. Propagation delay, i.e., the delay when traversing through the host board connector and the adapter board connector, was calculated assuming 175 ps/inch. Propagation delay is the total between each male and female connector pair.

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All signals with length matching requirements, MGT and LVDS pairs, must include an offset to account for the Z-Dok+ propagation delays. The ML410 platforms account for one-half of the offset, while a user-designed adapter board must account for the other half. The relative offsets for the ML410 host board PM connector are included in Table 2-46. Users are required to compensate for these offsets when designing adapter boards.

Table 2-46: **Relative Offsets from the FPGA to the PM1 and PM2 Connectors**

ZDOK+ Connector	Difference	Offset	Offset/2[1]
Row A	F – A = 1513 – 830	683	342
Row C	F – C = 1513 – 1125	389	194
Row D	F – D = 1513 – 1219	294	147
Row F	F – F = 0 – 0	0	0

Notes:

1. All offsets are normalized to row F. The ML410 design is based on the data in the Offset/2 column.

PM1 Connector

The PM1 connector provides the following signals:

- 8 RocketIO 3.125 Gb/s transceivers
- 3 LVDS pairs at 2.5V (can be used as 6 single-ended I/O at 2.5V)
- 1 LVDS clock pair at 2.5V
- 12 single- ended I/O at 2.5V
- 26 single-ended I/O at 3.3V
- 1 single-ended clock at 2.5V
- 1 pin not connected

PM2 Connector

The PM2 connector on provides the following signals:

- 39 LVDS pairs at 2.5V (can be used as 78 single-ended I/O at 2.5V)
- 1 single-ended clock at 2.5V
- 1 pin not connected

Adapter Board PM Connectors

Tyco Z-Dok+ adapter board connectors (part number 1367555-1) are the receptacle connectors on the personality modules that mate to the ML410 host board connectors. See the 1367555-1 data sheet at Tyco's website (www.z-dok.com).

On the adapter board connectors, located on the personality module, each signal pair has a pair of ground pins on the opposite side of the open space, as shown in Figure 2-27, page 87. The signal pairs alternate from side to side along the length of the open space. All of the B and E pins are two contacts tied together and grounded on the personality module. The A, C, D, and F pins are signal pins.

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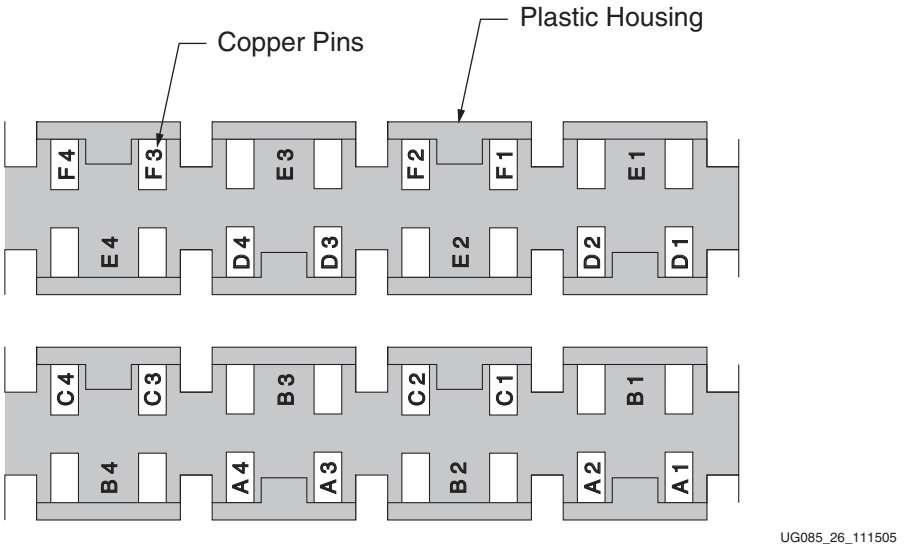

Figure 2-27: **Adapter Board Connector Pin Detail**

Z-DOK+ Utility Pins

Figure 2-28 shows the Z-DOK+ utility pins and numbering for the host board PM connector.

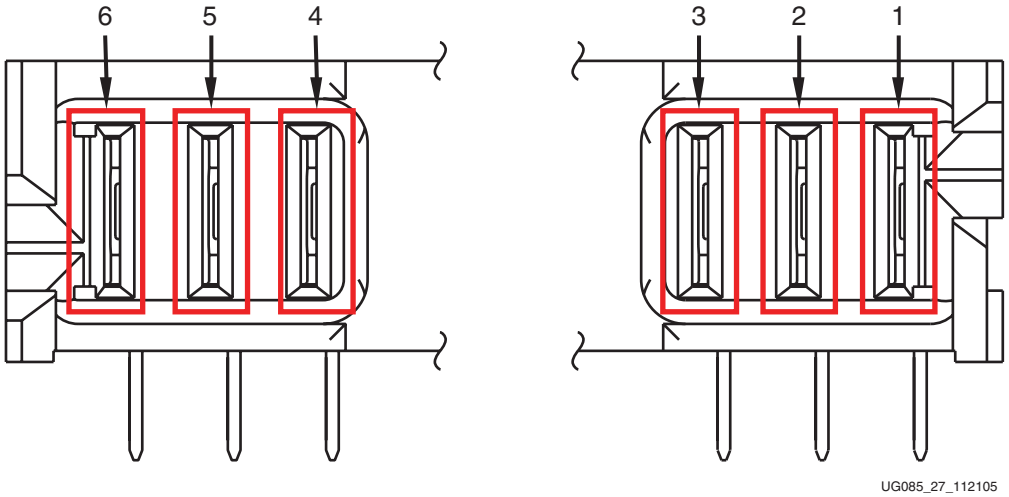

Figure 2-28: **Z-DOK+ Utility Pins (ML410 Side)**

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Figure 2-29 shows the Z-DOK+ utility pins and numbering for the adapter board connector.

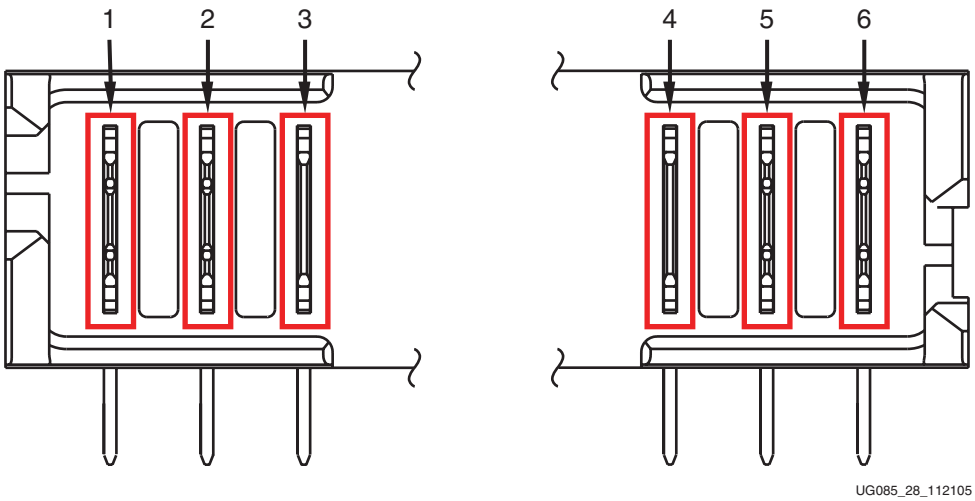

Figure 2-29: **Z-DOK+ Utility Pins (Adapter Side)**

Note: The pins on the adapter board connector are at varying heights, as shown in Table 2-47 and Table 2-48, page 89.

Contact Order

The Z-Dok+ power and ground pins contact in the following order:

- 1 and 6;
- then 2 and 5;
- then 3 and 4

PM1 Power and Ground

Table 2-47 shows the power and ground pins for the PM1 connector on the ML410.

Table 2-47: **PM1 Power and Ground Pins**

Pin Number	Description	Length	Contact Order
1, 6	Ground	Level 4	First
2, 5	2.5V	Level 3	Second
3	3.3V	Level 2	Third
4	1.2V	Level 2	Third

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PM User I/O Pins

PM1 User I/O

The PM1 connector makes the MGT signals from the eight RocketIO transceivers available to the user, along with LVDS pairs and single-ended signals. Table 2-48 shows the pinout for the PM1 connector.

Table 2-48: **PM1 Pinout**

PM1 Pin	FPGA Pin (U37)	Pin Description	ML410 Schematic Net	FPGA Bank V_{CCO}	Pin Function
A1	AL9	IO_L10P_8	PM_IO_94	2.5V	Single-ended 50Ω impedance
A2	AK9	IO_L10N_8	PM_IO_95	2.5V	Single-ended 50Ω impedance
A3	AD14	IO_L7P_8	PM_IO_86	2.5V	Single-ended 50Ω impedance
A4	AC13	IO_L7N_8	PM_IO_87	2.5V	Single-ended 50Ω impedance
A5	AA8	IO_L13N_12	PM_IO_3V_25	3V	Single-ended 50Ω impedance
A6	AA9	IO_L13P_12	PM_IO_3V_18	3V	Single-ended 50Ω impedance
A7	Y6	IO_L10N_12	PM_IO_3V_7	3V	Single-ended 50Ω impedance
A8	AA6	IO_L10P_12	PM_IO_3V_22	3V	Single-ended 50Ω impedance
A9	AL3	IO_L26N_12	PM_IO_3V_9	3V	Single-ended 50Ω impedance
A10	AM3	IO_L26P_12	PM_IO_3V_13	3V	Single-ended 50Ω impedance
A11	AK14	IO_L31P_8	PM_IO_82	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A12	AL14	IO_L31N_8	PM_IO_83	2.5V	
A13	F1	RXPPADB_113	RXPPADB_110		MGT RX pair received by host FPGA
A14	G1	RXNPADB_113	RXNPADB_110		
A15	AL1	RXPPADB_110	RXPPADB_110		MGT RX pair received by host FPGA
A16	AM1	RXNPADB_110	RXNPADB_110		
A17	U1	TXPPADB_112	TXPPADB_112		MGT TX pair driven by host FPGA
A18	V1	TXNPADB_112	TXNPADB_112		
A19	AP11	TXPPADB_109	TXPPADB_109		MGT TX pair driven by host FPGA
A20	AP12	TXNPADB_109	TXNPADB_109		
C1	AB11	IO_L1P_8	PM_IO_90	2.5V	Single-ended 50Ω impedance
C2	AA11	IO_L1N_8	PM_IO_91	2.5V	Single-ended 50Ω impedance
C3	AC3	IO_L14N_12	PM_IO_3V_16	3V	Single-ended 50Ω impedance
C4	AC4	IO_L14P_12	PM_IO_3V_12	3V	Single-ended 50Ω impedance
C5	Y9	IO_L12N_VREF_12	PM_IO_3V_1	3V	Single-ended 50Ω impedance
C6	W9	IO_L12P_12	PM_IO_3V_3	3V	Single-ended 50Ω impedance
C7	AG7	IO_L27N_12	PM_IO_3V_17	3V	Single-ended 50Ω impedance

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Table 2-48: **PM1 Pinout *(Cont'd)***

PM1 Pin	FPGA Pin (U37)	Pin Description	ML410 Schematic Net	FPGA Bank V_{CCO}	Pin Function
C8	AG8	IO_L27P_12	PM_IO_3V_5	3V	Single-ended 50Ω impedance
C9	AF15	IO_L17P_8	PM_IO_80	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C10	AG15	IO_L17N_8	PM_IO_81	2.5V	
C11	AB5	IO_L7N_12	PM_IO_3V_19	3V	Single-ended 50Ω impedance
C12	AC5	IO_L7P_12	PM_IO_3V_24	3V	Single-ended 50Ω impedance
C13	A7	RXPPADA_113	RXPPADA_113		MGT RX pair received by host FPGA
C14	A6	RXNPADA_113	RXNPADA_113		
C15	AC1	RXPPADA_110	RXPPADA_110		MGT RX pair received by host FPGA
C16	AD1	RXNPADA_110	RXNPADA_110		
C17	R1	TXPPADA_112	TXPPADA_112		MGT TX pair driven by host FPGA
C18	T1	TXNPADA_112	TXNPADA_112		
C19	AP9	TXPPADA_109	TXPPADA_109		MGT TX pair driven by host FPGA
C20	AP10	TXNPADA_109	TXNPADA_109		
D1	AC12	IO_L5P_8	PM_IO_92	2.5V	Single-ended 50Ω impedance
D2	AB12	IO_L5N_8	PM_IO_93	2.5V	Single-ended 50Ω impedance
D3	AE14	IO_L13P_8	PM_IO_84	2.5V	Single-ended 50Ω impedance
D4	AF14	IO_L13N_8	PM_IO_85	2.5V	Single-ended 50Ω impedance
D5	Y7	IO_L5N_12	PM_IO_3V_21	3V	Single-ended 50Ω impedance
D6	Y8	IO_L5P_12	PM_IO_3V_20	3V	Single-ended 50Ω impedance
D7	AA4	IO_L3N_12	PM_IO_3V_8	3V	Single-ended 50Ω impedance
D8	AA5	IO_L3P_12	PM_IO_3V_6	3V	Single-ended 50Ω impedance
D9	W4	IO_L1N_12	PM_IO_3V_2	3V	Single-ended 50Ω impedance
D10	W5	IO_L1P_12	PM_IO_3V_14	3V	Single-ended 50Ω impedance
D11	AH15	IO_L21P_8	PM_IO_78	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D12	AJ15	IO_L21N_8	PM_IO_79	2.5V	
D13	D1	TXNPADB_113	TXNPADB_113		MGT TX pair driven by host FPGA
D14	C1	TXPPADB_113	TXPPADB_113		
D15	AJ1	TXNPADB_110	TXNPADB_110		MGT TX pair driven by host FPGA
D16	AH1	TXPPADB_110	TXPPADB_110		
D17	AA1	RXNPADB_112	RXNPADB_112		MGT RX pair received by host FPGA
D18	Y1	RXPPADB_112	RXPPADB_112		

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Table 2-48: **PM1 Pinout *(Cont'd)***

PM1 Pin	FPGA Pin (U37)	Pin Description	ML410 Schematic Net	FPGA Bank V_{CCO}	Pin Function
D19	AP15	RXNPADB_109	RXNPADB_109		MGT RX pair received by host FPGA
D20	AP14	RXPPADB_109	RXPPADB_109		
F1	AB13	IO_L3P_8	PM_IO_88	2.5V	Single-ended 50Ω impedance
F2	AA13	IO_L3N_8	PM_IO_89	2.5V	Single-ended 50Ω impedance
F3	Y3	IO_L6N_12	PM_IO_3V_10	3V	Single-ended 50Ω impedance
F4	Y4	IO_L6P_12	PM_IO_3V_4	3V	Single-ended 50Ω impedance
F5	W6	IO_L4N_VREF_12	PM_IO_3V_15	3V	Single-ended 50Ω impedance
F6	W7	IO_L4P_12	PM_IO_3V_0	3V	Single-ended 50Ω impedance
F7	V7	IO_L2N_12	PM_IO_3V_23	3V	Single-ended 50Ω impedance
F8	V8	IO_L2P_12	PM_IO_3V_11	3V	Single-ended 50Ω impedance
F9	K16	IO_L2P_GC_VRN_LC_3	PM_CLK_TOP	2.5V	Clock
F10	NC	NC	NC	NC	No Connect
F11	K1	MGTCLK_N_113	LVDS_CLKEXT_N	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F12	J1	MGTCLK_P_113	LVDS_CLKEXT_P	2.5V	
F13	A3	TXNPADA_113	TXNPADA_113		MGT TX pair driven by host FPGA
F14	A4	TXPPADA_113	TXPPADA_113		
F15	AG1	TXNPADA_110	TXNPADA_110		MGT TX pair driven by host FPGA
F16	AF1	TXPPADA_110	TXPPADA_110		
F17	N1	RXNPADA_112	RXNPADA_112		MGT RX pair received by host FPGA
F18	M1	RXPPADA_112	RXPPADA_112		
F19	AP7	RXNPADA_109	RXNPADA_109		MGT RX pair received by host FPGA
F20	AP6	RXPPADA_109	RXPPADA_109		

PM2 User I/O

The PM2 connector makes most of the LVDS pairs available to the user, along with single-ended signals. Table 2-49 shows the pinout for the PM2 connector on the ML410.

Table 2-49: **PM2 Pinout**

PM2 Pin	FPGA Pin (U37)	Pin Description	ML410 Schematic Net	FPGA Bank VCCO	Pin Function
A1	AJ10	IO_L18N_8	PM_IO_63	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A2	AH10	IO_L18P_8	PM_IO_62	2.5V	

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Table 2-49: **PM2 Pinout *(Cont'd)***

PM2 Pin	FPGA Pin (U37)	Pin Description	ML410 Schematic Net	FPGA Bank VCCO	Pin Function
A3	AM12	IO_L30N_8	PM_IO_67	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A4	AM13	IO_L30P_8	PM_IO_66	2.5V	
A5	AH9	IO_L14N_8	PM_IO_55	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A6	AJ9	IO_L14P_8	PM_IO_54	2.5V	
A7	AL23	IO_L14N_7	PM_IO_51	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A8	AM23	IO_L14P_7	PM_IO_50	2.5V	
A9	AM11	IO_L22N_8	PM_IO_45	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A10	AL11	IO_L22P_8	PM_IO_44	2.5V	
A11	AD11	IO_L11P_8	PM_IO_72	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A12	AE11	IO_L11N_8	PM_IO_73	2.5V	
A13	AF9	IO_L28P_8	PM_IO_28	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A14	AE9	IO_L28N_VREF_8	PM_IO_29	2.5V	
A15	AF23	IO_L20P_7	PM_IO_22	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A16	AE23	IO_L20N_VREF_7	PM_IO_23	2.5V	
A17	AM28	IO_L13N_7	PM_IO_32	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A18	AM27	IO_L13P_7	PM_IO_33	2.5V	
A19	AM32	IO_L3P_7	PM_IO_0	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A20	AM31	IO_L3N_7	PM_IO_1	2.5V	
C1	AM21	IO_L10N_7	PM_IO_53	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C2	AM22	IO_L10P_7	PM_IO_52	2.5V	
C3	AF13	IO_L15N_8	PM_IO_61	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C4	AE13	IO_L15P_8	PM_IO_60	2.5V	
C5	AJ25	IO_L32N_SMI_7	PM_IO_39	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C6	AJ26	IO_L32P_SMI_7	PM_IO_38	2.5V	
C7	AK22	IO_L16N_7	PM_IO_49	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C8	AK23	IO_L16P_7	PM_IO_48	2.5V	
C9	AK32	IO_L1P_7	PM_IO_74	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C10	AK31	IO_L1N_7	PM_IO_75	2.5V	

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Table 2-49: **PM2 Pinout *(Cont'd)***

PM2 Pin	FPGA Pin (U37)	Pin Description	ML410 Schematic Net	FPGA Bank VCCO	Pin Function
A3	AM12	IO_L30N_8	PM_IO_67	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A4	AM13	IO_L30P_8	PM_IO_66	2.5V	
A5	AH9	IO_L14N_8	PM_IO_55	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A6	AJ9	IO_L14P_8	PM_IO_54	2.5V	
A7	AL23	IO_L14N_7	PM_IO_51	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A8	AM23	IO_L14P_7	PM_IO_50	2.5V	
A9	AM11	IO_L22N_8	PM_IO_45	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A10	AL11	IO_L22P_8	PM_IO_44	2.5V	
A11	AD11	IO_L11P_8	PM_IO_72	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A12	AE11	IO_L11N_8	PM_IO_73	2.5V	
A13	AF9	IO_L28P_8	PM_IO_28	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A14	AE9	IO_L28N_VREF_8	PM_IO_29	2.5V	
A15	AF23	IO_L20P_7	PM_IO_22	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A16	AE23	IO_L20N_VREF_7	PM_IO_23	2.5V	
A17	AM28	IO_L13N_7	PM_IO_32	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A18	AM27	IO_L13P_7	PM_IO_33	2.5V	
A19	AM32	IO_L3P_7	PM_IO_0	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
A20	AM31	IO_L3N_7	PM_IO_1	2.5V	
C1	AM21	IO_L10N_7	PM_IO_53	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C2	AM22	IO_L10P_7	PM_IO_52	2.5V	
C3	AF13	IO_L15N_8	PM_IO_61	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C4	AE13	IO_L15P_8	PM_IO_60	2.5V	
C5	AJ25	IO_L32N_SMI_7	PM_IO_39	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C6	AJ26	IO_L32P_SMI_7	PM_IO_38	2.5V	
C7	AK22	IO_L16N_7	PM_IO_49	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C8	AK23	IO_L16P_7	PM_IO_48	2.5V	
C9	AK32	IO_L1P_7	PM_IO_74	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C10	AK31	IO_L1N_7	PM_IO_75	2.5V	

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Table 2-49: **PM2 Pinout *(Cont'd)***

PM2 Pin	FPGA Pin (U37)	Pin Description	ML410 Schematic Net	FPGA Bank VCCO	Pin Function
C11	AE22	IO_L12P_7	PM_IO_20	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C12	AD22	IO_L12N_VREF_7	PM_IO_21	2.5V	
C13	AL26	IO_L30P_SM3_7	PM_IO_34	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C14	AM26	IO_L30N_SM3_7	PM_IO_35	2.5V	
C15	AE27	IO_L21P_7	PM_IO_14	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C16	AE26	IO_L21N_7	PM_IO_15	2.5V	
C17	AM30	IO_L7P_7	PM_IO_4	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C18	AL29	IO_L7N_7	PM_IO_5	2.5V	
C19	AH29	IO_L11P_7	PM_IO_8	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
C20	AH28	IO_L11N_7	PM_IO_9	2.5V	
D1	AH12	IO_L29N_8	PM_IO_71	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D2	AG12	IO_L29P_8	PM_IO_70	2.5V	
D3	AK12	IO_L26N_8	PM_IO_69	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D4	AJ12	IO_L26P_8	PM_IO_68	2.5V	
D5	AL18	IO_L2N_7	PM_IO_59	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D6	AL19	IO_L2P_7	PM_IO_58	2.5V	
D7	AG23	IO_L18N_7	PM_IO_43	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D8	AH23	IO_L18P_7	PM_IO_42	2.5V	
D9	AL20	IO_L6N_7	PM_IO_57	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D10	AM20	IO_L6P_7	PM_IO_56	2.5V	
D11	AJ16	IO_L19P_8	PM_IO_76	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D12	AK16	IO_L19N_8	PM_IO_77	2.5V	
D13	AF26	IO_L27P_SM5_7	PM_IO_26	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D14	AG26	IO_L27N_SM5_7	PM_IO_27	2.5V	
D15	AF25	IO_L31P_SM2_7	PM_IO_24	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D16	AF24	IO_L31N_SM2_7	PM_IO_25	2.5V	
D17	AG28	IO_L17P_7	PM_IO_10	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D18	AG27	IO_L17N_7	PM_IO_11	2.5V	

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Table 2-49: **PM2 Pinout *(Cont'd)***

PM2 Pin	FPGA Pin (U37)	Pin Description	ML410 Schematic Net	FPGA Bank VCCO	Pin Function
D19	AE28	IO_L19P_7	PM_IO_12	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
D20	AF28	IO_L19N_7	PM_IO_13	2.5V	
F1	AH25	IO_L29N_SM4_7	PM_IO_41	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F2	AG25	IO_L29P_SM4_7	PM_IO_40	2.5V	
F3	AL13	IO_L32N_8	PM_IO_65	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F4	AK13	IO_L32P_8	PM_IO_64	2.5V	
F5	AK24	IO_L22N_7	PM_IO_47	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F6	AL24	IO_L22P_7	PM_IO_46	2.5V	
F7	AM25	IO_L26N_SM6_7	PM_IO_37	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F8	AL25	IO_L26P_SM6_7	PM_IO_36	2.5V	
F9	NC	NC	NC	2.5V	No Connect
F10	AD21	IO_L1P_GC_LC_4	PM_CLK_BOT	2.5V	Clock
F11	AL10	IO_L16P_8	PM_IO_6	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F12	AM10	IO_L16N_8	PM_IO_7	2.5V	
F13	AK28	IO_L15P_7	PM_IO_30	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F14	AL28	IO_L15N_7	PM_IO_31	2.5V	
F15	AC23	IO_L4P_7	PM_IO_18	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F16	AC22	IO_L4N_VREF_7	PM_IO_19	2.5V	
F17	AL31	IO_L5P_7	PM_IO_2	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F18	AL30	IO_L5N_7	PM_IO_3	2.5V	
F19	AD24	IO_L28P_7	PM_IO_16	2.5V	LVDS pair 100Ω differential impedance; can also be used as single-ended
F20	AE24	IO_L28N_VREF_7	PM_IO_17	2.5V	

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Appendix A

Board Revisions

This appendix describes the major differences in revisions of the ML410 platform. Table A-1 shows the features unique to each ML410 platform.

Table A-1: **Platforms, Devices, and Features**

Feature	Board Rev. C ML410-P(1)	Board Rev. D ML410-P(1)	Board Rev. E ML410(1)	Board Rev. E ML410(1)
Virtex-4 FX FPGA	XC4VFX60-CES1-FF1152	XC4VFX60-CES4-FF1152(2)	XC4VFX60-CES4S-FFG1152(2)	XC4VFX60-C-FFG115
RoHS-compliant	No	No	Yes	Yes
PCI Express slots with 16x physical connectors		One 4x slot One 1x slot	One 4x slot One 1x slot	One 4x slot One 1x slot
Serial ATA connectors		2	2	2
RocketIO transceivers		8	8	8
Ethernet PHYs	PHY address[4:0]=`0b00000` • MII/RGMII (Top RJ-45)	PHY address [4:0]=`0b00111` • MII/RGMII (Top RJ-45) • SGMII (Bottom RJ-45)	PHY address=`0b00111` • MII/RGMII (Top RJ-45) • SGMII (Bottom RJ-45)	PHY address=`0b00111` • MII/RGMII (Top RJ-45) • SGMII (Bottom RJ-45)
SGMII MGT Clock(3)		125 MHz	250 MHz	250 MHz
SATA MGT Clock(4)		150 MHz	300 MHz	300 MHz

Notes:

1. Board revision markings are located in the corner of the board near the gold Xilinx logo.
2. ML410-P Rev. D boards with CES4 devices support up to 3.125 Gb/s RocketIO transceiver interfaces, while Rev. E boards with CES4S devices upport up to 6.5 Gb/s. Refer to the Virtex-4 Errata for more details regarding Virtex-4 FX silicon errata.
3. See Virtex-4 Errata regarding FX GT11 jitter and AR23392 regarding Virtex-4 FX GT11 jitter errata for SGMII. Refer to Figure A-1, page 98 for more details regarding clock distribution on Rev. C and Rev. D boards.
4. See Virtex-4 Errata regarding FX GT11 jitter. Refer to Figure A-1, page 98 for more details regarding clock distribution on Rev. C and Rev. D boards.

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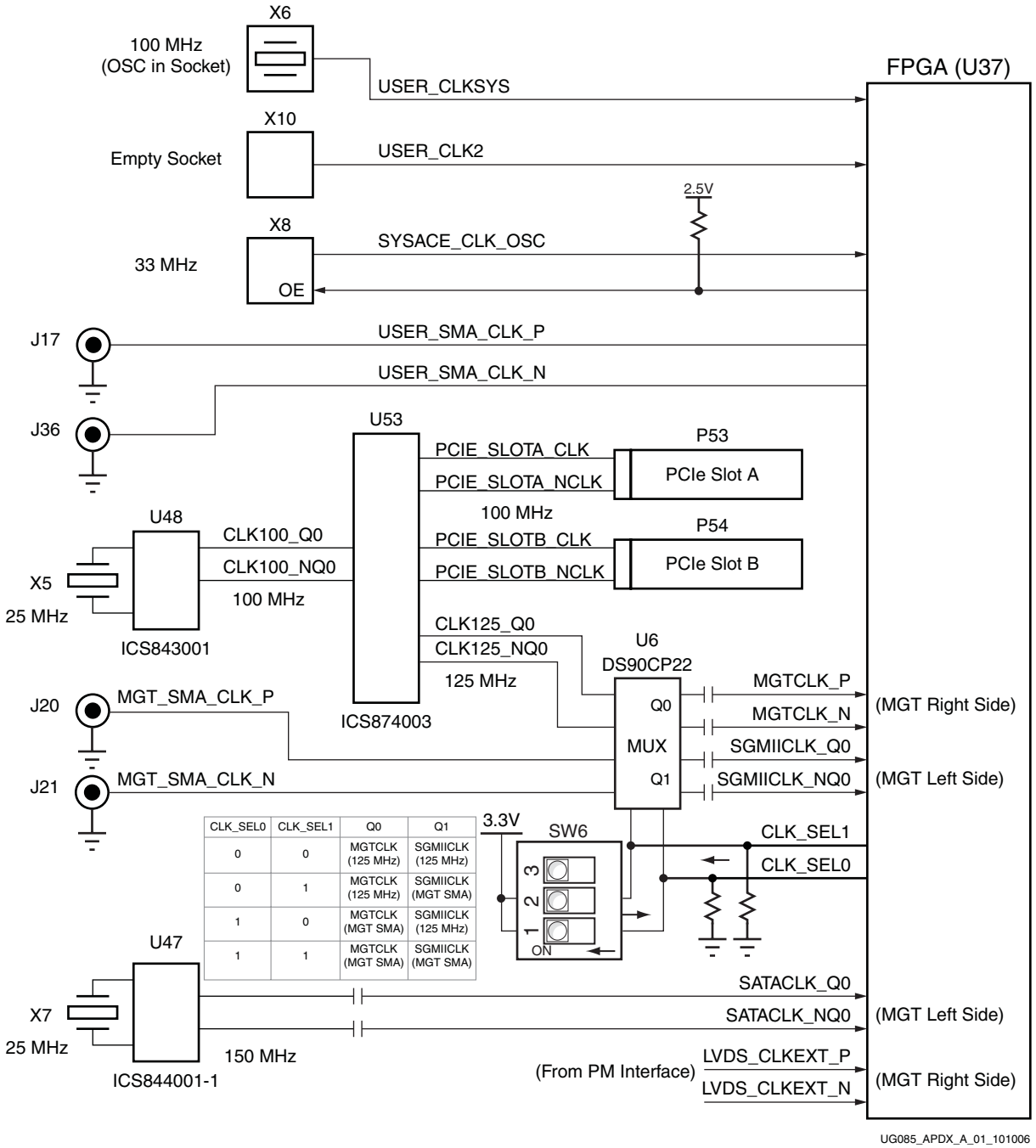
The MGT and SATA clock generation and distribution for earlier board revisions (Figure A-1) differs from revision E (Figure 2-3, page 27).



CLK_SEL0	CLK_SEL1	Q0	Q1
0	0	MGTCLK (125 MHz)	SGMIICLK (125 MHz)
0	1	MGTCLK (125 MHz)	SGMIICLK (MGT SMA)
1	0	MGTCLK (MGT SMA)	SGMIICLK (125 MHz)
1	1	MGTCLK (MGT SMA)	SGMIICLK (MGT SMA)

Figure A-1: **Clock Distribution for Revisions C and D**

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Table A-2 describes the MGT and SATA clock connections for earlier board revisions.

Table A-2: **MGT and SATA Clock Connections for Revisions C and D**

Schematic Net Name	Clock Source	FPGA Pin (U37)	Description[1]
SGMIICLK_Q0	(Fixed)	M34	SMA or onboard 125 MHz clock source selectable through SW6.
SGMIICLK_NQ0	(Fixed)	N34	SMA or onboard 125 MHz clock source selectable through SW6.
MGTCLK_P_110	(Fixed)	AP3	SMA or onboard 125 MHz clock source selectable through SW6.
MGTCLK_N_110	(Fixed)	AP4	SMA or onboard 125 MHz clock source selectable through SW6.
SATACLK_Q0	(Fixed)	AP29	150 MHz Serial ATA clock.
SATACLK_NQ0	(Fixed)	AP28	150 MHz Serial ATA clock.

Notes:

5. These clocks are differential pairs through the RocketIO transceivers and are not available on ML410-P boards. See Figure A-1, page 98.

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Appendix B

References

1. UG018, *PowerPC 405 Processor Block Reference Guide*
2. *Processor IP User Guide*
   www.xilinx.com/ise/embedded/proc_ip_ref_guide.pdf
3. DS302, *Virtex-4 Data Sheet*
4. UG076, *Virtex-4 RocketIO Transceiver User Guide*
5. DS080, *System ACE CompactFlash Solution.*
6. UG070, *Virtex-4 User Guide*
7. UG074, *Virtex-4 Embedded Tri-Mode Ethernet MAC User Guide*

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