Xilinx Personality Module (XPM) Interface Specification

For RocketIO MGT and LVDS Access

UG142 (v1.1) April 26, 2006



www.BDTIC.com/XILINX



Xilinx is disclosing this Specification to you solely for use in the development of designs to operate on Xilinx FPGAs. Except as stated herein, none of the Specification may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx. Any unauthorized use of this Specification may violate copyright laws, trademark laws, the laws of privacy and publicity, and communications regulations and statutes.

Xilinx does not assume any liability arising out of the application or use of the Specification; nor does Xilinx convey any license under its patents, copyrights, or any rights of others. You are responsible for obtaining any rights you may require for your use or implementation of the Specification. Xilinx reserves the right to make changes, at any time, to the Specification as deemed desirable in the sole discretion of Xilinx. Xilinx assumes no obligation to correct any errors contained herein or to advise you of any correction if such be made. Xilinx will not assume any liability for the accuracy or correctness of any engineering or technical support or assistance provided to you in connection with the Specification.

THE SPECIFICATION IS PROVIDED "AS IS" WITH ALL FAULTS, AND THE ENTIRE RISK AS TO ITS FUNCTION AND IMPLEMENTATION IS WITH YOU. YOU ACKNOWLEDGE AND AGREE THAT YOU HAVE NOT RELIED ON ANY ORAL OR WRITTEN INFORMATION OR ADVICE, WHETHER GIVEN BY XILINX, OR ITS AGENTS OR EMPLOYEES. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE SPECIFICATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

IN NO EVENT WILL XILINX BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOST DATA AND LOST PROFITS, ARISING FROM OR RELATING TO YOUR USE OF THE SPECIFICATION, EVEN IF YOU HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. THE TOTAL CUMULATIVE LIABILITY OF XILINX IN CONNECTION WITH YOUR USE OF THE SPECIFICATION, WHETHER IN CONTRACT OR TORT OR OTHERWISE, WILL IN NO EVENT EXCEED THE AMOUNT OF FEES PAID BY YOU TO XILINX HEREUNDER FOR USE OF THE SPECIFICATION. YOU ACKNOWLEDGE THAT THE FEES, IF ANY, REFLECT THE ALLOCATION OF RISK SET FORTH IN THIS AGREEMENT AND THAT XILINX WOULD NOT MAKE AVAILABLE THE SPECIFICATION TO YOU WITHOUT THESE LIMITATIONS OF LIABILITY.

The Specification is not designed or intended for use in the development of on-line control equipment in hazardous environments requiring fail-safe controls, such as in the operation of nuclear facilities, aircraft navigation or communications systems, air traffic control, life support, or weapons systems ("High-Risk Applications"). Xilinx specifically disclaims any express or implied warranties of fitness for such High-Risk Applications. You represent that use of the Specification in such High-Risk Applications is fully at your risk.

© 2004-2006 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

Revision History

Date	Version	Revision
09/28/04	1.0	Initial Xilinx release.
10/04/04	1.0.1	Minor non-technical edits. Corrected TOC.
01/14/05	1.0.2	Corrected typos in Table 2-6, page 22.
04/26/06	1.1	Minor edits throughout. Updated Table 2-5, page 19 and Table 2-6, page 22.

The following table shows the revision history for this document.

Table of Contents

Preface: About This Guide

Guide Contents	5
Additional Resources	5
Conventions	6
Typographical	6
Online Document	7

1 Introduction

1.1	verview
1.2	-Dok Personality Module Connectors 10
1.3	ost Board Connectors
	1.3.0.1 Connector 1
	1.3.0.2 Connector 2 13
1.4	dapter Board Connectors 14
1.5	elated Documents 14

2 Signal Definitions

2.1	Z-Dok+ Connector Pin Overview	15 15
	2.1.1.1 Z-Dok+ Connector Offsets	16 17
2.2	Z-DOK+ Utility Pins	17
	2.2.1 Contact Order 2.2.2 PM1 Power and Ground	18 18
	2.2.3 PM2 Power and Ground	19
2.3	Host Board User I/O Pins	19
	2.3.1 PM1 User I/O	19
	2.3.2 PM2 User I/O	22

3 Mechanical Specification

3.1	Personality Module Dimensions	25
3.2	PCB Layout for Host Board Connector	26
3.3	PCB Layout for Adapter Board Connector	26



Preface

About This Guide

This document provides the specifications for designing customized personality modules for Xilinx Embedded Development Platforms that are equipped with personality module interface connectors.

Guide Contents

This manual contains the following chapters:

- Section 1, "Introduction," provides an overview of the host board and the personality module as adapter board
- Section 2, "Signal Definitions," defines the signals of the XPM connectors
- Section 3, "Mechanical Specification," shows the dimensions for personality modules and the XPM connectors

Additional Resources

For additional information, go to http://www.xilinx.com/support/. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL	
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging	
	http://www.xilinx.com/support/techsup/tutorials/index.htm	
Answer Browser	Database of Xilinx solution records	
	http://www.xilinx.com/xlnx/xil_ans_browser.jsp	
Application Notes	Descriptions of device-specific design techniques and approaches <u>http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?c</u> <u>ategory=Application+Notes</u>	
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging	
	http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp_	

Resource	Description/URL	
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues	
	http://www.xilinx.com/support/troubleshoot/psolvers.htm	
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment	
	http://www.xilinx.com/xlnx/xil_tt_home.jsp	

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays	speed grade: - 100
Courier bold	Literal commands that you enter in a syntactical statement	ngdbuild design_name
Helvetica bold	Commands that you select from a menu	$\textbf{File} \rightarrow \textbf{Open}$
	Keyboard shortcuts	Ctrl+C
	Variables in a syntax statement for which you must supply values	ngdbuild design_name
Italic font	References to other manuals	See the <i>Development System</i> <i>Reference Guide</i> for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus [7:0] , they are required.	ngdbuild [option_name] design_name
Braces { }	A list of items from which you must choose one or more	lowpwr ={on off}
Vertical bar	Separates items in a list of choices	lowpwr ={on off}



Convention	Meaning or Use	Example
Vertical ellipsis	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN'
Horizontal ellipsis	Repetitive material that has been omitted	allow block block_name loc1 loc2 locn;

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the <i>Virtex-II Handbook</i> .
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.



1 Introduction

1.1 Overview

Xilinx Personality Module (XPM) interface connectors provide users with access to the high-speed LVDS and RocketIO transceiver pins on Xilinx embedded development boards, thereby extending the functionality of these boards. This document defines the XPM interface connector signals and mechanical specifications for an add-on personality module.

Figure 1-1 is an example of a personality module connected to an ML310 Embedded Development Platform (the host board) through the XPM connectors. The plug is referred to as the *host board connector*. The receptacle, located on the personality module, is referred to as the *adapter board connector*.



Figure 1-1: Personality Module Connected to an Embedded Development Platform

1.2 Z-Dok Personality Module Connectors

Figure 1-2 shows a close-up view of the two XPM connectors on an ML310 host board.



Figure 1-2: XPM Connectors on the ML310 Board (Detail)

The connectors are Tyco Z-Dok+ docking connectors, similar to the Z-Dok plug and receptacle illustrated in Figure 1-3. In addition to having the differential pairs and shielding ground connections of Z-Dok connectors, Z-Dok+ connectors include added utility connections for power, ground, and sensing. Tyco Z-Dok+ high-speed connectors are rated to 6.25 Gb/s.



UG142_01_03_1000404

Figure 1-3: Z-Dok Connector, Plug and Receptacle Detail





Figure 1-4 is a detailed drawing showing the pin numbering for the Z-Dok+ connector. Zoom in for greater detail.

Figure 1-4: Z-Dok+ Connector Pin Numbering



Figure 1-5: Utility Pin (Detail)

1.3 Host Board Connectors

Figure 1-6 is a mechanical drawing of the host board connector.



Figure 1-6: Z-Dok+ Host Board Connector, Mechanical Drawing

Each host board is equipped with two XPM connectors. Each connector has 40 differential pairs and several power and ground pins. Together, the two XPM connectors support 158 high-speed I/O pins that can be user defined. The XPM signals include:

- 8 RocketIO MGT pairs (32 pins total)
- 42 LVDS pairs (can be used as 84 single-ended I/O at 2.5V)
- 1 LVDS clock pair
- 38 single-ended I/O
 - 12 at 2.5V
 - ◆ 26 at 3.3V
- 2 single-ended 2.5V clocks
- 2 pins not connected

For details on Z-Dok+ host board connectors, see the <u>1367550-5 data sheet</u> at Tyco's website (www.z-dok.com). For host board connector pinouts, see the user guide for the specific Xilinx embedded development platform you are using.

1.3.0.1 Connector 1

Connector 1 on the host board provides the following signals:

- 8 RocketIO 3.125 Gb/s MGTs
- 3 LVDS pairs at 2.5V (can be used as 6 single-ended I/O at 2.5V)
- 1 LVDS clock pair at 2.5V
- 12 single- ended I/O at 2.5V
- 26 single-ended I/O at 3.3V
- 1 single-ended clock at 2.5V
 Note: One pin not connected

1.3.0.2 Connector 2

Connector 2 on the host board provides the following signals:

- 39 LVDS pairs at 2.5V (can be used as 78 single-ended I/O at 2.5V)
- 1 single-ended clock at 2.5V *Note:* One pin not connected

XILINX®

1.4 Adapter Board Connectors

Figure 1-7 is a mechanical drawing of the Z-Dok+ adapter board connector. For details on the adapter board connectors, see the <u>1367555-1 data sheet</u> at Tyco's website (www.z-dok.com).



Figure 1-7: Z-Dok+ Adapter Board Connector, Mechanical Drawing

1.5 Related Documents

Visit the Xilinx website for documentation specific to the target FPGA family.

- For information on printed-circuit board (PCB) layout, refer to the RocketIO user guide
- For information on electrical characteristics, refer to the device data sheet
- For information on signal integrity, see the Xcell Journal online: http://www.xilinx.com/publications/xcellonline/xc_si49.htm
- For information and documentation on Xilinx Embedded Development Platforms, see http://www.xilinx.com/xob



2 Signal Definitions

2.1 Z-Dok+ Connector Pin Overview

2.1.1 Host Board Connector

Figure 2-1 shows an edge view of the host board connectors on an ML310 board.



Figure 2-1: Edge View of Host Board Connectors

Each signal pair on the host board connectors has a wide ground pin on the opposite side of the plastic divider, as shown in Figure 2-2. The signal pairs alternate from side to side along the length of the divider. All of the B and E pins are grounded on the ML310. The A, C, D, and F pins are signal pins.



Figure 2-2: Host Board Connector Pin Detail

2.1.1.1 Z-Dok+ Connector Offsets

The Z-Dok+ connectors used on the embedded development platforms provide four rows of signals pairs. Each row has a particular propagation delay through a mated pair of connectors as shown in Table 2-1.

ZDOK+ Connector	Connector Propagation Delay ⁽¹⁾	Physical Length
Row A	145.2 ps	830 mils
Row C	196.8 ps	1125 mils
Row D	213.3 ps	1219 mils
Row F	264.8 ps	1513 mils

Notes:

1. Propagation delay, i.e., the delay when traversing through the host board connector and the adapter board connector, was calculated assuming 175 ps/inch. Propagation delay is the total between each male and female connector pair.

All signals with length matching requirements, MGT and LVDS pairs, must include an offset to account for the Z-Dok+ propagation delays. Xilinx embedded development platforms account for one-half of the offset, while a user-designed adapter board must account for the other half. The relative offsets for the ML310 host board PM connector are included in Table 2-2. Users are required to compensate for these offsets when designing adapter boards.

ZDOK+ Connector	Difference	Offset	Offset/2
Row A	F-A = 1513 - 830	683	342
Row C	F-C = 1513 - 1125	389	194
Row D	F-D = 1513 - 1219	294	147
Row F	F-F = 0 - 0	0	0

Table 2-2: Relative Offsets from the FPGA to the PM1 and PM2 Connectors

Notes:

1. All offsets are normalized to row F. Xilinx host boards are designed based on the data in the Offset/2 column.



2.1.2 Adapter Board

On the adapter board connectors, located on the personality module, each signal pair has a pair of ground pins on the opposite side of the open space, as shown in Figure 2-3. The signal pairs alternate from side to side along the length of the open space. All of the B and E pins are two contacts tied together and grounded on the personality module. The A, C, D, and F pins are signal pins.



UG142_02_03_1000404

Figure 2-3: Adapter Board Connector Pin Detail

2.2 Z-DOK+ Utility Pins

Figure 2-4 shows the Z-DOK+ utility pins and numbering for the host board connector.



Figure 2-4: Z-DOK+ Utility Pins (Host Board Side)

Figure 2-5 shows the Z-DOK+ utility pins and numbering for the adapter board connector.



Figure 2-5: Z-DOK+ Utility Pins (Adapter Side)

Note: The pins on the adapter board connector are at varying heights, as shown in Table 2-3 and Table 2-4.

2.2.1 Contact Order

The Z-Dok+ power and ground pins contact in the following order:

- 1 and 6;
- then 2 and 5;
- then 3 and 4

2.2.2 PM1 Power and Ground

Table 2-3 shows the power and ground pins for the PM1 host board connector.

Table 2-3:PM1 Power and Ground Pins

Pin Number	Description	Length	Contact Order
1,6	Ground	Level 4	First
2, 5	2.5V	Level 3	Second
3	3.3V	Level 2	Third
4	FPGA Core Voltage ⁽¹⁾	Level 2	Third

Notes:

1. Pin 4 provides access to the host board FPGA core voltage. To maintain compatibility across different host boards, treat this pin as a no connect when designing personality modules. To ascertain the core voltage value of a specific board, refer to the applicable host board's documentation.



Table 2-4 shows the power and ground pins for the PM2 host board connector.

Pin Number	Description	Length	Contact Order
1,6	Ground	Level 4	First
2,5	5V	Level 3	Second
3,4	12V	Level 2	Third

Table 2-4: PM2 Power and Ground Pins

2.3 Host Board User I/O Pins

2.3.1 PM1 User I/O

The PM1 connector makes the MGT signals from the eight RocketIO transceivers available to the user, along with LVDS pairs and single-ended signals. Table 2-5 shows the pinout for the PM1 connector.

PM1 Pin	Pin Description	FPGA Bank V _{CCO}	Pin Function
A1	IO_PM1_A1	2.5V	Single-ended 50Ω impedance
A2	IO_PM1_A2	2.5V	Single-ended 50Ω impedance
A3	IO_PM1_A3	2.5V	Single-ended 50Ω impedance
A4	IO_PM1_A4	2.5V	Single-ended 50Ω impedance
A5	IO_PM1_A5	3V	Single-ended 50Ω impedance
A6	IO_PM1_A6	3V	Single-ended 50Ω impedance
A7	IO_PM1_A7	3V	Single-ended 50Ω impedance
A8	IO_PM1_A8	3V	Single-ended 50Ω impedance
A9	IO_PM1_A9	3V	Single-ended 50Ω impedance
A10	IO_PM1_A10	3V	Single-ended 50Ω impedance
A11	IO_PM1_A11_P	2.5V	LVDS pair 100Ω differential impedance;
A12	IO_PM1_A12_N	2.5V	can also be used as single-ended
A13	RX_PM1_A13_P		MCT RX pair received by best EPC A
A14	RX_PM1_A14_N		NGT IX pair received by nost 11 GA
A15	RX_PM1_A15_P		MCT PX pair received by best EPC A
A16	RX_PM1_A16_N		NGT IX pail received by host FFGA
A17	TX_PM1_A17_P		MCT TY pair driven by best EPC A
A18	TX_PM1_A18_N		NGT TX pair unven by host FFGA

Table 2-5: PM1 Pinout

XILINX[®]

PM1 Pin	Pin Description	FPGA Bank V _{CCO}	Pin Function
A19	TX_PM1_A19_P		
A20	TX_PM1_A20_N		MG1 1X pair driven by host FPGA
C1	IO_PM1_C1	2.5V	Single-ended 50 Ω impedance
C2	IO_PM1_C2	2.5V	Single-ended 50 Ω impedance
C3	IO_PM1_C3	3V	Single-ended 50 Ω impedance
C4	IO_PM1_C4	3V	Single-ended 50 Ω impedance
C5	IO_PM1_C5	3V	Single-ended 50 Ω impedance
C6	IO_PM1_C6	3V	Single-ended 50Ω impedance
C7	IO_PM1_C7	3V	Single-ended 50 Ω impedance
C8	IO_PM1_C8	3V	Single-ended 50 Ω impedance
С9	IO_PM1_C9_P	2.5V	LVDS pair 100Ω differential impedance;
C10	IO_PM1_C10_N	2.5V	can also be used as single-ended
C11	IO_PM1_C11	3V	Single-ended 50 Ω impedance
C12	IO_PM1_C12	3V	Single-ended 50Ω impedance
C13	RX_PM1_C13_P		MCT DV main received by best EDCA
C14	RX_PM1_C14_N		NGT KA pair received by host FFGA
C15	RX_PM1_C15_P		MCT DV main received by best EDCA
C16	RX_PM1_C16_N		NGT KA pair received by host FFGA
C17	TX_PM1_C17_P		MCT TV pair driven by best EPC A
C18	TX_PM1_C18_N		MG1 1X pair driven by nost FFGA
C19	TX_PM1_C19_P		MCT TY pair driven by best EPC A
C20	TX_PM1_C20_N		NGT TX pair driven by host FFGA
D1	IO_PM1_D1	2.5V	Single-ended 50Ω impedance
D2	IO_PM1_D2	2.5V	Single-ended 50Ω impedance
D3	IO_PM1_D3	2.5V	Single-ended 50 Ω impedance
D4	IO_PM1_D4	2.5V	Single-ended 50Ω impedance
D5	IO_PM1_D5	3V	Single-ended 50 Ω impedance
D6	IO_PM1_D6	3V	Single-ended 50 Ω impedance
D7	IO_PM1_D7	3V	Single-ended 50 Ω impedance
D8	IO_PM1_D8	3V	Single-ended 50 Ω impedance
D9	IO_PM1_D9	3V	Single-ended 50 Ω impedance

Table 2-5: PM1 Pinout (Continued)



ns			XILINX
Table 2-5:	PM1 Pinout <i>(Contir</i>	nued)	
PM1 Pin	Pin Description	FPGA Bank V _{CCO}	Pin Function
D10	IO_PM1_D10	3V	Single-ended 50 Ω impedance
D11	IO_PM1_D11_P	2.5V	LVDS pair 100Ω differential impedance;
D12	IO_PM1_D12_N	2.5V	can also be used as single-ended
D13	TX_PM1_D13_N		MCT TV as in driver has been EDC A
D14	TX_PM1_D14_P		MG1 1X pair driven by nost FFGA
D15	TX_PM1_D15_N		MCT TV as in driver has been EDC A
D16	TX_PM1_D16_P		MG1 1X pair driven by nost FFGA
D17	RX_PM1_D17_N		MCT DV as in an all as head EDCA
D18	RX_PM1_D18_P		MG1 KX pair received by nost FPGA
D19	RX_PM1_D19_N		
D20	RX_PM1_D20_P		MG1 KX pair received by nost FPGA
F1	IO_PM1_F1	2.5V	Single-ended 50 Ω impedance
F2	IO_PM1_F2	2.5V	Single-ended 50 Ω impedance
F3	IO_PM1_F3	3V	Single-ended 50 Ω impedance
F4	IO_PM1_F4	3V	Single-ended 50 Ω impedance
F5	IO_PM1_F5	3V	Single-ended 50 Ω impedance
F6	IO_PM1_F6	3V	Single-ended 50 Ω impedance
F7	IO_PM1_F7	3V	Single-ended 50 Ω impedance
F8	IO_PM1_F8	3V	Single-ended 50 Ω impedance
F9	PM_CLK_TOP	2.5V	Clock
F10	No Connect		No Connect
F11	LVDS_CLKEXT_N	2.5V	LVDS pair 100Ω differential impedance;
F12	LVDS_CLKEXT_P	2.5V	can also be used as single-ended
F13	TX_PM1_F13_N		MCT TV pair driver by best EDC A
F14	TX_PM1_F14_P		wigi in pair driven by nost FrGA
F15	TX_PM1_F15_N		

TX_PM1_F16_P

 $RX_PM1_F17_N$

RX_PM1_F18_P

RX_PM1_F19_N

 $RX_PM1_F20_P$

F16

F17

F18

F19

F20

MGT TX pair driven by host FPGA

MGT RX pair received by host FPGA

MGT RX pair received by host FPGA

2.3.2 PM2 User I/O

The PM2 connector makes most of the LVDS pairs available to the user, along with singleended signals. Table 2-6 shows the pinout for the PM2 connector.

PM2 Pin	Pin Description	FPGA Bank V _{CCO}	Pin Function
A1	IO_PM2_A1_N	2.5V	LVDS pair 100Ω differential impedance;
A2	IO_PM2_A2_P	2.5V	can also be used as single-ended
A3	IO_PM2_A3_N	2.5V	LVDS pair 100Ω differential impedance;
A4	IO_PM2_A4_P	2.5V	can also be used as single-ended
A5	IO_PM2_A5_N	2.5V	LVDS pair 100Ω differential impedance;
A6	IO_PM2_A6_P	2.5V	can also be used as single-ended
A7	IO_PM2_A7_N	2.5V	LVDS pair 100Ω differential impedance;
A8	IO_PM2_A8_P	2.5V	can also be used as single-ended
A9	IO_PM2_A9_N	2.5V	LVDS pair 100Ω differential impedance;
A10	IO_PM2_A10_P	2.5V	can also be used as single-ended
A11	IO_PM2_A11_P	2.5V	LVDS pair 100Ω differential impedance;
A12	IO_PM2_A12_N	2.5V	can also be used as single-ended
A13	IO_PM2_A13_P	2.5V	LVDS pair 100Ω differential impedance;
A14	IO_PM2_A14_N	2.5V	can also be used as single-ended
A15	IO_PM2_A15_P	2.5V	LVDS pair 100Ω differential impedance;
A16	IO_PM2_A16_N	2.5V	can also be used as single-ended
A17	IO_PM2_A17_P	2.5V	LVDS pair 100Ω differential impedance;
A18	IO_PM2_A18_N	2.5V	can also be used as single-ended
A19	IO_PM2_A19_P	2.5V	LVDS pair 100Ω differential impedance;
A20	IO_PM2_A20_N	2.5V	can also be used as single-ended
C1	IO_PM2_C1_N	2.5V	LVDS pair 100Ω differential impedance;
C2	IO_PM2_C2_P	2.5V	can also be used as single-ended
C3	IO_PM2_C3_N	2.5V	LVDS pair 100Ω differential impedance;
C4	IO_PM2_C4_P	2.5V	can also be used as single-ended
C5	IO_PM2_C5_N	2.5V	LVDS pair 100Ω differential impedance;
C6	IO_PM2_C6_P	2.5V	can also be used as single-ended
C7	IO_PM2_C7_N	2.5V	LVDS pair 100Ω differential impedance;
C8	IO_PM2_C8_P	2.5V	can also be used as single-ended

Table 2-6: PM2 Pinout



PM2 Pin	Pin Description	FPGA Bank V _{CCO}	Pin Function
C9	IO_PM2_C9_P	2.5V	LVDS pair 100Ω differential impedance;
C10	IO_PM2_C10_N	2.5V	can also be used as single-ended
C11	IO_PM2_C11_P	2.5V	LVDS pair 100Ω differential impedance;
C12	IO_PM2_C12_N	2.5V	can also be used as single-ended
C13	IO_PM2_C13_P	2.5V	LVDS pair 100Ω differential impedance;
C14	IO_PM2_C14_N	2.5V	can also be used as single-ended
C15	IO_PM2_C15_P	2.5V	LVDS pair 100Ω differential impedance;
C16	IO_PM2_C16_N	2.5V	can also be used as single-ended
C17	IO_PM2_C17_P	2.5V	LVDS pair 100Ω differential impedance;
C18	IO_PM2_C18_N	2.5V	can also be used as single-ended
C19	IO_PM2_C19_P	2.5V	LVDS pair 100Ω differential impedance;
C20	IO_PM2_C20_N	2.5V	can also be used as single-ended
D1	IO_PM2_D1_N	2.5V	LVDS pair 100Ω differential impedance;
D2	IO_PM2_D2_P	2.5V	can also be used as single-ended
D3	IO_PM2_D3_N	2.5V	LVDS pair 100Ω differential impedance;
D4	IO_PM2_D4_P	2.5V	can also be used as single-ended
D5	IO_PM2_D5_N	2.5V	LVDS pair 100Ω differential impedance;
D6	IO_PM2_D6_P	2.5V	can also be used as single-ended
D7	IO_PM2_D7_N	2.5V	LVDS pair 100Ω differential impedance;
D8	IO_PM2_D8_P	2.5V	can also be used as single-ended
D9	IO_PM2_D9_N	2.5V	LVDS pair 100Ω differential impedance;
D10	IO_PM2_D10_P	2.5V	can also be used as single-ended
D11	IO_PM2_D11_P	2.5V	LVDS pair 100Ω differential impedance;
D12	IO_PM2_D12_N	2.5V	can also be used as single-ended
D13	IO_PM2_D13_P	2.5V	LVDS pair 100Ω differential impedance;
D14	IO_PM2_D14_N	2.5V	can also be used as single-ended
D15	IO_PM2_D15_P	2.5V	LVDS pair 100Ω differential impedance;
D16	IO_PM2_D16_N	2.5V	can also be used as single-ended
D17	IO_PM2_D17_P	2.5V	LVDS pair 100Ω differential impedance;
D18	IO_PM2_D18_N	2.5V	can also be used as single-ended

Table 2-6: PM2 Pinout (Continued)

PM2 Pin	Pin Description	FPGA Bank V _{CCO}	Pin Function
D19	IO_PM2_D19_P	2.5V	LVDS pair 100Ω differential impedance;
D20	IO_PM2_D20_N	2.5V	can also be used as single-ended
F1	IO_PM2_F1_N	2.5V	LVDS pair 100Ω differential impedance;
F2	IO_PM2_F2_P	2.5V	can also be used as single-ended
F3	IO_PM2_F3_N	2.5V	LVDS pair 100Ω differential impedance;
F4	IO_PM2_F4_P	2.5V	can also be used as single-ended
F5	IO_PM2_F5_N	2.5V	LVDS pair 100Ω differential impedance;
F6	IO_PM2_F6_P	2.5V	can also be used as single-ended
F7	IO_PM2_F7_N	2.5V	LVDS pair 100 Ω differential impedance;
F8	IO_PM2_F8_P	2.5V	can also be used as single-ended
F9	No Connect		No Connect
F10	PM_CLK_BOT	2.5V	Clock
F11	IO_PM2_F11_P	2.5V	LVDS pair 100 Ω differential impedance;
F12	IO_PM2_F12_N	2.5V	can also be used as single-ended
F13	IO_PM2_F13_P	2.5V	LVDS pair 100 Ω differential impedance;
F14	IO_PM2_F14_N	2.5V	can also be used as single-ended
F15	IO_PM2_F15_P	2.5V	LVDS pair 100 Ω differential impedance;
F16	IO_PM2_F16_N	2.5V	can also be used as single-ended
F17	IO_PM2_F17_P	2.5V	LVDS pair 100 Ω differential impedance;
F18	IO_PM2_F18_N	2.5V	can also be used as single-ended
F19	IO_PM2_F19_P	2.5V	LVDS pair 100 Ω differential impedance;
F20	IO_PM2_F20_N	2.5V	can also be used as single-ended

Table 2-6: PM2 Pinout (Continued)



3 Mechanical Specification

3.1 Personality Module Dimensions

Figure 3-1 shows the dimensions for the personality module, also known as the adapter board.



Figure 3-1: Module Dimensions

3.2 PCB Layout for Host Board Connector

Figure 3-2 shows the PCB layout for the XPM connectors on the host board.



Figure 3-2: PCB Layout for Host Board Connector

3.3 PCB Layout for Adapter Board Connector



Figure 3-3 shows the PCB layout for the XPM connectors on the personality module.

