Virtex-6 FPGA GTX Transceiver Signal Integrity Simulation Kit User Guide

For Mentor Graphics HyperLynx

UG376 (v1.1) July 20, 2010

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/02/10	1.0	Initial Xilinx release.
07/20/10	1.1	Updated SIS Kit version from 1.0 to 1.1 in Table 1-1 and Installation and Requirements, page 7.

About This Guide

This guide describes the Virtex®-6 FPGA GTX Transceiver Signal Integrity Simulation (SIS) Kit for Mentor Graphics HyperLynx.

Guide Contents

This user guide contains the following sections:

- Chapter 1, Virtex-6 FPGA GTX Transceiver Signal Integrity Simulation Kit, explains installation, configuration, and use of the HyperLynx software to simulate Virtex-6 FPGA GTX transceivers.
- Appendix A, Frequently Asked Questions, explains HyperLynx error messages.
- Appendix B, HSPICE and HyperLynx/Eldo Correlation Results, contains the correlation results and explains how they were derived.

Additional Support Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**

Convention	Meaning or Use	Example
Italic font	References to other documents	See the *Virtex-6 FPGA Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **bus[7:0]**, they are required.	**ngdbuild** [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**lowpwr ={on|off}**
Vertical bar |	Separates items in a list of choices	**lowpwr ={on|off}**
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	**allow block** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section Additional Support Resources for details. Refer to Overview, page 7 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

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Chapter 1

Virtex-6 FPGA GTX Transceiver Signal Integrity Simulation Kit

Introduction

The Virtex®-6 FPGA GTX Transceiver Signal Integrity Simulation (SIS) Kit for Mentor Graphics HyperLynx provides a simulation environment for evaluating channel designs for Virtex®-6 FPGA GTX transceivers. This document explains how to install the SIS Kit and associated files, gives an overview of the SIS Kit-file hierarchy, and describes the steps for getting started with simulations. The appendices describe how the HyperLynx and Eldo simulation results are correlated with the HSPICE simulations. Results are documented with waveform plots.

Additional information on the models, ports, and options is available in UG375, *Virtex-6 FPGA GTX Transceiver Signal Integrity Simulation Kit User Guide for Synopsys HSPICE*, and UG366, *Virtex-6 FPGA GTX Transceivers User Guide*.

Release Notes for the GTX Transceiver SIS Kit

Table 1-1 shows the UG376 document version and the associated Virtex-6 FPGA GTX Transceiver SIS Kit version.

Table 1-1: **Document and SIS Kit Version Correlation**

UG376 Version	SIS Kit Version
1.1	1.1

Installation and Requirements

The software requirements and the installation instructions for the GTX Transceiver SIS Kit are provided in this section.

SIS Kit Versions 1.1 and 1.0

The requirements for the GTX Transceiver SIS Kit are:

- HyperLynx 8.0, build number 433 or later
- Microsoft Windows XP Professional, version 2002, Service Pack 3

To install the GTX Transceiver SIS Kit, follow these steps:

1. Unzip the `.zip` file into any directory, provided that the path name does not contain any spaces.

2. To prevent errors or warnings when the project files are moved to a different directory (or computer), replace the path listed on the last line in the `.pjh` files (located in the `HL_projects` subdirectory) with a relative path as follows: `INIFILE=.\V6_kit.ini`.

Note: HyperLynx automatically replaces this relative path with a full path when opening the project. Therefore, this change should be made every time the project is moved or copied to a different location.

3. For better convergence, set ForceFixedStep = 0 under the [SPICE] keyword in the `bsw.ini` file, in the HyperLynx Installation directory.

File Hierarchy

The top-level directory into which the ZIP file is unzipped contains several subdirectories. The HyperLynx project files are all located in the `hl_projects` subdirectory. Any example project can be opened by double-clicking on the respective `.ffs` file in Windows Explorer or by starting HyperLynx, going to **File/Open Schematic...**, and then clicking on **Open Linesim File**.

Model files are located in the subcircuits under the top-level project directory.

Subcircuits are referenced by the HyperLynx schematic symbols. The `.inc` files containing the simulation parameters are located under the `testbenches` directory along with the configurator executable programs. There should be no reason to manually modify these files. All modifications are made via the HyperLynx Graphical User Interface.

Getting Started

The following steps must be observed to run simulations:

To Open an Example

The user can double-click on any `.ffs` file in Windows Explorer to start a project in HyperLynx. This user guide uses `GTX_Tx_channel_GTX_Rx` as an example, but this discussion applies to the other testbenches as well. The user can double-click on the `GTX_RefClk.ffs` or the `GTX_Tx_channel_GTX_Rx.ffs` file in the `hl_projects` directory in Windows Explorer to start HyperLynx. Because the latter file is the more complicated testbench, the remaining part of this document discusses that testbench only.

HyperLynx should start without any error or warning messages and look as shown in Figure 1-1.

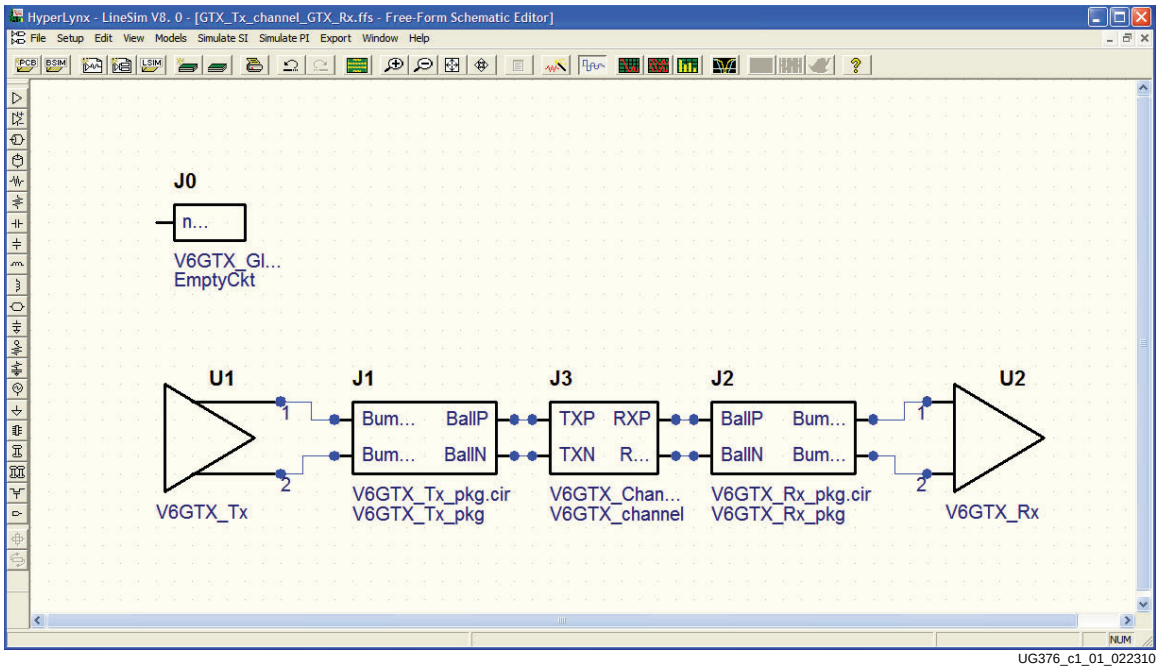

Figure 1-1: **HyperLynx**

Note: The *J0* symbol must appear unconnected on the schematics screen. This symbol should not be removed from the schematics because it is used to insert global simulation parameters, such as **`.TEMP`** and **`.option compat`** (the HSPICE compatibility switch for Eldo), into the project. These parameters are managed automatically by the configurator programs. Removing *J0* results in incorrect simulations.

To Modify the Driver Settings

1. Double-click on U1 to open the **Assign Models** dialog box and single-click on the **Configure Model** button, as shown in Figure 1-2.

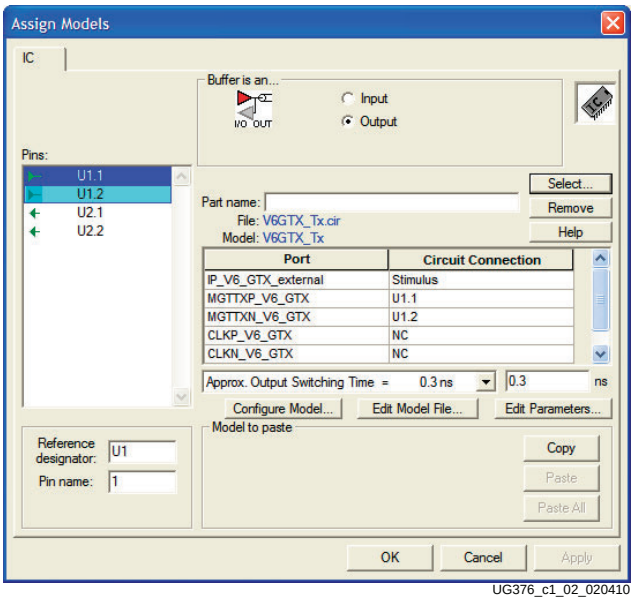

Figure 1-2: **Assign Models**

For more information on the driver settings, refer to UG366, *Virtex-6 FPGA GTX Transceivers User Guide*.

Important. The global simulation temperature setting can be changed in either driver or receiver configurators. However, being a global setting in Eldo, the last change made is applied to the entire circuit, regardless of whether the TX or RX configurator was used to make that change.

Note: Be sure to click only once, because each click starts a new instance of the configurator. If multiple instances of the configurators are open, close all but one of them by clicking on their **Cancel** button.

2. Make the desired changes to any of the parameters, and press the **OK** button to exit. This writes the necessary configuration files for the simulation.

   Note: The frequency of the pulse train or the time of the bit interval specified in the oscilloscope *must* match the Data rate setting in the TX configurator (see Figure 1-3). Each setting must be done explicitly.

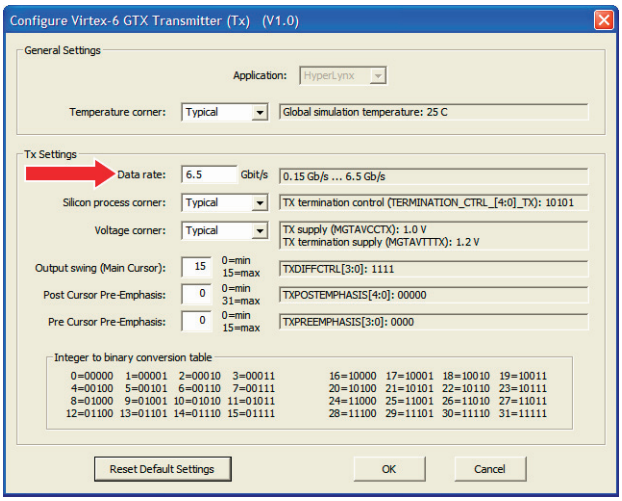

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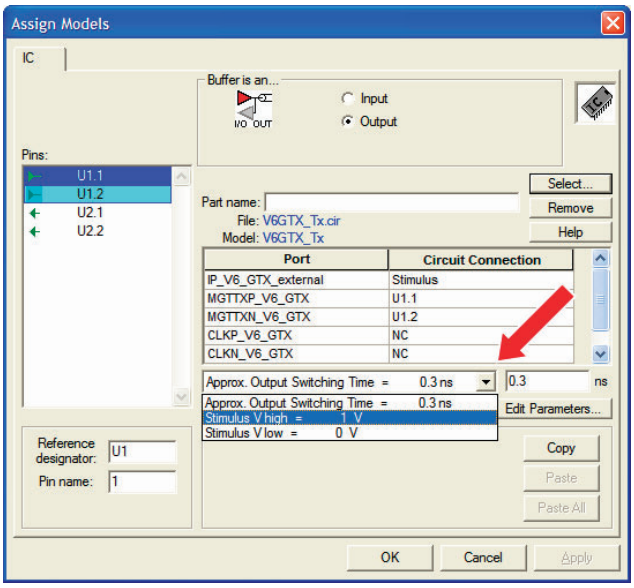
Figure 1-3: **Configure GTX Transmitter**

The setting for the **Approx. Output Switching Time = 0.3 ns** drop-down box shown in Figure 1-4 is meant to be the SPICE driver output (not stimulus) rise or fall time and is used to set the step size and estimate crosstalk effects in the simulation. The value of this parameter can be changed if desired. Relaxing this parameter allows the user to select larger simulation time steps in the **Run Eldo/ADMS Simulation** dialog box, which might result in non-converging simulations.



UG376_c1_04_020410

Figure 1-4: **Output Switching Time**

The drop-down box shown in Figure 1-4 also has two additional entries for the High and Low voltage levels of the stimulus generated by HyperLynx. Do not modify these numbers because they are closely related to the content of the netlist. The voltage levels in the `GTX_RefClk.ffs` testbench must be set to **`-1V`** for **`Stimulus V low`**

and **+1V** for **Stimulus V high**. In the rest of the testbenches, they should be set to **0V** for **Stimulus V low** and **+1V** for **Stimulus V high**.

3. When the desired changes are made, click on the **OK** button to close the **Assign Models** dialog.
4. When finished making changes to the parameters, click on the **OK** button to close the **Assign Models** dialog box.

Customizing the Channel Representation

Use the available HyperLynx toolbox to add S-parameter models, transmission lines, vias, and so forth.

The provided example contains an S-parameter model representing a 20-inch microstrip trace with SMA connectors on each side. The board material is FR-4. A custom channel representation can be created using the HyperLynx toolbox to add S-parameter models, transmission lines, vias, and so forth.

Modifying the Receiver Settings

Repeat To Modify the Driver Settings. Adjust the receiver (**U2**) simulation parameters.

For more information on the driver settings, refer to UG366, *Virtex-6 FPGA GTX Transceivers User Guide*.

Important. The global simulation temperature setting can be changed in either driver or receiver configurators (see Figure 1-5). However, because it is a global setting in Eldo, the last change made is applied to the entire circuit, regardless of whether the TX or RX configurator was used to make that change.

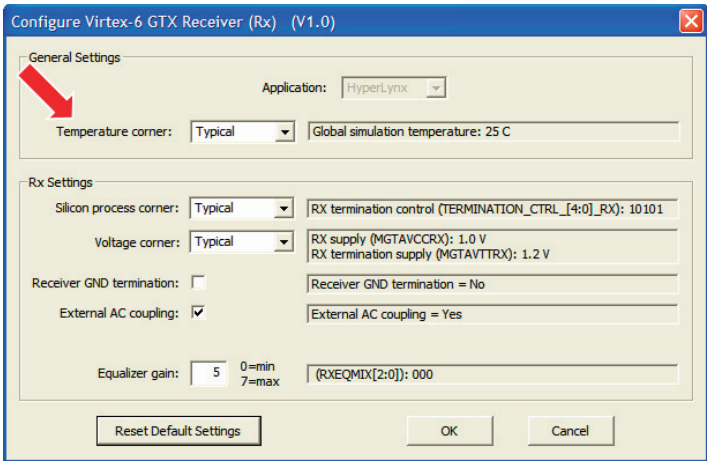


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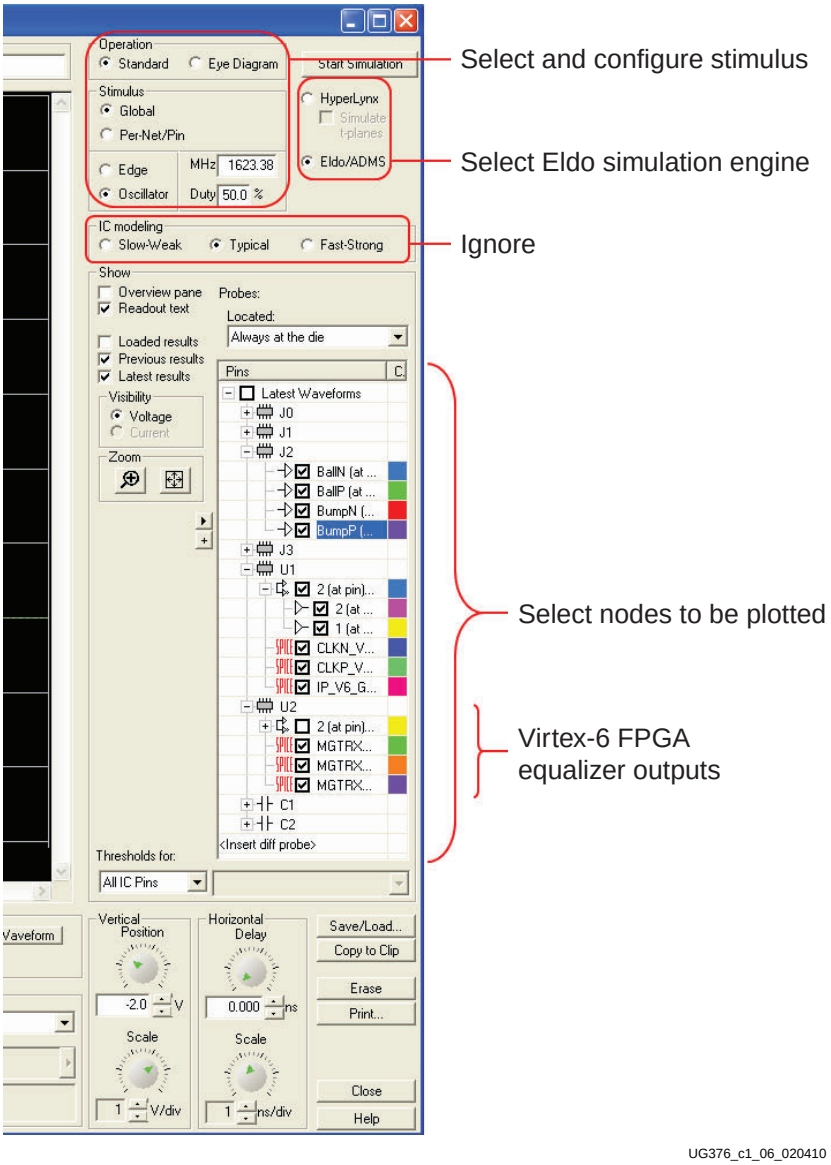
Figure 1-5: **Configuration Dialog Box**

Note: Be sure to click only once. If multiple instances of the configurators are open, close all but one by clicking on their **Cancel** buttons.

Adjusting Simulation Settings

1. Click **Run Interactive Simulation (Oscilloscope)** under the **Simulate** tab.

2. Select the **Eldo/ADMS** radio button under the **Start Simulation** button, as shown in Figure 1-6.

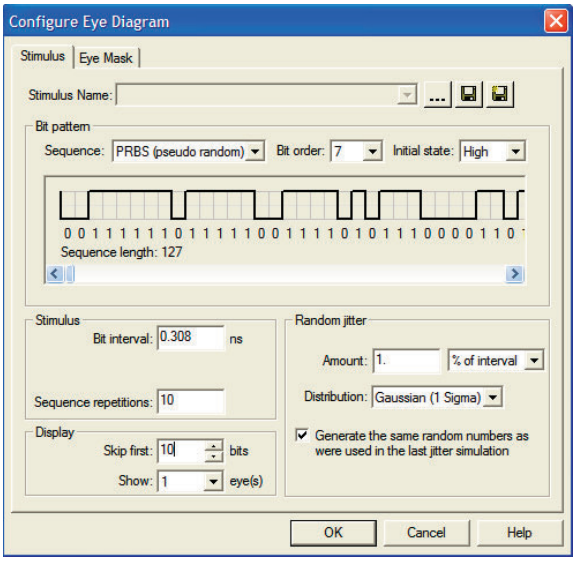


UG376_c1_06_020410

Figure 1-6: **Assign Probes, Select Eldo as Simulation Engine, and Specify Stimulus Type**

3. Add a checkmark to all nodes to plot.
4. Select the type of stimulus for HyperLynx to generate. The oscilloscope has several stimulus waveform options available:
   a. The **Standard** radio button under the **Operation** section provides options to run a single rising or falling edge simulation or a pulse train of a certain frequency and duty cycle.
   b. The **Eye Diagram** radio button under the Operation section provides capabilities to set up various bit sequences after the **Configure** button is clicked. The available **Bit Pattern** selection includes **PRBS, 8B/10B, Toggling, USB 2.0** and **Custom** patterns (see Figure 1-7). The **Configure Eye Diagram** dialog box also allows the

user to set up an eye mask for the eye diagram display in the oscilloscope. Refer to the HyperLynx manuals for more details on how to set up these parameters.



UG376_c1_07_020410

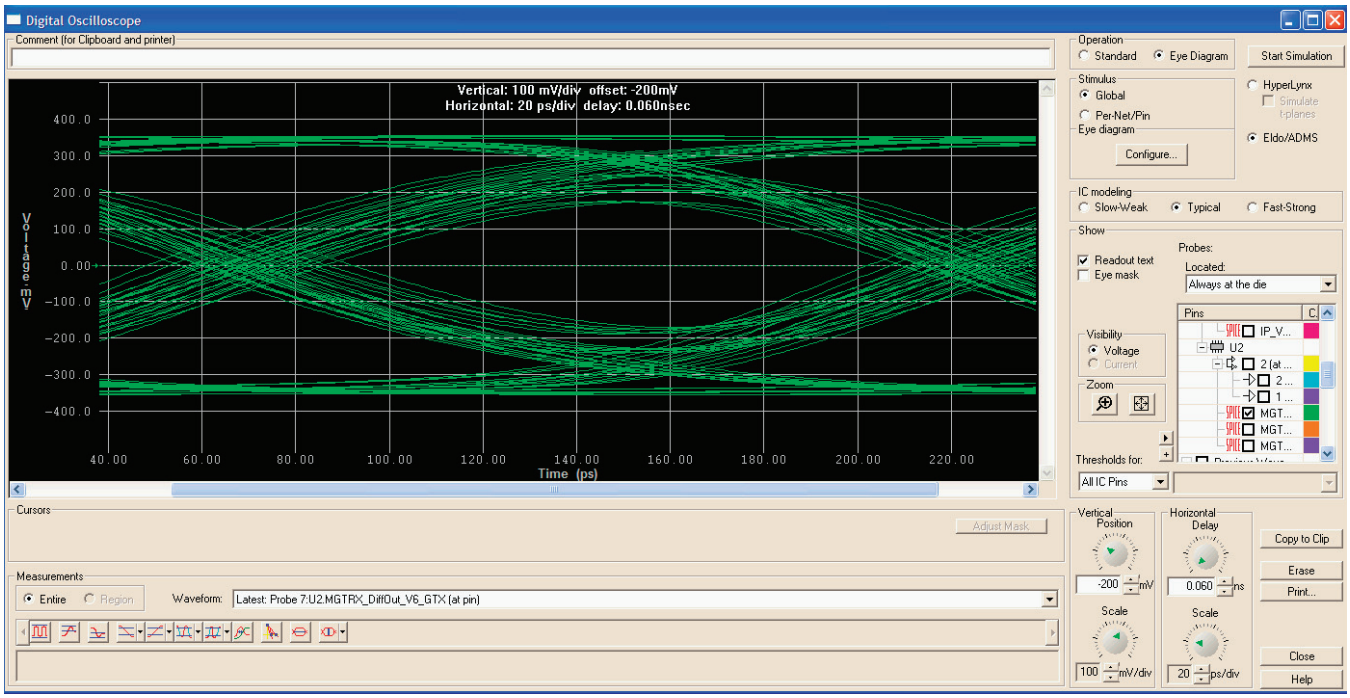
Figure 1-7: **6.5 Gb/s PRBS 27 Stimulus**

Notes relevant to this section:

- *Important*! The frequency of the pulse train and the time of the bit interval specified in the oscilloscope must match the data rate setting in the TX configurator. Each setting has to be done explicitly.
- The radio buttons in the IC modeling group (Figure 1-6) are ineffective because the simulation corner selections are made using the **Configure Model** button in the **Assign Models** dialog box.
- Checkboxes with the red SPICE label on their (Figure 1-6) left represent schematic symbol nodes that are connected to **NC** in the **Assign Models** dialog box. These nodes are defined on the subcircuit definition line of the symbol, but do not need to be connected to anything else on the schematics because they are used solely to provide probing capabilities for waveforms inside the subcircuits.

Running the Simulation

Click the **Start Simulation** button and wait for the simulator to finish the simulation. The waveform window automatically displays the results for the selected waveforms in the oscilloscope. The vertical and horizontal scales can be adjusted to maximize the waveforms, as shown in Figure 1-8.



UG376_c1_08_020410

Figure 1-8: **Example Simulation Results**

Appendix A

Frequently Asked Questions

All Versions

1. What does the "Device-kit .INI file where_am_i\V6_kit.ini does not exist or cannot be read" message shown in Figure A-1 mean?

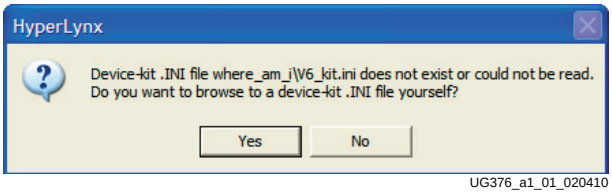
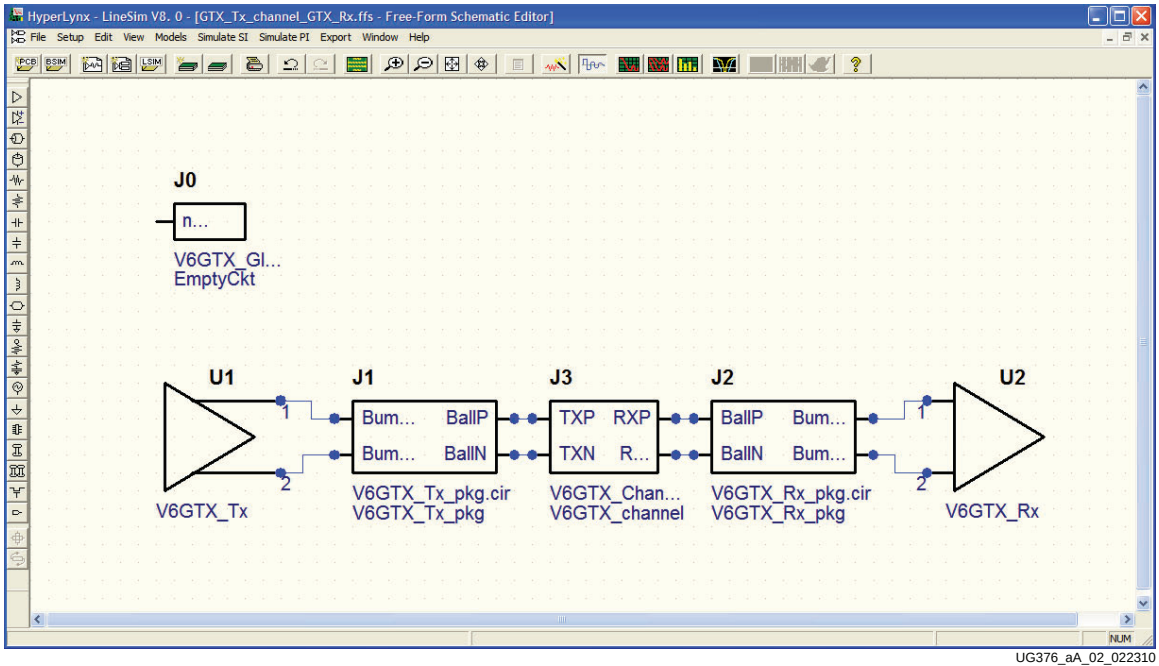


Figure A-1: **Device-kit .INI Error Message**

HyperLynx cannot find the `Device-kit.INI` file, most likely because the `DesignName.pjh` file has an incorrect path for the `.ini` file. The `V6_kit.ini` file is located in the `hl_projects` directory. Do one of the following:

- Click **No**, close HyperLynx and edit the `.pjh` file as described in Installation and Requirements, page 7 and start HyperLynx again.
- Click **Yes** and browse to the `hl_projects` directory to locate the `DesignName.pjh` file.

2. What is the J0 symbol on the schematic screen (Figure A-2)?

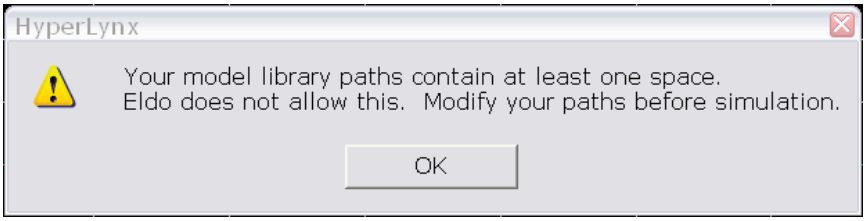


UG376_aA_02_022310

Figure A-2: **J0 Symbol**

The J0 symbol appears unconnected on the schematics screen and must *not* be removed from the schematics. The J0 symbol inserts global simulation parameters, such as **`.TEMP`** and **`.option compat`** (the HSPICE compatibility switch for Eldo) into the project. These parameters are managed automatically by the configurator programs. Removing J0 results in incorrect simulations.

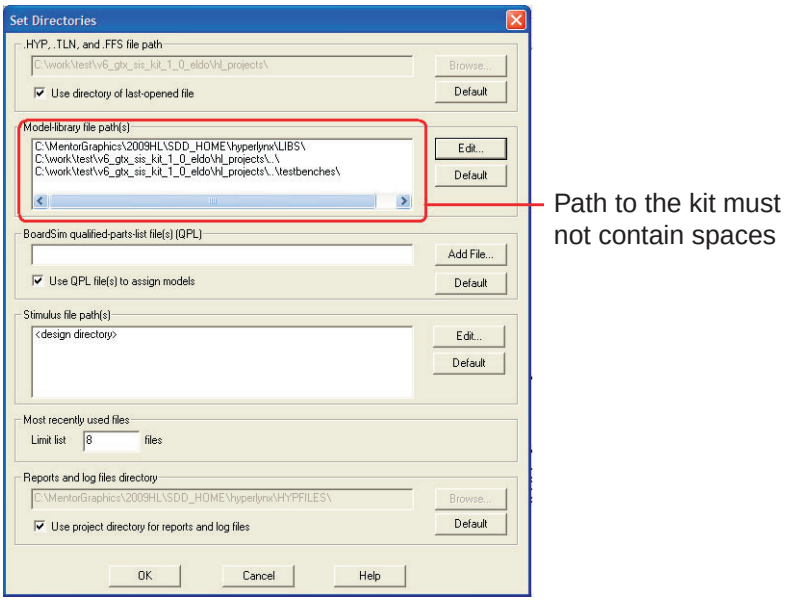
3. What does the "Your model library paths contain at least one space" message shown in Figure A-3 mean?



UG376_aA_03_011110

Figure A-3: **Spaces in Path Error Message**

If the installation instructions in Installation and Requirements are followed, this message can usually be ignored. This message appears when model search path directories contain space characters. From the menu bar, select **Options → Directories** to verify in the list (Figure A-4) that there are no spaces in the path pointing to the root of this kit.



UG376_a2_04_0209410

Figure A-4: **Example of Path**

4. What if the simulation does not start or aborts prematurely?

   This might occur if:

   - The correct simulation in HyperLynx is not selected. Verify that Eldo/ADMS is the selected simulator engine in the **Digital Oscilloscope** window.
   - The **HSPICE compatible** radio button is not selected or the Eldo executable is not listed in the **Circuit Simulators** tab of the **Setup** → **Options** → **General** dialog box. See Figure A-5 for proper selection.
   - The HyperLynx license is not set to perform Eldo simulations. Contact the license manager or a Mentor Graphics representative to resolve this issue.

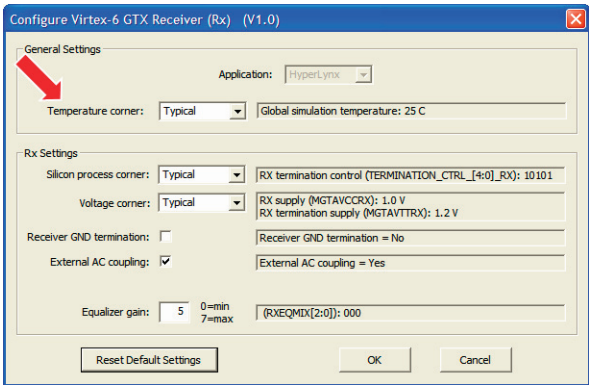


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Figure A-5: **HSPICE Compatible Radio Button**

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Appendix B

HSPICE and HyperLynx/Eldo Correlation Results

Introduction

The results generated by the Hyperlynx and Eldo simulators are validated by executing a set of the same simulations in both simulators and plotting the waveform results on top of each other to verify identical outcomes.

Note: HSPICE version A-2009.03 was used for the S-parameter/circuit correlation and the GTX REFCLK and GTX transceiver simulations.

For this correlation, only the silicon models for the GTX transmitter and receiver are used. Package and channel models are ignored, except for the GTX reference clock, where the package model is included.

Table B-1 lists the parameter settings used by the GTX transceiver simulations.

Table B-1: **GTX Transceiver Simulations Parametric Settings**

File Extension	TXDIFFCTRL	TXPOSTEMPHASIS	TXPREEMPHASIS	RXEQMIX
Typical Process Corner with Typical Voltage and Typical Temperature				
.tr0	4'b0000	5'b00000	4'b0000	3'b000
.tr1	4'b0100	5'b00000	4'b0000	3'b000
.tr2	4'b1010	5'b00000	4'b0000	3'b000
.tr3	4'b1111	5'b00000	4'b0000	3'b000
.tr4	4'b1010	5'b00000	4'b0100	3'b000
.tr5	4'b1010	5'b00000	4'b1010	3'b000
.tr6	4'b1010	5'b00000	4'b1111	3'b000
.tr7	4'b1010	5'b01100	4'b0000	3'b000
.tr8	4'b1010	5'b10010	4'b0000	3'b000
.tr9	4'b1010	5'b11111	4'b0000	3'b000
.tr10	4'b1010	5'b00111	4'b0011	3'b000
.tr11	4'b1010	5'b00000	4'b0000	3'b010
.tr12	4'b1010	5'b00000	4'b0000	3'b100
.tr13	4'b1010	5'b00000	4'b0000	3'b111

Table B-1: **GTX Transceiver Simulations Parametric Settings *(Cont'd)***

File Extension	TXDIFFCTRL	TXPOSTEMPHASIS	TXPREEMPHASIS	RXEQMIX
Fast Process Corner with Maximum Voltage and Cold Temperature				
.tr14	4'b1010	5'b00000	4'b0000	3'b000
.tr15	4'b1010	5'b0011	4'b0011	3'b000
Slow Process Corner with Minimum Voltage and Hot Temperature				
.tr16	4'b1010	5'b00000	4'b0000	3'b000
.tr17	4'b1010	5'b0011	4'b0011	3'b000

The plots are zoomed in and aligned to better highlight the correlation.

These conditions were used for the transceiver correlation:

- A data rate of 6.5 Gb/s
- PRBS7 data pattern
- No external capacitor
- No ground termination

The simulation results are provided in these sections:

- GTX REFCLK Model Correlation, page 23
- GTX Transceiver Model Correlation, page 26

GTX REFCLK Model Correlation

Figure B-1 through Figure B-3 contain the waveform overlays of the correlation simulations for the GTX REFCLK testbench (`GTX_RefClk.ffs`).

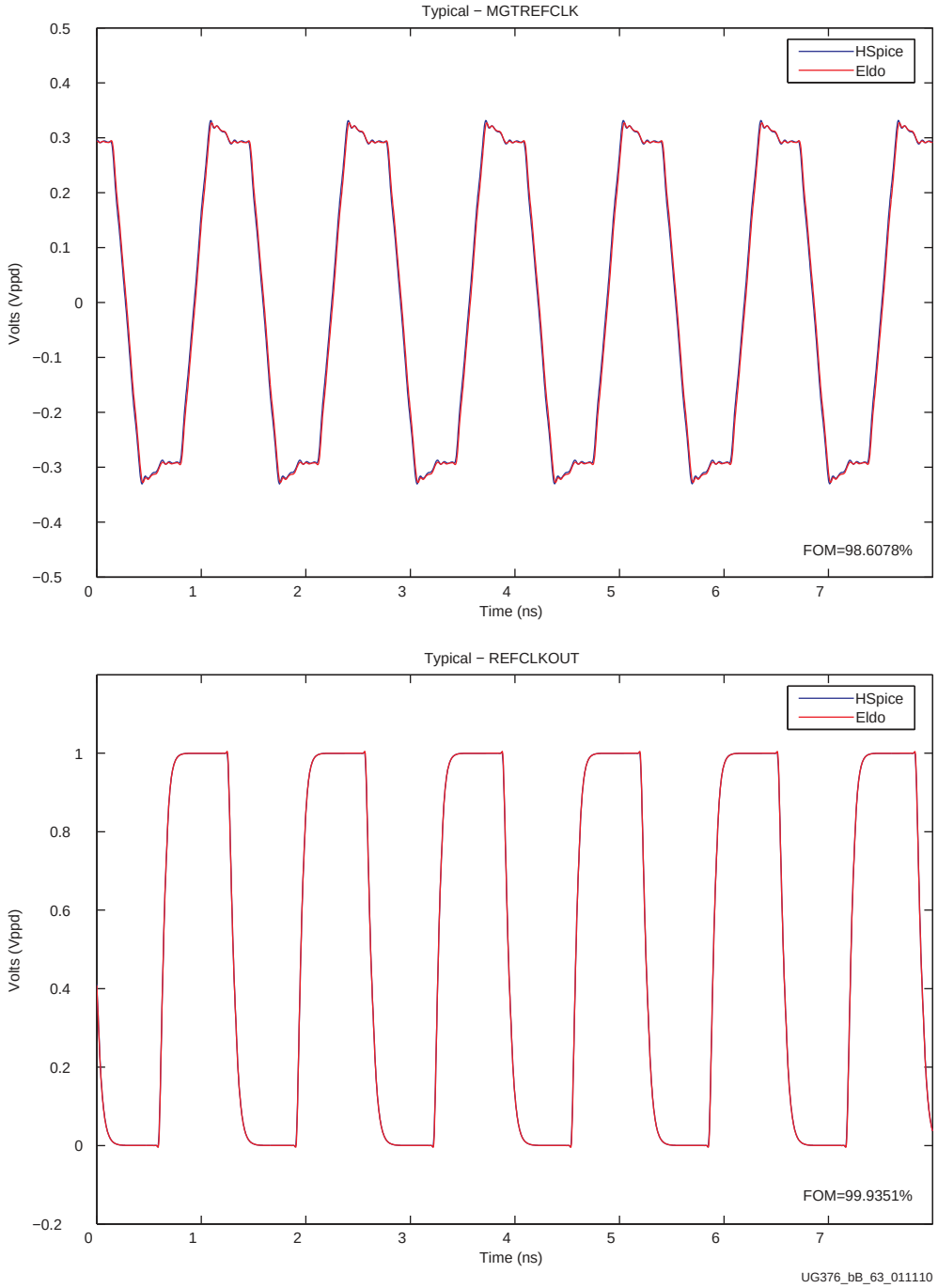

Figure B-1: **GTX REFCLK - Typical**

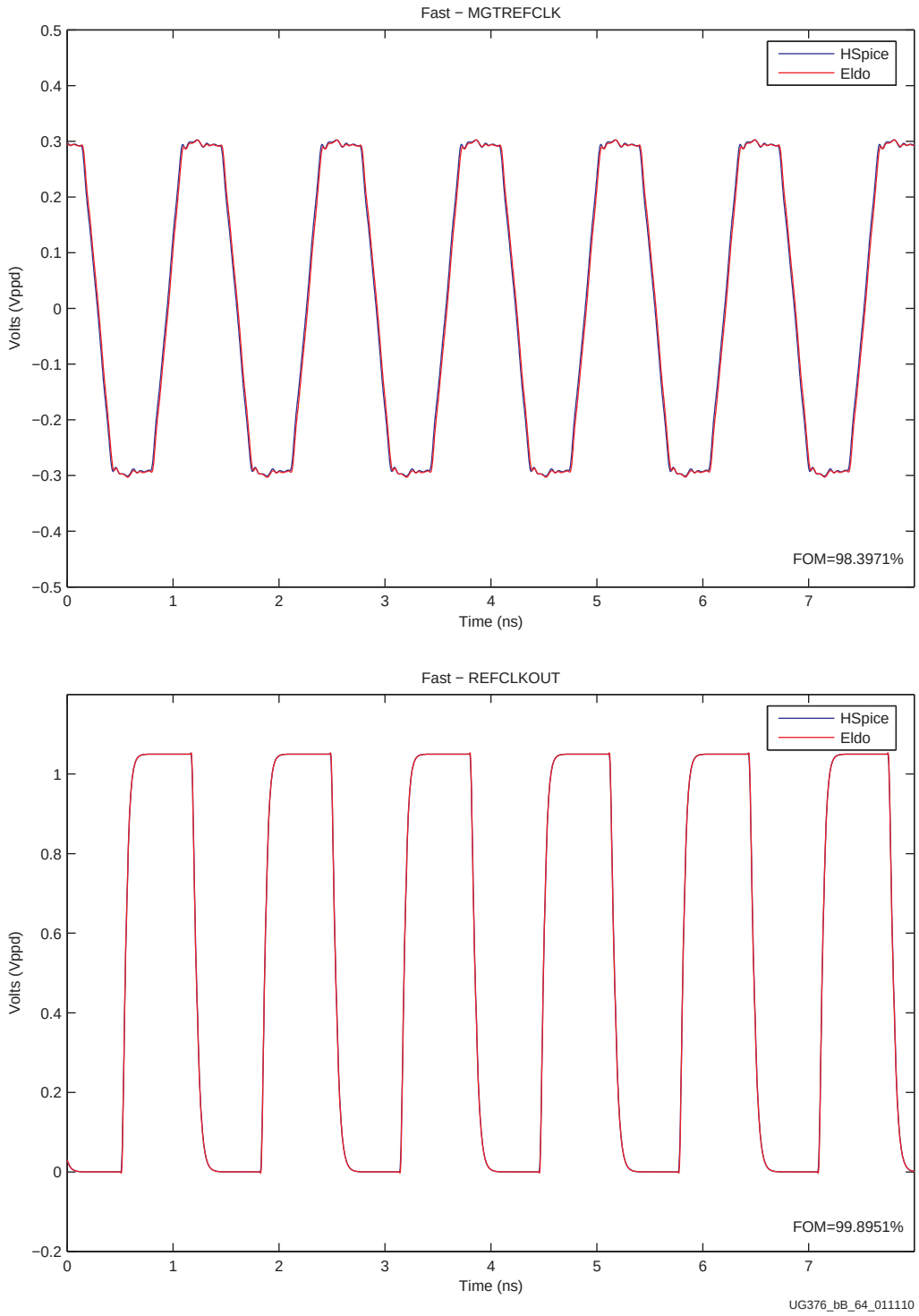

Figure B-2: **GTX REFCLK - Fast**

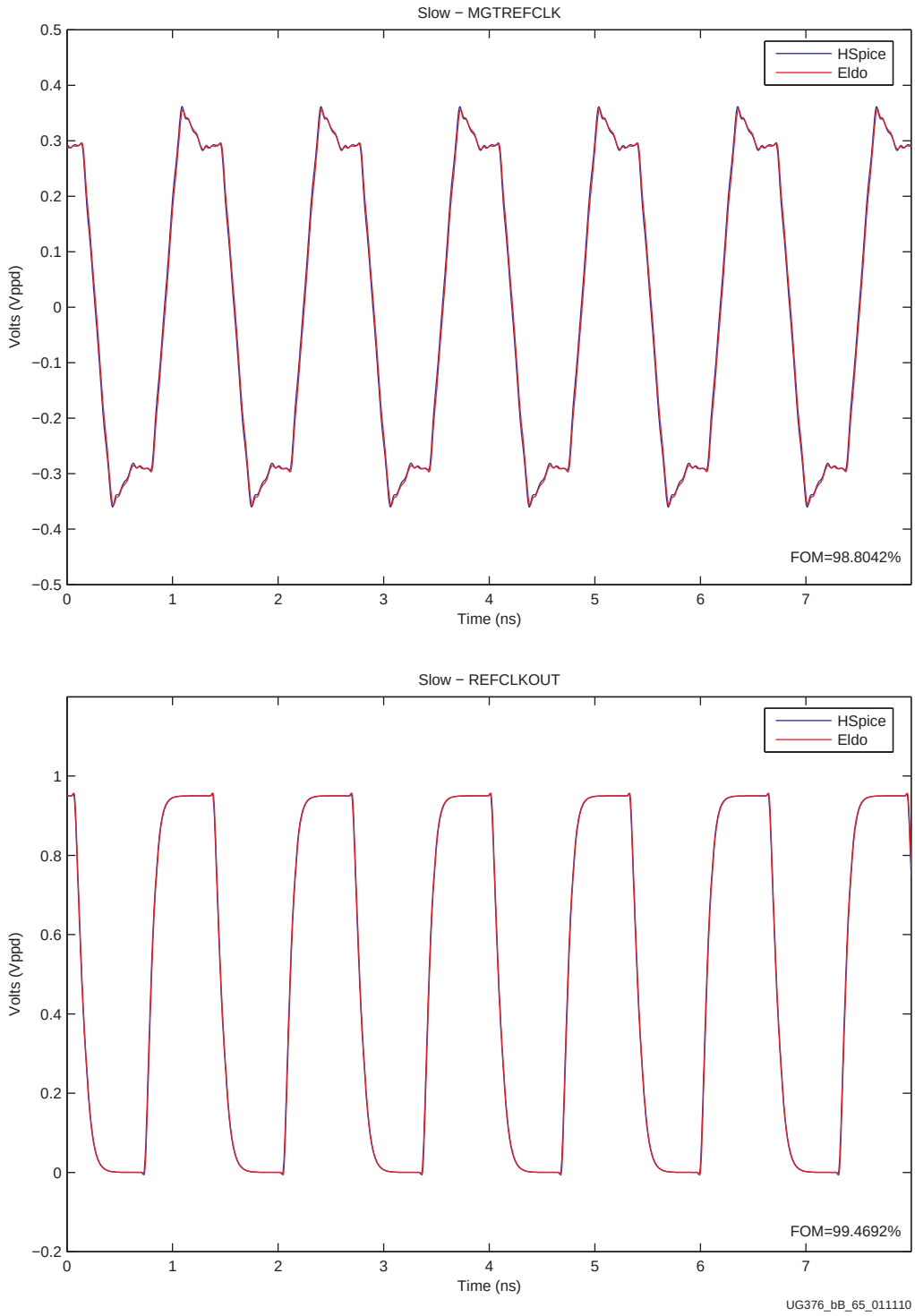

Figure B-3: **GTX REFCLK - Slow**

GTX Transceiver Model Correlation

Figure B-4 through Figure B-21 contain the waveform overlays of the correlation simulations for the GTX transceiver models.

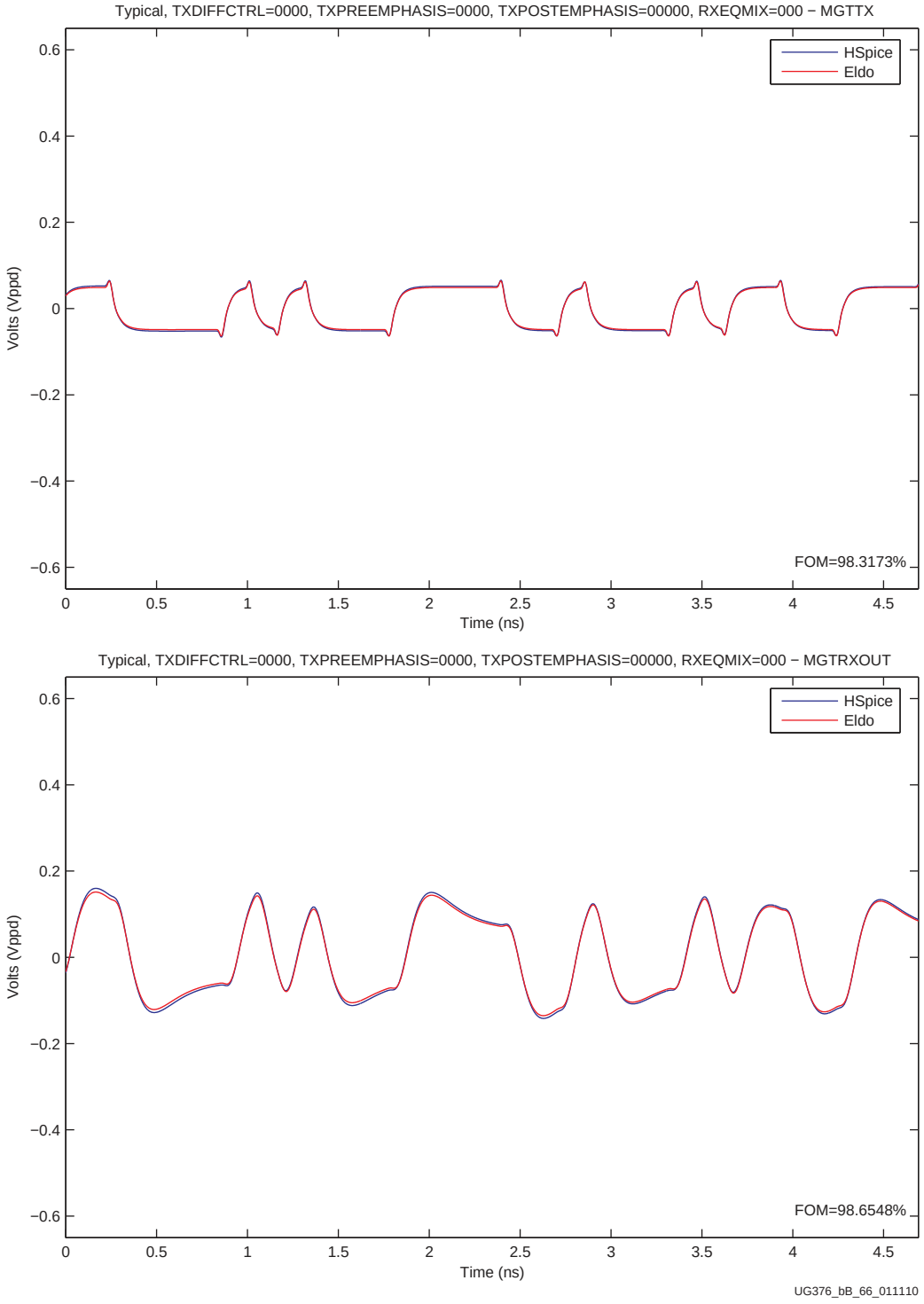

Figure B-4: **.tr0 TXDIFFCTRL = 0000, TXPREEMP = 0000, TXPOSTEMP = 00000, RXEQMIX = 000 (Typical - GTX Transceiver)**

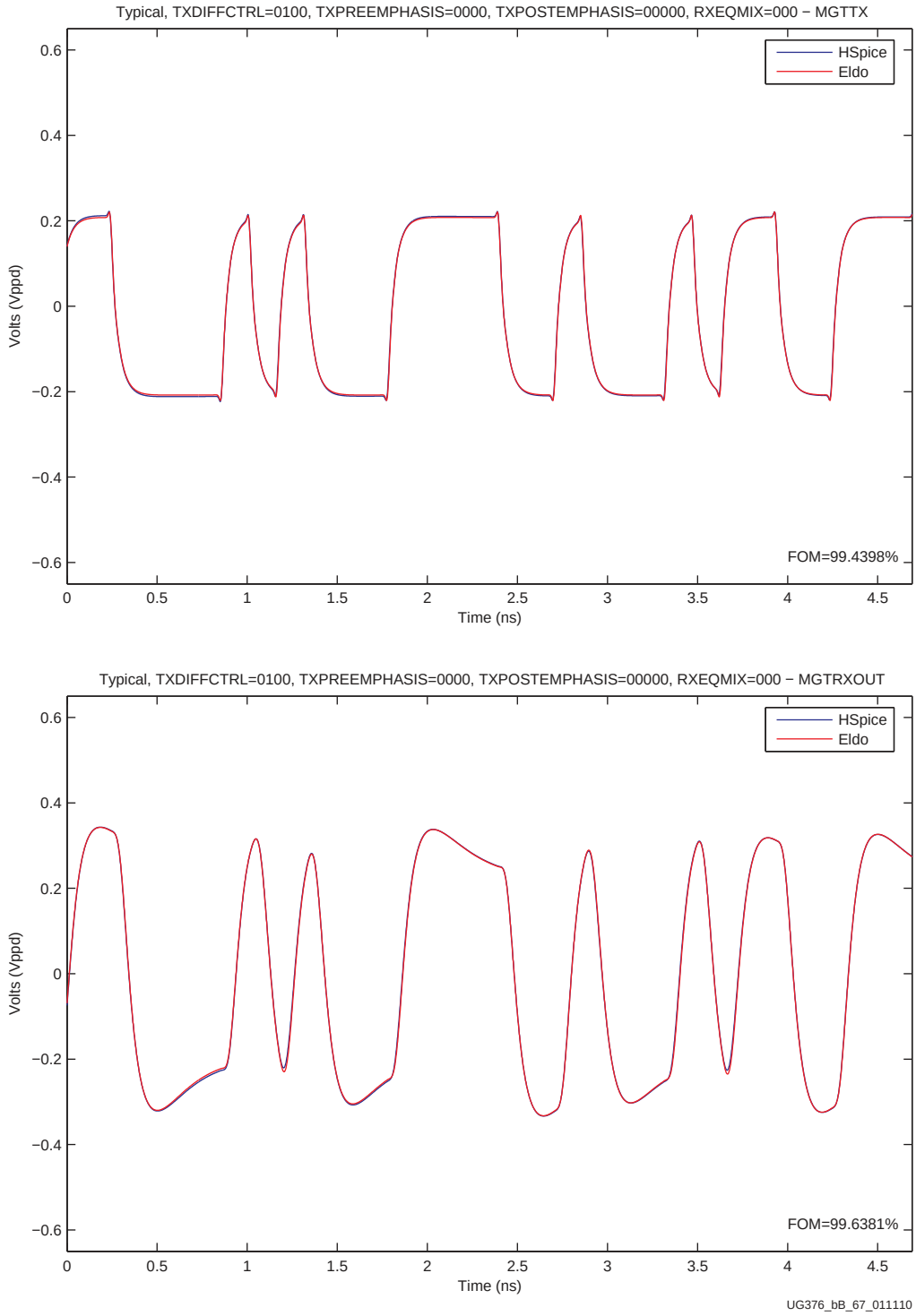

Figure B-5: **.tr1 TXDIFFCTRL = 0100, TXPREEMP = 0000, TXPOSTEMP = 00000, RXEQMIX = 000 (GTX Transceiver - Typical)**

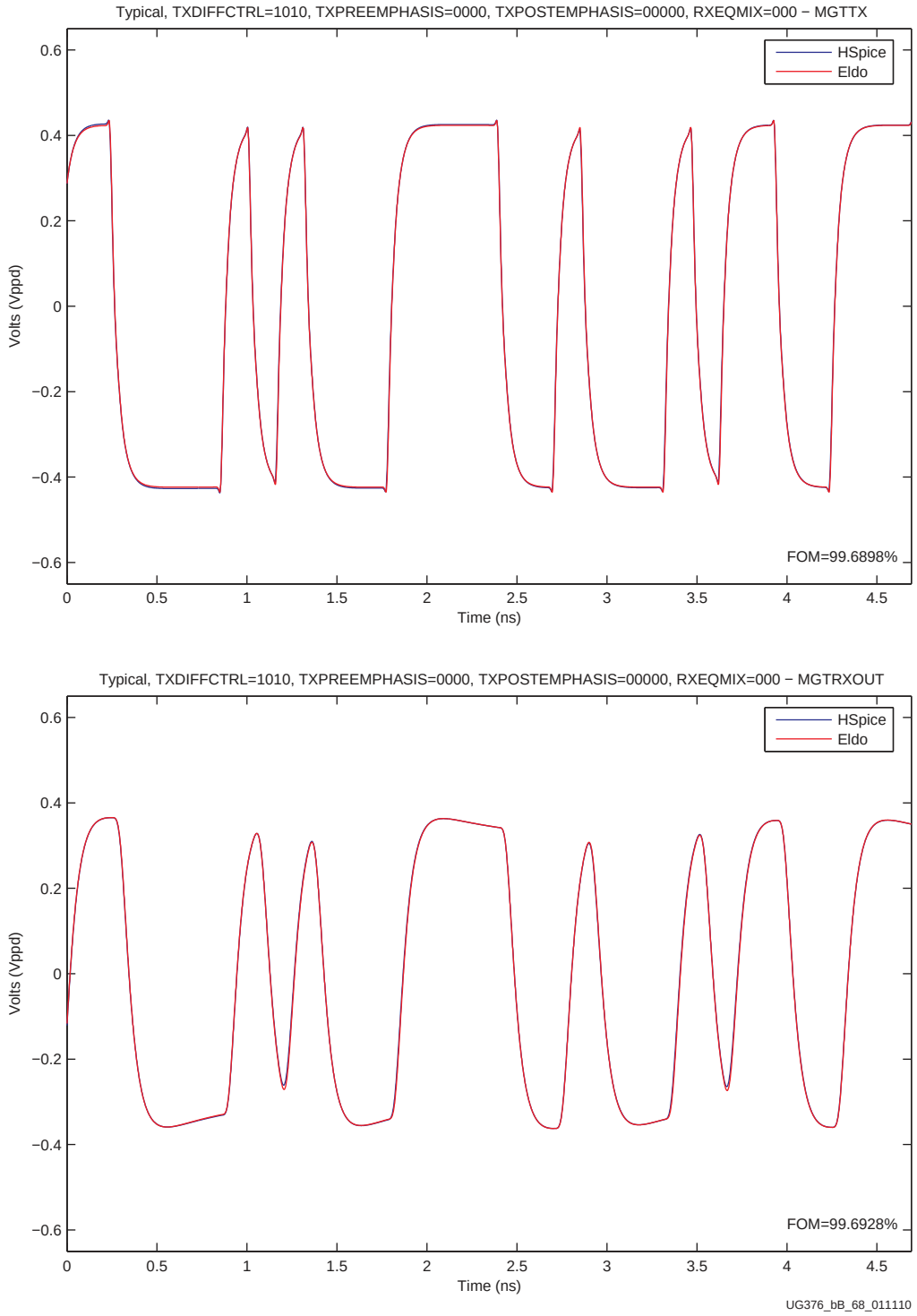

Figure B-6: **.tr2 TXDIFFCTRL = 1010, TXPREEMP = 0000, TXPOSTEMP = 00000, RXEQMIX = 000 (Typical - GTX Transceiver)**

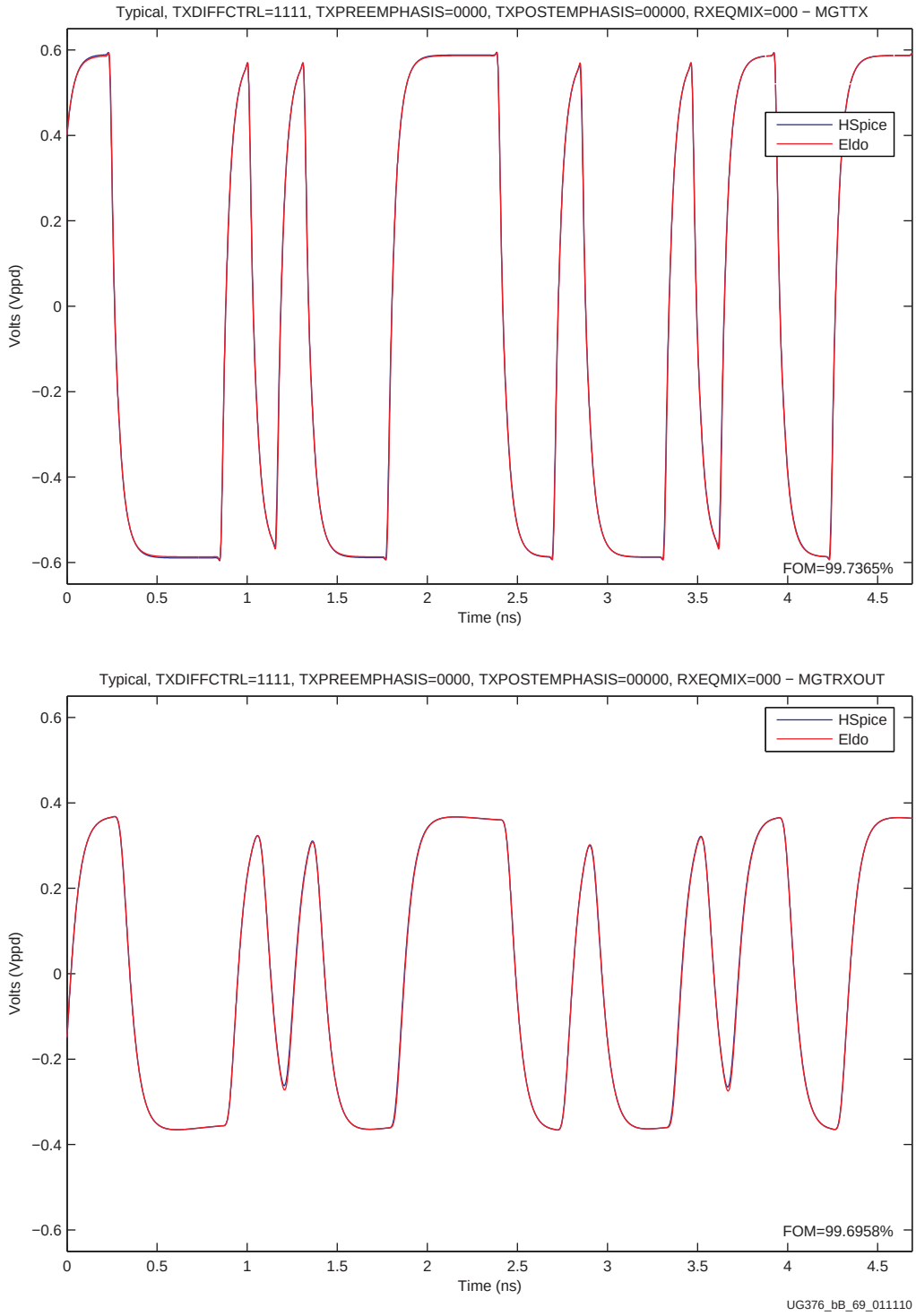

Figure B-7: **.tr3 TXDIFFCTRL = 1111, TXPREEMP = 0000, TXPOSTEMP = 00000, RXEQMIX = 000 (Typical - GTX Transceiver)**

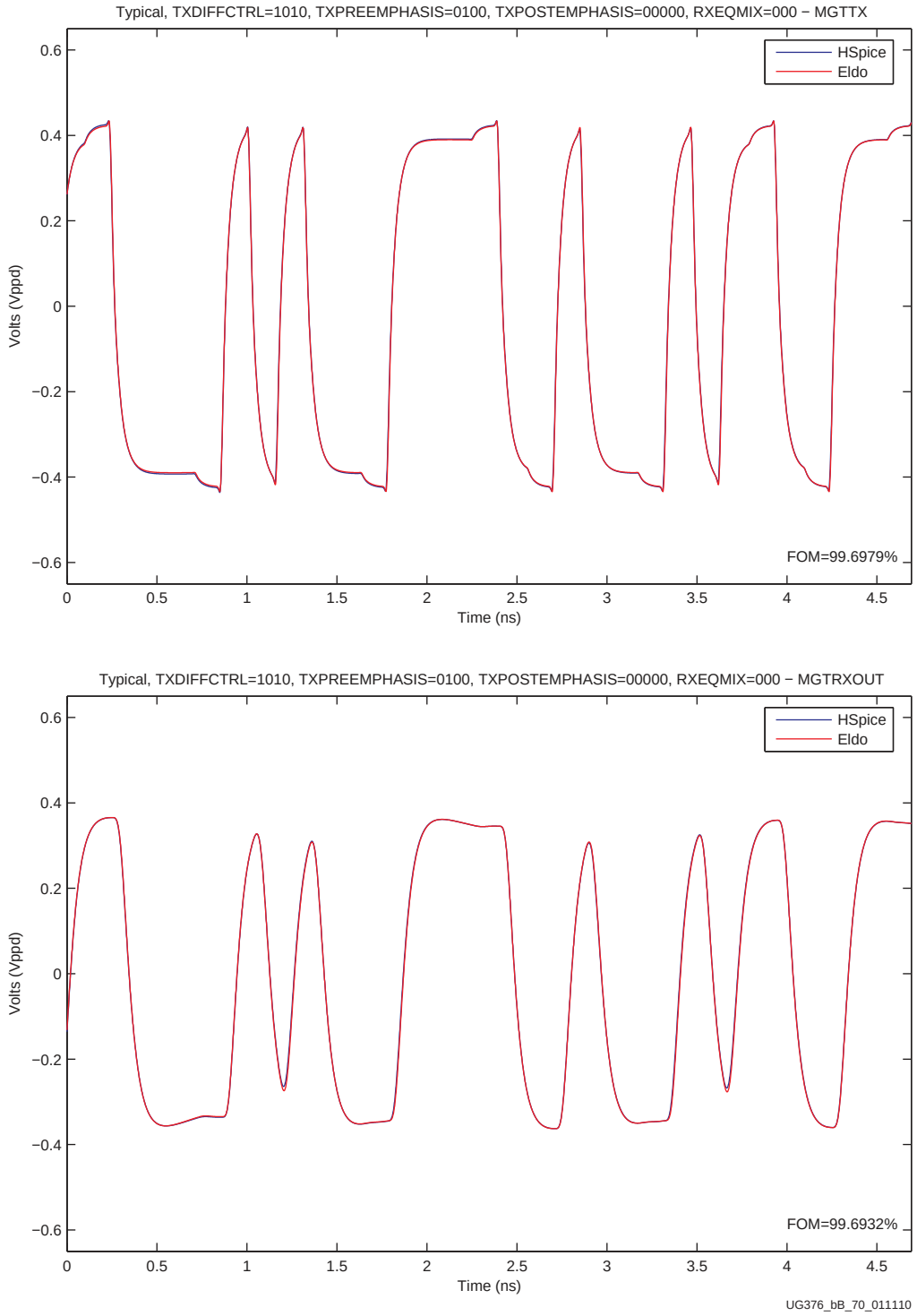

Figure B-8: **.tr4 TXDIFFCTRL = 1010, TXPREEMP = 0100, TXPOSTEMP = 00000, RXEQMIX = 000 (Typical - GTX Transceiver)**

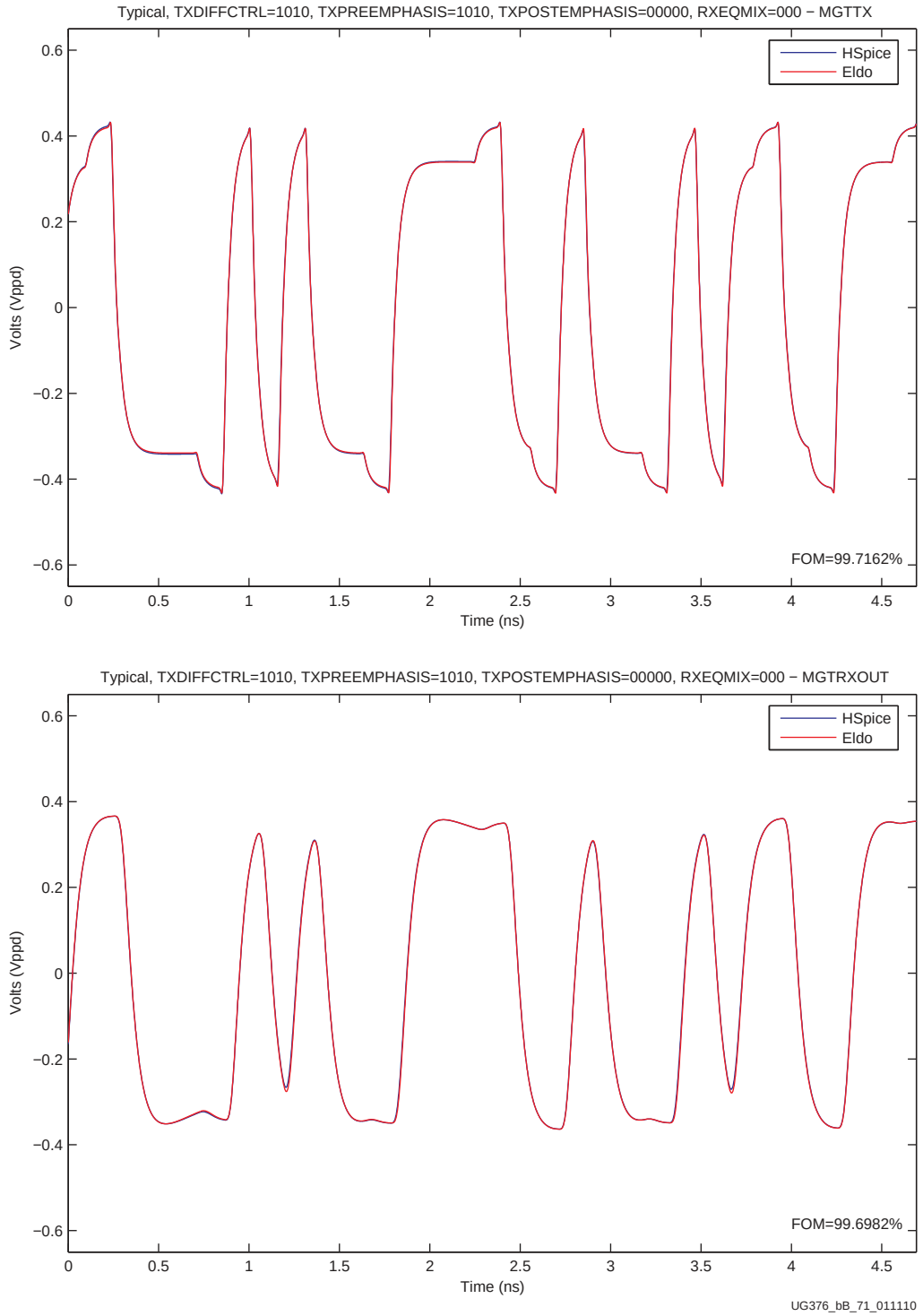

Figure B-9: **.tr5 TXDIFFCTRL = 1010, TXPREEMP = 1010, TXPOSTEMP = 00000, RXEQMIX = 000 (Typical - GTX Transceiver)**

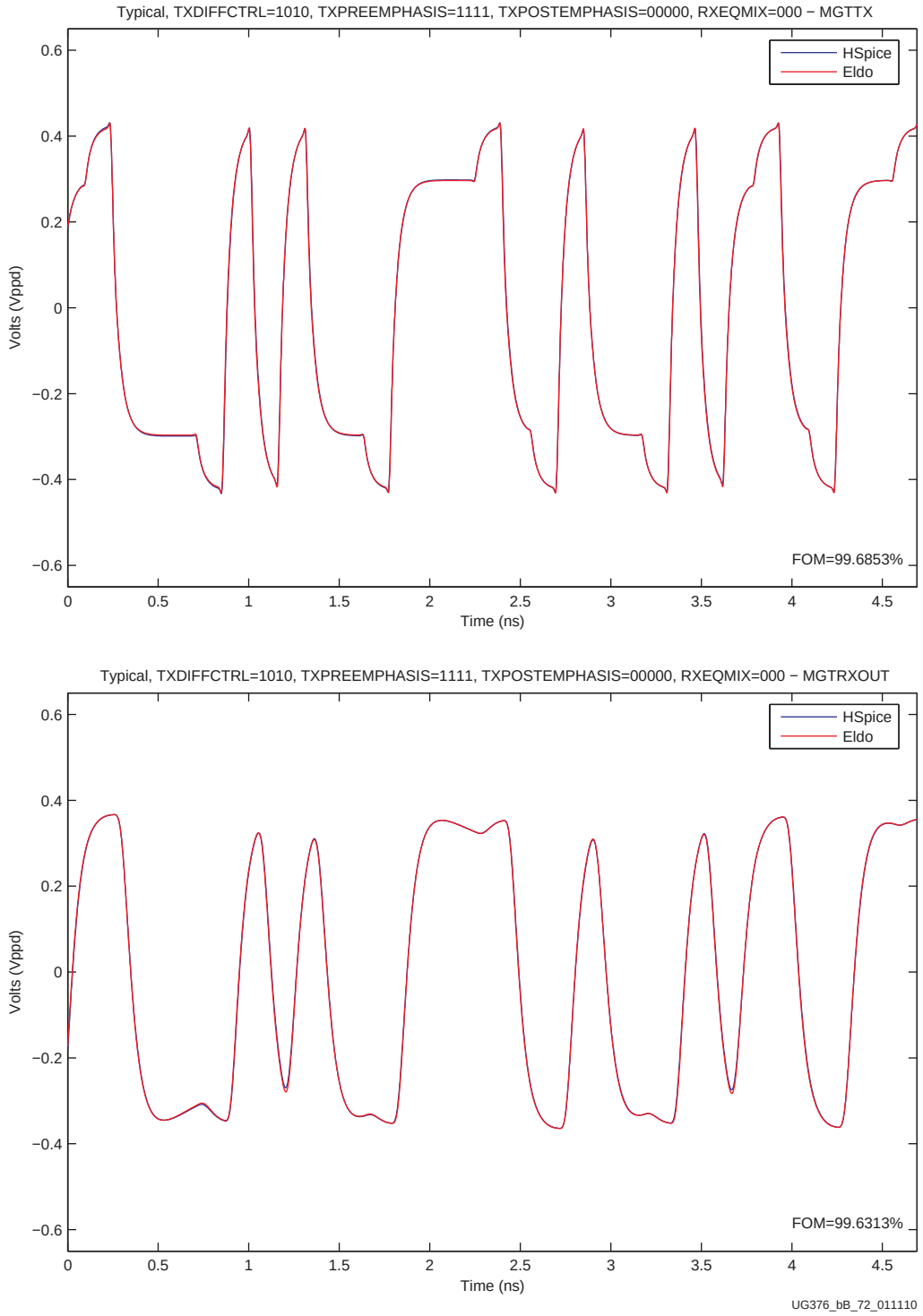

Figure B-10: **.tr6 TXDIFFCTRL = 1010, TXPREEMP = 1111, TXPOSTEMP = 00000, RXEQMIX = 000 (Typical - GTX Transceiver)**

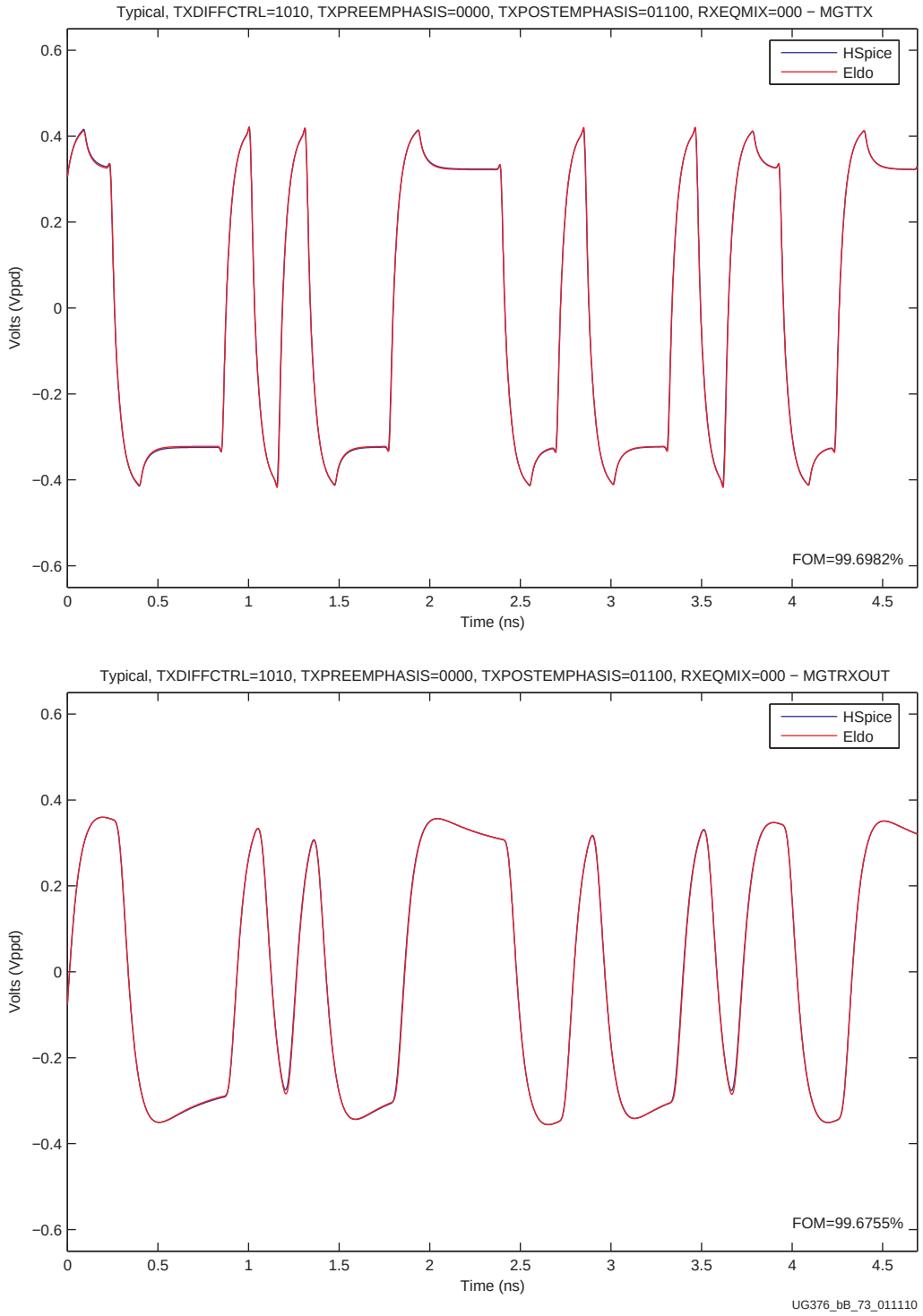

Figure B-11: **.tr7 TXDIFFCTRL = 1010, TXPREEMP = 0000, TXPOSTEMP = 01100, RXEQMIX = 000 (Typical - GTX Transceiver)**

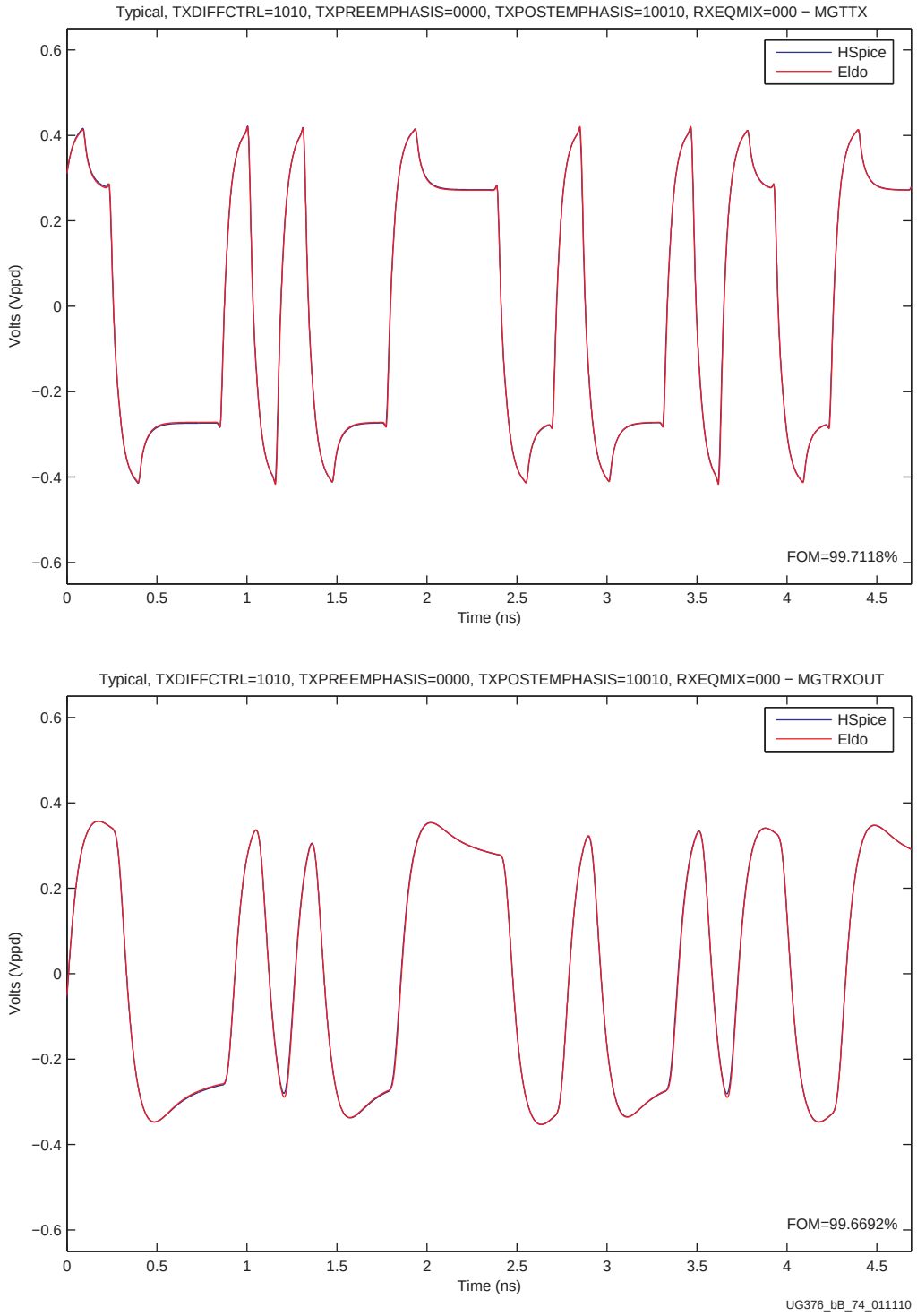

Figure B-12: **.tr8 TXDIFFCTRL = 1010, TXPREEMP = 0000, TXPOSTEMP = 10010, RXEQMIX = 000 (Typical - GTX Transceiver)**

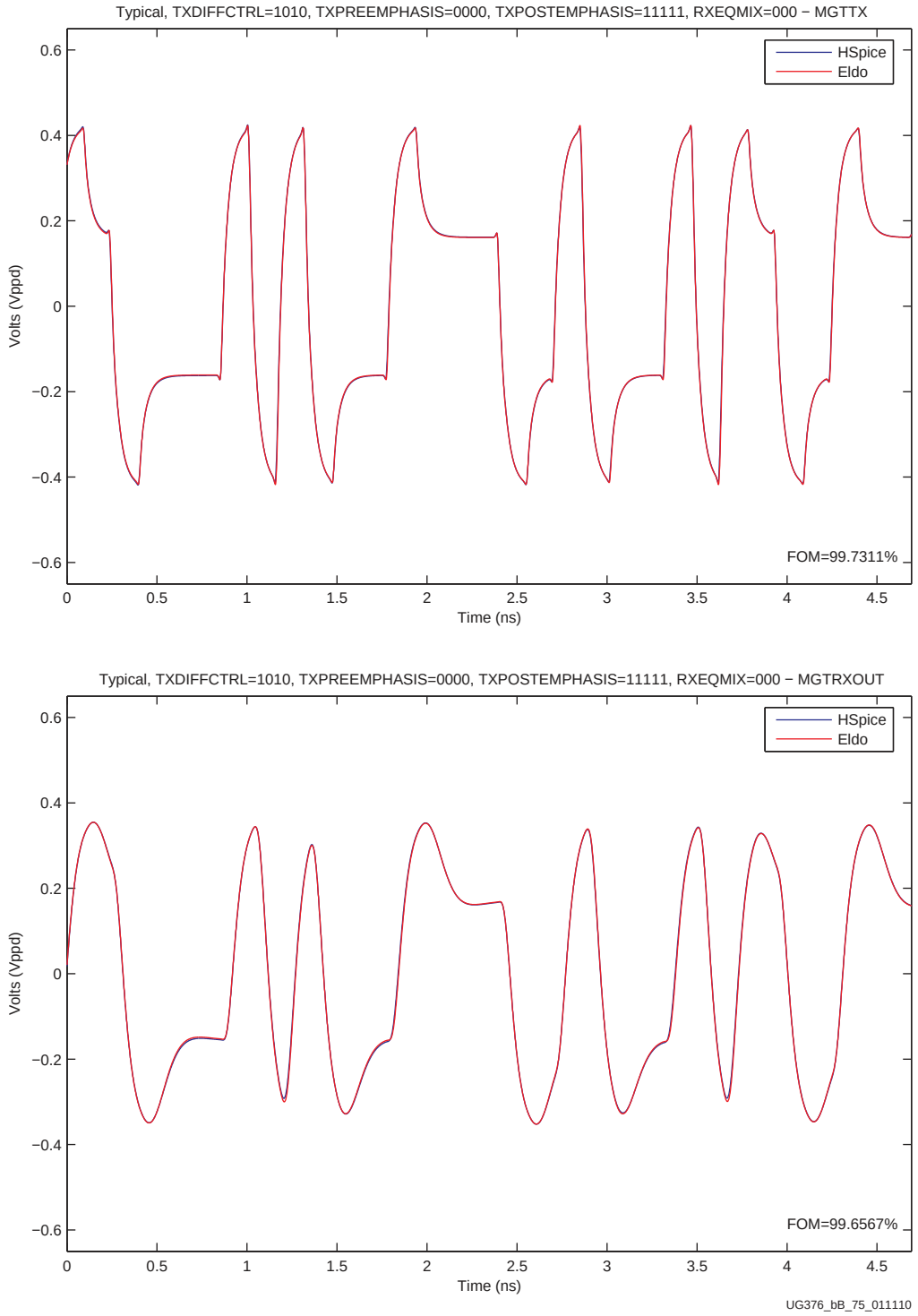

Figure B-13: **.tr9 TXDIFFCTRL = 1010, TXPREEMP = 0000, TXPOSTEMP = 11111, RXEQMIX = 000 (Typical - GTX Transceiver)**

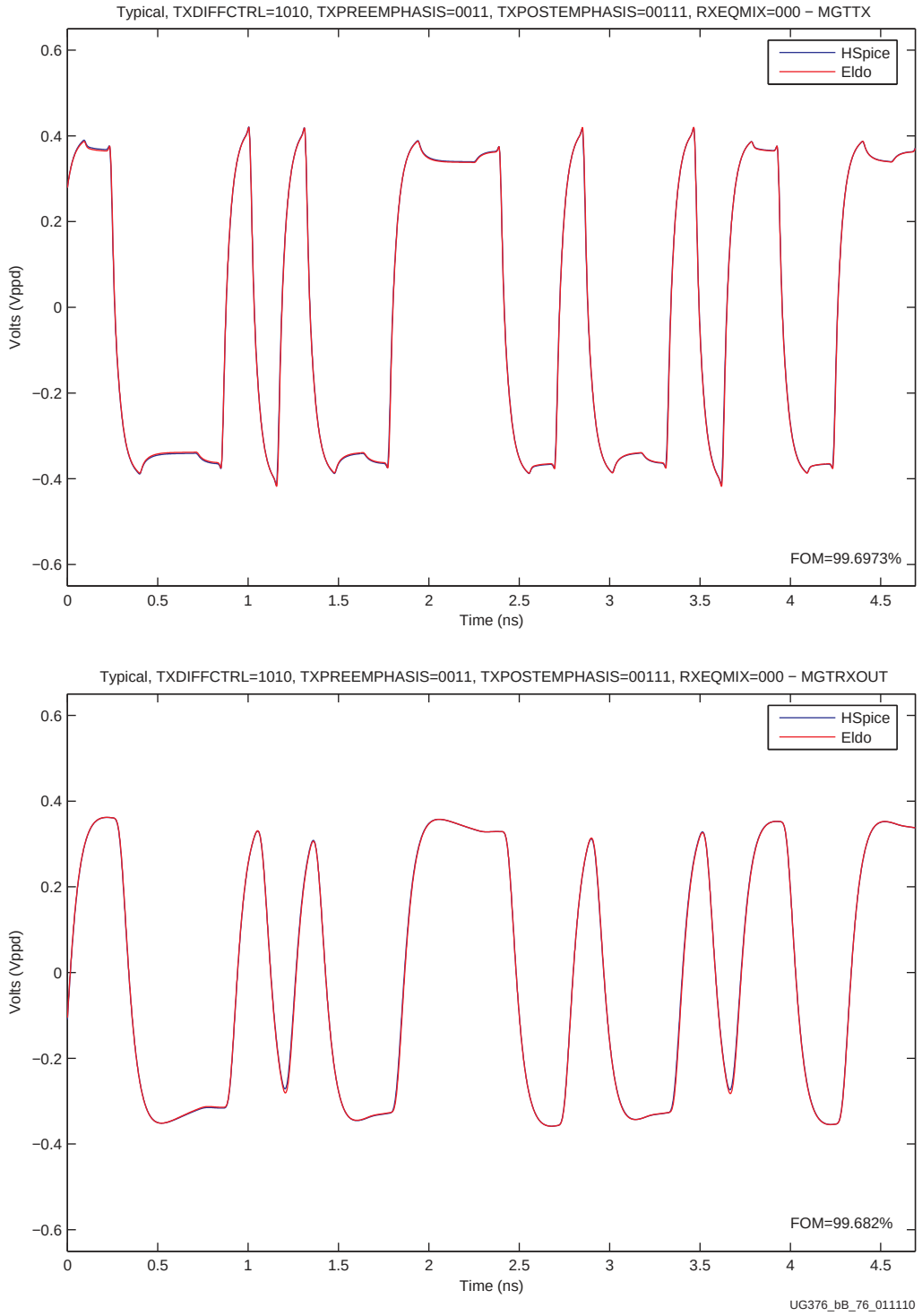

Figure B-14: **.tr10 TXDIFFCTRL = 1010, TXPREEMP = 0011, TXPOSTEMP = 00111, RXEQMIX = 000 (Typical - GTX Transceiver)**

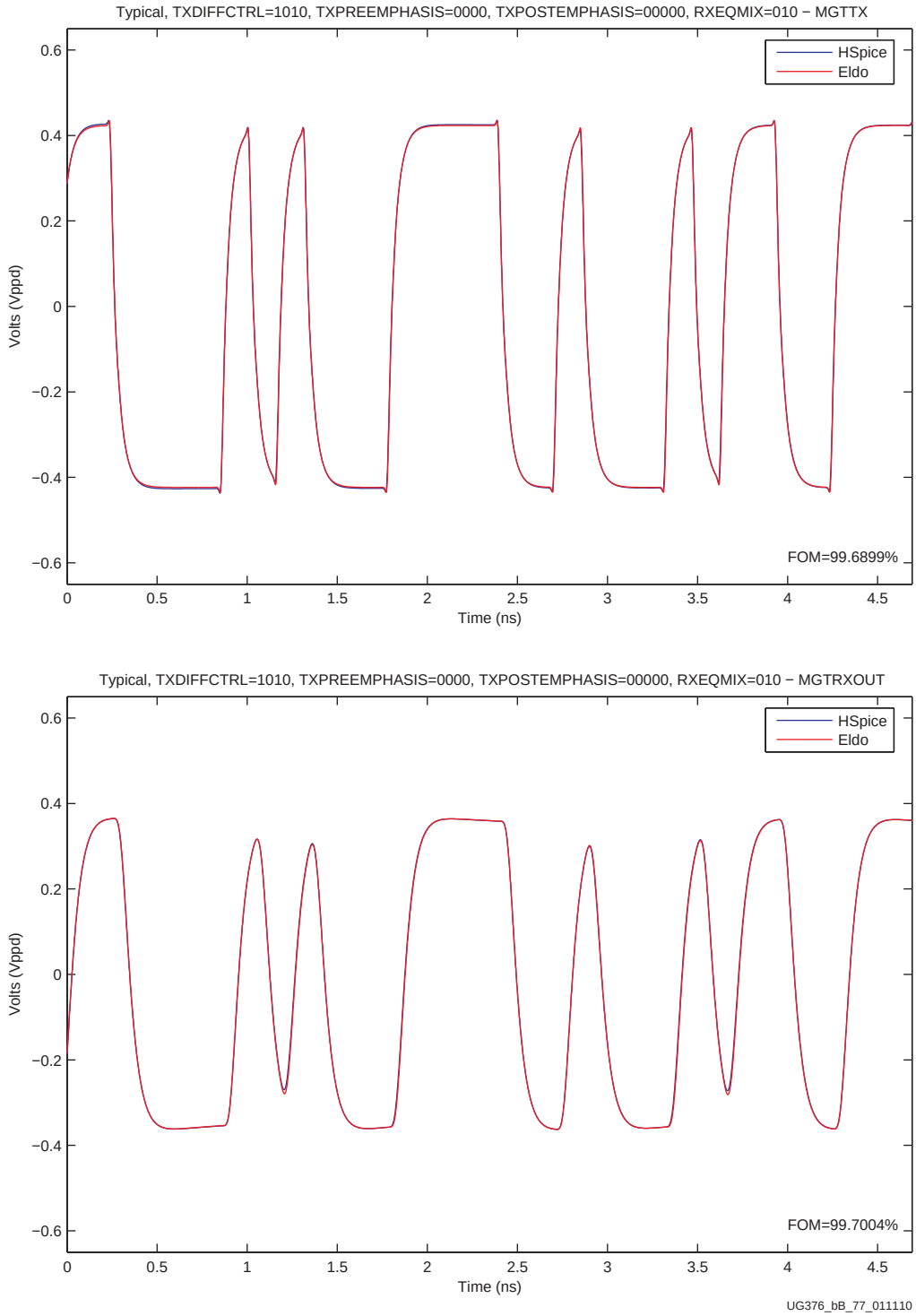

Figure B-15: **.tr11 TXDIFFCTRL = 1010, TXPREEMP = 0000, TXPOSTEMP = 00000, RXEQMIX = 010 (Typical - GTX Transceiver)**

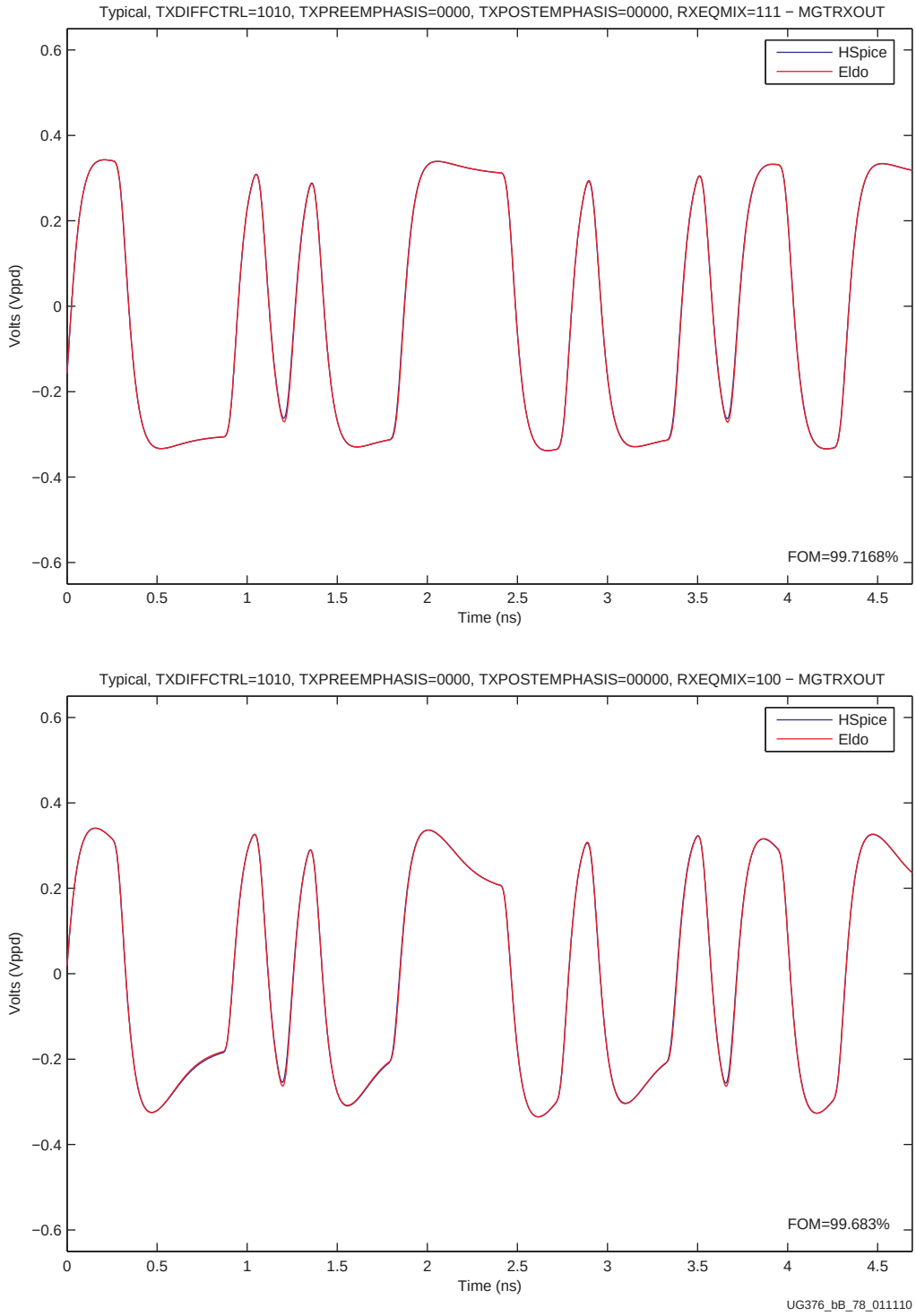

Figure B-16: **.tr12 TXDIFFCTRL = 1010, TXPREEMP = 0000, TXPOSTEMP = 00000, RXEQMIX = 100 (Typical - GTX Transceiver)**

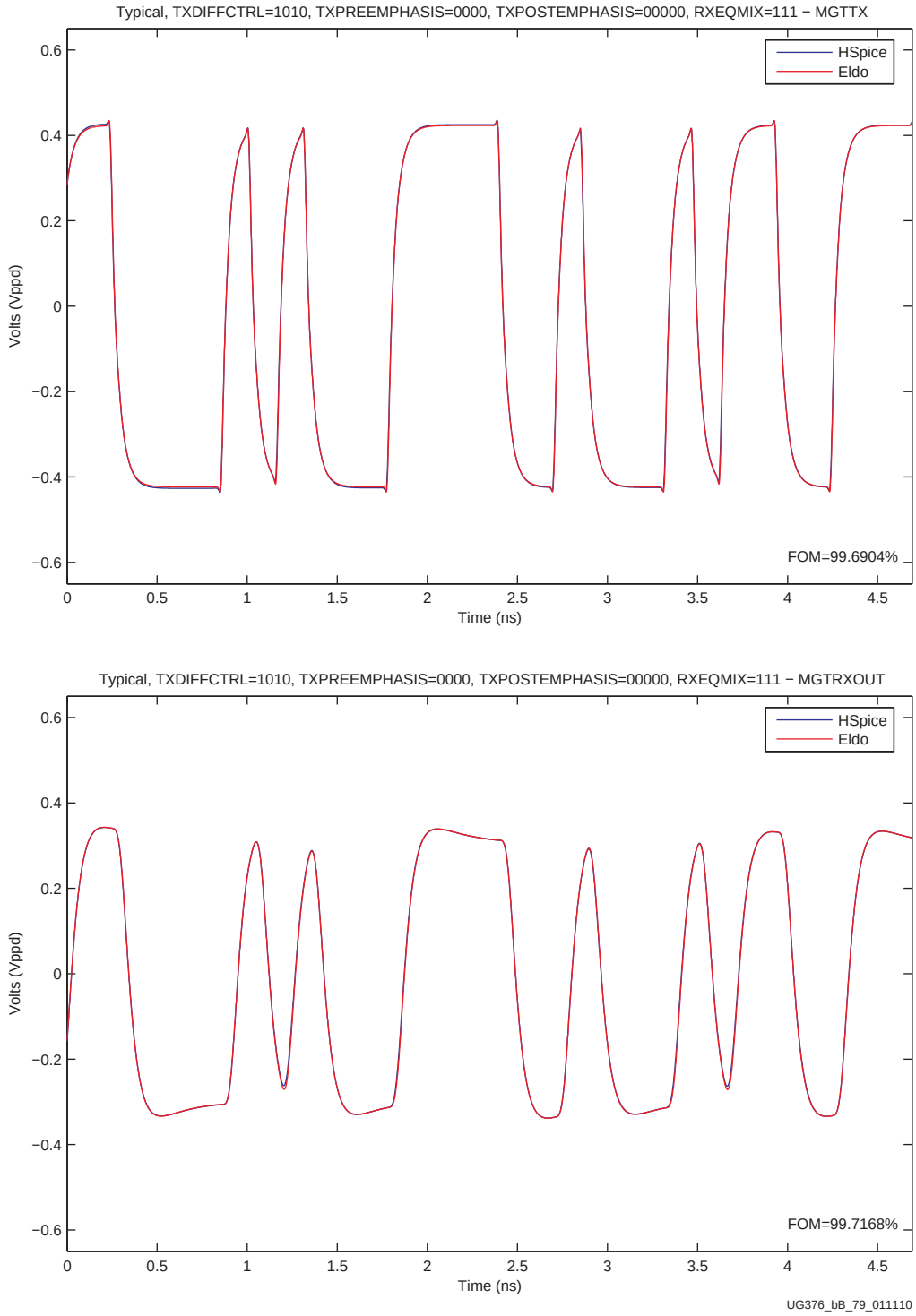

Figure B-17: **.tr13 TXDIFFCTRL = 1010, TXPREEMP = 0000, TXPOSTEMP = 00000, RXEQMIX = 111 (Typical - GTX Transceiver)**

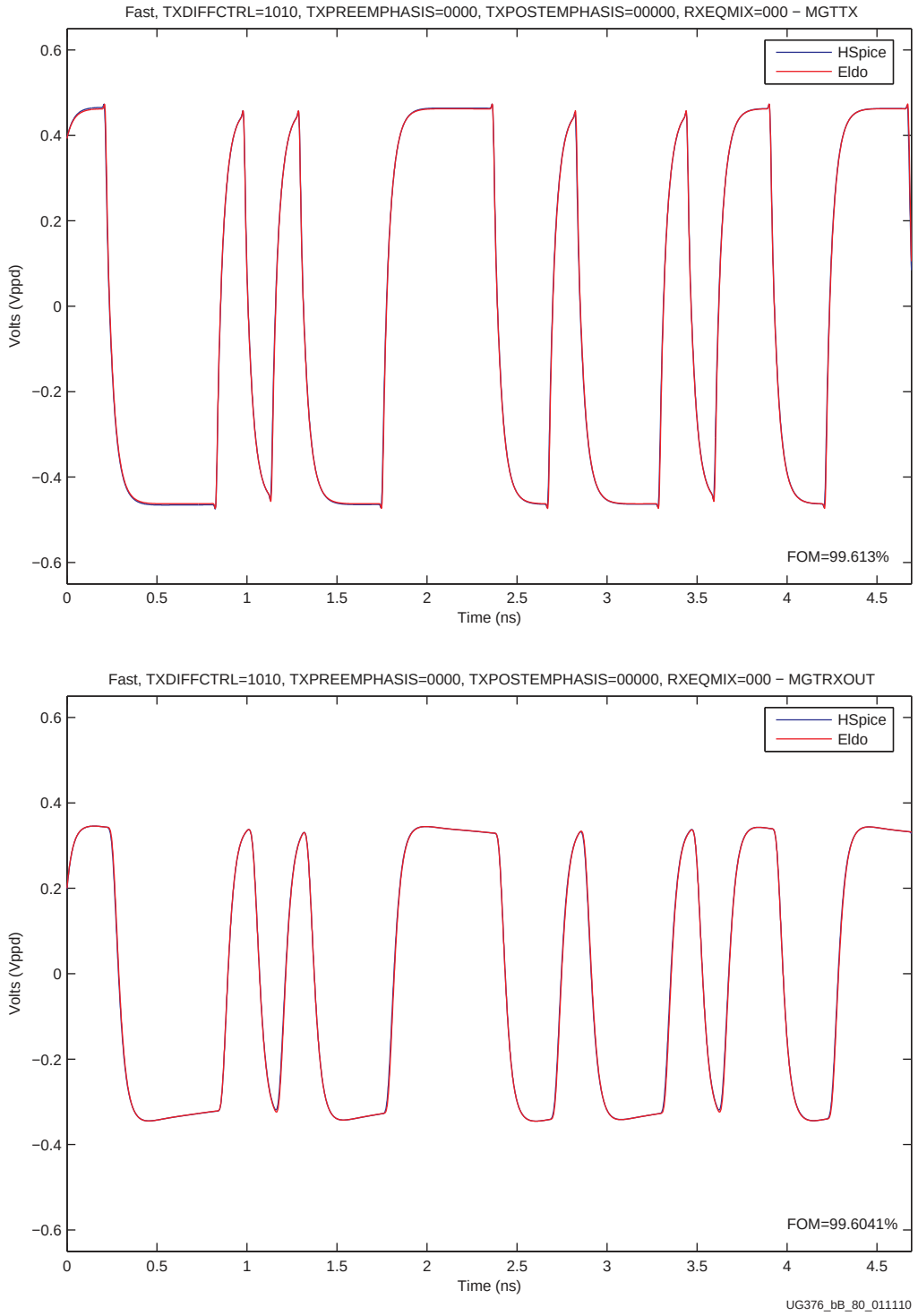

Figure B-18: **.tr14 TXDIFFCTRL = 1010, TXPREEMP = 0000, TXPOSTEMP = 00000, RXEQMIX = 000 (Fast - GTX Transceiver)**

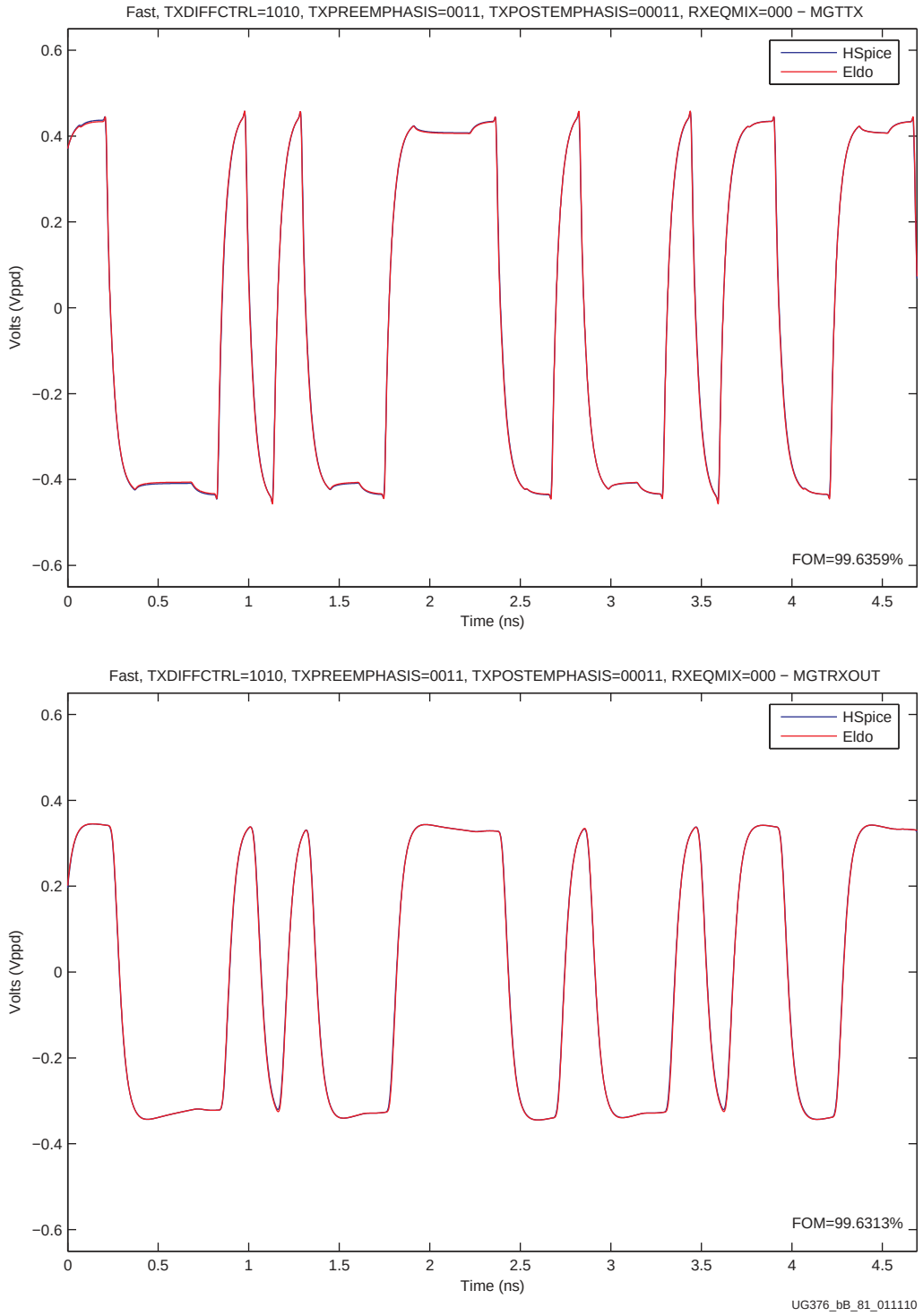

Figure B-19: **.tr15 TXDIFFCTRL = 1010, TXPREEMP = 0011, TXPOSTEMP = 00011, RXEQMIX = 000 (Fast - GTX Transceiver)**

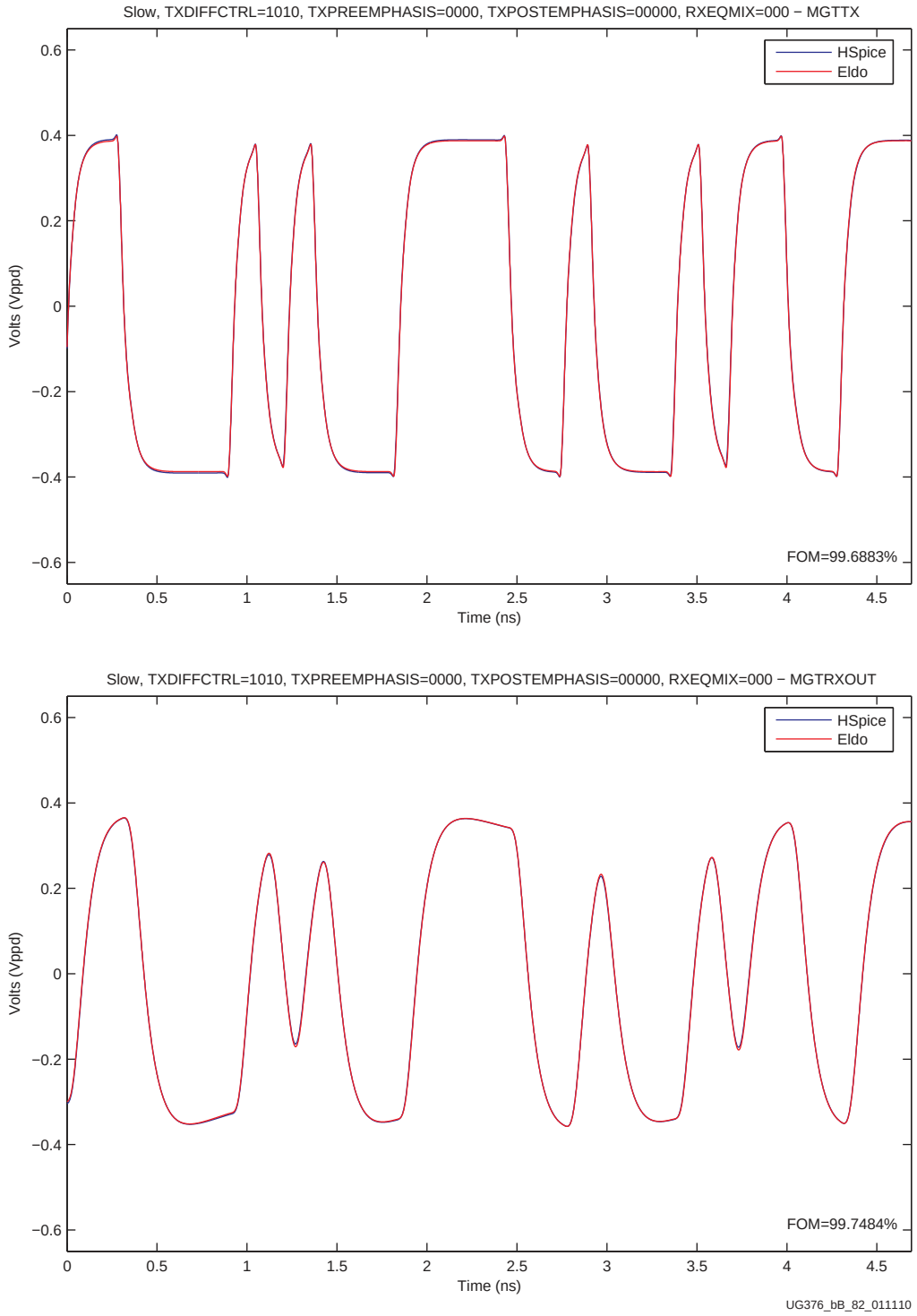

Figure B-20: **.tr16 TXDIFFCTRL = 1010, TXPREEMP = 0000, TXPOSTEMP = 00000, RXEQMIX = 000 (Slow - GTX Transceiver)**

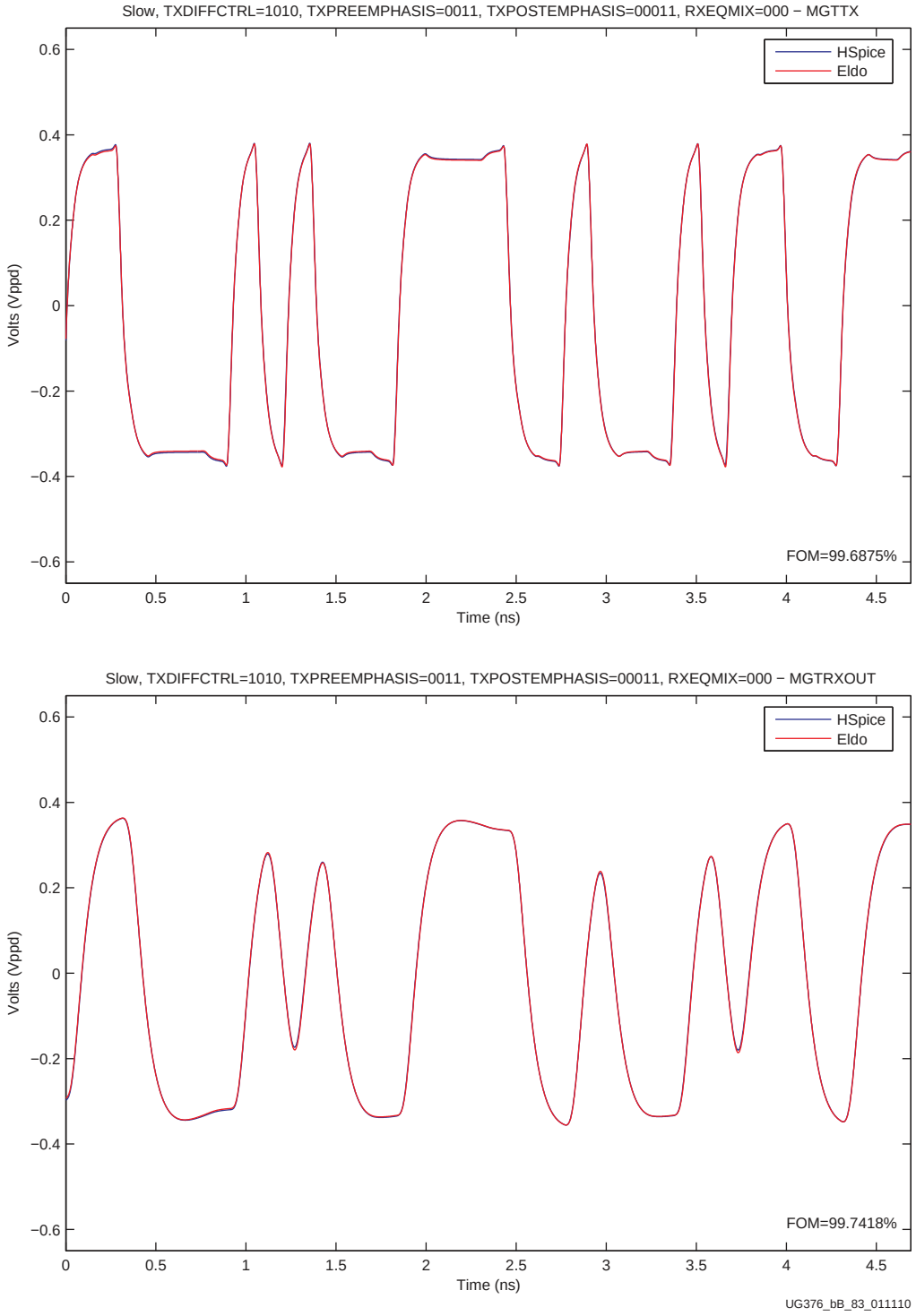

Figure B-21: **.tr17 TXDIFFCTRL = 1010, TXPREEMP = 0011, TXPOSTEMP = 00011, RXEQMIX = 000 (Slow - GTX Transceiver)**