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Negative-Bias Temperature Instability (NBTI) Effects in 90 nm PMOS

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This paper describes Negative-Bias Instability (NBTI), an unwanted transistor behavior that is pervasive in all deep sub-micron designs. It also describes how Xilinx has proactively addressed this challenging behavior.

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Introduction

A gradual shift of threshold voltage (V_T) over time is commonly observed in p type metal-oxide-semiconductor field-effect transistors (p-MOSFET or PMOS). This shift is caused by: voltage stress on the gate oxide, temperature, and the duty cycle of the stressing voltage (static stress as compared to dynamic stress). Known since 1961, this effect has become more severe as:

- Transistor dimensions have shrunk.
- The electric field applied to the gate oxide has increased.
- The operating voltage has become lower (making a given threshold shift cause a relatively larger impact on the circuit behavior).

All advanced fabrication processes that use PMOS transistors experience this effect.

What is the NBTI Effect?

The semiconductor process evolution that produces small transistors increases the potential for interface traps in PMOS transistors during prolonged times of negative bias stress. An interface trap is created when a negative voltage is applied to the gate of a PMOS device for a prolonged time (see Figure 1). An interface trap is located near the Si-oxide/Si-crystal lattice boundary where *holes* (positive charge) can get stuck, and in doing so, they shift the threshold voltage. This hole trapping creates interface states as well as fixed charges. Both are positive charges and result in a negative shift of threshold voltage. This phenomenon is called PMOS Negative Bias Temperature Instability (NBTI). NMOS transistors are far less affected because interface states and fixed charges are of opposite polarity and eventually cancel each other.
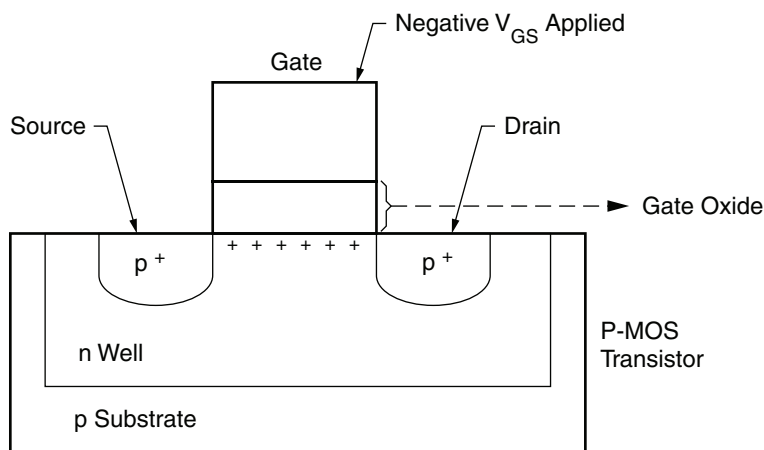
Figure 1: **PMOS Transistor**

NBTI can determine the useful lifetime of complementary metal-oxide semiconductor (CMOS) devices. The designer must consider the bias conditions of each PMOS transistor, not only at the beginning of life but throughout the expected lifetime of the product [Ref 1]. Typically, these conditions must allow for at least ten years of operation at the highest voltage and the highest temperature. Removal of power allows for some release (annealing) of the trapped charges [Ref 2].

Static stress shifts the voltage threshold roughly ten times more than does dynamic stress [Ref 3]. For example, a shift of 10 mV can occur in a dynamic (switching) situation, and a shift of 100 mV can occur in the static case.

How are NBTI Effects Measured?

To perform an NBTI study of a PMOS transistor, a constant negative bias is applied to the gate electrode at high temperatures, with source, drain, and substrate grounded. To perform the equivalent study on a complete FPGA device requires the device to be cycled through all of its possible operating conditions (both static and dynamic) and tested at elevated temperatures and voltages.

The gate bias of a PMOS in a CMOS inverter is either at a high or low voltage, while the drain bias is either low or high. It is important to investigate NBTI under such static (stuck at *1* or *0*), as well as dynamic stress conditions.

Virtex-4 NBTI Characterization

The Virtex™-4 FPGA was designed and simulated with an understanding that the NBTI effect would be present on all PMOS transistors. NBTI affects not only the 250 nm I/O transistors, but also the mid-oxide 100 nm memory and pass gate devices, and the 90 nm logic circuits. It affects only the PMOS transistors and not the NMOS transistors.

Simulations showed that the fabric speed decreases by about 3% over the lifetime of the part under the worst case static condition. Speed binning margins were increased to guarantee specifications at end-of-life.

Virtex-4 sub-circuits were also simulated under beginning and end-of-life conditions to verify that the designs are fully robust through the inevitable PMOS gate threshold voltage shifts that occur during the operating life of the product [Ref 1].

During qualification testing, the device was operated at voltages and temperatures well beyond the absolute maximum ratings in order to accelerate the aging of the device. This procedure ensures that the design meets its lifetime expectations under the worst case conditions allowed in the DS302: *Virtex-4 Data Sheet*.

Results of NBTI Qualification Testing

The accelerated stress qualification testing showed that the DCM maximum operating frequency decreases if the DCM is held in a persistent static (non-operational) condition for an extended time. This means that the DCM might not achieve Lock up to the maximum frequency specifications. The Virtex-4 DCM is a high-frequency digital circuit, leveraging 90 nm advances and advanced circuit techniques in order to achieve picosecond precision and provide a wide range of advanced clock management features. Each DCM contains over a dozen finely tuned, multi-tap delay lines. Static NBTI stress creates small variations in the duty cycle precision of each delay tap. Cumulatively, this variation reduces the maximum frequency at which the DCM can operate. Dynamic NBTI stress, however, does not lead to any reduction in performance because any voltage shift is applied equally to both of the matched PMOS transistors in each delay tap. Therefore, full performance is maintained if the DCM is placed into a continuous calibration mode (effectively toggling all delay taps) during periods of non-operation.

The Virtex-4 DCM Solution for NBTI Effects

Xilinx has fully addressed all aspects of the NBTI effect on the Virtex-4 DCM and offers several solutions. These solutions avoid static NBTI stress either directly or by placing the DCM into a continuous calibration mode during periods of non-operation:

1. Static device burn-in (where the device is powered but unconfigured) is not permitted. Dynamic device burn-in (where the device is both powered and configured) is permitted as long as the DCMs are properly operated per the items below.

2. If for any reason the device might be powered but stays unconfigured for an extended time (see new specifications in the Virtex-4 data sheet), then a *null design*, provided by Xilinx, must be loaded. The null design configures the DCMs into continuous calibration mode.

3. If the DCM input clocks might stop for an extended time (see new specifications in the Virtex-4 data sheet), then a drop-in macro is available to support longer durations.

4. If the DCM reset might be held asserted for an extended time (see new specifications in the Virtex-4 data sheet), then a drop-in macro is available to support longer durations.

5. Unused DCMs in designs are automatically configured into continuous calibration mode by the ISE 7.1i SP4 software.

Virtex-4 LX/SX stepping 2 production silicon has been updated, removing the need for all of these solutions except #3 and #5. Unused DCMs (#5) continue to be handled automatically by the software. Additionally, when using LX/SX stepping 2 devices, ISE 7.1i SP4 and later software inserts a small amount of logic (~15 slices) along with each instantiated DCM to automatically facilitate # 3. And all designs must continue to be compiled using ISE 7.1i SP4 software (or later versions).

Summary

NBTI stresses, which shift PMOS transistor threshold voltages, have become more prominent as transistor geometries reach 90 nm and below. These effects were monitored in the design, simulation, and testing of Virtex-4 FPGAs. Full solutions have been provided for the DCM sensitivity. Following the solutions provided by Xilinx ensures that the DCM continues to meet maximum frequency specifications.

References and Resources

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/13/05	1.0	Initial Xilinx release.
11/21/05	1.1	Updated speed file/service pack information and made typographical edits.