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Memory Interface Application Notes Overview

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Summary

This document provides an overview of all Xilinx memory interface application notes that support Virtex™ series and Spartan™ series FPGAs. In addition, some key features of the prevalent memory technologies are also provided. For each application note, the data capture technique, clocking scheme, FPGA resources used, and supported memory technology are described briefly.

Introduction

Memory interfaces are source-synchronous interfaces where the clock/strobe and data being transmitted from a memory device are edge aligned. Most memory interface and controller vendors leave the read data capture implementation as an exercise for the user. In fact, the read data capture implementation in FPGAs is the most challenging portion of the design. Xilinx provides multiple read data capture techniques for different memory technologies and performance requirements. All of these techniques are implemented and verified in Xilinx FPGAs.

The following sections provide a brief overview of prevalent memory technologies.

Double Data Rate Synchronous Dynamic Random Access Memory

Key features of Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM) memories include:

- Source synchronous read and write interfaces using the SSTL-2.5V Class I/II I/O standard
- Data available both on the positive and negative edges of the strobe
- Bidirectional, non-free-running, single-ended strobes that are output edge aligned with read data, and must be input center aligned with write data
- One strobe per 4 or 8 data bits
- Data bus widths varying between 8, 16, and 32 for components, and 32, 64, and 72 for DIMMs
- Reads and writes with burst lengths of 2, 4, or 8 data words are supported, where each data word is equal to the data bus width
- Read latency of 2, 2.5, or 3 clock cycles, with frequencies of 100 MHz, 133 MHz, 166 MHz, and 200 MHz
- Row activation required before accessing column addresses in an inactive row
- Refresh cycles required every 7.8 µs
- Initialization sequence required after power on and before normal operation

Double Data Rate Synchronous Dynamic Random Access Memory

Key features of Double Data Rate Synchronous Dynamic Random Access Memory (DDR2 SDRAM) memories, the second generation DDR SDRAMs, include:

- Source synchronous read and write interfaces using the SSTL-1.8V Class I/II I/O standard
- Data available both on the positive and negative edges of the strobe
- Bidirectional, non-free-running, differential strobes that are output edge aligned with read data, and must be input center aligned with write data
- One differential strobe pair per 4 or 8 data bits
- Data bus widths varying between 4, 8, and 16 for components, and 64 and 72 for DIMMs
- Reads and writes with burst lengths of 4, or 8 data words are supported, where each data word is equal to the data bus width

- Read latency is a minimum of three clock cycles, with frequencies ranging from 200 MHz, to 400 MHz
- Row activation before accessing column addresses in an inactive row
- Refresh cycles required every 7.8 µs
- Initialization sequence required after power on and before normal operation

Design Challenges with DDR or DDR 2 SDRAM

The non-free-running strobes and the edge-aligned read data provided by these memories make it challenging to implement the read data capture interface in FPGAs. Figure 1 shows a timing diagram during a read operation. Depending on performance requirements, a few different read data capture techniques can be employed. Details of these techniques are provided in the application notes listed in Table 1.

- For low frequency (100 MHz) interfaces, the read memory strobe can be ignored and DCM phase-shifted outputs can be used instead. A block diagram of the data capture using DCM phase-shifted outputs is shown in Figure 2.
- For higher frequencies (133 MHz to 200 MHz), the read memory strobe must be used for higher margins. To center it in the data window for data capture, the strobe must be delayed. The delayed strobe is distributed in the FPGA using local clocking resources.
  - Externally delayed strobe using discrete delay components or additional trace lengths on the PCB (as shown in Figure 3)
  - Internally delayed strobe in the FPGA using continuously calibrated delay elements
    - Read data capture in CLB flip-flops (as shown in Figure 4)
    - Read data capture in LUT RAM FIFO (as shown in Figure 5)
- For high frequencies, Virtex™-4 devices have 64-tap absolute delay elements built into each I/O, called IDELAY blocks. The resolution of each tap is approximately 75 ps over process, voltage, and temperature. This feature provides flexibility and makes read data capture easy.
  - Direct clocking technique for data capture delays read data such that the FPGA clock is centered in the valid data window. The read memory strobe is used to determine the amount of read data delay. The read data delay is determined by detecting the phase relationship between the memory strobe and the FPGA clock. (Figure 6 shows the block diagram.)
  - With the SERDES technique, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the ISERDES. The IDELAY element is used to delay read strobe to center in the read data window. Both read strobe and data are further delayed to align to the FPGA clock domain. The received serial, double data rate (DDR) read data is converted to 4-bit parallel single data rate (SDR) data at half the frequency of the interface using the ISERDES. The differential strobe is placed on a clock-capable I/O pair in order to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data ISERDES clock inputs. Figure 7 shows the block diagram for the SERDES data capture technique in Virtex-4 devices.
- For high frequencies, Virtex-5 devices, like Virtex-4 devices, have 64-tap absolute delay elements (IDELAY) and an input Serializer-Deserializer (ISERDES) built into each I/O. The resolution of each tap is 75 ps over process, voltage, and temperature. This feature provides flexibility and makes read data capture easy.
  - In this technique, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the ISERDES. The IDELAY element is used to delay read strobe to center in the read data window. Both read strobe and data are further delayed to align to the FPGA clock domain. The received serial, DDR read data is converted to 2-bit parallel SDR data at the frequency of the interface using the ISERDES. The differential strobe is placed on a clock-capable I/O pair in order to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data ISERDES clock inputs. Figure 8 shows the block diagram of the SERDES data capture technique in Virtex-5 devices.

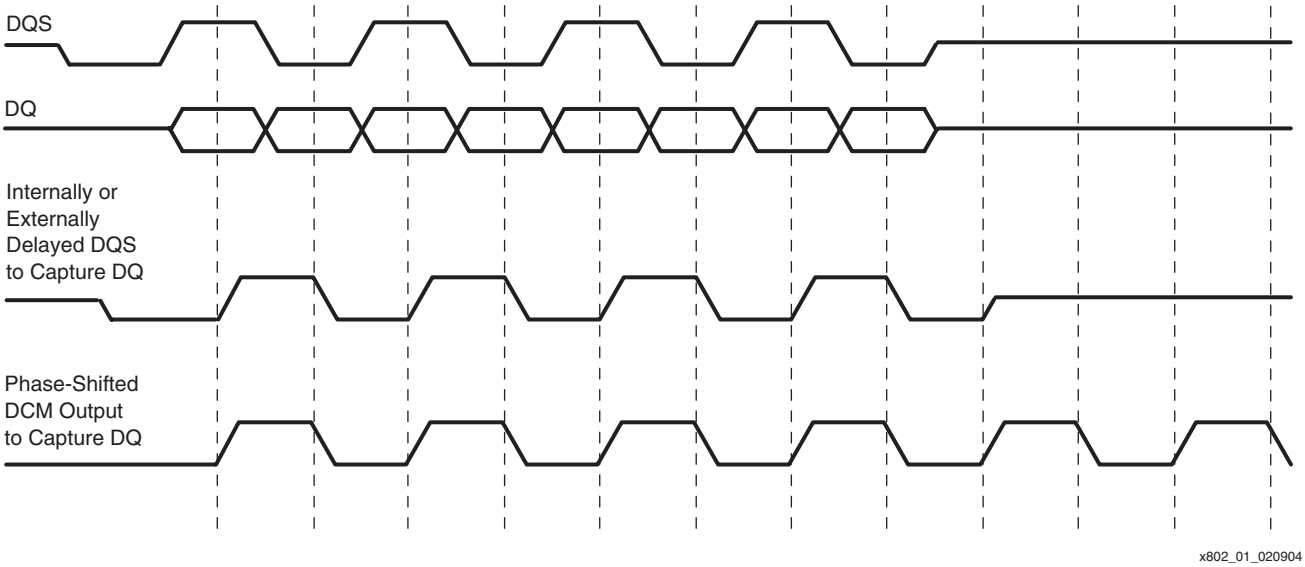

Figure 1: **Read Operation Timing Diagram**

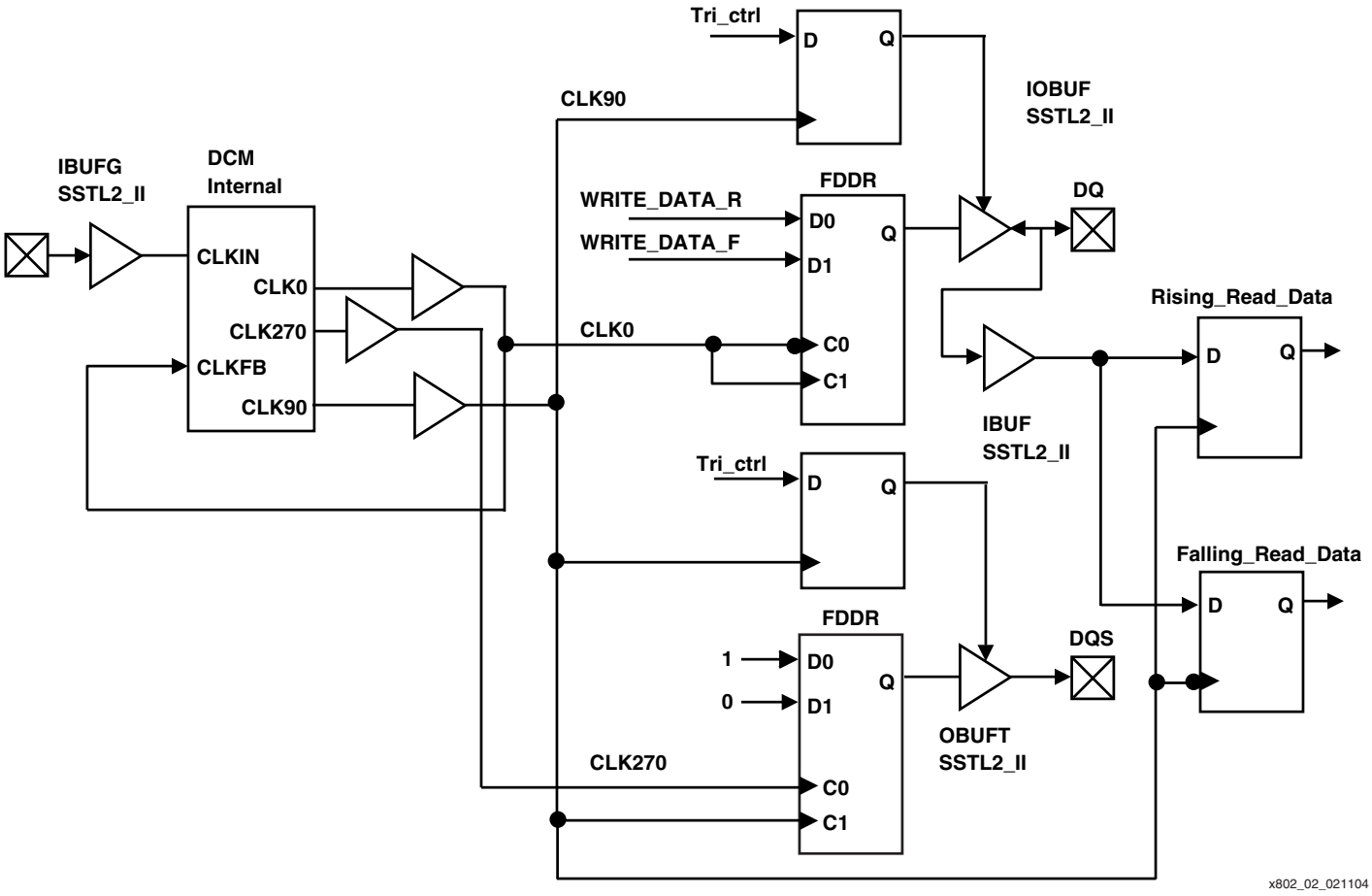

Figure 2: **Data Capture in IOB Flip-Flops Using Phase-Shifted DCM Outputs**

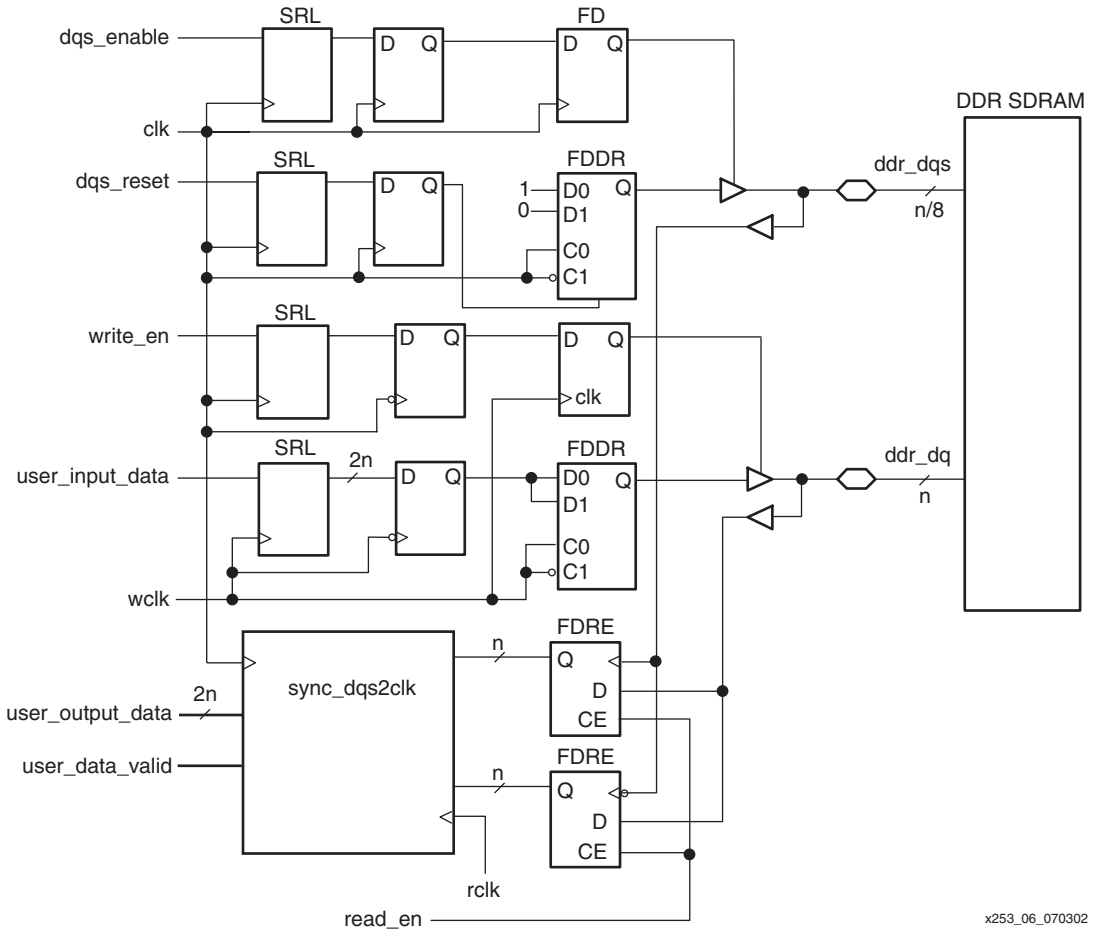

Figure 3: **Data Capture in IOB Flip-Flops Using Externally Delayed DQS**

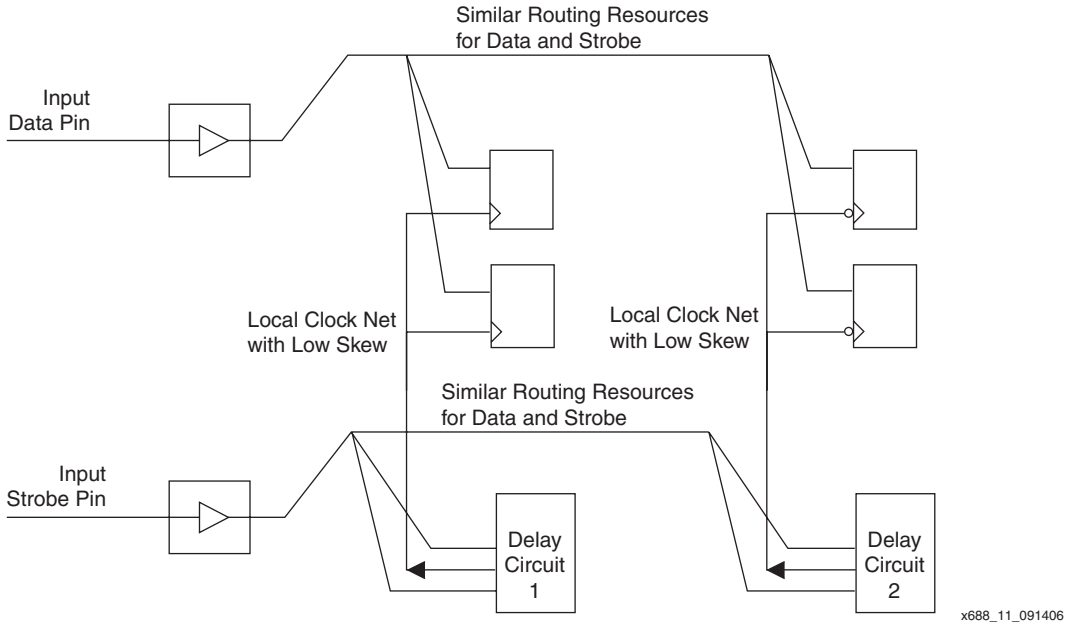

Figure 4: **Data Capture in CLB Flip-Flops Using Internally Delayed DQS**

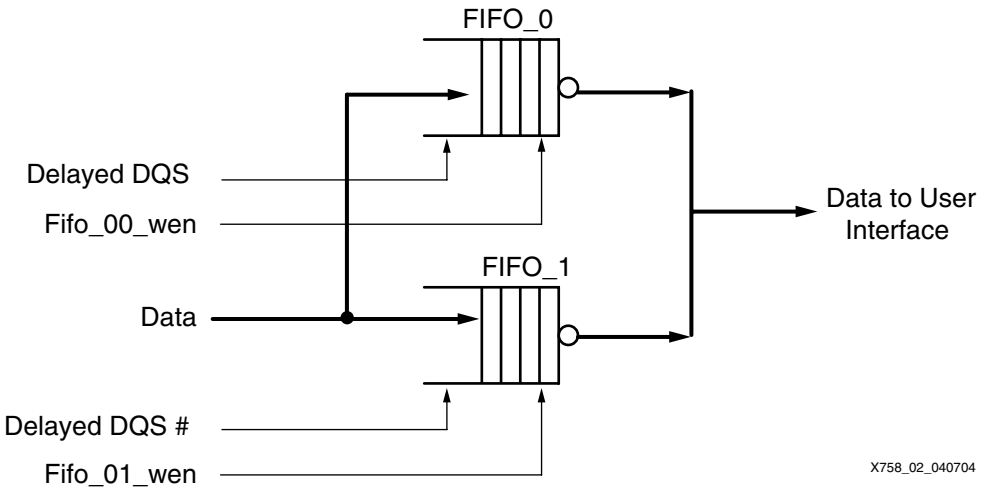

Figure 5: **Data Capture in LUT RAM FIFO using Internally Delayed DQS**

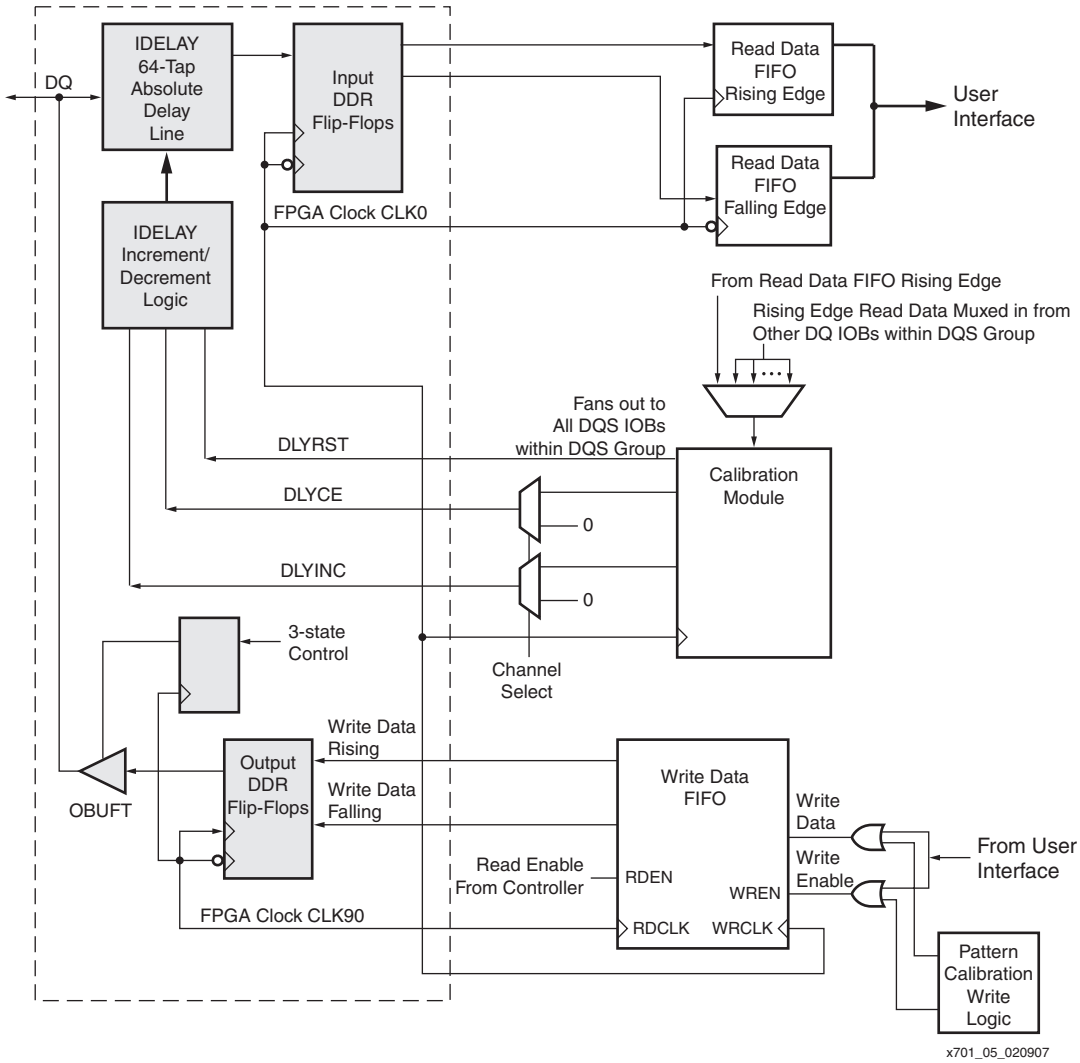

Figure 6: **Data Capture Using Direct Clocking Technique**

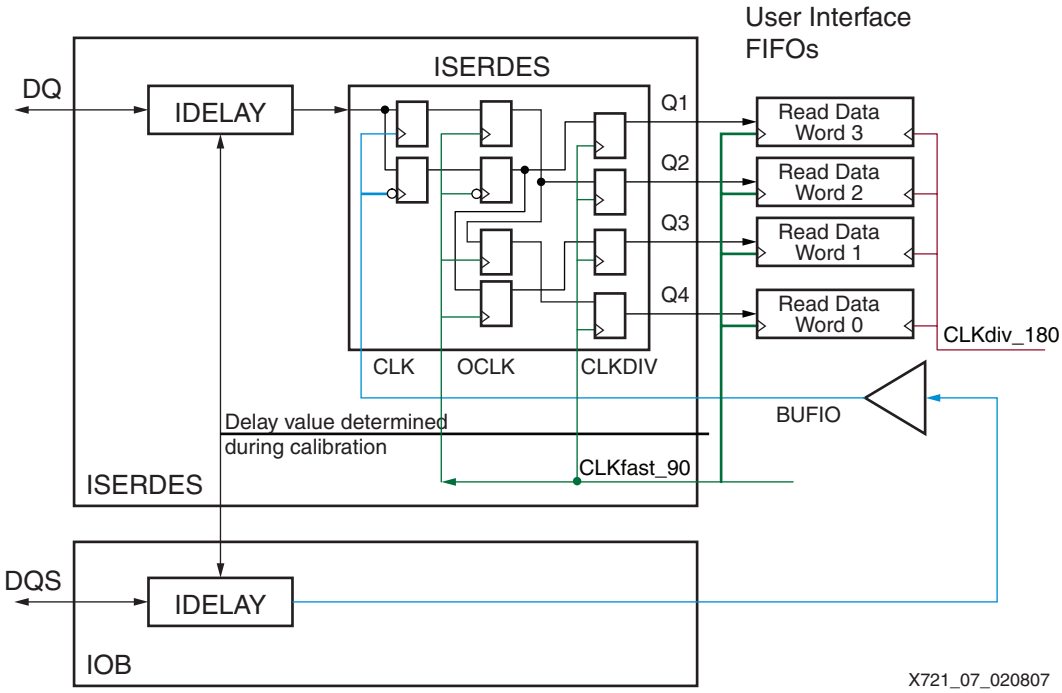

Figure 7: **Read Data Capture Using Virtex-4 ISERDES**

Quad Data Rate Synchronous Random Access Memory

Key features of Quad Data Rate Synchronous Random Access Memory (QDR I SRAM) memories include:

- Source synchronous read and write interfaces using the HSTL-2.5V I/O standard
- Data available both on the positive and negative edges of the strobe
- Unidirectional, free-running, differential data / echo clocks that are edge aligned with read data and center aligned with write data
- One differential strobe pair per 8, 9, or 18 data bits
- Data bus widths varying between 8, 9, and 18 for components; no QDR I DIMMs available
- Reads and writes with burst lengths of 2 or 4 data words, where each data word is equal to the data bus width
- Read latency at 1.5 clock cycles, with frequencies from 154 MHz to 267 MHz
- No row activation, refresh cycles, or an initialization sequence after power-on required, resulting in more efficient memory bandwidth utilization

Quad Data Rate Synchronous Random Access Memory

Key features of Quad Data Rate Synchronous Random Access Memory (QDR II SRAM) memories, the second generation QDR I SRAMs, include:

- Source synchronous read and write interfaces using the HSTL-1.8V I/O standard
- Data available both on the positive and negative edges of the strobe
- Unidirectional, free-running, differential data / echo clocks that are edge aligned with read data and center aligned with write data
- One differential strobe pair per 9, 18, or 36 data bits
- Data bus widths varying varying between 9, 18, and 36 for components, and no QDR II SDRAM DIMMs available
- Reads and writes with burst lengths of 2 or 4 data words, where each data word is equal to the data bus width
- Read latency is 1.5 clock cycles, with frequencies from 167 MHz to 300 MHz
- No row activation, refresh cycles, or an initialization sequence after power-on required, resulting in more efficient memory bandwidth utilization

Design Challenges with QDR I or QDR II SRAM

The free-running data clock provided by QDR memories makes implementation of the read data capture interface in FPGAs easier. Depending on performance requirements, different read data capture techniques can be employed. Details of these techniques are provided in application notes listed in Table 1.

- For low frequency (100 MHz) interfaces, the memory data clock can be ignored and DCM phase-shifted outputs can be used instead.
- For high frequencies, either the memory data clock or the echo clock must be used for higher margins.
  - Data clock, C, is input to the DCM, and the DCM phase-shifted outputs are used to capture read data (up to 200 MHz)
  - Echo clock, CQ, is input to the DCM, and the DCM phase-shifted outputs are used to capture read data (up to 200 MHz) (see Figure 9)
  - Echo clock, CQ, is delayed in the FPGA using continuously calibrated delay elements and the delayed CQ is distributed using local clocking resources (up to 200 MHz) (see Figure 4)
- For high frequencies, Virtex-4 devices have 64-tap absolute delay elements built into each I/O, called IDELAY blocks. The resolution of each tap is approximately 75 ps over process, voltage, and temperature. This feature provides flexibility and makes read data capture easy.
  - Direct clocking technique for data capture delays read data such that the FPGA clock is centered in the valid data window. The read memory clock is used to determine the amount of read data delay. The read data delay is determined by detecting the phase relationship between the memory clock and the FPGA clock. (See Figure 6.)
- For high frequencies, Virtex-5 devices, like Virtex-4 devices, have 64-tap absolute delay elements (IDELAY) and an input Serializer-Deserializer (ISERDES) built into each I/O. The resolution of each tap is 75 ps over process, voltage, and temperature. This feature provides flexibility and makes read data capture easy.
  - In this technique, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the ISERDES. The IDELAY element is used to delay read strobe to center in the read data window. Both read strobe and data are further delayed to align to the FPGA clock domain. The received serial, DDR read data is converted to 2-bit parallel SDR data at the frequency of the interface using the ISERDES. The differential strobe is placed on a clock-capable I/O pair in order to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data ISERDES clock inputs. Figure 8 shows the block diagram of the SERDES data capture technique in Virtex-5 devices.

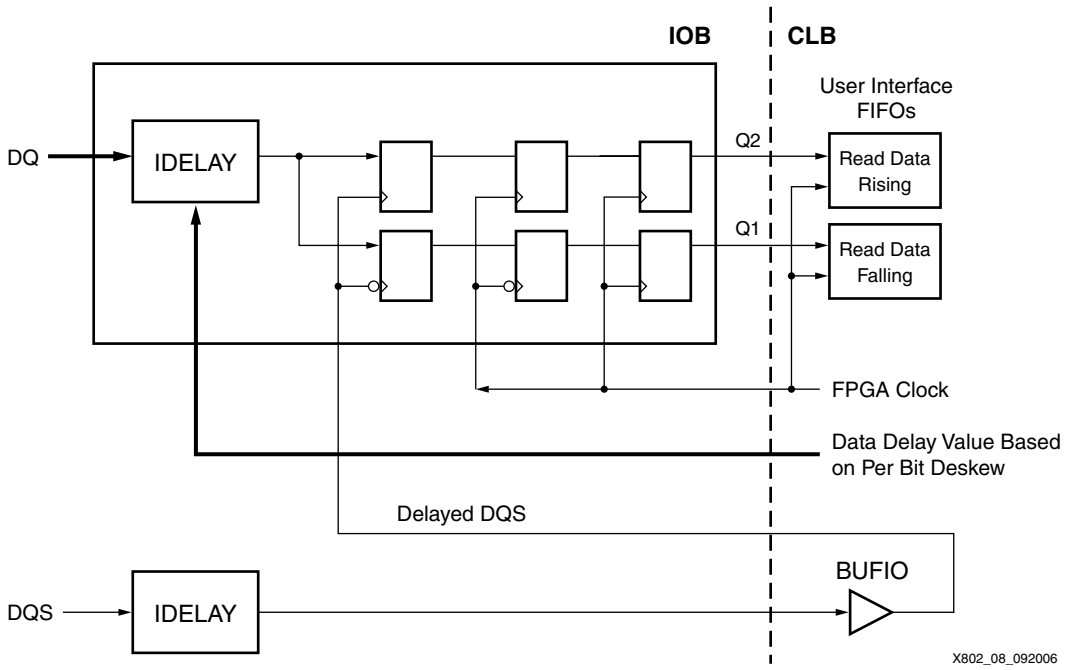

Figure 8: **Read Data Capture Using Virtex-5 ISERDES**

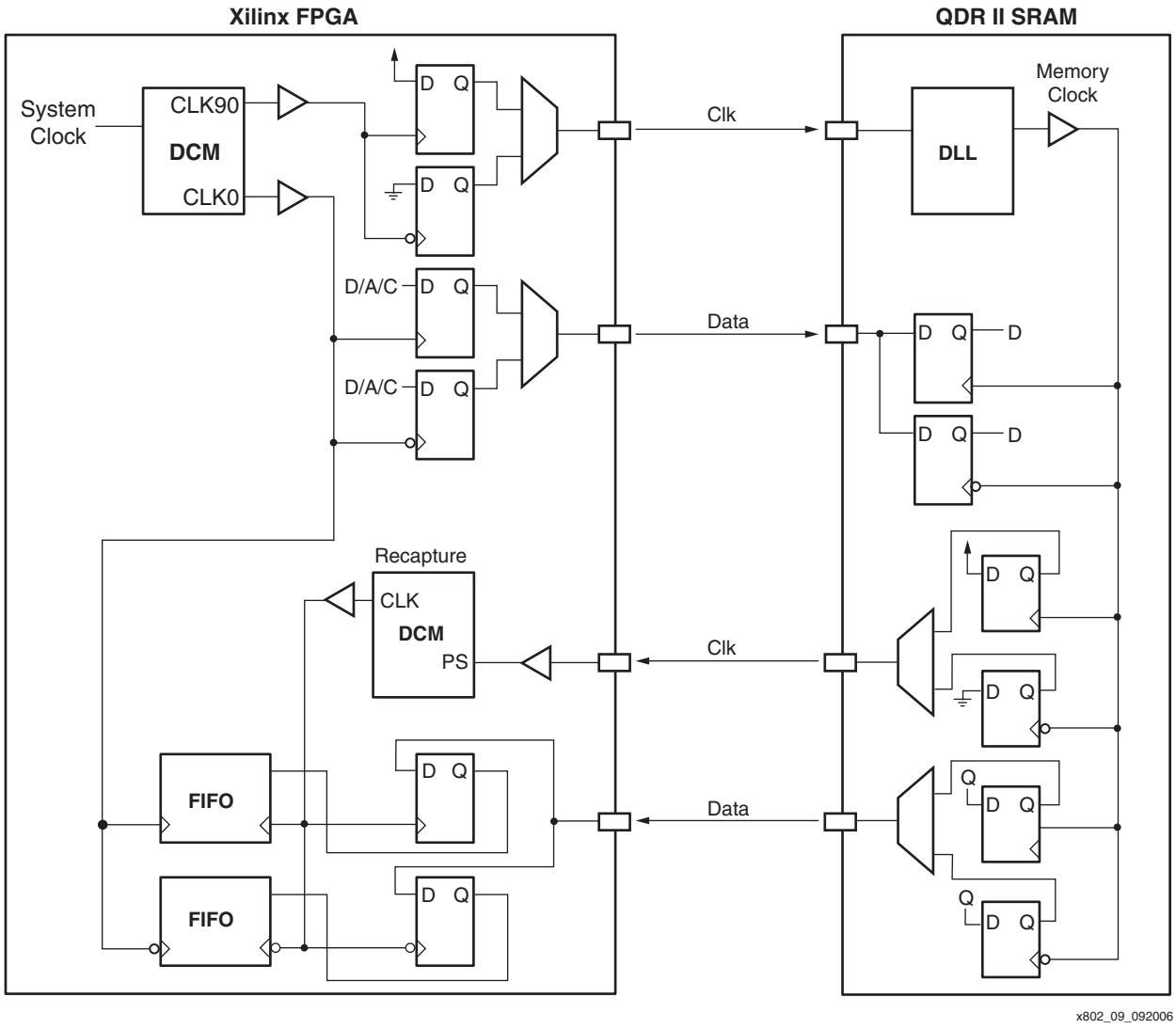

Figure 9: **Data Capture Using DCM Phase-Shifted Outputs**

Reduced Latency Dynamic Random Access Memory

Key features of Reduced Latency Dynamic Random Access Memory (RLDRAM II) memories include:

- Source synchronous read and write interfaces using the HSTL-1.8V I/O standard
- Data available both on the positive and negative edges of the strobe
- Unidirectional, free-running, differential memory clocks that are edge aligned with read data and center aligned with write data
- One strobe per 9 or 18 data bits
- Data bus widths varying between 9, 18, and 36 for components and no DIMMs
- Reads and writes with burst lengths of 2, 4, or 8 data words are supported, where each data word is equal to the data bus width
- Read latency of 4, 6, or 8 clock cycles, with frequencies of 200 MHz, 300 MHz, and 400 MHz
- Data valid signal provided by memory device
- No row activation required; row and column can be addressed together
- Refresh cycles required every 3.9 µs
- Initialization sequence required after power on and before normal operation

Design Challenges with RLDRAM II

The output data clocks are transmitted by the RLDRAM II device and are edge-aligned with read data. One technique that can be used for data capture is as follows:

- For high frequencies, Virtex-4 devices have 64-tap absolute delay elements built into each I/O, called IDELAY blocks. The resolution of each tap is approximately 75 ps over process, voltage, and temperature. This feature provides flexibility and makes read data capture easy.
  - Direct clocking technique for data capture delays read data such that the FPGA clock is centered in the valid data window. The read memory strobe is used to determine the amount of read data delay. The read data delay is determined by detecting the phase relationship between the memory strobe and the FPGA clock. (Figure 6 shows the block diagram.)
- For high frequencies, Virtex-5 devices, like Virtex-4 devices, have 64-tap absolute delay elements (IDELAY) and an input Serializer-Deserializer (ISERDES) built into each I/O. The resolution of each tap is 75 ps over process, voltage, and temperature. This feature provides flexibility and makes read data capture easy.
  - In this technique, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the ISERDES. The IDELAY element is used to delay read strobe to center in the read data window. Both read strobe and data are further delayed to align to the FPGA clock domain. The received serial, DDR read data is converted to 2-bit parallel SDR data at the frequency of the interface using the ISERDES. The differential strobe is placed on a clock-capable I/O pair in order to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data ISERDES clock inputs. Figure 8 shows the block diagram of the SERDES data capture technique in Virtex-5 devices.

Fast Cycle Random Access Memory

Key features of Fast Cycle Random Access Memory (FCRAM-I) memories include:

- Source synchronous read and write interfaces using the SSTL-2.5V Class I/II I/O standard
- Data available both on the positive and negative edges of the strobe
- Bidirectional, non-free-running, single-ended strobes that are output edge aligned with read data, and must be input center aligned with write data
- One strobe per 8 data bits
- Data bus widths varying between 8 and 16 for components and no DIMMs
- Reads and writes with burst lengths of 2 or 4 data words are supported, where each data word is equal to the data bus width
- Read latency of 3 or 4 clock cycles, with frequencies from 154 MHz to 267 MHz
- Row activation required before accessing column addresses in an inactive row
- Refresh cycles required every 7.8 µs
- Initialization sequence required after power-on and before normal operation

Design Challenges with FCRAM-I

The non-free-running strobes and the edge-aligned read data provided by these memories makes it challenging to implement the read data capture interface in FPGAs. There are a couple of techniques that can be used to implement an FCRAM-I read data capture interface.

- The read memory strobe must be used for higher margins. The strobe must be delayed to center it in the data window for data capture. The delayed strobe is distributed in the FPGA using local clocking resources.
  - Externally delayed strobe using discrete delay components or additional trace lengths on the PCB (see Figure 3)
  - Internally delayed strobe in the FPGA using continuously calibrated delay elements (see Figure 4)

Fast Cycle Random Access Memory

Key features of Fast Cycle Random Access Memory (FCRAM-II), the second generation of FCRAM-I memories, include:

- Source synchronous read and write interfaces using the SSTL-1.8V Class I/II I/O standard
- Data available both on the positive and negative edges of the strobe
- Unidirectional, non-free-running or free-running, single-ended strobes/clock that are output edge aligned with read data and must be input center aligned with write data

- One strobe per 9 or 18 data bits
- Data bus widths varying between 9, 18, and 36 for components and no DIMMs
- Reads and writes with burst lengths of 2 or 4 data words are supported, where each data word is equal to the data bus width
- Read latency of 4, 5, 6, or 7 clock cycles, with frequencies from 154 MHz to 267 MHz
- Row activation required before accessing column addresses in an inactive row
- Refresh cycles required every 3.9 µs
- Initialization sequence required after power on and before normal operation

Table 1 lists all of the Virtex series and Spartan-3 series memory interface application notes (XAPPs) currently available, with a brief description of the read data capture technique used.

Table 1: **Memory Interface Application Notes Data Capture Scheme**

Memory Technology and I/O Std	Supported FPGAs	Maximum Performance	Maximum Data Width	XAPP Number	XAPP Title	Data Capture Scheme
DDR2 SDRAM SSTL1.8V Class II	Virtex-5	333 MHz	64 bits (Registered DIMM)	XAPP858	High-Performance DDR2 SDRAM Interface in Virtex-5 Devices	In this design, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the ISERDES. The IDELAY element is used to delay read strobe to center in the read data window. Both read strobe and data are further delayed to align to the FPGA clock domain. The received serial, DDR read data is converted to 2-bit parallel SDR data at the frequency of the interface using the ISERDES. The differential strobe is placed on a clock-capable I/O pair in order to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data ISERDES clock inputs. The controller operates at the frequency of the interface, thereby, enabling efficient bank management. (See Figure 8.)
DDR SDRAM SSTL-2.5V Class I/II	Virtex-5	200 MHz	72 bits (Registered DIMM)	XAPP851	DDR SDRAM Controller Using Virtex-5 FPGA Devices	In this design, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the IDDR. The IDELAY element is used to delay read strobe to center in the read data window. Both read strobe and data are further delayed to align to the FPGA clock domain. The received serial, DDR read data is converted to 2-bit parallel SDR data at the frequency of the interface using the IDDR. The differential strobe is placed on a clock-capable I/O pair in order to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data IDDR clock inputs. The controller operates at the frequency of the interface, thereby, enabling efficient bank management. (See Figure 8.)

Table 1: **Memory Interface Application Notes Data Capture Scheme *(Continued)***

Memory Technology and I/O Std	Supported FPGAs	Maximum Performance	Maximum Data Width	XAPP Number	XAPP Title	Data Capture Scheme
QDR II SRAM HSTL-1.8V Class I	Virtex-5	300 MHz	72 bits (Components)	XAPP853	QDR II SRAM Interface for Virtex-5 Devices	In this design, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the ISERDES. The IDELAY element is used to delay read strobe to center in the read data window. Both read strobe and data are further delayed to align to the FPGA clock domain. The received serial, DDR read data is converted to 2-bit parallel SDR data at the frequency of the interface using the ISERDES. The differential strobe is placed on a clock-capable I/O pair in order to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data ISERDES clock inputs. The controller operates at the frequency of the interface, thereby, reducing command latency. (See Figure 8.)
RLDRAM II HSTL-1.8V Class II	Virtex-5	333 MHz	36 bits (Components)	XAPP852	Synthesizable CIO DDR RLDRAM II Controller for Virtex-5 FPGAs	In this design, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the ISERDES. The IDELAY element is used to delay read strobe to center in the read data window. Both read strobe and data are further delayed to align to the FPGA clock domain. The received serial, DDR read data is converted to 2-bit parallel SDR data at the frequency of the interface using the ISERDES. The differential strobe is placed on a clock-capable I/O pair in order to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data ISERDES clock inputs. The controller operates at the frequency of the interface, thereby, reducing command latency. (See Figure 8.)
DDR2 SDRAM SSTL1.8V Class II	Virtex-4	300 MHz	8 bits (Components) 72-bits (Registered DIMM)	XAPP721	High-Performance DDR2 SDRAM Interface Data Capture Using ISERDES and OSERDES	In this design, the read data is captured in the delayed strobe domain and recaptured in the FPGA clock domain in the ISERDES. The IDELAY element is used to delay read strobe to center in the read data window. Both read strobe and data are further delayed to align to the FPGA clock domain. The received serial, DDR read data is converted to 4-bit parallel SDR data at half the frequency of the interface using the ISERDES. The differential strobe is placed on a clock-capable I/O pair in order to access the BUFIO clock resource. The BUFIO clocking resource routes the delayed read DQS to its associated data ISERDES clock inputs. The controller operates at half the frequency of the interface without affecting throughput. (See Figure 7.)
				XAPP723	DDR2 Controller (267 MHz and Above) Using Virtex-4 Devices	

Table 1: **Memory Interface Application Notes Data Capture Scheme *(Continued)***

Memory Technology and I/O Std	Supported FPGAs	Maximum Performance	Maximum Data Width	XAPP Number	XAPP Title	Data Capture Scheme
DDR2 SDRAM SSTL-1.8V Class II	Virtex-4	240 MHz	16 bits (Components) 144 bits (Registered DIMM)	XAPP702	DDR2 SDRAM Controller Using Virtex-4 Devices	Read data delayed such that FPGA clock is centered in data window. Memory read strobe used to determine amount of read data delay. (See Figure 6.)
				XAPP701	Memory Interfaces Data Capture Using Direct Clocking Technique	
DDR SDRAM SSTL-2.5V Class I/II	Virtex-4	175 MHz	16 bits (Components) 144-bit (Registered DIMM)	XAPP709	DDR SDRAM Controller Using Virtex-4 Devices	Read data delayed such that FPGA clock is centered in data window. Memory read strobe used to determine amount of read data delay. (See Figure 6.)
QDR II SRAM HSTL-1.8V	Virtex-4	250 MHz	72 bits (Components)	XAPP703	QDR II SRAM Interface	Read data delayed such that FPGA clock is centered in data window. Memory read strobe used to determine amount of read data delay. (See Figure 6.)
RLDRAM II HSTL-1.8V	Virtex-4	250 MHz	36 bits (Components)	XAPP710	Synthesizable CIO DDR RLDRAM II Controller for Virtex-4 FPGAs	Read data delayed such that FPGA clock is centered in data window. Memory read strobe used to determine amount of read data delay. (See Figure 6.)
DDR2 SDRAM SSTL1.8V Class II	Virtex-II Pro	200 MHz	72 bits (Components and DIMM)	XAPP549	DDR2 SDRAM Memory Interface for Virtex-II Pro FPGAs	Internally delayed read memory strobe (DQS) using continuously calibrated delay elements captures data in CLB flip-flops. (See Figure 4.)
DDR SDRAM SSTL-2.5V Class I/II	Virtex-II Virtex-II Pro	200 MHz	72 bits (Components and DIMM)	XAPP678c (available under license agreement)	Data Capture Technique Using CLB Flip-Flops	Internally delayed read memory strobe (DQS) using continuously calibrated delay elements captures data in CLB flip-flops. (See Figure 4.)
				XAPP688	Creating High-Speed Memory Interfaces with Virtex-II and Virtex-II Pro FPGAs	
DDR SDRAM SSTL-2.5V Class I/II	Virtex-II Virtex-II Pro	167 MHz	8 bits (Components)	XAPP758c (available under license agreement)	Interfacing Virtex-II Devices with DDR Memories for Performance to 167 MHz	Internally delayed read memory strobe (DQS) using continuously calibrated delay elements captures data in LUT RAM FIFOs. (See Figure 5.)
DDR SDRAM SSTL-2.5V Class I/II	Virtex-II Virtex-II Pro	200 MHz	32 bits (Components)	XAPP253 (See Note 1)	Synthesizable 400 Mb/s DDR SDRAM Controller	Externally delayed read memory strobe (DQS) captures data in IOB flip-flops. (See Figure 3.)
DDR SDRAM SSTL-2.5V Class I/II	Virtex-II Virtex-II Pro	100 MHz	64 bits (DIMM)	XAPP608 (See Note 1)	DDR SDRAM DIMM Interface for Virtex-II Devices	Read memory strobe (DQS) is ignored, and DCM phase-shifted outputs are used to capture data in IOB flip-flops. (See Figure 2.)
QDR I SRAM HSTL-2.5V	Virtex-II Virtex-II Pro	200 MHz	18 bits (Components) 2-word burst	XAPP262	QDR SRAM Interface for Virtex-II and Virtex-II Pro Devices	Memory data clock is input to a DCM, and phase-shifted DCM outputs are used to capture data in IOB flip-flops. (See Figure 9.)

Table 1: **Memory Interface Application Notes Data Capture Scheme *(Continued)***

Memory Technology and I/O Std	Supported FPGAs	Maximum Performance	Maximum Data Width	XAPP Number	XAPP Title	Data Capture Scheme
QDR II SRAM HSTL-1.8V	Virtex-II Virtex-II Pro	200 MHz	36 bits (Components) 4-word burst	XAPP750	QDR II SRAM Local Clocking Interface	Internally delayed read memory strobe (CQ) using continuously calibrated delay elements captures data in CLB flip-flops. (See Figure 4.)
				XAPP770c (available under license agreement)	Interfacing Local Clocking Physical Layer in Virtex-II Series FPGAs with QDR II SRAM	
FCRAM-I SSTL-2.5V Class I/II	Virtex-II Virtex-II Pro	154 MHz	16 bits (Components)	XAPP266	Synthesizable FCRAM Controller	Externally delayed read memory strobe (DQS) captures data in IOB flip-flops. (See Figure 3.)
DDR2 SDRAM SSTL1.8V Class II	Spartan-3	166 MHz 32 bits or less 133 MHz beyond 32 bits	64 bits (DIMM/ Components)	XAPP454 /XAPP768c	DDR2 SDRAM Memory Interface for Spartan-3 FPGAs	Internally delayed read memory strobe (DQS) using continuously calibrated delay elements captures data in LUT RAM FIFOs. (See Figure 5.)
DDR SDRAM SSTL-2.5V Class I/II	Spartan-3	166 MHz 32 bits or less 133 MHz beyond 32 bits	64 bits (DIMM/ Components)	XAPP768c (available under license agreement)	Interfacing Spartan-3 Devices with DDR Memories for Performance to 133 MHz	Internally delayed read memory strobe (DQS) using continuously calibrated delay elements captures data in LUT RAM FIFOs. (See Figure 5.)
DDR SDRAM SSTL-2.5V Class I/II	Virtex Virtex-E Spartan-II	133 MHz	64 bits (Components)	XAPP200 (See Note 1)	Synthesizable DDR SDRAM Controller	Read memory strobe (DQS) is ignored, and DLL outputs are used to capture data in CLB flip-flops.
QDR I SRAM HSTL-2.5V	Virtex Virtex-E	100 MHz	9 bits (Components)	XAPP214 (See Note 1)	Virtex Devices Quad Data Rate (QDR) SRAM Interface	Memory data clock is ignored, and DLL outputs are used to capture data in CLB flip-flops.
ZBT SRAM LVTTL	Virtex Spartan-II	200 MHz	36 bits (Components)	XAPP136	Synthesizable 200 MHz ZBT SRAM Interface	Single data rate, read data is captured using DLL outputs.
SDRAM LVTTL	Virtex Spartan-II	125 MHz	32 bits (Components)	XAPP134	Synthesizable High-Performance SDRAM Controllers	Single data rate, read data is captured using DLL outputs.

Notes:
1. This application is NOT recommended for new designs. For existing designs, contact your local FAE for access.

Table 2 provides information on resource utilization for all of the Virtex series memory interface application notes currently available.

Table 2: **Memory Interface Application Notes Resource Utilization**

XAPP Number Memory Technology and I/O Standard	Maximum Performance	Number of DCMs/DLLs	Number of BUFGs	Number of Interfaces with Listed DCMs and BUFGs	Device(s) Used for Hardware Verification	Requirements
XAPP858 DDR2 SDRAM SSTL1.8V Class II	333 MHz	1	3	Multiple at same frequency	XC5VLX50 FF1136	All banks supported
XAPP851 DDR SDRAM SSTL-2.5V Class I/II	200 MHz	1	3	Multiple at same frequency	XC5VLX50 FF1136	All banks supported

Table 2: **Memory Interface Application Notes Resource Utilization *(Continued)***

XAPP Number Memory Technology and I/O Standard	Maximum Performance	Number of DCMs/DLLs	Number of BUFGs	Number of Interfaces with Listed DCMs and BUFGs	Device(s) Used for Hardware Verification	Requirements
XAPP853 QDR II SRAM HSTL-1.8V	300 MHz	1	3	Multiple at same frequency	XC5VLX50 FF1136	All banks supported
XAPP852 RLDRAM II HSTL-1.8V	333 MHz	1	4	Multiple at same frequency	XC5VLX50 FF1136	All banks supported
XAPP721 XAPP723 DDR2 SDRAM SSTL1.8V Class II	300 MHz	2 DCMs 1 PMCD	6	Multiple at same frequency	XC4VLX25 FF668	All banks supported
XAPP702 XAPP701 DDR2 SDRAM SSTL-1.8V Class II	240 MHz	1	6	Multiple at same frequency	XC4VLX25 -11 FF668	All banks supported
XAPP709 DDR SDRAM SSTL-2.5V Class I/II	175 MHz	1	6	Multiple at same frequency	XC4VLX25 -11 FF668	All banks supported
XAPP703 QDR II SRAM HSTL-1.8V	250 MHz	1	3	Multiple at same frequency	XC4VLX25 -11 FF668	All banks supported
XAPP710 RLDRAM II HSTL-1.8V	250 MHz	1	5	Multiple at same frequency	XC4VLX25 -11 FF668	All banks supported
XAPP549 DDR2 SDRAM SSTL1.8V Class II	200 MHz	2	5	Multiple at same frequency	XC2VP20 -6 FF1152	Supported banks: 2, 3, 6, 7
XAPP678c (avail. under license agreement) XAPP688 DDR SDRAM SSTL-2.5V Class I/II	200 MHz	2	5	Multiple at same frequency	XC2V1000 -5 FG456 XC2VP20 -6 FF1152	Supported banks: 2, 3, 6, 7
XAPP758c (avail. under license agreement) DDR SDRAM SSTL-2.5V Class I/II	167 MHz	1	4	Multiple at same frequency	XC2VP20 -6 FF1152	All banks supported
XAPP253 (See Note 1) DDR SDRAM SSTL-2.5V Class I/II	200 MHz	3	5	Single 32-bit components	XC2V1000 -5 FG456	Supported banks: 2, 3, 6, 7
XAPP608 (See Note 1) DDR SDRAM SSTL-2.5V Class I/II	100 MHz	2	6	Single 64-bit DIMM	XC2V6000 -5 FF1152	All banks Supported
XAPP262 QDR I SRAM HSTL-2.5V	200 MHz	2	6	Single 18-bits component	XC2V3000	All banks Supported
XAPP750 XAPP770c (available under license agreement) QDR II SRAM HSTL-1.8V	200 MHz	2	5	Multiple at same frequency	XC2VP20 -6 FF1152	Supported banks: 2, 3, 6, 7

Table 2: **Memory Interface Application Notes Resource Utilization *(Continued)***

XAPP Number Memory Technology and I/O Standard	Maximum Performance	Number of DCMs/DLLs	Number of BUFGs	Number of Interfaces with Listed DCMs and BUFGs	Device(s) Used for Hardware Verification	Requirements
XAPP266 FCRAM-I SSTL-2.5V Class I/II	154 MHz	2	3	Single 16-bit components	XC2V1000 -4 FG456	Supported banks: 2, 3, 6, 7
XAPP454/XAPP768c DDR2 SDRAM SSTL1.8V Class II	166 MHz	1	2	Multiple at same frequency	Spartan-3 FPGAs (See Note 2)	Side banks for 166 MHz performance (with data width of 32 bits or less) and all banks for 133 MHz performance.
XAPP768c (available under license agreement) DDR SDRAM SSTL-2.5V Class I/II	166 MHz	1	2	Multiple at same frequency	3S1500 -5 FG676	Side banks supported for 166 MHz performance (with data width of 32 bits or less) and all banks supported for 133 MHz performance.
XAPP200 (See Note 1) DDR SDRAM SSTL-2.5V Class I/II	133 MHz	2 DLLs	2	Single 64-bit components	Virtex FPGAs (See Note 2) Spartan-II FPGAs (See Note 2)	All banks supported
XAPP214 (See Note 1) QDR I SRAM HSTL-2.5V	100 MHz	2 DLLs	5	Single 9-bit components	Virtex (See Note 2)	All banks supported
XAPP136 ZBT SRAM LVTTL	200 MHz	2 DLLs	2	Single 36-bit components	Virtex (See Note 2) Spartan (See Note 2)	All banks supported
XAPP134 SDRAM LVTTL	125 MHz	2 DLLs	3	Single 32-bit components	Virtex (See Note 2)	All banks supported

Notes:
1. This application is NOT recommended for new designs. For existing designs, please contact your local FAE for access.
2. This design was not hardware verified. This application note supports the Virtex family and the Spartan-II family of FPGAs in the -6 speed grade.

Conclusion

Application notes for various memory technologies and performance requirements are available at http://www.xilinx.com/products/design_resources/mem_corner/index.htm. The summary provided by Table 1 and Table 2 of this document can help users determine which application note is relevant for a particular design.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/11/04	1.0	Initial Xilinx release.
05/10/04	1.1	Added information about XAPP758c.
6/22/04	1.2	Minor corrections.
6/28/04	1.3	Minor corrections.
8/31/04	1.4	Updated Table 1 and Table 2.

Date	Version	Revision
11/18/04	1.5	Revised Figure 7.
01/21/05	1.6	Added Virtex-4 related information throughout.
10/2/06	1.7	Updated "Design Challenges with DDR or DDR 2 SDRAM," and "Design Challenges with QDR I or QDR II SRAM" sections. Updated Figure 7. Added Figure 8 and Figure 9. Updated Table 1 and Table 2.
12/05/06	1.8	Added DDR2 SDRAM SSTL1.8V Class II information to Table 1 and Table 2.
03/23/07	1.9	• Figure 6: Replaced with updated version. • Figure 7: Replaced with updated version. • Table 1, Table 2: Updated maximum performance values for XAPP701, XAPP702, XAPP703, XAPP709, XAPP710, and XAPP852. • Table 1, Table 2: Added 32-bit data width qualification to XAPP454 and XAPP768c.