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RLDRAM II Memory Interface for Virtex-5 FPGAs

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Summary

This application note describes how to use a Virtex®-5 device to interface to Common I/O (CIO) Double Data Rate (DDR) Reduced Latency DRAM (RLDRAM II) devices. The reference design targets two CIO DDR RLDRAM II devices at a clock rate of up to 333 MHz with data transfers up to 667 Mb/s per pin.

Introduction

This application note describes a CIO DDR RLDRAM II memory interface implemented in a Virtex-5 device. The first section describes the functionality of the RLDRAM II device. Other sections describe implementation and timing analysis details.

RLDRAM II Devices

RLDRAM II, the second generation of RLDRAM, is a high-performance memory. It combines the performance-critical features that networking and cache applications need, such as high density (up to 288 MB), high bandwidth, and fast SRAM-like random access.

[Table 1](#) lists a summary of the RLDRAM II reference design described in this application note.

Table 1: RLDRAM II Reference Design Summary

Parameters for Specification Details	Specification Details
	Speed Grade / Performance
Maximum Frequency, by Speed Grade (over $\pm 3\%$ voltage range)	-1 / 250 MHz
	-2 / 300 MHz
	-3 / 333 MHz
Parameters for Design Details	Design Details
Device Utilization (without testbench)	1,192 Slices
	3 GLK Buffers
	6 FIFO36 (Block RAM)
Target Memory Device for Verification	Simulation: Micron MT49H16M18 x18 CIO
	Hardware: Micron MT49H16M18BM-25 x18 CIO (See <i>MT49H16M18-25 288 Mb CIO RLDRAM II Data Sheet</i> [Ref 1])
RLD2 SDRAM Operation	2-Word Burst/4-Word Burst
Bus Width	36 Bits
I/O Standard	HSTL_II_18 (1.8V Signaling)
HDL Language Support	Verilog/VHDL

RLDRAM II memory uses an internal eight-bank architecture that minimizes data-access time. This architecture provides minimized latency and reduced row-cycle times for applications such as networking, graphics, and cache that require critical response times and very fast random access. RLDRAM II memory operates at a clock frequency of up to 400 MHz and uses a DDR interface. For each clock cycle, the DDR interface transfers two data words that are either 36 bits, 18 bits, or 9 bits wide.

Output data is referenced to the free-running output data clock (QK). Commands, addresses, and control signals are registered at every positive edge of the differential input clock (CK), while input data is registered at both positive and negative edges of the input data clock (DK). RLDRAM II devices are offered in the following types. (See *Micron RLDRAM II Design Guide Technical Note* [Ref 2].)

- Separate I/O (SIO) devices: RLDRAM II SIO devices have separate read and write ports to eliminate bus turnaround cycles and contention. They are also optimized for near-term read and write balance and full bus utilization. (This application note does not discuss RLDRAM II SIO device types in detail.)
- Common I/O (CIO) devices: RLDRAM II CIO devices have a shared read/write port, resulting in a bidirectional data bus that requires one additional cycle to turn the bus around. The RLDRAM II CIO architecture is optimized for data streaming, in which the near-term bus operation is either 100% read or 100% write, independent of the long-term balance.
 - ♦ During read commands, the data is output from the device and is referenced to both edges of the QK clocks.
 - ♦ During write commands, the data is input to the device and is sampled at both edges of the DK clocks.

Read and write access to RLDRAM II memory is burst-oriented. The burst length (BL) is programmable at 2, 4, or 8 through the Mode register. RLDRAM II I/Os use the 1.5V or 1.8V High-Speed Transceiver Logic (HSTL) I/O standard.

Designers should choose an I/O version that provides an optimal compromise between performance and utilization.

Clocking

Clocking for the RLDRAM II device includes two required differential-input clock pairs (the CK/ $\overline{\text{CK}}$ pair and the DK/ $\overline{\text{DK}}$ pair) as well as a generated differential-output clock pair QK/ $\overline{\text{QK}}$.

CK and $\overline{\text{CK}}$. The RLDRAM II device requires a differential-input master-clock pair, CK and $\overline{\text{CK}}$. When CK and $\overline{\text{CK}}$ are 180° out of phase, they provide the best system margins. Only the rising edge of CK is used for address and control latching.

DK and $\overline{\text{DK}}$. The RLDRAM II device also requires a differential-input data-clock pair, DK and $\overline{\text{DK}}$. Both rising edges of DK and $\overline{\text{DK}}$ are used to latch data to the RLDRAM II device. When DK and $\overline{\text{DK}}$ are 180° out of phase, they provide the best margin on write data.

- For the x36 configuration, two differential-input data-clock pairs are available.
 - ♦ DQ0 through DQ17 are referenced to DK0 and $\overline{\text{DK0}}$.
 - ♦ DQ18 through DQ35 are referenced to DK1 and $\overline{\text{DK1}}$.
- For the x18 and x9 configurations, all DQ are referenced to DK and $\overline{\text{DK}}$ as a single differential-input data-clock pair.

QK and \overline{QK} . The RLDRAM II device feeds an internal delay-locked loop (DLL) to create the differential-output data-clock pair, QK and \overline{QK} . During a read command, RLDRAM II transmits QK and \overline{QK} and edge aligns them with the output data.

- For the x36 configuration, alignment occurs as follows:
 - QK0 and $\overline{QK0}$ align with the least significant data bits (DQ0 through DQ17).
 - QK1 and $\overline{QK1}$ align with the most significant data bits (DQ18 through DQ35).
- For the x18 configuration, alignment occurs as follows:
 - QK0 and $\overline{QK0}$ align with the least significant data bits (DQ0 through DQ8).
 - QK1 and $\overline{QK1}$ align with the most significant data bits (DQ9 through DQ17).
- The x9 configuration uses only QK0 and $\overline{QK0}$, aligned with data bits (DQ0 through DQ8).

Mode Register

[Table 2](#) lists the fields for the Mode register, which stores data that controls the RLDRAM II memory operating modes. During a Mode register set command, the RLDRAM II device samples address inputs A[17:0] and stores the contents in the Mode register fields. The Mode register can be configured at any time during device operation.

Note: To read or modify the contents of the Mode register, use the apConf signals indicated in [Figure 2](#).

Table 2: Mode Register Fields

Address Bits	Field Name	Description
A[17:10]	Reserved	Must be set to zero.
A9	On-Die Termination	0 - Disabled 1 - Enabled
A8	Impedance Matching	0 - Internal 50 Ω 1 - External resistor determines impedance
A7	DLL Reset	0 - DLL reset 1 - DLL enabled
A6	Unused	Not used. Set to 0.
A5	Address MUX	0 - Non-multiplexed 1 - Multiplexed
A[4:3]	Burst Length (BL)	00 - 2 01 - 4 10 - 8 11 - Not valid
A[2:0]	Configuration	000 - Config 1 (Default, BL of 8 not available) 001 - Config 1 (BL of 8 not available) 010 - Config 2 011 - Config 3 100 to 111 - Reserved

Configuration Table

Table 3 lists the RLDRAM II device configurations that can be programmed into the Mode register for a range of operating frequencies. For each frequency, the table lists row cycle times (t_{RC}), the read latency (t_{RL}), and the write latency (t_{WL}), both in clock cycles as well as nanoseconds (ns).

Table 3: RLDRAM II Device Configurations

Frequency	Symbol	Configuration			Unit
		1	2	3	
—	t_{RC}	4	6	8	cycles
	t_{RL}	4	6	8	cycles
	t_{WL}	5	7	9	cycles
400 MHz	t_{RC}	-	-	20.0	ns
	t_{RL}	-	-	20.0	ns
	t_{WL}	-	-	22.5	ns
300 MHz	t_{RC}	-	20.0	26.7	ns
	t_{RL}	-	20.0	26.7	ns
	t_{WL}	-	23.3	30.0	ns
200 MHz	t_{RC}	20.0	30.0	40.0	ns
	t_{RL}	20.0	30.0	40.0	ns
	t_{WL}	25.0	35.0	45.0	ns

RLDRAM II Burst Length and Frequency Configuration Matrix

Table 4 is a matrix that lists the configurations that are valid for each RLDRAM II burst length (BL) and frequency of operation.

Table 4: RLDRAM II Burst Lengths and Corresponding Frequency Configuration

RLDRAM II Burst Length	Frequency Configuration		
	200 MHz (-5)	300 MHz (-3.3)	400 MHz (-2.5)
BL = 2	Config = 1	—	—
	Config = 2	Config = 2	—
	Config = 3	Config = 3	Config = 3
BL = 4	Config = 1	—	—
	Config = 2	Config = 2	—
	Config = 3	Config = 3	Config = 3
BL = 8 ⁽¹⁾	—	—	—
	Config = 2	Config = 2	—
	Config = 3	Config = 3	Config = 3

Notes:

1. The RLDRAM II controller implementation does not currently support BL = 8.

RLDRAM II Burst Lengths and Bus Address Usage Matrix

Table 5 is a matrix that lists, for each RLDRAM II burst length, the corresponding bus address usage for each bus width configuration.

Table 5: RLDRAM II Burst Lengths and Corresponding Bus Address Usage

RLDRAM II Burst Length	Corresponding Bus Address Usage for Bus Width Configurations		
	x36	x18	x9
BL = 2	[18:0]	[19:0]	[20:0]
BL = 4	[17:0]	[18:0]	[19:0]
BL = 8	N/A	[17:0]	[18:0]

Commands

Table 6 lists and describes commands the memory interface can send to an RLDRAM II device.

Table 6: Commands to RLDRAM II Device

Command	Description
DESEL/NOP	Deselect / No Operation. Deselects the RLDRAM II device so that it performs no operation, which prevents the execution of unwanted commands.
MRS	Mode Register Set. Uses inputs A[17:0] to set the Mode register. The MRS command can be issued only when all banks are idle and no bursts are in progress.
READ	Read. Initiates a burst read access to a bank. The value on inputs BA[2:0] selects the bank, and the address provided on inputs A[20:0] selects the data location within the bank.
WRITE	Write. Initiates a burst write access to a bank. The value on inputs BA[2:0] selects the bank, and the address provided on inputs A[20:0] selects the data location within the bank. The input data appearing on the DQ bus is written to the memory array, according to the data mask (DM) input logic level appearing with the data. <ul style="list-style-type: none"> If a DM signal is Low, the associated data is written to memory. If a DM signal is High, the associated data is ignored. (That is, this part of the data word is not written.)
AREF	Auto Refresh. Refreshes the memory content of a bank during normal operation of the RLDRAM II device. Each time a refresh is required by the RLDRAM II, the RLDRAM II controller must issue the AREF command. The value on BA[2:0] inputs selects the bank. An internal refresh controller generates the refresh address and makes each address bit unused during the AREF command. The RLDRAM II requires 64K cycles at an average periodic interval of 0.49 μ s (maximum). To improve efficiency, post eight AREF commands (one for each bank) to the RLDRAM II at periodic intervals of 3.9 μ s.

Bank Usage

The Mode register controls both the burst length and the RLDRAM II configuration. The selected t_{RC} defines how frequently the RLDRAM II can access any one bank. The burst length determines how often the RLDRAM II requires a new address. The RLDRAM II can access banks in any order at any time as long as t_{RC} timing is met before revisiting a bank.

Note: To optimize use of the eight-bank RLDRAM II architecture, read data from or write data to the RLDRAM II device by cyclically switching banks. (That is, use a round-robin approach to access the least recently used bank in the RLDRAM II device [Ref 2].)

Correspondence of WL and RL Times

Read-to-write cycles. To make the data pipelining both correct and efficient, each time a read-to-write cycle is performed, the RLDRAM II device imposes this equation:

Write Latency (WL) = Read Latency (RL) + 1.

Write-to-read cycles. In contrast, for a write-to-read cycle, a dead cycle must be added to the write-to-read cycle. Unless the dead cycle is added, the result is either bus contention or data loss, in which case the CIO DDR RLDRAM II controller must handle the contention.

CIO DDR RLDRAM II Interface Implementation

Implementation Details

Figure 1 shows a top-level block diagram of the CIO DDR RLDRAM II memory interface.

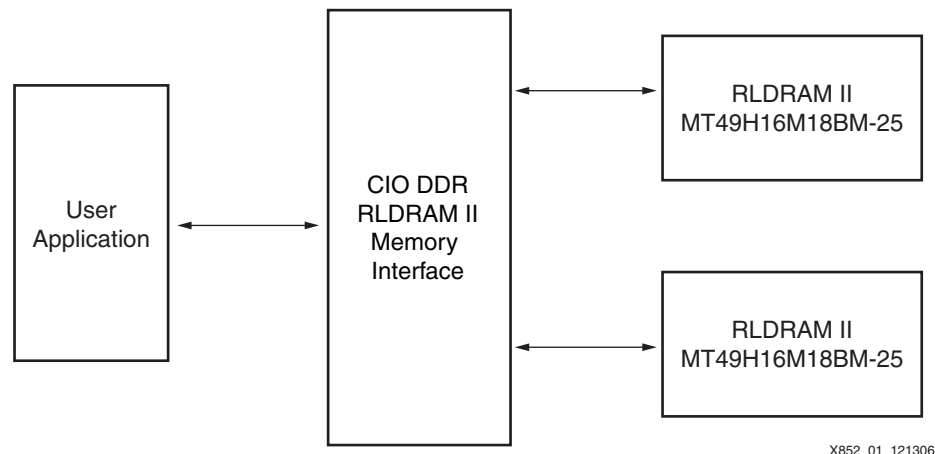


Figure 1: CIO DDR RLDRAM II Memory Interface (Top Level)

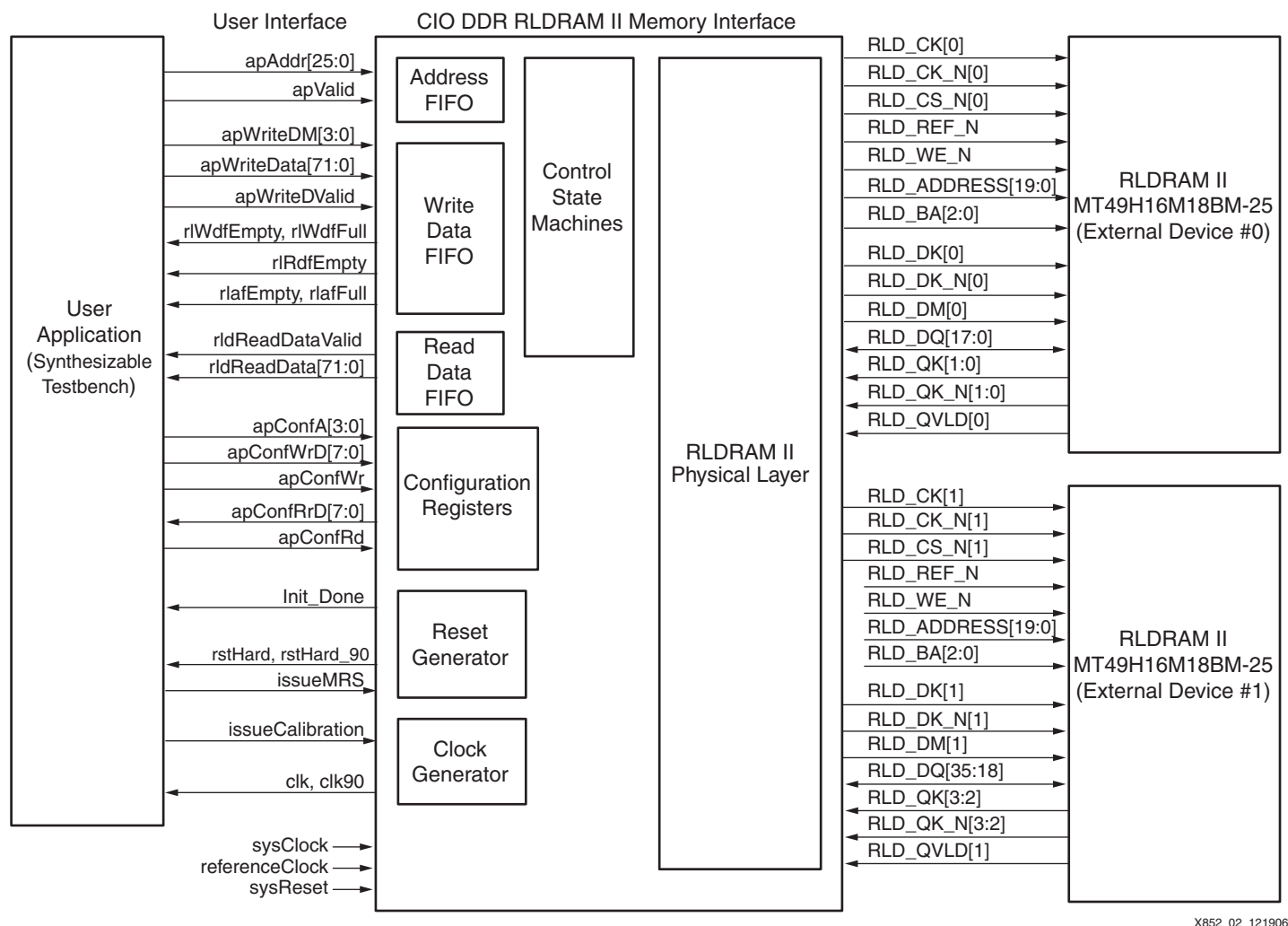
Design Features

The key features of the CIO DDR RLDRAM II memory interface design are:

- Micron compliant to RLDRAM II specification [Ref 1]
- Data interface width of 36 bits using two MT49H16M18BM-25 devices from Micron, supporting two 16 Mb x 18 bits devices [Ref 1]
- Common I/O mode for the bidirectional data bus
- ChipSync™ technology is used by the physical layer of the Virtex-5 FPGA
- FIFO-based user interface
- Burst lengths of 2 and 4
- Pre-set Mode register, where Config = 2 and BL = 4
- Non-multiplexed address bus
- Automatic refresh

Block Diagram Description

This section includes a detailed block diagram of the CIO DDR RLDRAM II memory interface (see Figure 2) and descriptions of the major blocks.



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Figure 2: Detailed Block Diagram of CIO DDR RLDRAM II Memory Interface

User Interface Block Description

The user interface for the RLDRAM II memory interface is a FIFO-based implementation that consists of:

- FIFOs
 - ◆ Address FIFO
 - ◆ Write data FIFO
 - ◆ Read data FIFO
- Configuration registers

Address FIFO

The address FIFO serves as the buffer for the backend interface to store addresses corresponding to the read and write data as well as scheduling all reads and writes. This synchronous FIFO is 26 bits wide.

[Table 7](#) lists and describes the 26 configuration bits.

Table 7: Address FIFO Bit Configuration

Bit Configuration	Description
25	User Refresh (Not supported currently)
24	Read/ $\overline{\text{Write}}$
23	Reserved
[22:3]	Memory Address bits A[19:0]
[2:0]	Memory Bank Address bits BA[2:0]

Write Data FIFO

The write data FIFO serves as the buffer for the backend interface to store data that must be written into the memory. This synchronous FIFO is 76 bits wide.

- For a burst length of 2, each location in the write data FIFO constitutes the required data.
- For a burst length of 4, two locations in the write data FIFO constitute the required data.

[Table 8](#) lists and describes the 76 configuration bits.

Table 8: Write Data FIFO Bit Configuration

Bit Configuration	Description
[75:72]	Write Data Mask
[71:0]	Write Data

Read Data FIFO

The read data FIFO serves as a buffer to store data read by the controller from the RLDRAM II memory. The testbench reads the data from the FIFO to compare with the expected data. This asynchronous FIFO is 4 x 18 bits wide.

- For a burst length of 2, each location in the read data FIFO consists of the data read from the RLDRAM II memory.
- For a burst length of 4, two locations in the read data FIFO consist of the data read from the RLDRAM II memory.

[Table 9](#) lists and describes the 72 configuration bits.

Table 9: Read Data FIFO Bit Configuration

Bit Configuration	Description
[71:0]	Read Data

Configuration Registers

The configuration registers block provides an interface for the user application to read from and write to the configuration registers.

Note:

- The ODT bit (A[9] in [Table 2](#)) is OFF by default, requiring placement of termination resistors close to the memory.
- The Burst Length bits (A[4:3] in [Table 2](#)) can be reprogrammed during run time to change the burst length. Alternatively, the burst length can be changed at compile time in the code.

Reset Generator

This block generates different reset signals. It also performs the initialization and configuration of the RLDRAM II device.

Clock Generator

This block generates all required clocks for the RLDRAM II controller by using a DCM. The output for the two clock phases is 0 and 90 degrees. The 200 MHz reference clock buffer, which goes to all IDELAYCTRL primitives, is included in this block.

Control State Machines

This block contains a state machine that controls NOP, READ, WRITE, and AUTO REFRESH operations to and from the RLDRAM II memory.

RLDRAM II Physical Layer

This block contains the pads that interface with the RLDRAM II control, address, and data signals, along with the logic to calibrate the physical layer for read data capture.

Pin Descriptions

Table 10 lists pin descriptions for the CIO DDR RLDRAM II memory interface when replacing the synthesizable testbench included with the design with an application.

Table 10: CIO DDR RLDRAM II Memory Interface Pin Descriptions

Pin Name	Pin Direction	Pin Description
Global Ports⁽¹⁾		
clk	I	clk0 from DCM (FPGA system clock)
clk90	I	clk90 from DCM (90-degree phase-shifted system clock)
refClk	I	200 MHz reference clock for IDELAYCTRL (needed for ChipSync technology)
sync_sysReset	I	Active-Low reset, asynchronous set, synchronous clear for phy_cs_n
rstHard	I	Active-High reset until DCM is locked
rstHard_90	I	Active-High reset until DCM is locked, synchronous with clk90
rstHard_180	I	Active-High reset until DCM is locked, synchronous with clk180
rstHard_270	I	Active-High reset until DCM is locked, synchronous with clk270
rstHard_refClk	I	Active-High reset until DCM is locked, synchronous with refClk
rstConfig	I	Active-High Configuration reset
rstCmd[3:0]	I	Memory command issued during configuration reset
rstAd[19:0]	I	Memory address for command during configuration reset
rstBa[2:0]	I	Memory bank for command during configuration reset
calibration_done	O	Physical layer has finished calibration, and normal operation can begin.
Application Interface Signals⁽¹⁾		
rldReadData[71:0]	O	Read Data FIFO data output
rldReadDataValid	O	Valid signal to indicate Read Data
apValid	I	Address FIFO data valid input (write enable)
apAddr[25:0]	I	Address FIFO data input
apWriteDValid	I	Write Data FIFO data valid input (write enable)
apWriteDM[3:0]	I	Write Data FIFO data mask (DM) input
apWriteData[71:0]	I	Write Data FIFO data input
apConfWr	I	Configuration registers write data valid (write enable)
apConfA[3:0]	I	Configuration registers address bus
apConfWrD[7:0]	I	Configuration registers write data
apConfRd	I	Configuration registers read enable
apConfRdD[7:0]	O	Configuration registers read data
rlWdfEmpty	O	Write Data FIFO empty flag

Table 10: CIO DDR RLDRAM II Memory Interface Pin Descriptions (Continued)

Pin Name	Pin Direction	Pin Description
rIWdfFull	O	Write Data FIFO full flag
rIRdfEmpty	O	Read Data FIFO empty flag
rlafEmpty	O	Address FIFO empty flag
rlafFull	O	Address FIFO full flag
rIWdfWrCount[12:0]	O	Write Data FIFO write count
rIWdfWordCount[12:0]	O	Write Data FIFO word count
rlafWrCount[12:0]	O	Write address FIFO write count
rlafWordCount[12:0]	O	Write address FIFO word count
Init_Done	O	Indicates memory initialization and physical layer calibration are complete
issueCalibration	I	Signal to recalibrate the physical layer after normal operation without a reset. User must save data at address locations used for calibration and wait for Init_Done and calibration_done signal before proceeding.
issueMRS	I	A pulse on this input causes the controller to program the Mode register into the memory. (At power-up, MRS is done as part of the initialization.)
confMReg[17:0]	O	MRS value, for testbench to check burst length during normal operation
Interface to Two CIO DDR RLDRAM II Devices		
phy_ck_p[1:0], phy_ck_n[1:0]	O	Master differential clocks, center aligned with command, address, and bank address
phy_dk_p[1:0], phy_dk_n[1:0]	O	Differential write data clocks, center-aligned with write data
phy_a[19:0]	O	Row and column addresses for read and write operations. During a MODE REGISTER SET, the address inputs define the register settings.
phy_ba[2:0]	O	Bank addresses select the internal bank to apply a command.
phy_cs_n[1:0]	O	Chip Select command
phy_we_n	O	Write Enable command
phy_ref_n	O	Refresh command
phy_dm[1:0]	O	Data mask (DM) signals for write data
phy_qk_p[1:0], phy_qk_n[1:0]	I	Differential read data clocks transmitted by the RLDRAM II devices and edge aligned with read data.
phy_qvld[1:0]	I	Data valid signals transmitted by the RLDRAM II devices. Indicate valid read data.
phy_dq[35:0]	I/O	Data input/outputs. During read commands, the data is sampled at both edges of QK. During write commands, the data is referenced to both edges of DK.

Notes:

1. Unless otherwise noted, signals are synchronous with clk0.

Memory Initialization

The RLDRAM II device must be powered up and initialized in a predefined manner. The initialization sequence is handled by the RLDRAM II memory interface as follows:

1. After all power supply and reference voltages are stable and the master clock (RLD_CK and RLD_CK_N) is stable, the RLDRAM II requires a 200 μ s (minimum) delay prior to applying an executable command.
2. After the 200 μ s (minimum) delay has passed, the RLDRAM II memory interface issues three MRS commands: two dummies and one valid MRS.
3. Six clock cycles (t_{MRSC}) after the valid MRS, the RLDRAM II memory interface issues eight AUTO REFRESH commands: one command on each bank and each command separated by 2,048 cycles.
4. After six clock cycles (t_{RC}) for Configuration 2, the physical layer performs data calibration to ensure correct read data capture. After calibration is complete, the RLDRAM II interface is ready for normal operation as indicated by the `Init_Done` output to the application.

Clocking Methodology and Read/Write Datapaths

The clocking methodology and read/write datapath of the Virtex-5 FPGA are integrated in the input/output block (IOB) delay functionality. Read data is first captured using the clock forwarded by the memory and then transferred to the global clock domain inside the FPGA. Write data and clocks forwarded to the memory are transmitted using quadrature phase-shifted outputs of the DCM.

Implementation Details

The RLDRAM II reference design takes advantage of these features of the Virtex-5 family: improvements in I/O, clocking resources, and storage elements. All these features contribute to the high performance and ease of use for this reference design. The following sections describe the design implementation in more detail.

User Interface Timing Description

The user interface module uses four FIFOs to store the address and data values for Read/Write commands. One FIFO holds the commands (read, write, and/or user refresh) and the Read/Write addresses. The second FIFO stores the Write data, while the third FIFO stores the data mask (used as byte write enable). The fourth FIFO stores the Read data.

The user sends commands through the user interface with concurrent rising and falling data. The commands and data are transferred by the system clock (single data-rate transfers). This reference design shows an external 36-bit data bus, thus a 72-bit internal data bus is submitted/received to/from the controller FIFOs.

Before sending new commands, the user must monitor the appropriate FIFO full signals so that commands and data are written to the FIFOs correctly.

[Figure 3](#) shows a timing diagram for sending commands through the user interface for a burst length of 2.

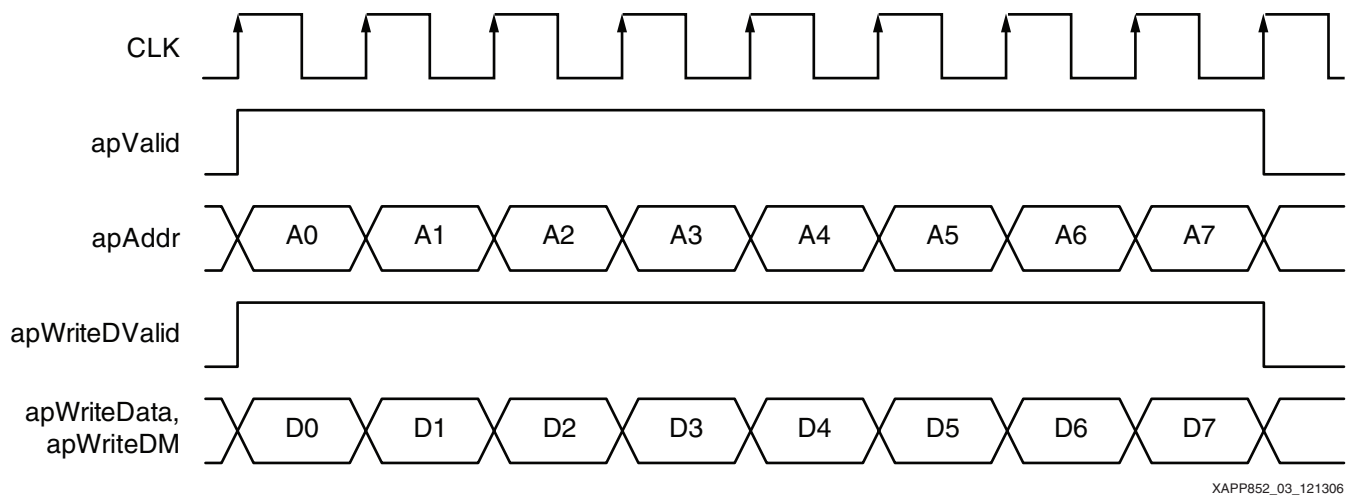


Figure 3: User Interface Timing Diagram for BL = 2, 8 Write Commands

Figure 4 shows a timing diagram for sending commands through the user interface for a burst length of 4. For this burst length, a single write command requires two locations of data in the FIFO. The command follows the data so that the controller can access the necessary data for processing the command.

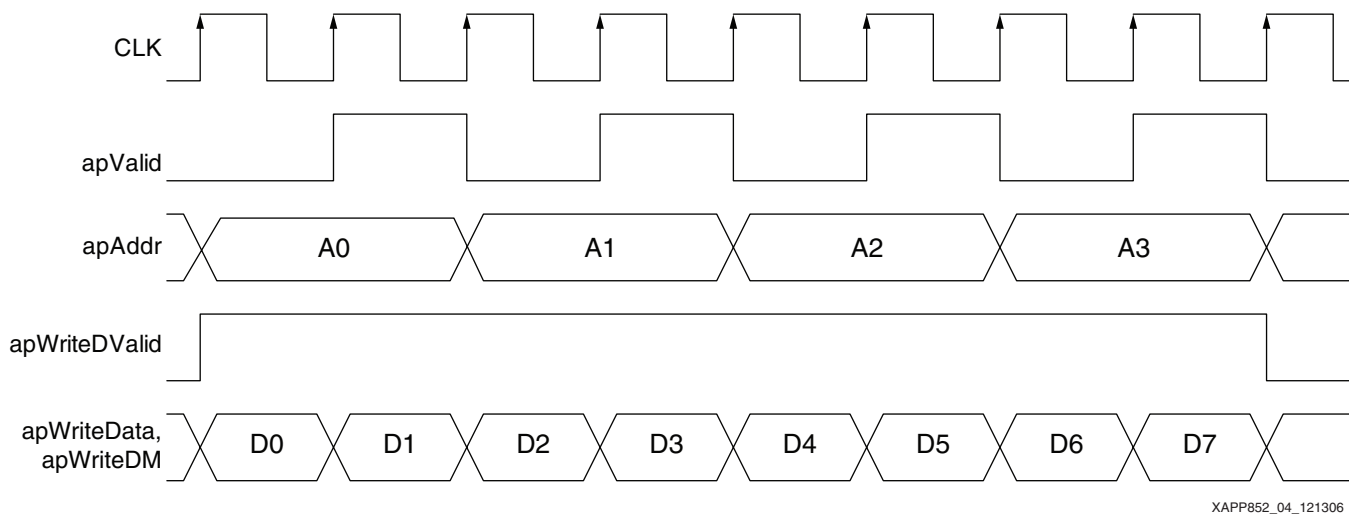


Figure 4: User Interface Timing Diagram for BL = 4, 4 Write Commands

Figure 5 shows read commands written to the FIFO. A 72-bit read data bus (with both rising edge and falling edge read data) is automatically extracted from the Read FIFO when new read data is received by the physical layer.

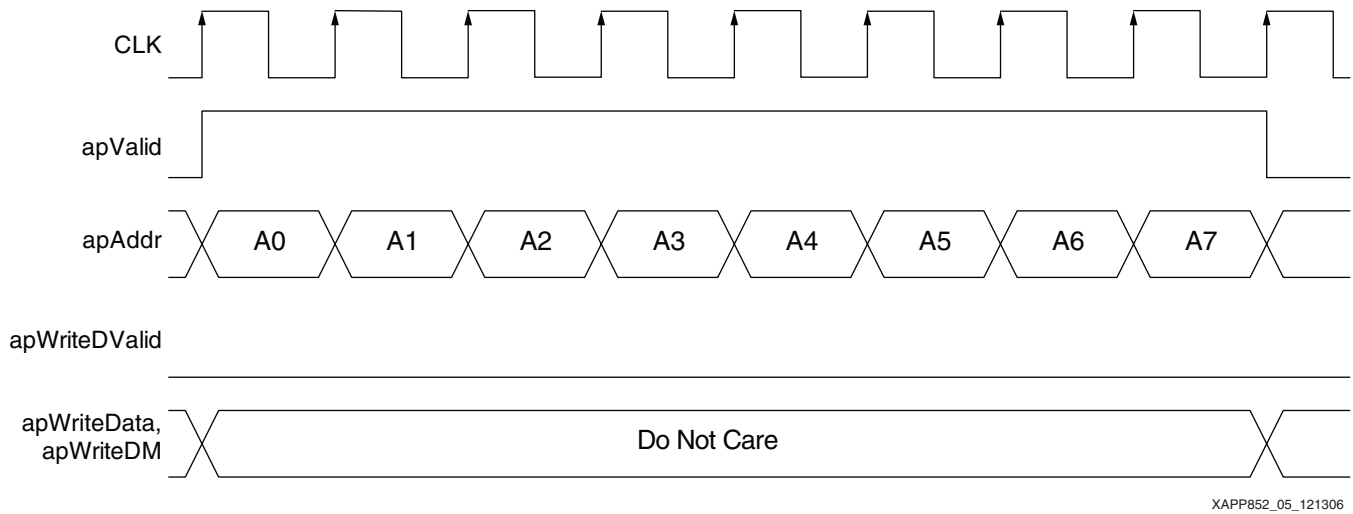


Figure 5: User Interface Timing Diagram for 8 Read Commands

Reset/Init State Machine

Figure 6 shows the state diagram for the Reset/Init state machine. This state machine is responsible for handling the reset condition, preparing the memory initialization, initiating the calibration process (data capture), and supporting memory mode changes.

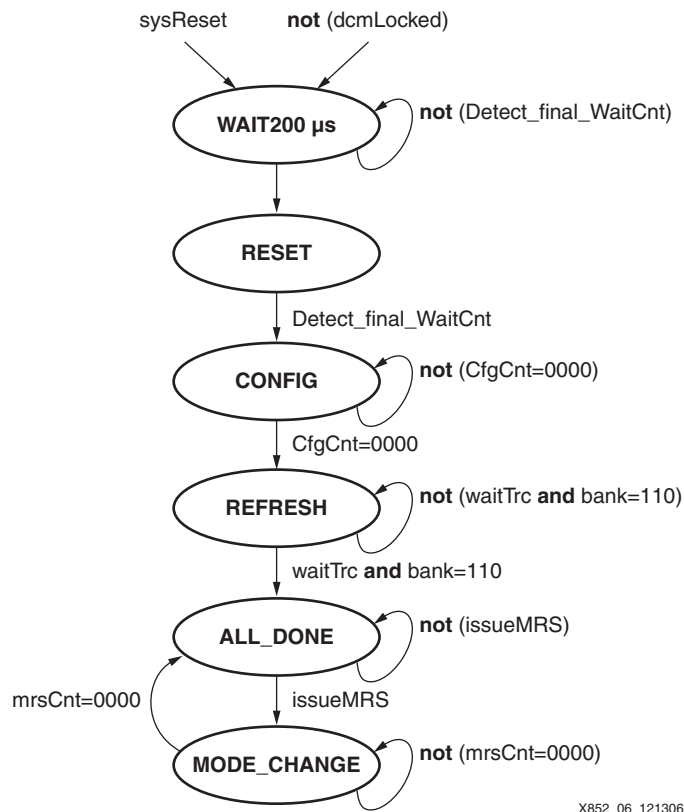
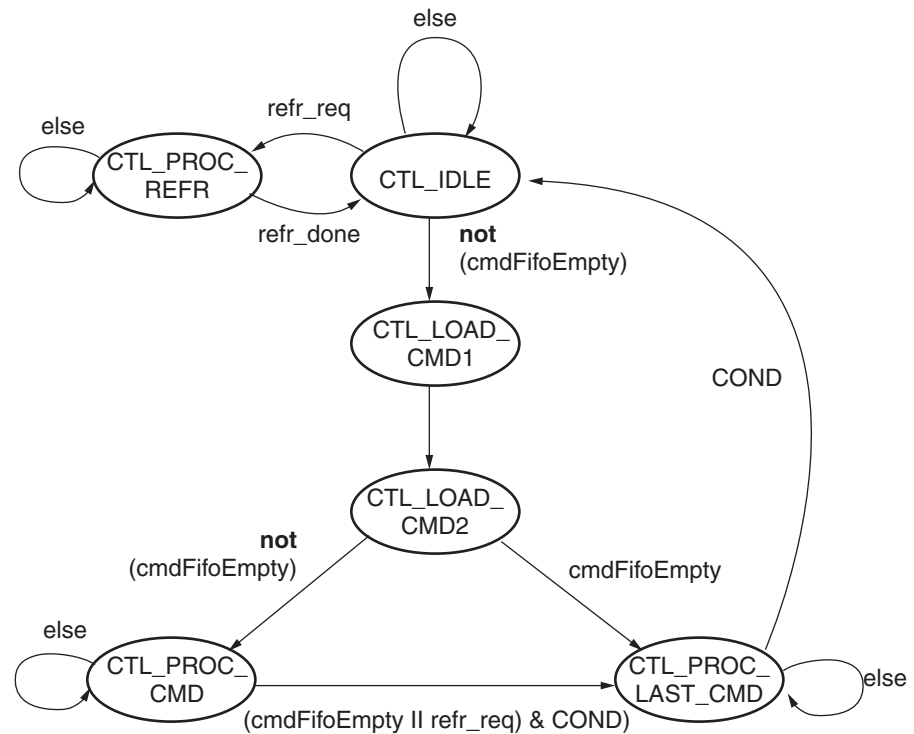


Figure 6: State Diagram for the Reset/Init Machine

Controller State Machine

Figure 7 shows the state diagram for the RLDRAM II controller state machine. The RLDRAM II controller reads commands and addresses from the user interface FIFOs and generates the commands to the RLDRAM II memory. The RLDRAM II controller is responsible for adhering to the RLDRAM II specification [Ref 1] and processes commands in the order presented by a user application.



COND = (write_req2 || (read_req2 & ~prev_is_wr_grant)) & trc_ok & burst_allow

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Figure 7: State Diagram for the RLDRAM II Controller State Machine

Data Capture Scheme

Figure 8 shows the data capture scheme. The QK-based data capture scheme enables capture of read data from memory at very high clock rates. This data capture scheme uses the ISERDES module available in the I/O of every Virtex-5 FPGA. Inside the ISERDES module, the incoming clock (QK) and data (DQ) are delayed and synchronized to the system clock (CLK270).

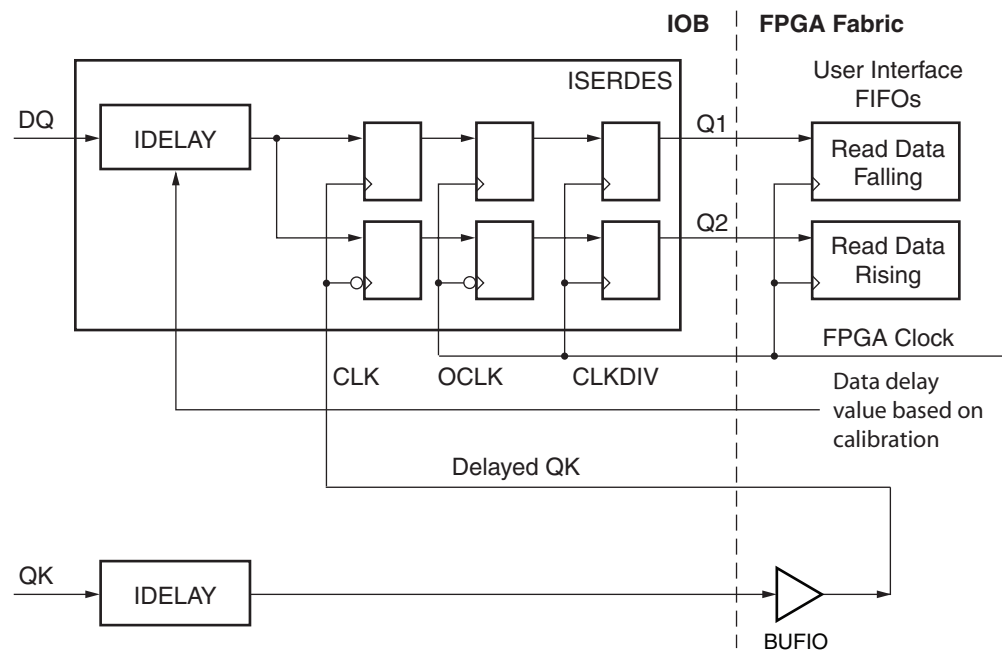
Note: This technique requires the incoming clock (QK) to be placed on clock-capable I/Os in the FPGA.

The read datapath comprises two stages: read data capture and read data recapture. Both stages are implemented inside the built-in ISERDES available in every I/O. The QK signal routed through the I/O clock buffer (BUFIO) captures the incoming read data (DQ) in the first set of registers inside the ISERDES block. The second set of registers are used to transfer the data in the QK domain to the system clock domain.

The ISERDES has three clock inputs: CLK, OCLK, and CLKDIV. The read data (DQ) capture is done in the CLK (QK) domain and transferred to the system clock using OCLK and CLKDIV.

- CLK: The read clock (QK), routed through the BUFIO, provides the CLK clock input.
- OCLK and CLKDIV: These clocks deserialize the incoming data. The system clock (CLK270) provides inputs to OCLK and CLKDIV because the data transfer occurs at the same frequency as the interface speed.

The data captured in the ISERDES module can be written into built-in FIFO36 modules available inside Virtex-5 FPGAs.



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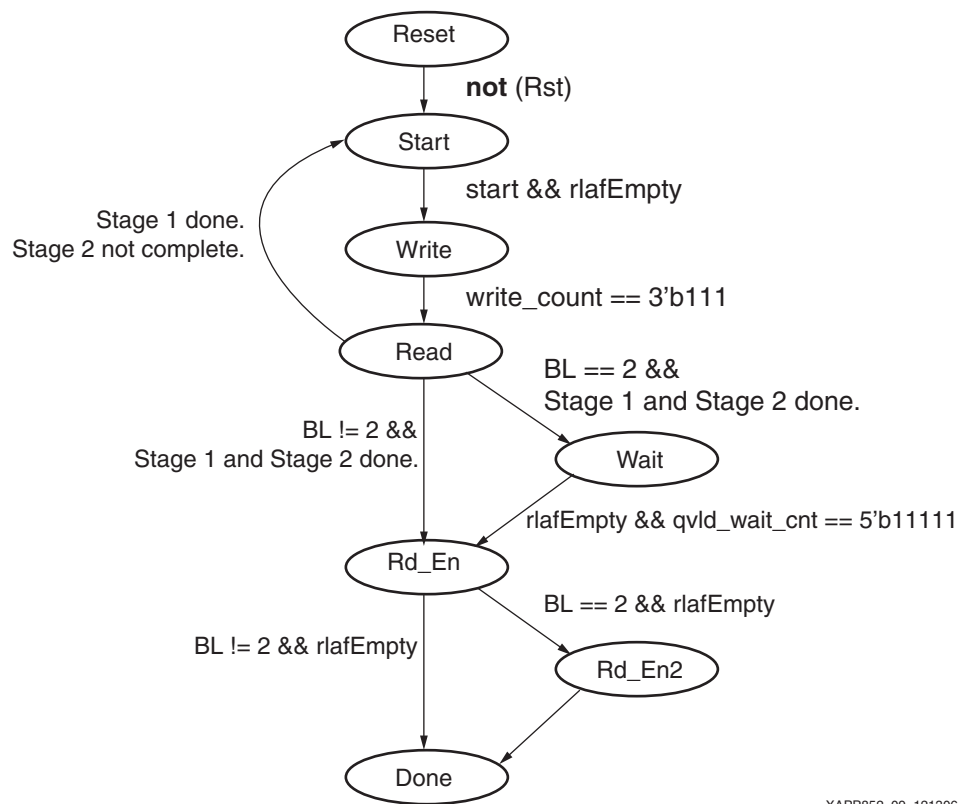
Figure 8: Data Capture Scheme

Data Calibration

Figure 9 shows the state machine diagram for the physical layer command state machine. The state machine generates the needed commands for data calibration. The data calibration logic provides the required amount of delay on the read data (DQ) and clock (QK) to align the captured data to the center of the FPGA clock. The physical layer command state machine is enabled both when the IDELAY_READY signal from the IDELAYCTRLs is asserted High and when the required clock cycles are met for the memory initialization. Calibration consists of writes to the RLDRAM II device memory, followed by consecutive reads to the same locations until the right delay values required for the DQ and QK signals are identified.

The physical layer command state machine sends commands to the FIFOs for processing, so that the controller can generate the read commands to the memory for data calibration.

After calibration is complete, this state machine transfers control to the User Interface for normal operation.



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Figure 9: Physical Layer Command State Machine
(Used to Generate Commands to RLDRAM II Devices for Data Calibration)

The stages of calibration are:

First Stage of Calibration

The first stage of calibration aligns DQ and QK so that QK falls in the middle of the data valid window and can correctly capture the read data.

A pattern is written to the memory, read back, and checked using the rising and falling outputs of the ISERDES. The patterns used are:

- For rising data, use the F pattern (all bits High).
- For falling data, use the 0 pattern (all bits Low).

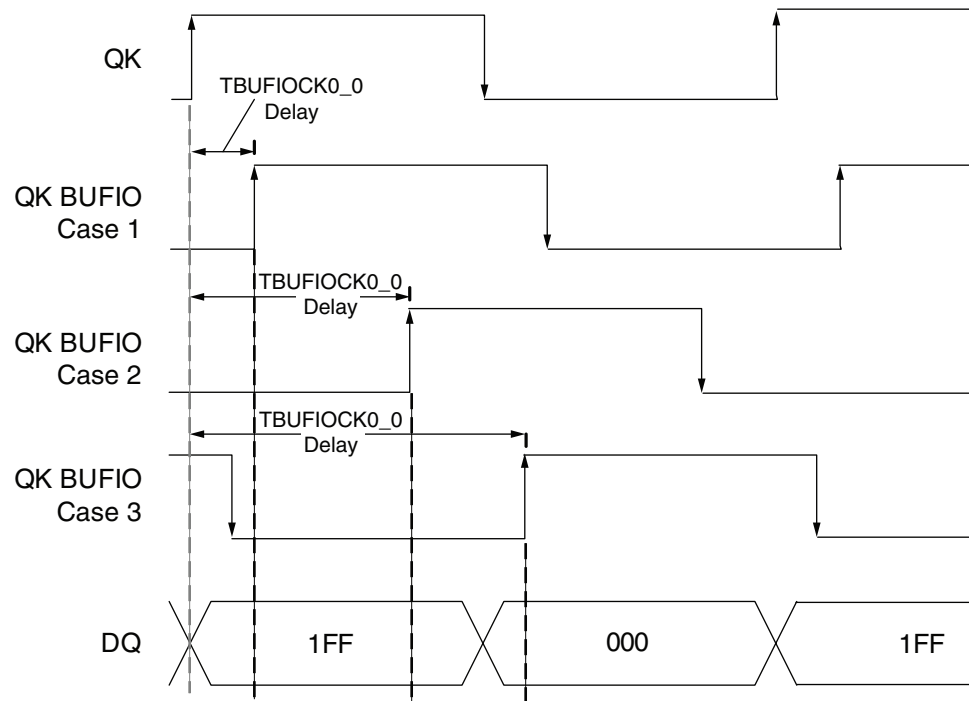
Note: Because data capture in the FPGA clock domain does not occur until the second stage of calibration, this first stage of calibration relies on the data staying constant for the input of the Rise/Fall flip-flops in the ChipSync block.

The clock (QK) used to capture data (DQ) is routed through a BUFIO. The BUFIO includes a clock-to-out delay TBUFIOCK0_0 (see *Virtex-5 FPGA Data Sheet* [Ref 3]) that can place the clock in a non-optimal location in the data-valid window depending on the device, trace lengths, or frequency of operation.

Figure 10 shows three possible cases of QK alignment with DQ after TBUFIOCK0_0.

- Case 1: QK is to the left of the center of the data valid window.
- Case 2: QK is to the right of the center of the data valid window.
- Case 3: QK is outside of the data valid window.

The data calibration state machine centers the strobe (QK) in the data valid window (DQ) by either incrementing the taps on QK (as in case 1 in Figure 10) or incrementing the taps on DQ (as in case 2 and 3 in Figure 10).



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Figure 10: Three Possible Cases of QK Alignment with DQ after TBUFIOCK0_0

After the first stage of calibration is complete, the following occurs:

1. The data calibration state machine notifies the physical layer command state machine. (See [Figure 9](#).)
2. The physical layer command state machine halts the read commands for the first stage of calibration.
3. Both the physical layer command state machine and the data calibration state machine proceed to the second stage of calibration.

Second Stage of Calibration

The second stage of calibration transfers read data from the QK domain to the FPGA clock domain. A second pattern is written to the memory, read back, and checked using the rising and falling outputs of the ISERDES. The strobe (QK) and data (DQ) are incremented/decremented together to find the center of a window where data is captured correctly using the FPGA clock.

After the second stage of calibration is complete, the data calibration state machine notifies the physical layer command state machine, which halts the read commands for the second stage of calibration.

Third Stage of Calibration

The third stage of calibration aligns both bytes in the FPGA and writes the read data to the FIFOs.

The QVLD signal from the RLDRAM II memory specifies when the read data is valid. This signal is used as a write enable to the read data FIFOs in the FPGA. The QVLD signal is treated similarly to a data pin, in that it is captured with QK using the ISERDES and transferred to the FPGA clock.

Only one clock (QK) can be used for capture of QVLD. QVLD receives the same number of taps as the data associated with this clock QK. Because two bytes of data can be calibrated separately but share the same QVLD signal from the memory, these two bytes can be misaligned by one clock cycle in the FPGA.

During calibration, the controller generates back-to-back reads to avoid gaps in the read data stream (aside from refreshes). By using the back-to-back reads, QVLD is not needed during the first and second stages of the calibration. To align the bytes and use QVLD as a write enable to the FIFOs, a single read burst checks the read data against QVLD and sets a flag for alignment.

Note: BL = 2 requires two back-to-back read bursts for QVLD alignment.

After all DQ signals are centered around QK and the data aligns with QVLD, the delay calibration is complete.

I/O Timing Analysis

This section provides an I/O timing analysis of the reference design. The I/O timing analysis uses a Xilinx XC5VLX50T device [Ref 3] and a Micron MT49H16M18BM-25 device for the timing parameters. The parameters in *italics* in Table 11 through Table 16 are from the Micron data sheet [Ref 1].

Read Timing Analysis

To capture data using the free-running QK clock provided by the memory, the timing analysis must take into account the skew between the QK and associated Q data bits that are being captured (t_{QK_Q}).

The BUFIO resource in the FPGA captures the data in the IOBs (where the sampling error must be considered), along with the clock skew associated with routing the QK clock to the IOBs.

The IDELAY tap pattern jitter is derived by taking the maximum number of taps required to delay a signal for one and a half clock cycles. The board layout skew between QK/QK_N and DQ (approximately 25 ps) and package skew in the same physical region are also considered for this timing analysis.

Table 11 lists the read timing analysis for 250 MHz.

Table 11: Read Timing Analysis for 250 MHz – XC5VLX50T Device (-1 Speed Grade)

Parameter	Value (ps)	Description
T_{CLOCK}	4000	Clock period.
T_{PHASE}	2000	Clock phase (DDR mode).
FPGA and PCB Uncertainties		
T_{BUFIO_SKEW}	80	T_{BUFIO_SKEW} parameter from <i>Virtex-5 FPGA Data Sheet</i> [Ref 3].
T_{SAMP_BUFIO}	450	Sample window from <i>Virtex-5 FPGA Data Sheet</i> (-1 speed grade). Includes setup and hold for an IOB flip-flop, clock jitter, and tap uncertainty.
T_{DCD_BUFIO}	100	BUFIO clock resource duty-cycle distortion.
$T_{IDELAYPAT_JIT}$	470	10 ps of jitter per tap (75 ps delay/tap resolution) in High Performance Mode.
Number of Taps	47	Worst-case number of IDELAY taps on read data is based on the taps needed to account for the BUFIO delay to center the clock with the data (worst case of 9 taps) and second stage calibration (38 taps).
$T_{PKGSKEW}$	50	Localized skew in the bank. Trace length matching on PCB accounts for some package skew in the same physical region or in the same bank.
$T_{PCB_LAYOUT_SKEW}$	50	Skew between data lines and strobes on the board. (167 ps/in).
RLDRAM II Memory Uncertainties		
$T_{QK_Q_SKEW}$	400	Worst-case QK-edge-to-output-data edge (-25 device).
Timing Summary		
Read Data Valid Window	400	Worst-case window.

Notes:

- Inter-symbol interference (ISI), crosstalk, user input clock jitter, and contributors to dynamic skew are not considered in this analysis.

Table 12 lists the read timing analysis for 333 MHz.

Table 12: Read Timing Analysis for 333 MHz – XC5VLX50T Device (-3 Speed Grade)

Parameter	Value (ps)	Description
T _{CLOCK}	3003	Clock period.
T _{PHASE}	1501.5	Clock phase (DDR mode).
FPGA and PCB Uncertainties		
T _{BUFIO_SKEW}	70	T _{BUFIO_SKEW} parameter from <i>Virtex-5 FPGA Data Sheet</i> [Ref 3].
T _{SAMP_BUFIO}	350	Sample window from <i>Virtex-5 FPGA Data Sheet</i> (-3 speed grade). Includes setup and hold for an IOB flip-flop, clock jitter, and 150 ps of tap uncertainty.
T _{DCD_BUFIO}	100	BUFIO clock resource duty-cycle distortion.
T _{IDELAYPAT_JIT}	410	10 ps of jitter per tap (75 ps delay/tap resolution) in High Performance Mode.
Number of Taps	41	Worst-case number of IDELAY taps on read data is based on the taps needed to account for the BUFIO delay to center the clock with the data (worst case of 11 taps) and second stage calibration (30 taps).
T _{PKGSKEW}	50	Localized skew in the bank. Trace length matching on PCB accounts for some package skew in the same physical region or in the same bank.
T _{PCB_LAYOUT_SKEW}	50	Skew between data lines and strobes on the board (167 ps/in).
RLDRAM II Memory Uncertainties		
T _{QK_Q_SKEW}	400	Worst-case QK-edge-to-output-data edge (-25 device).
Timing Summary		
Read Data Valid Window	71.5	Worst-case window.

Notes:

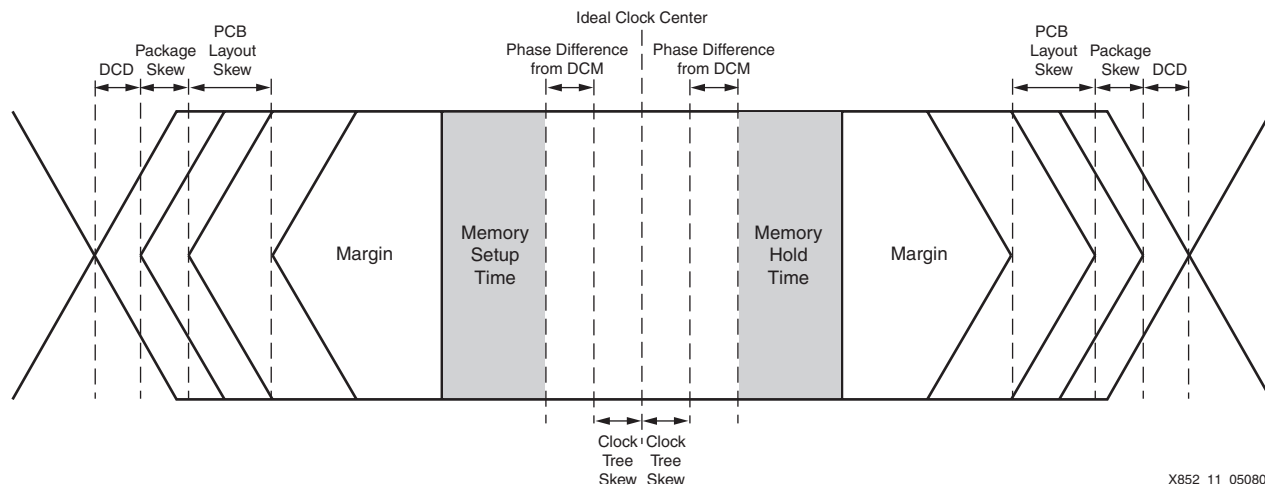
1. ISI, crosstalk, user input clock jitter, and contributors to dynamic skew are not considered in this analysis.

Write Timing Analysis

The FPGA-clock duty cycle distortion is subtracted from the ideal bit time to get the leading edge and trailing edge bit times. The uncertainty parameters are DCM jitter, a global clock tree skew between data I/O registers, and a phase offset error between different system clocks. A board layout skew between DK/DK and DQ (approximately 50 ps) and package skew in the same physical region are classified as uncertainties.

For the DQ data input to memory to be valid, it must meet setup and hold times relative to the DK/DK edges. The setup and hold times need to be derated based on the slew rate of DK/DK and DQ. After simulation with the IBIS models for the Virtex-5 FPGA, the setup and hold times do not need to be derated because the nominal slew rate of 2V/ns is attained. The same parameters apply also to the DM.

Figure 11 shows a graphical depiction of the write timing analysis.



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Figure 11: Write Timing Analysis Bit Time and Uncertainties

Table 13 lists the write timing analysis for 250 MHz. The table includes all parameters.

Table 13: Write Timing Analysis for 250 MHz – XC5VLX50T Device (-1 Speed Grade)

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
T_{CLOCK}	4000			Clock period.
Bit Period	2000			DDR memory works on two bits per clock period.
Bit Period Analysis		1000	1000	Each bit time edge is analyzed separately.
FPGA and PCB Uncertainties				
$T_{\text{DUTY_CYC_DLL}}$		90	90	Duty cycle distortion from DCM (-1 speed grade).
$T_{\text{PACKAGE_SKEW}}$		50	50	Worst-case package skew for an XC5VLX50T device/package.
T_{JITTER}		0	0	Same DCM used to generate CLK0 and CLK90.
$T_{\text{CLOCK_TREE_SKEW}}$		100	100	Small value considered for skew on global clock line because DK and associated DQ are placed close to each other. This is an estimate and is design dependent.
$T_{\text{OUT_OFFSET_1X}}$		160	160	Phase alignment between different DCM outputs (-1 speed grade).
$T_{\text{PCB_LAYOUT_SKEW}}$		50	50	Skew between data lines on the board (167 ps/in). Assumes a 1/3 inch difference.

Table 13: Write Timing Analysis for 250 MHz – XC5VLX50T Device (-1 Speed Grade)
(Continued)

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
RLDRAM II Memory Uncertainties				
T_{DS}		250	0	Data and data mask to DK setup time (-25 device).
T_{DH}		0	250	Data and data mask to DK hold time (-25 device).
Timing Summary				
Total Uncertainties		700	700	Sum of FPGA, PCB, and memory uncertainties.
Write Data Valid Window	600	300	300	Worst-case window. (Bit period minus total uncertainties.)

Notes:

1. ISI, crosstalk, user input clock jitter, and contributors to dynamic skew are not considered in this analysis.

Table 14 lists the write timing analysis for 333 MHz. The table includes all parameters.

Table 14: Write Timing Analysis for 333 MHz – XC5VLX50T Device (-3 Speed Grade)

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
T_{CLOCK}	3003			Clock period.
Bit Period	1501.5			DDR memory works on two bits per clock period.
Bit Period Analysis		750.75	750.75	Each bit time edge is analyzed separately.
FPGA and PCB Uncertainties				
$T_{DUTY_CYC_DLL}$		75	75	Duty cycle distortion from DCM (-3 speed grade).
$T_{PACKAGE_SKEW}$		50	50	Worst-case package skew for an XC5VLX50T device/package.
T_{JITTER}		0	0	Same DCM used to generate CLK0 and CLK90.
$T_{CLOCK_TREE_SKEW}$		100	100	Small value considered for skew on global clock line because DK and associated DQ are placed close to each other. This is an estimate and is design dependent.
$T_{OUT_OFFSET_1X}$		140	140	Phase alignment between different DCM outputs (-3 speed grade).
$T_{PCB_LAYOUT_SKEW}$		50	50	Skew between data lines on the board (167 ps/in). Assumes a 1/3 inch difference.

Table 14: Write Timing Analysis for 333 MHz – XC5VLX50T Device (-3 Speed Grade)
(Continued)

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
RLDRAM II Memory Uncertainties				
T_{DS}		250	0	Data and data mask to DK setup time (-25 device).
T_{DH}		0	250	Data and data mask to DK hold time (-25 device).
Timing Summary				
Total Uncertainties		665	665	Sum of FPGA, PCB, and memory uncertainties.
Write Data Valid Window	171.5	85.75	85.75	Worst-case window. (Bit period minus total uncertainties.)

Notes:

1. ISI, crosstalk, user input clock jitter, and contributors to dynamic skew are not considered in this analysis.

Address and Control Timing Analysis

Address and control signals are non-DDR. Therefore, the entire clock period is considered for this timing analysis, and no duty-cycle distortion applies.

The uncertainty parameters considered are:

- Global clock tree skew
- Board layout skew between CK/\overline{CK} and address/control signals (approximately 300 ps)
- Package skew

The address/control setup and hold times that the memory vendor specifies are also considered for this timing analysis. The setup and hold times need to be derated based on the slew rate of CK/\overline{CK} and the address and control signals. After simulation with the IBIS models for the Virtex-5 FPGA, the setup and hold times do not need to be derated because the nominal slew rate of 2V/ns is attained.

Table 15 lists the address and control timing analysis for 250 MHz.

Table 15: Address and Control Timing Analysis for 250 MHz – XC5VLX50T Device

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
T_{CLOCK}	4000			Clock period.
FPGA and PCB Uncertainties				
$T_{\text{DUTY_CYC_DLL}}$		180	180	Duty cycle distortion from DCM (-1 speed grade).
$T_{\text{PACKAGE_SKEW}}$		100	100	Worst-case package skew for an XC5VLX50T device/package.
$T_{\text{CLOCK_TREE_SKEW}}$		300	300	Small value used. Estimate only. Assumes CK/ $\overline{\text{CK}}$ outputs are placed close to address/control outputs.
$T_{\text{PCB_LAYOUT_SKEW}}$		167	167	Skew between clock and address/control lines on the board (167 ps/in). Assumes a 1 inch difference.
RLDRAM II Memory Uncertainties				
$T_{\text{AS}}/T_{\text{CS}}$		400	0	Address/command and input setup time (-25 device).
$T_{\text{AH}}/T_{\text{CH}}$		0	400	Address/command and input hold time (-25 device).
Timing Summary				
Total Uncertainties		1147	1147	Sum of FPGA, PCB, and memory uncertainties.
Address/Command Window	1706	853	853	Worst-case window.

Table 16 lists the address and control timing analysis for 333 MHz.

Table 16: Address and Control Timing Analysis for 333 MHz – XC5VLX50T Device

Parameter	Value (ps)	Leading Edge Uncertainties	Trailing Edge Uncertainties	Meaning
T_{CLOCK}	3003			Clock period.
FPGA and PCB Uncertainties				
$T_{\text{DUTY_CYC_DLL}}$		150	150	Duty cycle distortion from DCM (-3 speed grade).
$T_{\text{PACKAGE_SKEW}}$		100	100	Worst-case package skew for an XC5VLX50T device/package.
$T_{\text{CLOCK_TREE_SKEW}}$		300	300	Small value used. Estimate only. Assumes CK/ $\overline{\text{CK}}$ outputs are placed close to address/control outputs.
$T_{\text{PCB_LAYOUT_SKEW}}$		167	167	Skew between clock and address/control lines on the board (167 ps/in). Assumes a 1 inch difference.
RLDRAM II Memory Uncertainties				
$T_{\text{AS}}/T_{\text{CS}}$		400	0	Address/command and input setup time (-25 device).
$T_{\text{AH}}/T_{\text{CH}}$		0	400	Address/command and input hold time (-25 device).
Timing Summary				
Total Uncertainties		1117	1117	Sum of FPGA, PCB, and memory uncertainties.
Address/Command Window	769	384.5	384.5	Worst-case window.

Design Implementation

The CIO RLDRAM II memory interface targets an XC5VLX50T device and implements most of the features described in this application note.

Figure 12 shows the reference design file hierarchy.

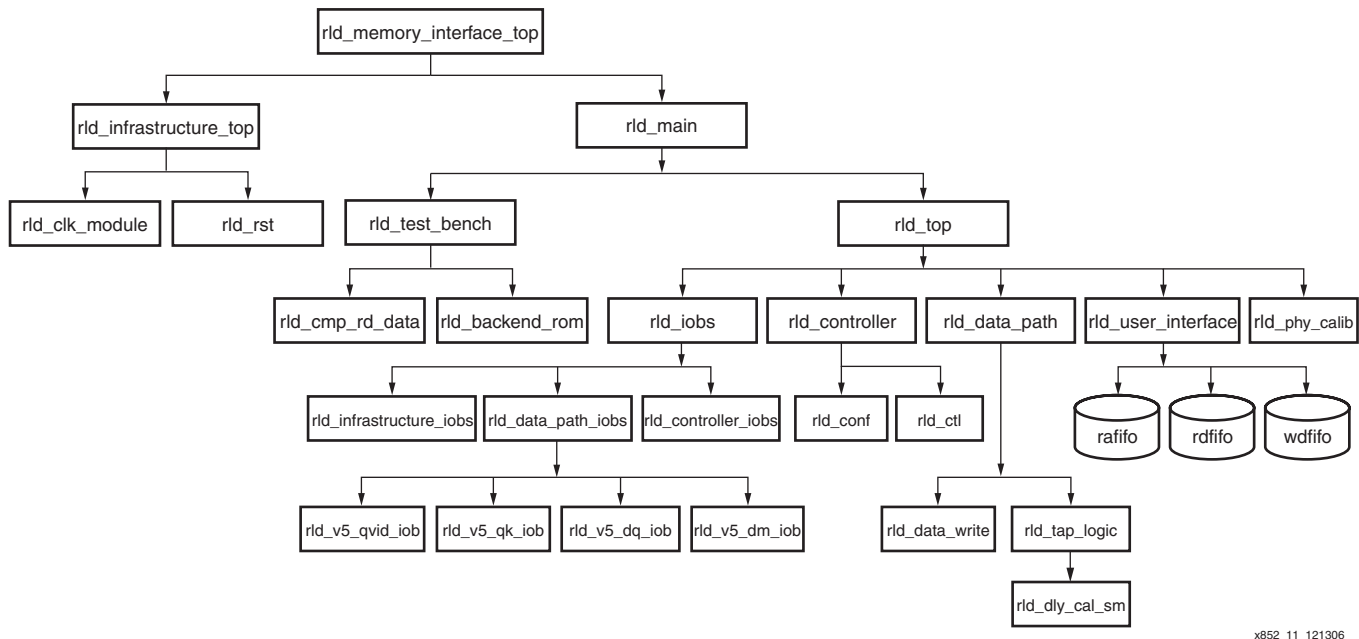


Figure 12: Reference Design File Hierarchy

Board Design Consideration

To use the data capture scheme, all the incoming clocks (QK_P and QK_N) should be placed on clock-capable I/O pairs and in the same bank as their associated data (DQ) for read data capture.

For all PC board designs, Xilinx strongly suggests simulating the board to determine the best termination scheme for the application. The *Virtex-5 FPGA User Guide* [Ref 4] suggests termination on both ends of PCB HSTL II buses. However, the final PCB design can suppress some termination resistors based on simulation. Digitally Controlled Impedance (DCI) can be used when creating prototypes or final production boards.

The Micron memory device has a board impedance matching capability that allows selection of a 50Ω impedance. An On-Die Termination (ODT) integrates a DCI-like termination scheme for the data bus. The ODT can be switched on or off at initialization time.

I/O Standards for RLDRAM II

The HSTL standard is used for interfacing Virtex-5 devices with RLDRAM II memory. HSTL I and HSTL III are intended to be used in unidirectional links, while HSTL II and HSTL IV are intended to be used in bidirectional links.

In contrast to other HSTL classes that have an 8 mA driver, the HSTL II class has a stronger 16 mA driver. The HSTL II class can hold bidirectional buses and can be used as complementary single-ended drivers/receivers for differential inputs or outputs on Virtex-5 devices with DIFF_HSTL_II or DIFF_HSTL_II_18 attributes, with and without DCI.

This information is described in detail in the *Virtex-5 FPGA User Guide* [Ref 4]. The reference design has some PCB routing rules. Each trace of a data word associated with one read clock QK/QK_N must be the same length as that specific read clock.

Reference Design

The reference design for the RLDRAM II memory controller using the strobe capture technique is available in Verilog and VHDL at:

<https://secure.xilinx.com/webreg/clickthrough.do?cid=55686>

Table 17 shows the reference design matrix.

Table 17: Reference Design Matrix

Parameter	Description
General	
Developer Name	Benoit Payette, Rodrigo Angel
Target Devices (Stepping Level, ES, Production, Speed Grades)	Virtex-5 FPGA XC5VLX50T-FF1136 (-1, -2, -3)
Source Code Provided?	Yes
Source Code Format	VHDL, Verilog
Design Uses Code or IP from Existing Reference Design, Application Note, 3rd party, or CORE Generator™ Software?	No
Simulation	
Functional Simulation Performed?	Yes
Timing Simulation Performed?	No
Testbench Provided for Functional and Timing Simulations?	Yes
Testbench Format	VHDL, Verilog
Simulator Software and Version	ModelSim SE 6.2c
SPICE/IBIS Simulations?	Yes
Implementation	
Synthesis Software Tools and Version	XST, version 10.1
Implementation Software Tools and Version	ISE® software, version 10.1
Static Timing Analysis Performed?	Yes
Hardware Verification	
Hardware Verified?	Yes
Hardware Platform Used for Verification	ML561 memory interfaces development board

Conclusion

RLDRAM II memory provides a solution positioned between high cost per bit, low-cycle time SRAM and low cost per bit, high-cycle time DDR/DDR2 SDRAM. RLDRAM II memory devices provide high density, high bandwidth, and fast SRAM-like random access for applications such as networking, graphics, and cache.

The Verilog reference design included with this application note implements a 36-bit CIO RLDRAM II memory interface in a Virtex-5 FPGA using two 18-bit-wide devices from Micron. The techniques described in this reference design take advantage of improvements in I/O, clocking resources, and storage elements in the Virtex-5 family to achieve a clock rate up to 333 MHz with data transfers up to 667 Mb/s per pin.

References

The following references were used in this application note:

1. *Micron MT49H16M18-25 288 Mb CIO RDRAM II Data Sheet*
<http://download.micron.com/pdf/datasheets/rldram/MT49H8M36.pdf>
 2. *Micron RDRAM II Design Guide Technical Note*
<http://download.micron.com/pdf/technotes/RLDRAMII/TN4901.pdf>
 3. [DS202](#), *Virtex-5 FPGA Data Sheet*
 4. [UG190](#), *Virtex-5 FPGA User Guide*
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Additional Resources

The following resources provide additional information useful to this application note:

1. IBIS Models for the Virtex-5 FPGA
<http://www.xilinx.com/support/download/virtex5ibis.htm>

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/12/06	1.0	Initial Xilinx release.
01/03/07	2.0	<p>Title changed.</p> <p>Changes to the following sections: “Summary” - Changed clock rates and data transfer rates; “Introduction”; “RLDRAM II Devices”; “Clocking”; “Mode Register”; “Bank Usage”; “Correspondence of WL and RL Times” - Changed title; “Design Features”; User Interface section under Block Diagram Description section - Retitled to “User Interface Block Description” and changed text; “Address FIFO”; “Write Data FIFO”; “Read Data FIFO”; “Configuration Registers”; “Control State Machines”; RLDRAM II Control Signals Physical Layer and RLDRAM II Data Signals Physical Layer - Combined text into “RLDRAM II Physical Layer” section and added text; “Memory Initialization”; User Interface section under Implementation Details - Retitled to “User Interface Timing Description”, changed text, and added Figure 3 through Figure 5; “Controller State Machine” section - Added new section and Figure 7; “Data Calibration” section - Changed text, and added Figure 9 and Figure 10; “Read Timing Analysis” section - Changed text and Table 11 and Table 12; “Write Timing Analysis”; “Address and Control Timing Analysis”; “Design Implementation”; “Board Design Consideration”; HTSL Class II section - Retitled to “I/O Standards for RLDRAM II” and clarified the text; “Conclusion”; and “References.”</p> <p>Updated the following tables: Table 1; Table 2; Table 4; Table 6; Table 10; and Table 13 through Table 17.</p> <p>Updated the following figures: Figure 1 - Changed simulation target device from a Micron MT49H32M9 x9 device to a Micron MT49H16M18 x18 device; Figure 2; Figure 8; and Figure 12.</p> <p>Reference Design - New reference design ZIP file</p>
05/29/07	2.1	Updated “Reference Design,” page 28 to include VHDL and Verilog and new ZIP file.
09/18/07	2.2	Updated software version information in Table 17 and updated reference design files. Also made minor formatting and grammatical edits, and condensed revision history for v2.0.
05/14/08	2.3	<ul style="list-style-type: none"> Updated Table 1, Table 11, and Table 12. Updated “Write Timing Analysis,” page 21, including Table 13 and Table 14. Updated “Address and Control Timing Analysis,” page 24, including Table 15 and Table 16. Removed Verification and Design Implementation Tools (Table 17). Added Reference Design Matrix (Table 17). Added Figure 11.

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